AD8158 HSPICE I/O Models

The AD8158 is an asynchronous quad-lane 2:1 switch with a total of 12 differential PECL/CML compatible inputs and 12 differential CML outputs. It is optimized for NRZ signaling with data rates of up to 6.5 Gbps.

The encrypted file *ad8158_model.inc* contains two HSPICE subcircuits, one that models a single input channel (ad8158_rx) and one that models a single output channel (ad8158_tx). The two subcircuits can be cascaded if desired to simulate the full data path with no switching functionality. The file *ad8158_test.sp* is an example of a full data path simulation, using a PRBS source as the input. The file *ad8158_lineloss.inc* implements a unidirectional and scalable transfer function which approximately describes the loss associated with an FR4 pc-board trace.

The HSPICE models are based on simplified circuits that include ideal dependent sources and passive elements. Simulation results using these models should be considered typical, and will not reproduce the performance of the circuit over supply and temperature variation.

Revision 2.0: January 5, 2009
Update Log

Rev 2.0 :
- Updated EQ Settings.
- ad8158_test.sp example updated to reflect EQ settings, comments expanded.
- Lineloss model updated to include impedance (50 Ohms) to reference plane.
- Updated documentation

Receiver Model

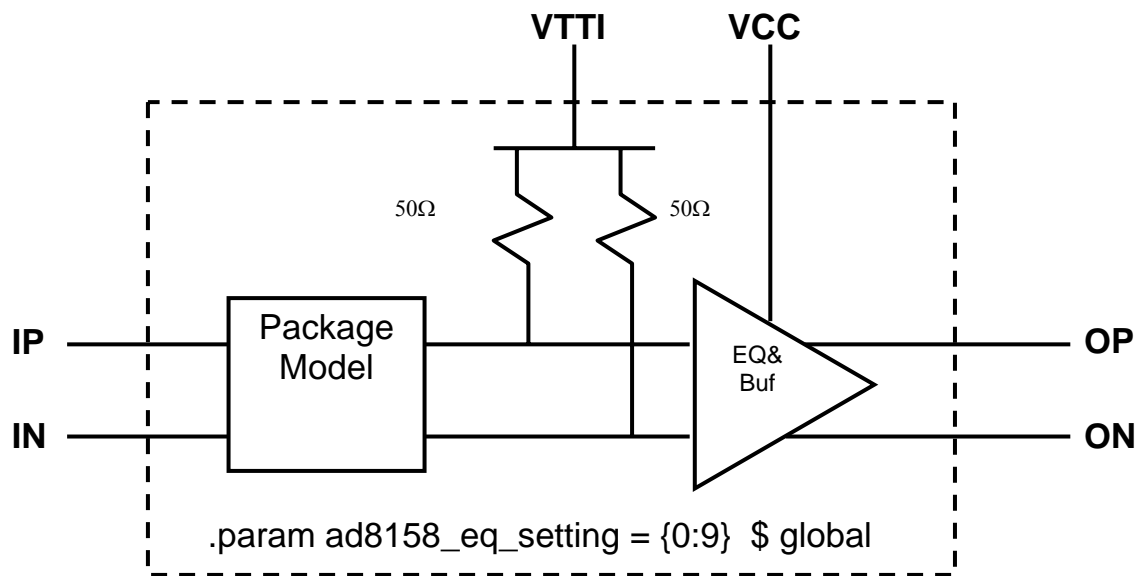Figure 1 describes the AD8158 receiver model.

Figure 1: AD8158 receiver model.

The package subcircuit is an RLC network that models the effect of the leads and bondwires on the differential input signal. This subcircuit includes the mutual inductance and capacitance of the leads and bondwires connected to IP/IN, as well as the capacitance to the neighboring VEE pins.

The differential input resistance to the model is 100 Ω.

The equalization level is set by the global variable "AD8158_EQ_SETTING." This variable may be set to a value between 0 and 9. If the user anticipates using the part in pin control mode, then only {0,2,4,9} are valid values for AD8158_EQ_SETTING. Altering the name of this variable or passing a different value to the ad8158_rx subcircuit through the "SETTING" parameter will cause the model to function incorrectly.

The output (OP/ON) of the receiver model is a CML-level signal (2V differential peak-to-peak) referenced to the VCC supply. It is a representation of the *on-chip* equalized signal, and it illustrates the capability of the device to reduce the jitter in a degraded input waveform. Since this is an on-chip signal, it can not be directly compared to a waveform obtained from the real device. A complete signal path through the ad8158 is obtained by using a series combination of the receiver and transmitter model.

Receiver Subcircuit Pin Descriptions
```
IP, IN – Differential input
OP, ON – Differential output
VTTI - Input termination supply
VCC – Positive supply voltage
VEE – Negative supply voltage
```

Receiver Subcircuit Parameter Descriptions

SETTING : 0 ≤ ad8158_eq_setting ≤ 9

      Equalizer setting as described in the AD8158 Datasheet.
      0 == lowest boost setting
      9 == highest boost setting

      In pin control mode, ad8158_eq_setting = {0,2,4,9}
      With I2C control, 0 < ad8158_eq_setting < 9

Warning: ad8158_eq_setting is a global variable that <u>must</u> be set for the receiver to operate correctly.

Example:
  Right:

```
*Instantiate AD8158 Receiver Model
```
<xrx> ip in op on vtti vcc vee ad8158_rx
+ setting = ad8158_eq_setting
<u>**.param ad8158_eq_setting**</u> **= 5**   **$ set equalization**

  Wrong:

```
*Instantiate AD8158 Receiver Model,
*neglecting to set global variable.
```
<xrx> ip in op on vtti vcc vee ad8158_rx
+ setting = myeqvar
.param myeqvar = 5   **$ eq not set correctly**

Transmitter Model

Figure 2 describes the AD8158 transmitter model.

VTTO

50Ω 50Ω

Add Jitter

LPF

IP

Out
Buf

Package
Model

OP

IN

ON

$ Model Parameters
.param ad8158_tx_olev = {0m,8m,12m,16m,24m}
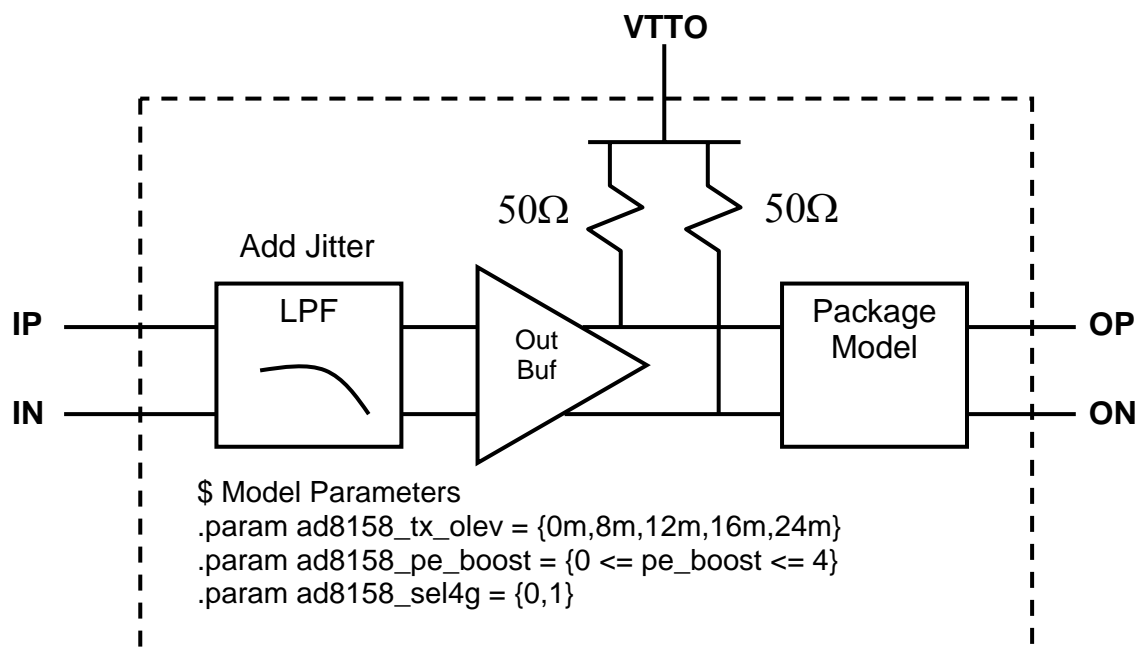.param ad8158_pe_boost = {0 <= pe_boost <= 4}
.param ad8158_sel4g = {0,1}

Figure 2: AD8158 transmitter model.

The inputs to the model are high impedance pins (IP/IN) which accept a PECL/CML signal from the output of the AD8158 receiver model. The low-pass filter adds a small amount of deterministic jitter to the signal to mimic the jitter that would typically be accumulated through the data path.

The Pre-emphasis level is set by the parameter "PE_BOOST," which may assume a scalar value between 1 and 4. See pages 16 and 17 of the Advanced Datasheet, Table 15, column four, (PE Boost), for more information on the allowed AD8158 pre-emphasis settings.

The dc output voltage level, (Table 15, column 1), is set with the "OLEV" parameter. Setting "OLEV" to the value in Table 15, column 2, will deliver the Output Level listed in Table 15, column 1. (Note that this number is peak differential voltage, not peak-to-peak differential voltage).

Setting the "SEL4G" parameter to "1" configures the pre-emphasis for datarates below 4.25 Gbps. A value of "0" is appropriate for datarates upto 6.5 Gbps.

The output buffer drives 50 Ω on-chip resistors that are terminated to the VTTO supply. The package model models the electrical characteristics of the leads, bondwires and pads.

Transmitter Subcircuit Pin Descriptions
```
IP, IN – Differential input
OP, ON – Differential output
```

```
VTTO    - Output termination supply
VEE     - Negative supply voltage
```

Transmitter Subcircuit Parameter Descriptions

OLEV : OLEV = {0m, 8m, 12m, 16m, 24m}
  Transmitter dc-output current level. OLEV = 16m corresponds to a dc-output voltage level of :
  16[mA] * 50[Ohm_diff] = 800mVpp differential.

  The values of OLEV shown above correspond to differential, peak-to-peak output voltage levels of:
  {0V, 400mV, 600mV, 800mV, 1200mV}

PE_BOOST : 1 < PE_BOOST < 4
  Pre-emphasis boost from column 5 of Table 20 in the AD8158 Datasheet. Note this parameter is specified as a scalar rather than "in dB" value. Boost is specified as the ratio of peak to settled output value. The value in decibels is given by the equation:
  PE_Boost [dB] = 20*log10(Boost)

- Note that setting the variable pe_boost=1 is equivalent to disabling pre-emphasis.
- Setting pe_boost=2 is equivalent to 6.02 dB of pre-emphasis.

Be aware that these models do not check any parameters for validity and will deliver results inconsistent with true device performance if invalid values are provided. For example, setting OLEV=80m and PE_BOOST=4 will simulate while in reality these settings exceed the transmitter's maximum achievable output current.

SEL4G : {0,1}

  SEL4G sets the pre-emphasis peak boost for legacy applications, (data-rates below 4.5 Gbps).

Transmitter Example:

```
            *Instantiate AD8158 Transmitter Model
            <xtx> ip in op on vtto vee ad8158_tx
            + olev = ad8158_tx_olev,  pe_boost = ad8158_pe_boost,
            + sel4g = ad8158_sel4g

            .param ad8158_tx_olev = 16m      $ Set "dc-level" output current
                                             $ 16 mA (equal to 800mVppd or
                                             $ 400mVd)
            .param ad8158_pe_boost= 2        $ Pre-emphasis boost factor
                                             $ Boost = 2 -> 6.02dB
            .param ad8158_sel4g = 0          $ Peak PE-boost set for 6.5G.
```

Test Bench

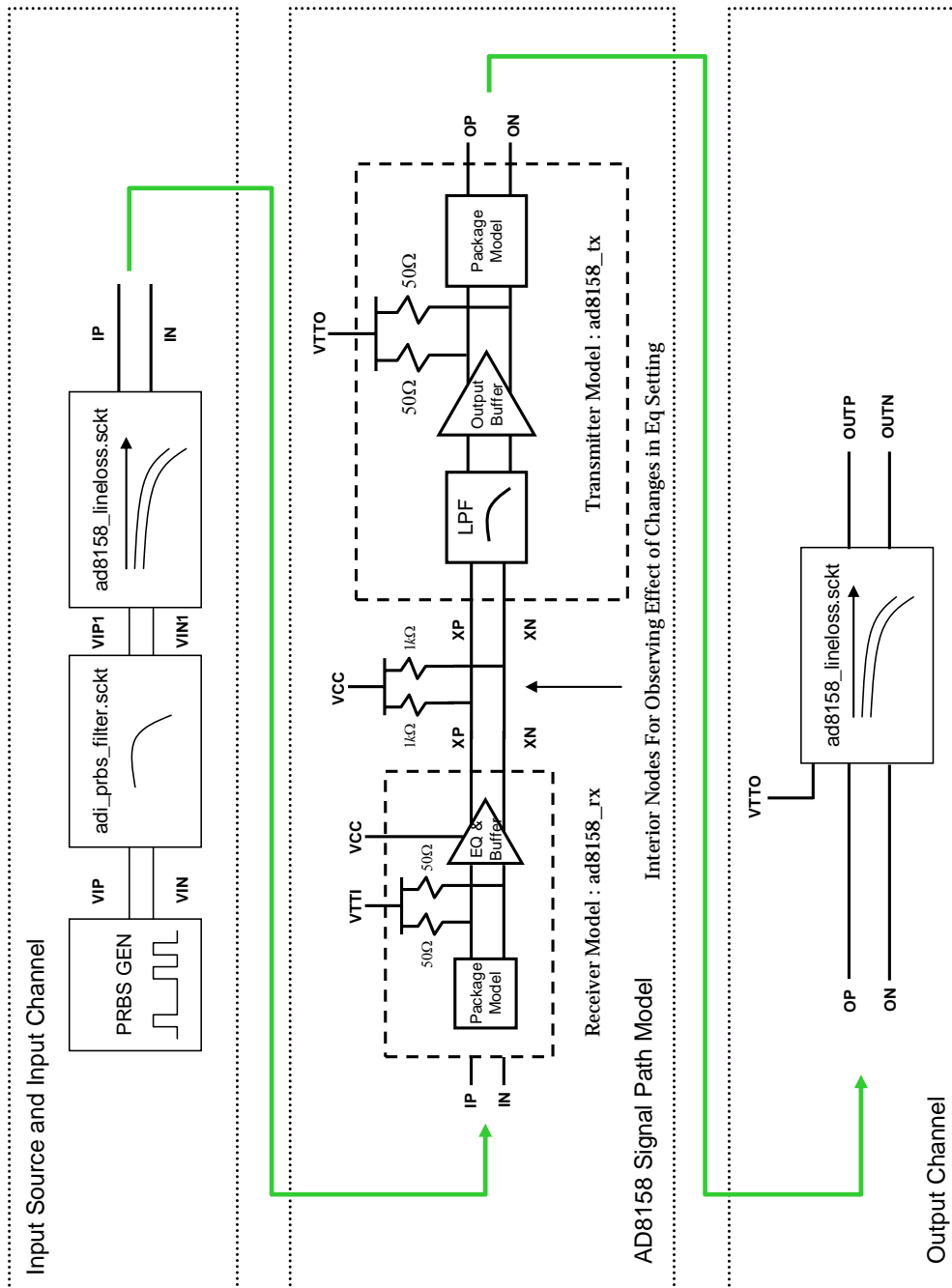Figure 3 shows the test bench implemented in the example file, AD8158_TEST.SP.

Figure 3: AD8158 Test Bench.

Note that the nodes XP and XN correspond to circuit nodes that are not directly accessible. Observing these nodes allows the designer to decouple the effects of equalizer and pre-emphasis settings on signal path performance.

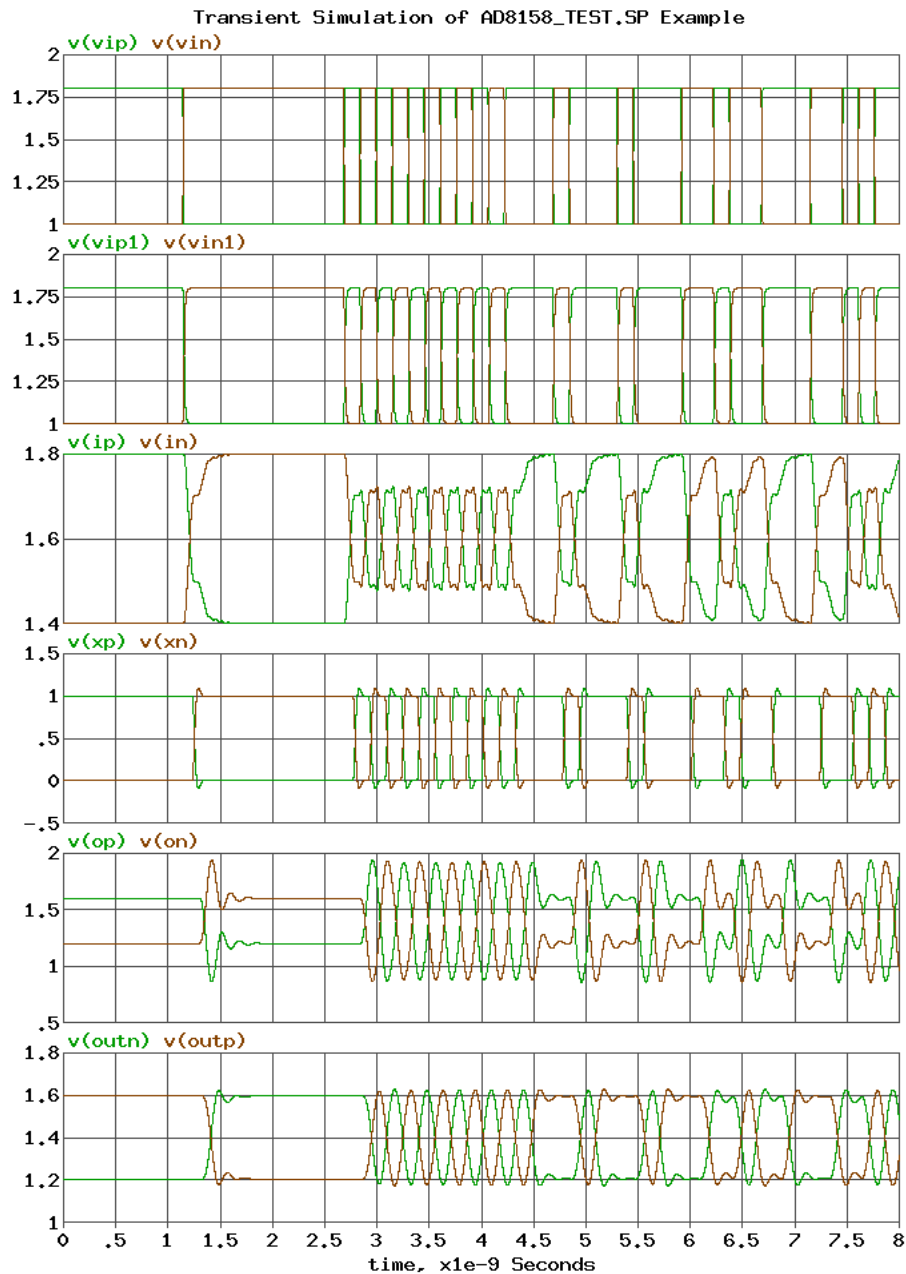The following plots show simulation results from running the file AD8158_TEST.SP.
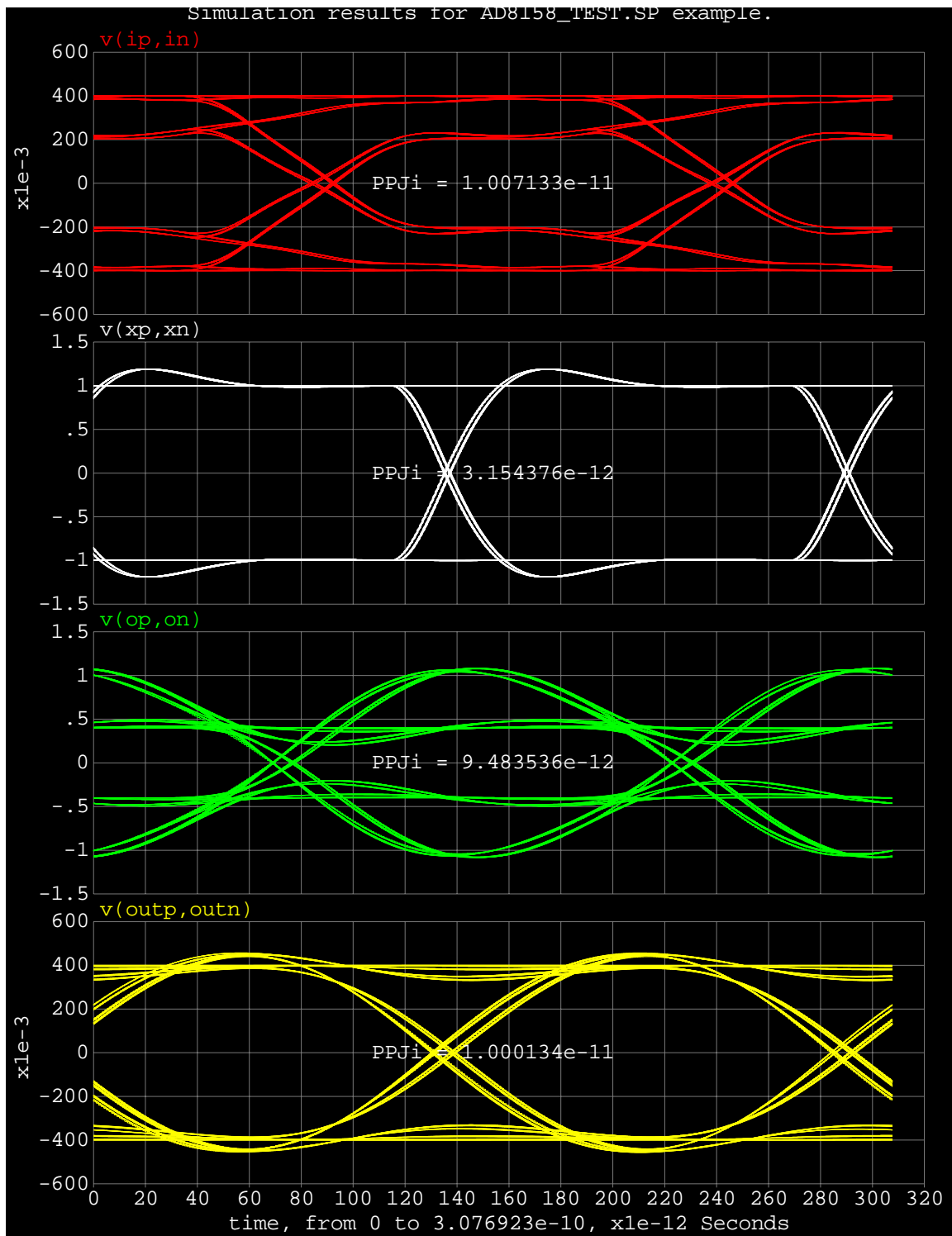

Figure 4. Single-ended Voltage Waveforms

Figure 5. Eye Diagram Plot of Transient Simulation Results