

## AD8159 HSPICE I/O Models

The AD8159 is an asynchronous quad-lane 2:1 switch with a total of 12 differential PECL/CML compatible inputs and 12 differential CML outputs. It is optimized for NRZ signaling with data rates of up to 3.2 Gbps.

The encrypted file *ad8159\_model.inc* contains two HSPICE subcircuits, one that models a single input channel (ad8159\_input) and one that models a single output channel (ad8159\_output). The two subcircuits can be cascaded if desired to simulate the full data path with no switching functionality. The file *ad8159\_test.sp* is an example of a full data path simulation, using a PRBS source as the input.

The HSPICE models are based on simplified circuits that include ideal dependent sources and passive elements. Simulation results using these models should be considered typical, and will not reproduce the performance of the real circuit over supply and temperature.

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## Input Model

Figure 1 describes the AD8159 input model.

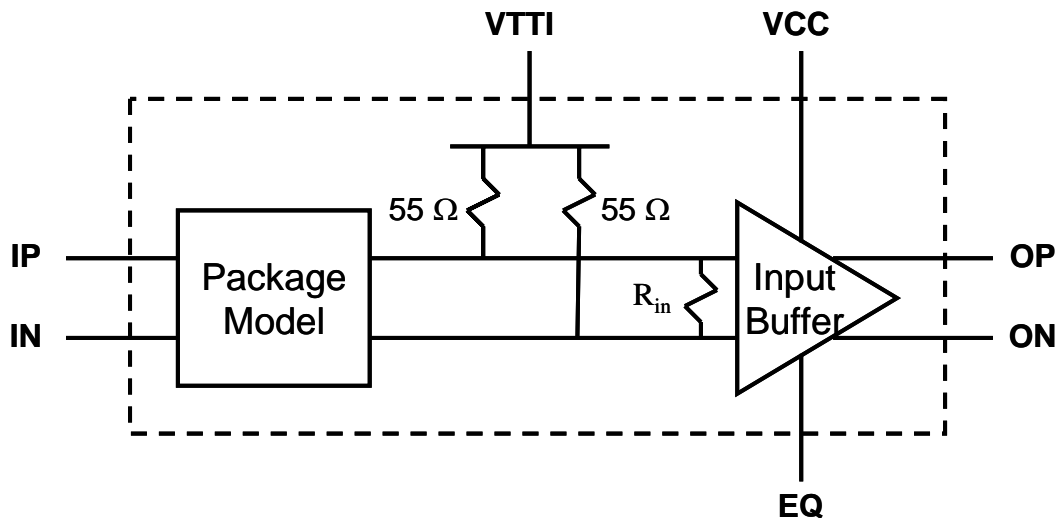


Figure 1: AD8159 input model.

The package subcircuit is an RLC network that models the effect of the leads and bondwires on the differential input signal. This subcircuit includes the mutual inductance and capacitance of the leads and bondwires connected to IP/IN, as well as the capacitance to the neighboring pins. Since the neighboring pins are supplies in the AD8159 pinout, the mutual inductance to those pins have little effect on the signal, and are not included in the model.

The differential input resistance to the model is  $100\ \Omega$ , which is the parallel combination of the  $55\ \Omega$  termination resistors and the finite input resistance of the buffer.

The input buffer has a single control pin (EQ) that selects the level of equalization. When  $EQ < 100\ \text{mV DC}$  (logic '0'), the model provides low equalization. When  $EQ > 100\ \text{mV DC}$  (logic '1'), the model provides high equalization. For more information on the AD8159 equalization settings, please refer to the Advance Specification.

The output (OP/ON) of the model is a CML-level signal (800 mV differential peak-to-peak) referenced to the VCC supply. It is a representation of the *on-chip* equalized signal, and it illustrates the capability of the device to reduce the jitter in a degraded waveform. Since this is an on-chip signal, it can not be directly compared to a waveform obtained from the real device.

## Input Subcircuit Pin Descriptions

IP, IN - Differential input  
OP, ON - Differential output  
EQ - EQ level control  
VTTI - Input termination supply  
VCC - Positive supply voltage

## Output Model

Figure 2 describes the AD8159 output model.

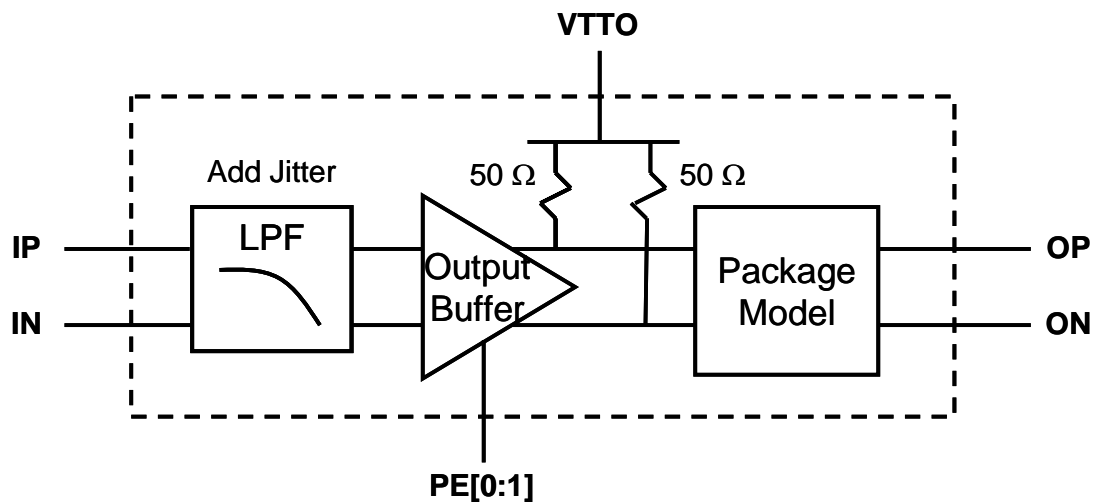


Figure 2: AD8159 output model.

The inputs to the model are high impedance pins (IP/IN) which accept a PECL/CML-type signal. The low-pass filter adds a small amount of deterministic jitter to the signal to mimic the jitter that would typically be accumulated through the data path. The two control pins PE[0:1] select the desired level of pre-emphasis. If the voltage at a control pin is < 100 mV, it is treated as a logic '0'. If the voltage is > 100 mV, it is treated as a logic '1'. For more information on the AD8159 pre-emphasis settings, please refer to the Advance Specification.

The output buffer drives 50 Ω on-chip resistors that are terminated to the VTTI supply. The package model is identical to that of the AD8159 Input Model.

## **Output Subcircuit Pin Descriptions**

IP, IN - Differential input  
OP, ON - Differential output  
PE[0] - Pre-emphasis level control (LSB)  
PE[1] - Pre-emphasis level control (MSB)  
VTTO - Output termination supply