High Speed Voltage Feedback Op Amps

In order to intelligently select the correct high speed op amp for a given application, an understanding of the various op amp topologies as well as the tradeoffs between them is required. The two most widely used topologies are voltage feedback (VFB) and current feedback (CFB). An overview of these topologies has been presented in previous tutorials (MT-050, MT-051, MT-052), but the following discussion treats the frequency-related aspects of the two topologies in considerably more detail.

HIGH SPEED VOLTAGE FEEDBACK (VFB) OP AMP TOPOLOGIES

A voltage feedback (VFB) op amp is distinguished from a current feedback (CFB) op amp by circuit topology. The VFB op amp is certainly the most popular in low frequency applications, but the CFB op amp has some advantages at high frequencies. We will discuss high speed CFB in detail in Tutorial MT-057, but first the more traditional VFB architecture.

Early IC voltage feedback op amps were made on "all NPN" processes. These processes were optimized for NPN transistors—the "lateral" PNP transistors had relatively poor performance. Some examples of these early VFB op amps which used these poor quality PNPs include the 709, the LM101 and the 741.

Lateral PNPs were generally only used as current sources, level shifters, or for other non-critical functions. A simplified diagram of a typical VFB op amp manufactured on such a process is shown in Figure 1 below.

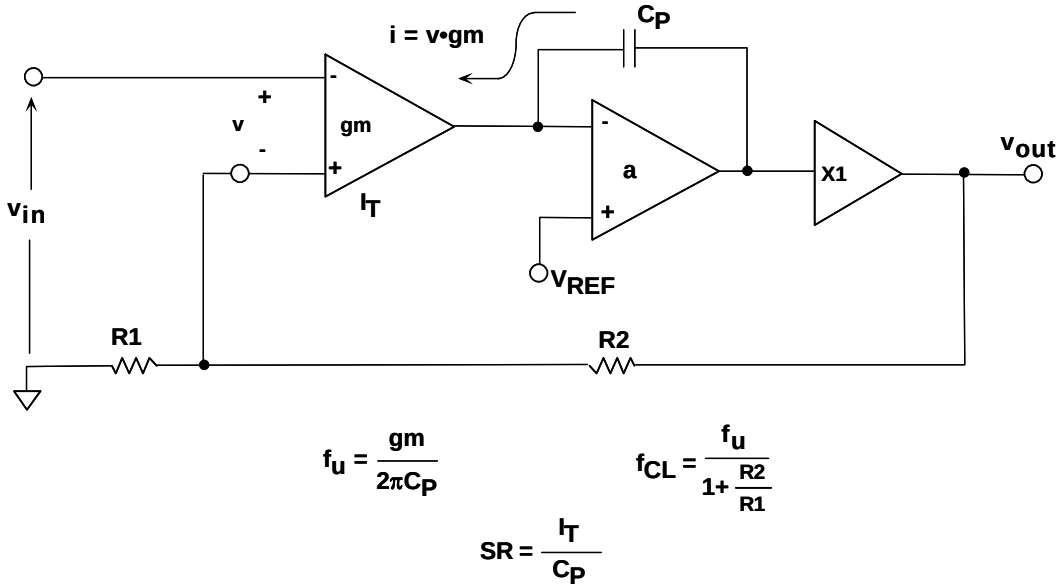

Figure 1: Voltage Feedback (VFB) Op Amp Designed on an "All NPN" IC Process

The input stage is a differential pair (sometimes called a *long-tailed pair*) consisting of either a bipolar pair (Q1, Q2) or a FET pair. This "g_m" (transconductance) stage converts the small-signal differential input voltage, v, into a current, i, and its transfer function is measured in units of conductance, 1/Ω, (or mhos). The small-signal emitter resistance, r_e, is approximately equal to the reciprocal of the small-signal g_m.

The formula for the small-signal g_m of a single bipolar transistor is given by the following equation:

$$g_m = \frac{1}{r_e} = \frac{q}{kT}(I_C) = \frac{q}{kT}\left(\frac{I_T}{2}\right), \text{ or} \qquad \text{Eq. 1}$$

$$g_m \approx \left(\frac{1}{26\text{mV}}\right)\left(\frac{I_T}{2}\right), \qquad \text{Eq. 2}$$

where I_T is the differential pair tail current, I_C is the collector quiescent bias current ($I_C = I_T/2$), q is the electron charge, k is Boltzmann's constant, and T is absolute temperature. At +25°C, V_T = kT/q= 26 mV (often called the *thermal voltage*, V_T).

As we will see shortly, the amplifier unity gain-bandwidth product, f_u, is equal to $g_m/2\pi C_P$, where the capacitance C_P is used to set the dominant pole frequency. For this reason, the tail current, I_T, is made proportional to absolute temperature (PTAT). This current tracks the variation in r_e with temperature thereby making g_m independent of temperature. It is relatively easy to make C_P reasonably constant over temperature.

The Q2 collector output of the g_m stage drives the emitter of a lateral PNP transistor (Q3). It is important to note that Q3 is not used to amplify the signal, only to level shift, i.e., the signal current variation in the collector of Q2 appears at the collector of Q3. The collector current of Q3 develops a voltage across high impedance node A, and C_P sets the dominant pole of the amplifier. Emitter follower Q4 provides a low impedance output.

The effective load at the high impedance node A can be represented by a resistance, R_T, in parallel with the dominant pole capacitance, C_P. The small-signal output voltage, v_{out}, is equal to the small-signal current, i, multiplied by the impedance of the parallel combination of R_T and C_P.

Figure 2 below shows a simple model for the single-stage amplifier and the corresponding Bode plot. The Bode plot is conveniently constructed on a log-log scale.

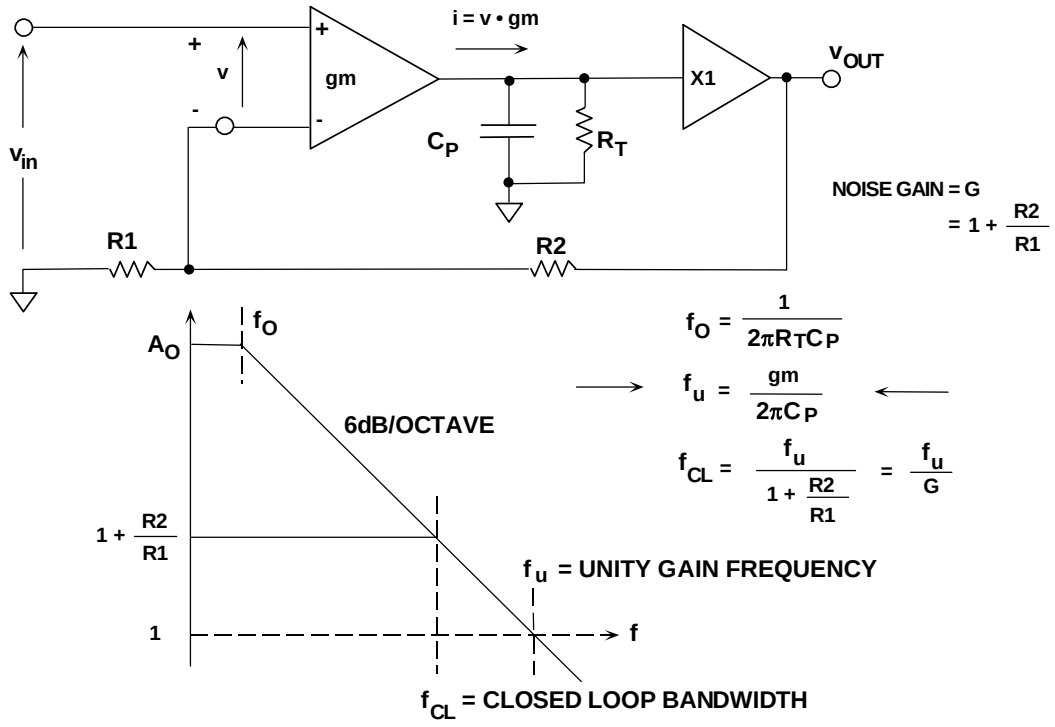

Figure 2: Model and Bode Plot for a VFB Op Amp

The low frequency breakpoint, f_O, is given by:

$$f_o = \frac{1}{2\pi R_T C_P}. \qquad \text{Eq. 3}$$

Note that the high frequency response is determined solely by g_m and C_P:

$$v_{out} = v \cdot \frac{g_m}{j\omega C_P}. \qquad \text{Eq. 4}$$

The unity gain-bandwidth frequency, f_u, occurs where $|v_{out}| = |v|$. Letting $\omega = 2\pi f_u$ and $|v_{out}| = |v|$, Eq. 4 can be solved for f_u,

$$f_u = \frac{g_m}{2\pi C_P}. \qquad \text{Eq. 5}$$

We can use feedback theory to derive the closed-loop relationship between the circuit's signal input voltage, v_{in}, and its output voltage, v_{out}:

$$\frac{v_{out}}{v_{in}} = \frac{1+\frac{R2}{R1}}{1+\frac{j\omega C_P}{g_m}\left(1+\frac{R2}{R1}\right)}. \quad \text{Eq. 6}$$

At the op amp 3 dB closed-loop bandwidth frequency, f_{cl}, the following is true:

$$\frac{2\pi f_{cl} C_P}{g_m}\left(1+\frac{R2}{R1}\right) = 1, \text{ and hence} \quad \text{Eq. 7}$$

$$f_{cl} = \frac{g_m}{2\pi C_P}\left(\frac{1}{1+\frac{R2}{R1}}\right), \text{ or} \quad \text{Eq. 8}$$

$$f_{cl} = \frac{f_u}{1+\frac{R2}{R1}}. \quad \text{Eq. 9}$$

This demonstrates the fundamental property of VFB op amps: *The closed-loop bandwidth multiplied by the closed-loop gain is a constant*, i.e., the VFB op amp exhibits a constant gain-bandwidth product over most of the usable frequency range.

As noted previously, some VFB op amps (called *de-compensated*) are not stable at unity gain, but designed to be operated at some minimum (higher) amount of closed-loop gain. However, even for these op amps, the gain-bandwidth product is still relatively constant over the region of stability.

Now, consider the following typical example: I_T = 100 µA, C_P = 2 pF. We find that:

$$g_m = \frac{I_T/2}{V_T} = \frac{50\mu A}{26mV} = \frac{1}{520\Omega} \quad \text{Eq. 10}$$

$$f_u = \frac{g_m}{2\pi C_P} = \frac{1}{2\pi(520)(2\cdot 10^{-12})} = 153MHz. \quad \text{Eq. 11}$$

Now, we must consider the large-signal response of the circuit. The slew-rate, SR, is simply the total available charging current, $I_T/2$, divided by the dominant pole capacitance, C_P. For the example under consideration,

$$I = C\frac{dv}{dt}, \ \frac{dv}{dt} = SR, \ SR = \frac{I}{C} \quad \text{Eq. 12}$$

$$SR = \frac{I_T / 2}{C_P} = \frac{50\mu A}{2pF} = 25V/\mu s. \quad \text{Eq. 13}$$

The full-power bandwidth (FPBW) of the op amp can now be calculated from the formula:

$$FPBW = \frac{SR}{2\pi A} = \frac{25V/\mu s}{2\pi \cdot 1V} = 4MHz, \quad \text{Eq. 14}$$

where A is the peak amplitude of the output signal. If we assume a 2 V peak-to-peak output sinewave (certainly a reasonable assumption for high speed applications), then we obtain a FPBW of only 4 MHz, even though the small-signal unity gain-bandwidth product is 153 MHz! For a 2 V p-p output sinewave, distortion will begin to occur much lower than the actual FPBW frequency. We must increase the SR by a factor of about 40 in order for the FPBW to equal 153 MHz. The only way to do this is to increase the tail current, I_T, of the input differential pair by the same factor. This implies a bias current of 4 mA in order to achieve a FPBW of 160 MHz. We are assuming that C_P is a fixed value of 2 pF and cannot be lowered by design. These calculations are summarized below in Figure 3.

- **Assume that I_T = 100µA, Cp = 2pF**

  $$g_m = \frac{I_C}{V_T} = \frac{50\mu A}{26mV} = \frac{1}{520\Omega}$$

  $$f_u = \frac{g_m}{2\pi\ Cp} = 153MHz$$

- **Slew Rate = SR =**

  BUT FOR 2V PEAK-PEAK OUTPUT (A = 1V)

  $$FPBW = \frac{SR}{2\pi\ A} = 4MHz$$

- **Must increase I_T to 4mA to get FPBW = 160MHz!!**

- **Reduce g_m by adding emitter degeneration resistors**

Figure 3: VFB Op Amp Bandwidth And Slew Rate Calculations

In practice, the FPBW of the op amp should be approximately 5 to 10 times the maximum output frequency in order to achieve acceptable distortion performance (typically 55-80 dBc @ 5 to 20 MHz, but actual system requirements vary widely).

Notice, however, that increasing the tail current causes a proportional increase in g_m and hence f_u. In order to prevent possible instability due to the large increase in f_u, g_m can be reduced by inserting resistors in series with the emitters of Q1 and Q2 (this technique, called *emitter degeneration*, also serves to linearize the g_m transfer function and thus also lowers distortion).

This analysis points out that a major inefficiency of conventional bipolar voltage feedback op amps is their inability to achieve high slew rates without proportional increases in quiescent current (assuming that C_P is fixed, and has a reasonable minimum value of 2 or 3 pF).

This of course is not meant to say that high speed op amps designed using this architecture are deficient, just that there are circuit design techniques available which allow equivalent performance at much lower quiescent currents. This is extremely important in portable battery operated equipment where every milliwatt of power dissipation is critical.

VFB OP AMPS DESIGNED ON COMPLEMENTARY BIPOLAR PROCESSES

With the advent of complementary bipolar (CB) processes having high quality PNP transistors as well as NPNs, VFB op amp configurations such as the one shown in the simplified diagram in Figure 4 below became popular.

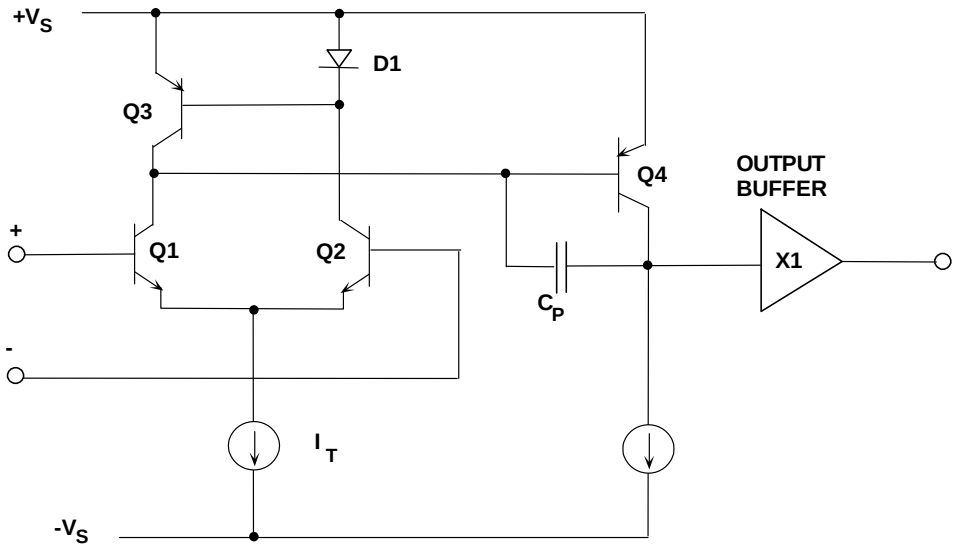

Figure 4: VFB op amp using two gain stages

Notice that the input differential pair (Q1, Q2) is loaded by a current mirror (Q3 and D1). We show D1 as a diode for simplicity, but it is actually a diode-connected PNP transistor (matched to Q3) with the base and collector connected to each other. This simplification will be used in many of the circuit diagrams to follow in this section. The common emitter transistor, Q4, provides a *second* voltage gain stage.

Since the PNP transistors are fabricated on a complementary bipolar process, they are high quality and matched to the NPNs, and therefore suitable for voltage gain. The dominant pole of the Fig. 4 amplifier is set by C_P, and the combination of the gain stage, Q4 and local feedback capacitor C_P is often referred to as a *Miller Integrator*. The unity-gain output buffer is usually a complementary emitter follower.

A model for this two-stage VFB op amp is shown in Figure 5 below. Notice that the unity gain-bandwidth frequency, f_u, is still determined by the input stage g_m and the dominant pole capacitance, C_P. The second gain stage increases the dc open-loop gain, but maximum slew rate is still limited by the input stage tail current as: $SR = I_T/C_P$.

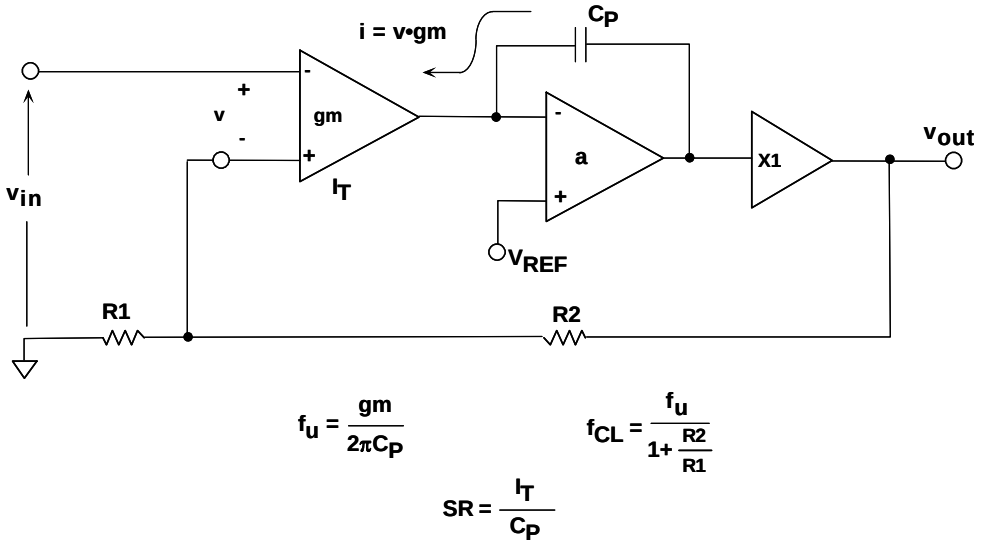

Figure 5: Model for Two Stage VFB Op Amp

A two-stage amplifier topology such as this is widely used throughout the IC industry in VFB op amps, both precision and high speed.

Another popular VFB op amp architecture is the *folded cascode* as shown in Figure 6. An industry-standard video amplifier family (the AD847) is based on this architecture. This circuit also takes advantage of the fast PNPs available on a CB process. The differential signal currents in the collectors of Q1 and Q2 are fed to the emitters of a PNP cascode transistor pair (hence the term *folded cascode*). The collectors of Q3 and Q4 are loaded with the current mirror, D1 and Q5, and voltage gain is developed at the Q4-Q5 node. This single-stage architecture uses the junction capacitance at the high-impedance node for compensation (C_{STRAY}).

Some variations of the design bring this node to an external pin so that additional external capacitance can be added if desired.

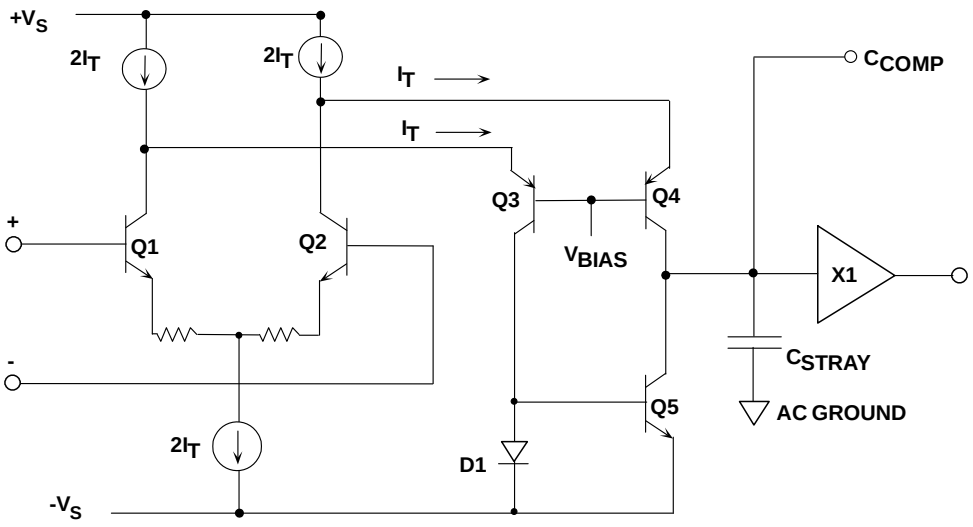

Figure 6: AD847-Family Folded Cascode Simplified Circuit

With no emitter degeneration resistors in Q1 and Q2, and no additional external compensating capacitance, this circuit is only stable for high closed-loop gains. However, unity-gain compensated versions of this family are available which have the appropriate amount of emitter degeneration.

The availability of JFETs on a CB process allows not only low input bias current but also improvements in the slew rate tradeoff, which must be made between g_m and I_T found in bipolar input stages. Figure 7 shows a simplified diagram of the AD845 16 MHz op amp. JFETs have a much lower g_m per mA of tail current than a bipolar transistor. This lower g_m of the FET allows the input tail current (hence the slew rate) to be increased, without having to increase C_P to maintain stability.

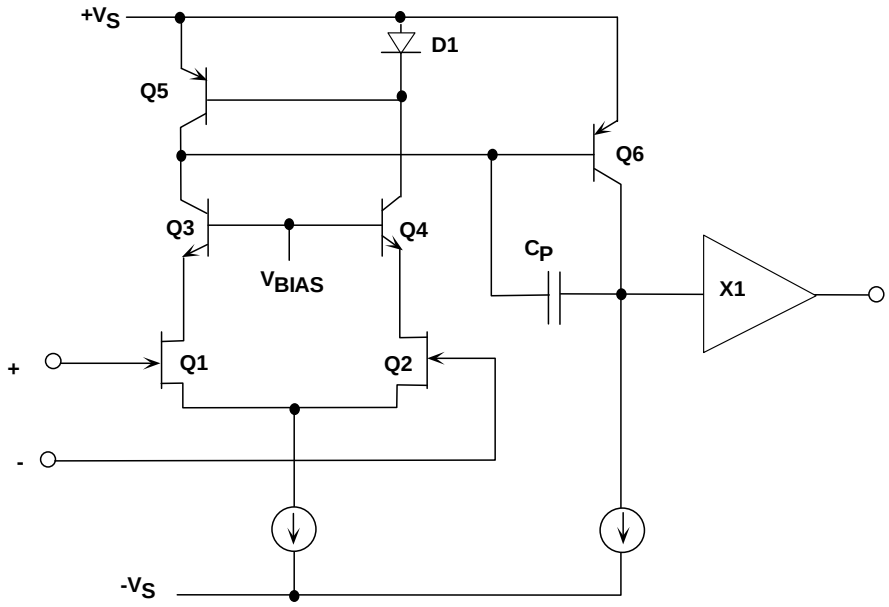

Figure 7: AD845 BiFET 16MHz Op Amp Simplified Circuit

The unusual thing about this seemingly poor performance of the JFET is that it is exactly what is needed for a fast, high SR input stage. For a typical JFET, the value of g_m is approximately $I_s/1V$ (I_s is the source current), rather than $I_c/26mV$ for a bipolar transistor, i.e., the FET g_m is about 40 times lower. This allows much higher tail currents (and higher slew rates) for a given g_m when JFETs are used as the input stage.

Until recently, op amp designers had to make the above tradeoffs between the input g_m stage quiescent current and the slew-rate and distortion performance. ADI has patented a circuit core which supplies *current-on-demand*, to charge and discharge the dominant pole capacitor, C_P, while allowing the quiescent current to be small. The additional current is proportional to the fast slewing input signal and adds to the quiescent current. A simplified diagram of the basic core cell is shown in Figure 8 below.

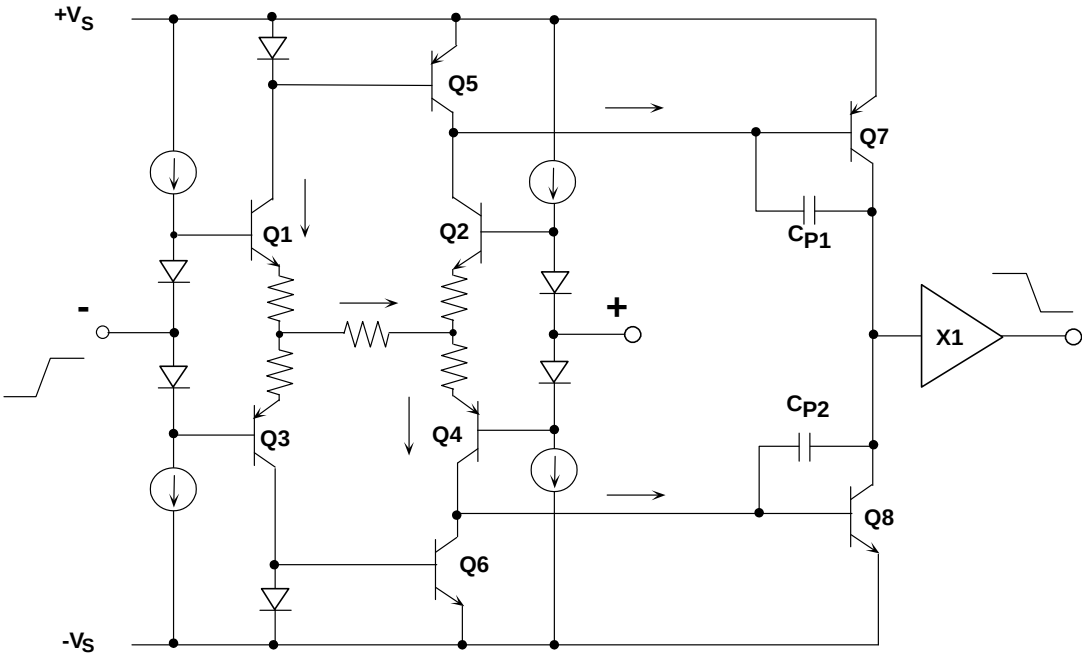

Figure 8: "Quad-Core" VFB gm Stage forCurrent-on-Demand

The *quad-core* (g_m stage) consists of transistors Q1, Q2, Q3, and Q4 with their emitters connected together as shown. Consider a positive step voltage on the inverting input. This voltage produces a proportional current in Q1 that is mirrored into C_{P1} by Q5. The current through Q1 also flows through Q4 and C_{P2}.

At the dynamic range limit, Q2 and Q3 are correspondingly turned off. Notice that the charging and discharging current for C_{P1} and C_{P2} is not limited by the quad core bias current. In practice, however, small current-limiting resistors are required forming an "H" resistor network as shown. Q7 and Q8 form the second gain stage (driven differentially from the collectors of Q5 and Q6), and the output is buffered by a unity-gain complementary emitter follower.

The quad core configuration is patented (see Reference 1), as well as the circuits that establish the quiescent bias currents (not shown in Fig. 8). The "quad core" is also often referred to as an "H-Bridge" core. A number of VFB op amps using this proprietary configuration have been released and have unsurpassed high frequency low distortion performance, bandwidth, and slew rate at low quiescent current levels. Figure 9 lists a few of the voltage feedback op amps using this architecture for comparison.

LISTED IN ORDER OF DECREASING SUPPLY CURRENT

PART #	I_{SY} / AMP	BANDWIDTH	SLEWRATE
AD8045 (1)	19mA	1000MHz	1350V/µs
ADA4899-1 (1)	16.2mA	600MHz	310V/µs
AD8099 (1)	16mA	500MHz	1600V/µs
AD8074 (3)	10mA	600MHz	1600V/µs
AD8057 (1)	7.5mA	325MHz	1150V/µs
AD8038 (1)	1.5mA	350MHz	425V/µs

Number in ( ) indicates single, dual, triple, or quad

Figure 9: Some High Speed VFB Op Amps

REFERENCES

1. Hank Zumbahlen, *Basic Linear Design*, Analog Devices, 2006, ISBN: 0-915550-28-1. Also available as *Linear Circuit Design Handbook*, Elsevier-Newnes, 2008, ISBN-10: 0750687037, ISBN-13: 978-0750687034. Chapter 1.

2. Walter G. Jung, *Op Amp Applications*, Analog Devices, 2002, ISBN 0-916550-26-5, Also available as *Op Amp Applications Handbook*, Elsevier/Newnes, 2005, ISBN 0-7506-7844-5. Chapter 1.