Ultralow Noise VGA with Preamplifier and Programmable R_{IN}

Enhanced Product

AD8331-EP

FEATURES

- Ultralow noise preamplifier (preamp)
  - Input voltage noise: 0.74 nV/√Hz typical
  - Input current noise: 2.5 pA/√Hz typical
- −3 dB small signal bandwidth: 120 MHz typical
- Low power dissipation: 125 mW typical
- Wide gain range with programmable postamp
  - −4.5 dB to +43.5 dB in low gain mode
  - 7.5 dB to 55.5 dB in high gain mode
- Low output-referred noise: 48 nV/√Hz typical
- Active input impedance matching
- Optimized for 10-bit/12-bit ADCs
- Selectable output clamping level
- Single 5 V supply operation

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Extended industrial temperature range: −55°C to +105°C
- Controlled manufacturing baseline
- 1 assembly/test site
- 1 fabrication site
- Product change notification
- Qualification data available on request

APPLICATIONS

- Radars
- Ultrasound and sonar time-gain controls
- High performance automatic gain control (AGC) systems
- In-phase quadrature (I/Q) signal processing
- High speed ADC drivers

GENERAL DESCRIPTION

The AD8331-EP is a single-channel, ultralow noise, linear in dB, variable gain amplifier (VGA). Optimized for ultrasound systems, the device is usable as a low noise variable gain element at frequencies up to 120 MHz.

Included in the channel are an ultralow noise preamp (LNA), an X-AMP® VGA with 48 dB of gain range, and a selectable gain postamp with adjustable output limiting. The LNA gain is 19 dB with a single-ended input and differential outputs. Using a single resistor, the LNA input impedance can be adjusted to match a signal source without compromising noise performance.

FUNCTIONAL BLOCK DIAGRAM

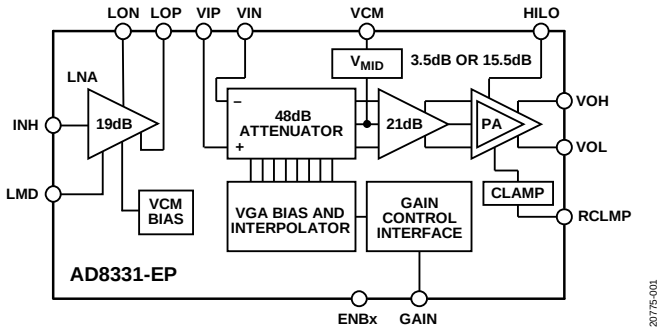

Figure 1.

The 48 dB gain range of the VGA makes this device suitable for a variety of applications. Excellent bandwidth uniformity is maintained across the entire range. The gain control interface provides precise linear in dB scaling of 50 dB/V for control voltages between 100 mV and 0.95 V. Factory trim ensures excellent part to part gain matching.

Differential signal paths result in superb second- and third-order distortion performance and low crosstalk.

The low output referred noise of the VGA is advantageous in driving high speed differential analog-to-digital converters (ADCs). The gain of the post amplifier (PA) can be pin selected to 3.5 dB or 15.5 dB to optimize gain range and output noise for 12-bit or 10-bit converter applications. The output can be limited to a user selected clamping level, preventing input overload to a subsequent ADC. An external resistor adjusts the clamping level.

The operating temperature is specified across the −55°C to +105°C extended industrial range.

Additional application and technical information can be found in the AD8331 data sheet.

Rev. 0 Document Feedback

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REVISION HISTORY

5/2019—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, supply voltage (V_S) = 5 V, load resistance (R_L) = 500 Ω, source resistance (R_S) = input resistance (R_{IN}) = 50 Ω, shunt feedback resistance (R_{IZ}) = 280 Ω, input shunt capacitance (C_{SH}) = 22 pF, frequency (f) = 10 MHz, RCLMP = ∞, load capacitance (C_L) = 1 pF, VCM pin floating, −4.5 dB to +43.5 dB gain (HILO = low), and differential output voltage, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit[1]
LNA CHARACTERISTICS					
Gain	Single-ended input to differential output		19		dB
	Input to output (single-ended)		13		dB
Input Voltage Range	AC-coupled		±275		mV
Input Resistance	R_{IZ} = 280 Ω		50		Ω
	R_{IZ} = 412 Ω		75		Ω
	R_{IZ} = 562 Ω		100		Ω
	R_{IZ} = 1.13 kΩ		200		Ω
	R_{IZ} = ∞		6		kΩ
Input Capacitance			13		pF
Output Impedance	Single-ended, either output		5		Ω
−3 dB Small Signal Bandwidth	Output voltage (V_{OUT}) = 0.2 V p-p		130		MHz
Slew Rate			650		V/µs
Input Voltage Noise	R_S = 0 Ω, high or low gain mode, R_{IZ} = ∞, f = 5 MHz		0.74		nV/√Hz
Input Current Noise	R_{IZ} = ∞, high or low gain mode, f = 5 MHz		2.5		pA/√Hz
Noise Figure	f = 10 MHz, LOP output				
Active Termination Match	R_S = R_{IN} = 50 Ω		3.7		dB
Unterminated	R_S = 50 Ω, R_{IZ} = ∞		2.5		dB
Harmonic Distortion at LOP	V_{OUT} = 0.5 V p-p, single-ended, f = 10 MHz				
Second Harmonic Distortion (HD2)			−56		dBc
Third Harmonic Distortion (HD3)			−70		dBc
Output Short-Circuit Current	Pin LON, Pin LOP		165		mA
LNA AND VGA CHARACTERISTICS					
−3 dB Signal Bandwidth					
Small	V_{OUT} = 0.2 V p-p		120		MHz
Large	V_{OUT} = 2 V p-p		110		MHz
Slew Rate					
	Low gain mode		300		V/µs
	High gain mode		1200		V/µs
Input Voltage Noise	R_S = 0 Ω, high or low gain mode, R_{IZ} = ∞, f = 5 MHz		0.82		nV/√Hz
Noise Figure	Gain voltage (V_{GAIN}) = 1.0 V				
Active Termination Match	R_S = R_{IN} = 50 Ω, f = 10 MHz, measured		4.15		dB
	R_S = R_{IN} = 200 Ω, f = 5 MHz, simulated		2.0		dB
Unterminated	R_S = 50 Ω, R_{IZ} = ∞, f = 10 MHz, measured		2.5		dB
	R_S = 200 Ω, R_{IZ} = ∞, f = 5 MHz, simulated		1.0		dB
Output Referred Noise					
	V_{GAIN} = 0.5 V, low gain mode		48		nV/√Hz
	V_{GAIN} = 0.5 V, high gain mode		178		nV/√Hz
Output Impedance, Postamplifier	DC to 1 MHz		1		Ω

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit[1]
Output Signal Range, Postamplifier	$R_L \geq 500\ \Omega$, unclamped, either pin		$V_{CM} \pm 1.125$		V
Differential			4.5		V p-p
Output Offset Voltage					
	Differential, $V_{GAIN} = 0.5$ V	−50	±5	+50	mV
	Common mode	−125	−25	+100	mV
Output Short-Circuit Current			45		mA
Harmonic Distortion	$V_{GAIN} = 0.5$ V, $V_{OUT} = 1$ V p-p, high gain mode				
HD2	f = 1 MHz		−88		dBc
HD3			−85		dBc
HD2	f = 10 MHz		−68		dBc
HD3			−65		dBc
Input 1 dB Compression Point	$V_{GAIN} = 0.25$ V, $V_{OUT} = 1$ V p-p, f = 1 MHz to 10 MHz		1		dBm
Two-Tone Intermodulation Distortion (IMD3)	$V_{OUT} = 1$ V p-p				
	$V_{GAIN} = 0.72$ V, f = 1 MHz		−80		dBc
	$V_{GAIN} = 0.5$ V, f = 10 MHz		−72		dBc
Output Third-Order Intercept	$V_{GAIN} = 0.5$ V, $V_{OUT} = 1$ V p-p				
	f = 1 MHz		38		dBm
	f = 10 MHz		33		dBm
Overload Recovery	$V_{GAIN} = 1.0$ V, input voltage (V_{IN}) = 50 mV p-p/ 1 V p-p, f = 10 MHz		5		ns
Group Delay Variation	5 MHz < f < 50 MHz, full gain range		±2		ns
ACCURACY					
Absolute Gain Error[2]	$0.05\text{ V} < V_{GAIN} < 0.10$ V	−1	+0.5	+2	dB
	$0.10\text{ V} < V_{GAIN} < 0.95$ V	−1	±0.3	+1	dB
	$0.95\text{ V} < V_{GAIN} < 1.0$ V	−2	−1	+1	dB
Gain Law Conformance[3]	$0.1\text{ V} < V_{GAIN} < 0.95$ V		±0.2		dB
GAIN CONTROL INTERFACE	GAIN pin				
Gain Scaling Factor	$0.10\text{ V} < V_{GAIN} < 0.95$ V	48.5	50	51.5	dB/V
Post Amplifier Gain	Low gain mode (HILO = low)		3.5		dB
	High gain mode (HILO = high)		15.5		dB
Gain Range	Low gain mode		−4.5 to +43.5		dB
	High gain mode		7.5 to 55.5		dB
Input Voltage (V_{GAIN}) Range			0 to 1.0		V
Input Impedance			10		MΩ
Response Time	48 dB gain change to 90% full scale		500		ns
COMMON-MODE INTERFACE	VCM pin				
Input Resistance[4]	Current limited to ±1 mA		30		Ω
Output Common-Mode Offset Voltage	Common-mode voltage (V_{CM}) = 2.5 V	−125	−25	+100	mV
Voltage Range	$V_{OUT} = 2.0$ V p-p		1.5 to 3.5		V
ENABLE INTERFACE	ENBL AND ENBV pins				
Logic Level to Enable Power		2.25		5	V
Logic Level to Disable Power		0		1.0	V
Input Resistance	ENB pin		25		kΩ
	ENBL pin		40		kΩ
	ENBV pin		70		kΩ
Power-Up Response Time	$V_{INH} = 30$ mV p-p		300		µs
	$V_{INH} = 150$ mV p-p		4		ms

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit[1]
HILO GAIN RANGE INTERFACE	HILO pin				
Logic Level to Select Gain Range					
High		2.25		5	V
Low		0		1.0	V
Input Resistance			50		kΩ
OUTPUT CLAMP INTERFACE	RCLMP pin, high or low gain				
Accuracy	V_{OUT} = 1 V p-p (clamped)				
HILO = Low	RCLMP = 2.74 kΩ		±50		mV
HILO = High	RCLMP = 2.21 kΩ		±75		mV
MODE INTERFACE	MODE pin				
Logic Level for Gain Slope					
Positive		0		1.0	V
Negative		2.25		5	V
Input Resistance			200		kΩ
POWER SUPPLY	VPSL and VPOS pins				
Supply Voltage		4.5	5.0	5.5	V
Quiescent Current		20	25		mA
Power Dissipation	No signal		125		mW
Power-Down Current	VGA and LNA disabled	50	240	400	µA
LNA Current (ENBL)		7.5	11	15	mA
VGA Current (ENBV)		7.5	14	20	mA
Power Supply Rejection Ratio	V_{GAIN} = 0 V, f = 100 kHz		−68		dB

[1] All dBm values are referred to 50 Ω.
[2] The absolute gain refers to the theoretical gain expression in Equation 1 of the AD8331 data sheet.
[3] Best fit to linear in dB curve.
[4] The current is limited to ±1 mA typical.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Voltage	
Supply Voltage (VPSL, VPOS)	5.5 V
Input Voltage (INH)	V_S + 200 mV
ENBL, ENBV, HILO Voltage	V_S + 200 mV
GAIN Voltage	2.5 V
Power Dissipation	See Figure 2
Temperature	
Extended Industrial Range	−55°C to +105°C
Junction Temperature (T_J)	125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

POWER DERATING CURVES

Figure 2 shows the maximum power dissipation vs. ambient temperature.

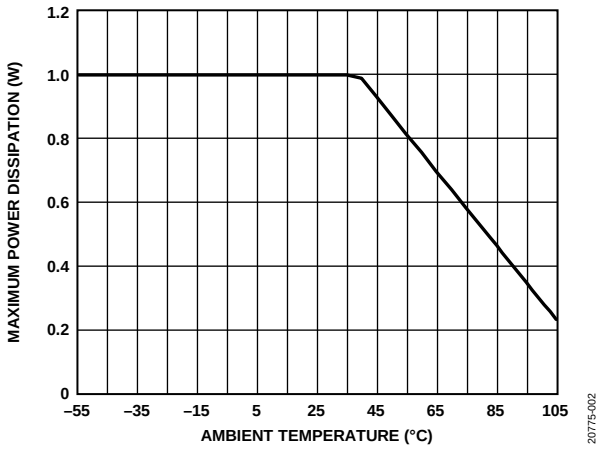


Figure 2. Maximum Power Dissipation vs. Ambient Temperature

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure, and θ_{JC} is the junction to case thermal resistance measured at package top.

Table 3. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}[2]	Unit
RQ-20	86	34	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board. See JEDEC JESD-51.
[2] Thermal impedance simulated values are based on a JEDEC 1S0P thermal test board. See JEDEC JESD-51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

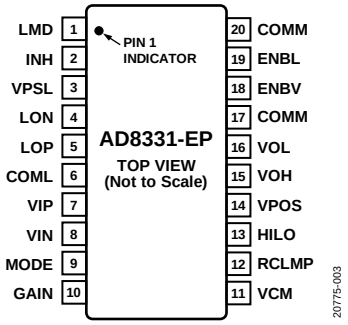


Figure 3. Pin Configuration

Table 4. Pin Function Description

Pin No.	Mnemonic	Description
1	LMD	LNA Midsupply Bypass Pin. Connect a capacitor to LMD to achieve a midsupply high frequency bypass.
2	INH	LNA Input.
3	VPSL	LNA 5 V Supply.
4	LON	LNA Inverting Output.
5	LOP	LNA Noninverting Output.
6	COML	LNA Ground.
7	VIP	VGA Noninverting Input.
8	VIN	VGA Inverting Input.
9	MODE	Gain Slope Logic Input.
10	GAIN	Gain Control Voltage.
11	VCM	Common-Mode Voltage.
12	RCLMP	Output Clamping Level.
13	HILO	Gain Range Select (High or Low).
14	VPOS	VGA 5 V Supply.
15	VOH	Noninverting VGA Output.
16	VOL	Inverting VGA Output.
17, 20	COMM	VGA Grounds.
18	ENBV	VGA Enable.
19	ENBL	LNA Enable.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = 5 V, R_L = 500 Ω, R_S = R_{IN} = 50 Ω, R_{IZ} = 280 Ω, C_{SH} = 22 pF, f = 10 MHz, R_{CLMP} = ∞, C_L = 1 pF, VCM pin floating, −4.5 dB to +43.5 dB gain (HILO = low), and differential output voltage, unless otherwise noted.

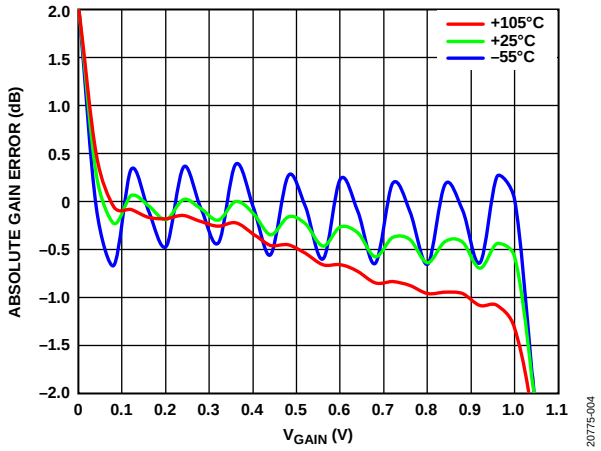


Figure 4. Absolute Gain Error vs. V_{GAIN} at Three Temperatures

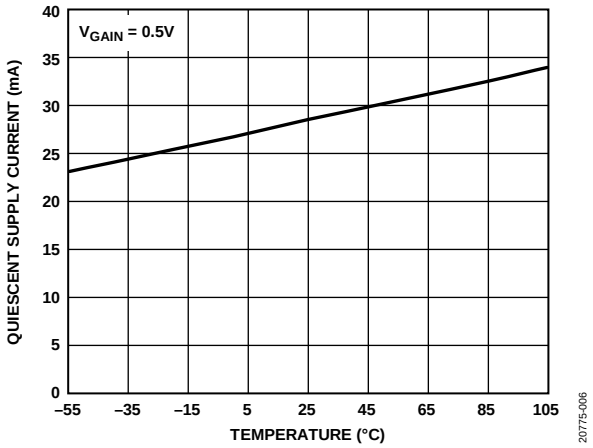


Figure 6. Quiescent Supply Current vs. Temperature

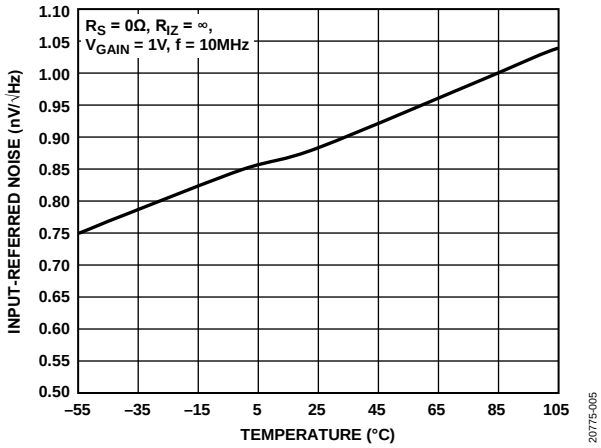
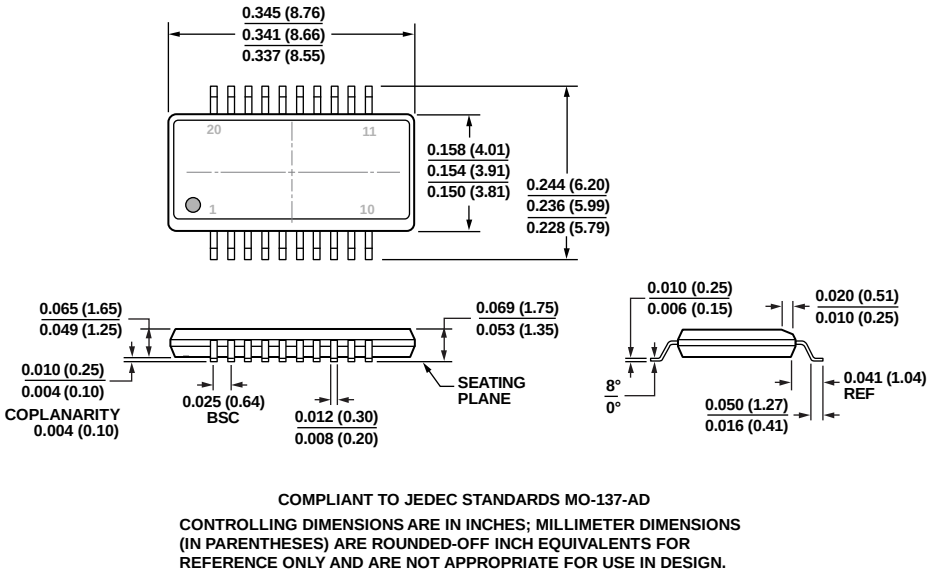


Figure 5. Input-Referred Noise vs. Temperature

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-137-AD

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

09-12-2014-A

Figure 7. 20-Lead Shrink Small Outline Package [QSOP]
(RQ-20)
Dimensions shown in Inches and (millimeters)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8331TRQZ-EP	−55°C to +105°C	20-Lead Shrink Small Outline Package [QSOP]	RQ-20
AD8331TRQZ-EP-R7	−55°C to +105°C	20-Lead Shrink Small Outline Package [QSOP]	RQ-20

[1] Z = RoHS Compliant Part.

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