AN-1192
APPLICATION NOTE

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Designing with the AD8338

by David Hunter

INTRODUCTION

The low power, high dynamic range AD8338 variable gain amplifier (VGA) provides many solutions to real-world systems through the device's rich feature set. Traditionally, VGAs are used in many applications, such as signal level normalization, programmable gain systems, dynamic range extension, and automatic gain control.

The core of the device gives the user a total dynamic range of 80 dB, which is configured through the GAIN pin. With a minimalist design, a gain of 1 to 10,000 is achieved in a board area as small as 18 mm^2. Upon the application of external resistors, the part becomes one of the most flexible VGAs on the market by either offering a lower input noise, a VGA that can serve as a variable attenuation-to-gain amplifier, or even a higher total gain amplifier.

This application note describes the design of the AD8338 and how to use this device in a variety of situations. This includes general design practices as well as information on how to obtain particular extended operational modes. Several application examples are provided.

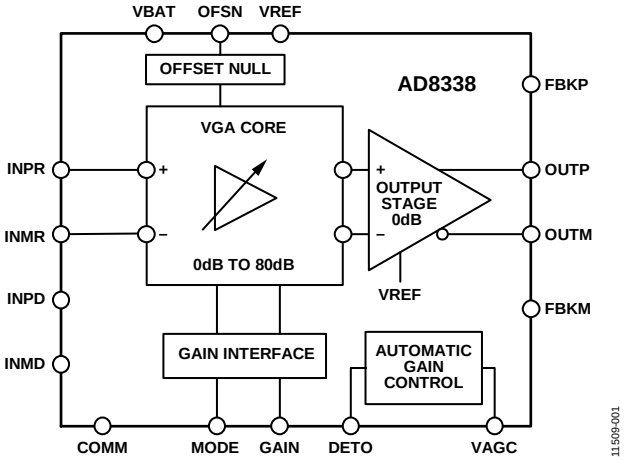

Figure 1. Block Diagram

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REVISION HISTORY

6/13—Revision 0: Initial Version

DESIGN CONSIDERATIONS

EFFECTIVE DESIGN

Effective design of the AD8338 requires an understanding of its strengths and weaknesses. The low power nature of the device provides longer operation in battery applications and minimizes power consumption in fixed installation systems. However, the low operating current of the AD8338, a key feature of the device, introduces a few limits that must be understood to use the part most effectively. Generally, the trade-offs for power are bandwidth and slew rate.

At mid-gain (40 dB), the AD8338 typically consumes 3 mA of current. The normal operating power on a 3 V supply is then only 9 mW quiescent operating supply. Compare this to the device's sister part: the AD8330 at a current of 20 mA on a 5.0 V supply, operates at nearly 10% of the power. However, unlike the AD8330, the AD8338 does not offer 1.5 kV/µs of slew rate, nor does it offer a −3 dB point operation to 150 MHz. However, unlike the AD8330, it offers 30 dB more gain, and many additional features to shape the performance of the design. The AD8338 then, is best applied for baseband or lower frequency intermediate frequency (IF) applications, where signals of interest are below 18 MHz and are small in magnitude.

For the power supply, the device operates from 3.0 V to 5.0 V. However, the internal reference voltage of 1.50 V sets the bias for the device, regardless of supply. This then means that the signal path of the AD8338 is normalized to a 3.0 V system, independent of supply considerations.

The LFCSP-16 package provides the user a very small solution for this highly integrated device. Some layout considerations are required for the best use case. In general, observe the following layout considerations:

- Inputs INMR/INMD and INPR/INPD should be kept close together and equal in length.
- Supply bypassing capacitors should be as close as reasonable for the design.
- When using external resistors, short the INMR and INPR inputs together to prevent possible instability, either directly or with a resistor of appropriate value.
- Exercise care with the GAIN and VAGC pins to minimize modulation effects.

OUTPUTS OF THE AD8338

To obtain the best performance from the AD8338, the design of the signal chain should begin with the output. Per the data sheet, the three key features to note are

- Small signal bandwidth of 18 MHz
- Slew rate of 50 V/µs
- Output swing of 2.8 V peak-to-peak

The slew rate and output swing specifications provide information about the large signal functions of the device. At the limits, each output swings about 700 mV from the 1.5 V reference.

Figure 2 shows the outputs swinging ±700 mV around the 1.5 V reference the difference of the two outputs becomes an effective swing of ±1.4 V (achieving the 2.8 V p-p as described in the data sheet).

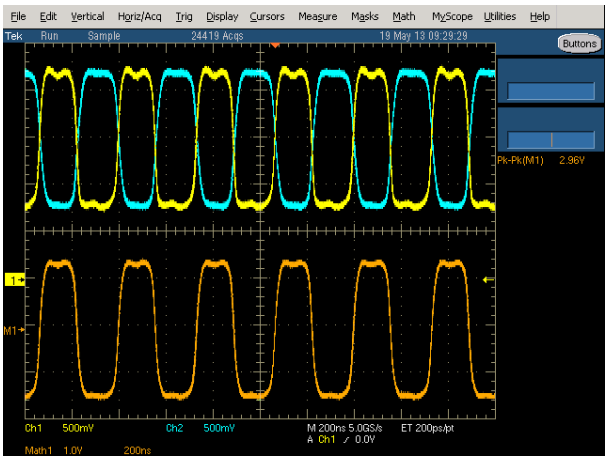

Figure 2. Output Waveforms with Difference Function Showing the Total Swing

In the overdriven state, the waveform is clipped which can potentially compromise the signal's integrity through losing amplitude information. An additional complication to be aware of besides overdriven outputs is limited slew limits.

While the small signal bandwidth is specified over all gains at 18 MHz, this does not mean the output can differentially swing ±1.4 V at this frequency. Supposing that the expected output was a single-ended amplitude of 0.7 V at a full 18 MHz, the function would be

$$V(t) = 0.7\sin(2\pi 18 \times 10^6 t) \quad (1)$$

The rate of change is given by the derivative of the signal

$$\frac{dV(t)}{dt} = 2\pi 18 \times 10^6 \times 0.7\cos(2\pi 18 \times 10^6 t) \quad (2)$$

At the instant where time t is zero, the peak rate of change is as follows or about 79 V per microsecond.

$$\frac{dV(t)}{dt} = 79.17 \times 10^6 V/s \quad (3)$$

This is almost 30 V/µs more than the AD8338 can offer. As a consequence then, for large output signals, the maximum effective frequency is

$$\frac{50V}{\mu s} = \frac{0.7\times 2\pi f}{10^6} \quad (4)$$

$$f = \frac{50\times 10^6}{2\pi 0.7} \quad (5)$$

From Equation 5, the frequency calculated comes out to approximately 11.3 MHz. Figure 3 provides a quick reference for large signal output amplitude values over frequency.

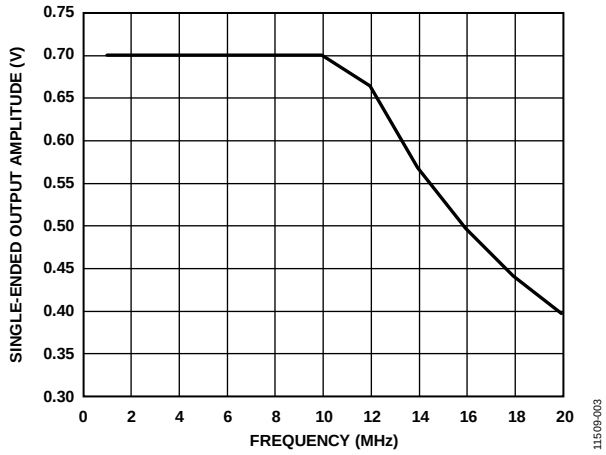

Figure 3. Large-Signal Amplitude over Frequency, Single Ended

An additional design consideration for the outputs is their loading. While the drivers have low output impedance over frequency, the linearity begins to degrade for a differential load of less than 1 kΩ.

Figure 4 illustrates a minimally loaded output (1.0 kΩ) of the AD8338. Here the two-tone intermodulation distortion is reasonably low. Figure 5 demonstrates the behavior of the output with a 200 Ω differential load.

Note the high level of intermodulation distortion compared to Figure 4. If the device following the AD8338 has an input impedance of less than 1 kΩ, a buffer, such as the AD8138, overcomes this obstacle.

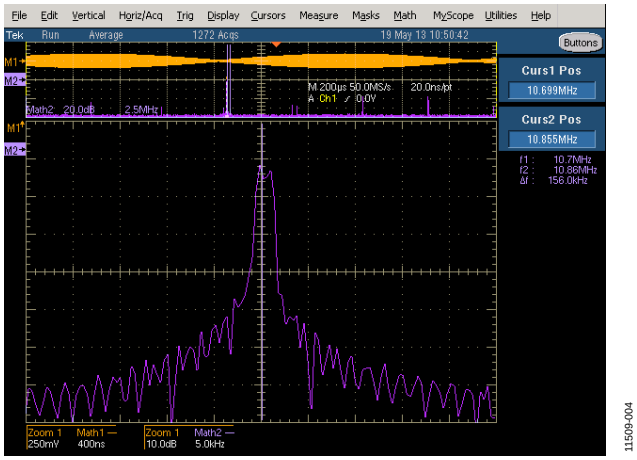

Figure 4. Two-Tone Distortion Analysis with Unloaded Outputs

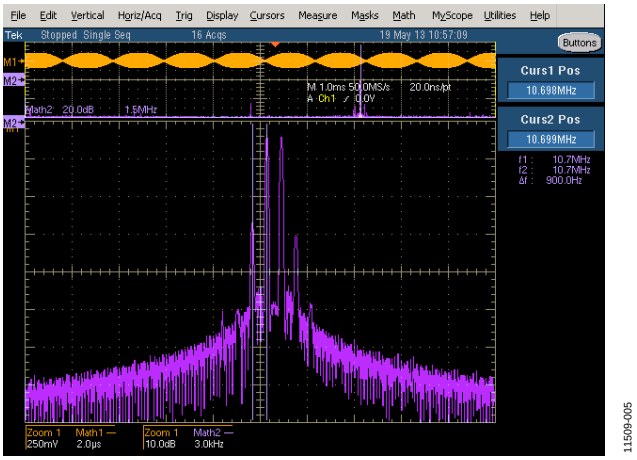

Figure 5. Two-Tone Distortion with 200 Ω Differential Load

The pinout of the AD8338 also provides the user with the ability to modify the feedback resistor values used in the output stage. This primarily provides a means to adjust the common-mode output from the 1.50 V set point.

Some users may wish to reduce the value of the feedback resistors, but for lower values, the output limits drop in proportion. This is due to the current output by the internal current-mode VGA block. The maximum amplitude of this current is fixed by design, therefore the maximum output amplitude is fixed by the feedback resistors. With an internal feedback resistor of 9.5 kΩ, the output is limited to ±0.7 V. With an additional 9.5 kΩ resistor in parallel, the output drops it ±0.35 V.

Design Example: Driving an AD8130

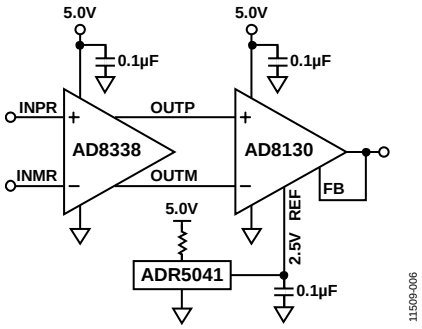

Figure 6. A Simple, Differential-to-Single-Ended, Solution Using an AD8130 Amplifier

In a situation where the user needs to convert the differential output of the AD8338 to a single-ended signal, while maintaining the best possible linearity, a follower amplifier, such as the AD8130, is an excellent choice.

The AD8130 is a high speed, high input impedance, differential-to-single-ended amplifier that provides a complete solution without the need for external components. The AD8130 states that this device offers a differential input impedance of 6 MΩ and a common-mode input impedance of 4 MΩ.

However, there are a few trade-offs. The minimum supply of the AD8130 is 4.5 V, which makes the design specific to a 5.0 V power supply. Additionally, the output of the AD8130 is limited to the range bound by 1.1 V from each rail (1.1 V to 3.9 V). This will achieve a full signal swing of 2.8 V p-p on the output, which matches the differential output from the AD8338.

A reference is also required for the correct application of the AD8130. If the reference is set away from a midscale of 2.5 V, the effective range of the output will diminish.

Design Example: Passively Coupling the Output Stage

In cases of a tightly constrained power budget, the designer must keep the number of active devices low. In such cases, non-resistive passive components offer effective solutions at the cost of board area and (usually) higher component cost.

There are, in general, two design paths for passive coupling: transformers, and inductor capacitors (LC circuits). Transformers are commercially available through numerous vendors, including Mini-Circuits and Coilcraft. Transformers typically apply ferrite cores, which offer good impedance matching, over a reasonable range of bandwidth. In contrast, lumped element LC circuits provide good results over a very narrow range of bandwidth.

This example applies a Mini-Circuits ADT16-6T+ to convert the differential-output of the AD8338 to a single-ended output. In most RF designs, a characteristic impedance of 50 Ω is used, so the ADT16-6T+ is designed around 50 Ω as well. Careful design using some considerations for transformer application discards the 50 Ω limitation and enables the designer to use other impedance standards.

Effective use of a transformer requires an understanding of the following equations used in modeling transformers:

$$\frac{V_2}{N_2} = \frac{V_1}{N_1} \tag{6}$$

$$V_2 = V_1 \frac{N_2}{N_1} \tag{7}$$

$$I_2 N_2 = I_1 N_1 \tag{8}$$

$$I_2 = I_1 \frac{N_1}{N_2} \tag{9}$$

The terms denoted here with a subscripted 2 are the components of the secondary side, while terms denoted with a subscripted 1 are the components of the primary side. The term, N denotes the number of turns for the windings of the associated side of the transformer.

Equation 10 through Equation 13 provide a relationship from the primary side to the secondary side, or vise-versa, in an ideal case. These terms are used to calculate the impedance seen by the secondary winding.

$$Z_2 = \frac{V_2}{I_2} = \frac{V_1 \frac{N_2}{N_1}}{I_1 \frac{N_1}{N_2}} \tag{10}$$

$$Z_2 = \frac{V_1}{I_1} \times \left[\frac{N_2}{N_1} \times \frac{N_2}{N_1}\right] \tag{11}$$

$$Z_2 = \frac{V_1}{I_1} \times \left(\frac{N_2}{N_1}\right)^2 \tag{12}$$

Note, that

$$Z_1 = \frac{V_1}{I_1} \tag{13}$$

Thus,

$$Z_2 = Z_1 \times \left(\frac{N_2}{N_1}\right)^2 \tag{14}$$

From Equation 14, the relationship of secondary impedance to primary impedance is shown to be the square of the windings ratio. The ADT16-6T+ transformer's data sheet specifies an impedance ratio of 16:1, which is different the winding ratio. In this particular case, the primary impedance is 50 Ω, while the secondary impedance is 800 Ω, for a winding ratio of 1:4.

For the best linearity, the load on the AD8338 outputs must be at least 1 kΩ. From Equation 14, impedance Z2 can be set to 1.0 kΩ, which resolves impedance Z1 to 62.5Ω. However, if Z2

is set to 1.2 kΩ, the impedance Z1 resolves to 75 Ω, which is a common industry standard.

Before the transformer begins to couple energy from the primary winding into the secondary, the magnetizing inductance of the part sets the lower frequency of use. In this case, for a 50 Ω system the device's 3 dB points couple at 100 kHz and fall off at 70 MHz.

For this design, the output is set to 75 Ω and the input is designated at 1.2 kΩ. If the transformer's secondary windings are connected directly to the outputs of the AD8338, the transformer will present an effective short circuit to frequencies below the 3 dB coupling point. DC blocking capacitors will be needed, and their values must be determined by the coupling frequency of the transformer. It is then necessary to calculate the 3 dB high-pass corner of the transformer (with respect to the secondary side that is interfacing to the AD8338). A simple approximation can be made: the change in coupling frequency is proportionate to the ratio of the change in loading over 50 Ω. Therefore, for the new impedance on the 75 Ω port

$$F_{HP} = 100kHz \times \frac{75}{50} \quad (15)$$

$$F_{HP} = 150kHz \quad (16)$$

Now knowing the approximated high-pass 3 dB corner of the transformer, output capacitors are chosen such that ac coupling begins just as the transformer begins coupling. A simple approach is to choose output capacitors of values that yield about 10 Ω at the corner frequency of interest. In this case, for a corner frequency of 150 kHz

$$C \approx \frac{1}{\omega Z} \quad (17)$$

$$C \approx \frac{1}{2\pi 150kHz \times 10\Omega} \quad (18)$$

$$C \approx 0.1\mu F \quad (19)$$

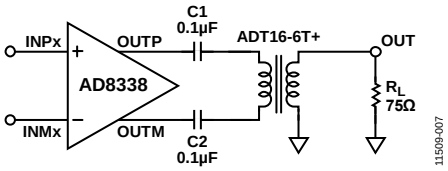

Figure 7. Example Circuit Using a Transformer

These techniques can also be applied for a 1:1 Balun transformer, however the challenge is finding an off-the-shelf transformer that can couple in at a low enough frequency.

Note that by the nature of the turns ratio, the voltage on the primary with a maximum signal swing on the output is

$$V_1 = \frac{N_1}{N_2} V_2 \quad (20)$$

Since the signal V2 is composed of the difference between OUTP and OUTM

$$V_1 = \frac{1}{4}(\pm 0.7 - \mp 0.7) \quad (21)$$

$$V_1 = \pm 0.350V \quad (22)$$

Note that Equation 21 expresses a voltage, V1, which changes as an instantaneous value of the difference of the two signals. In the case that OUTP is positive, OUTM will be negative. When OUTP is negative, OUTM will be positive.

One key attribute to keep in mind is that power is conserved in this impedance transformation. With a 75 Ω load, a peak current of 4.67 mA is obtained, while the AD8338 outputs are providing 1.17 mA into an equivalent of 1.2 kΩ load.

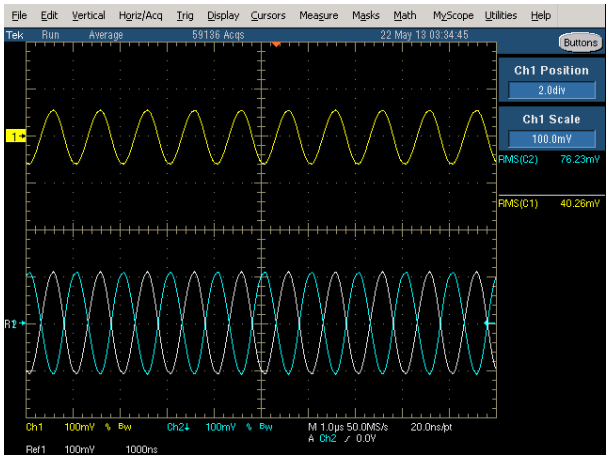

Figure 8. Output of the Transformer (CH1, yellow) from the Differential Input Signal (CH2/CH3, blue/gray) from the Circuit Shown in Figure 7

In Figure 8, each output produces an rms total output of 162 mV, while the output of the transformer is 40 mV rms.

INPUTS TO THE AD8338

Arguably, the input stage of the AD8338 makes it unique among other VGAs. The input of the device sets the limit on the input dynamic range, noise, bandwidth and power match considerations. Upon careful attention to the design of the input stage, the designer fine tunes the device for application improvements.

Impact of Input Resistors on Gain

A second subject to be aware of for choosing input resistors is their effect on gain. As the data sheet specifies in Equation 6, when the voltage applied to the GAIN pin is 0.1, the minimum gain is

$$Gain(dB) = 20 \times \log\left(\frac{R_{FEEDBACK}}{R_{INPUT}}\right) - 26 \quad (23)$$

Maintaining the 9.5 kΩ feedback resistor, and using the 210 Ω input resistor in the example above, the minimum gain is found.

$$Gain(dB) = 20 \times \log\left(\frac{9500}{210}\right) - 26 \quad (24)$$

$$Gain(dB) = 7.1dB \quad (25)$$

When the voltage applied to the GAIN pin is 1.1 V, the maximum gain is

$$Gain(dB) = 80 + 7.1 \quad (26)$$

$$Gain(dB) = 87.1dB \quad (27)$$

Figure 9 plots the measured gain against the calculated gain when 210 Ω input resistors are used.

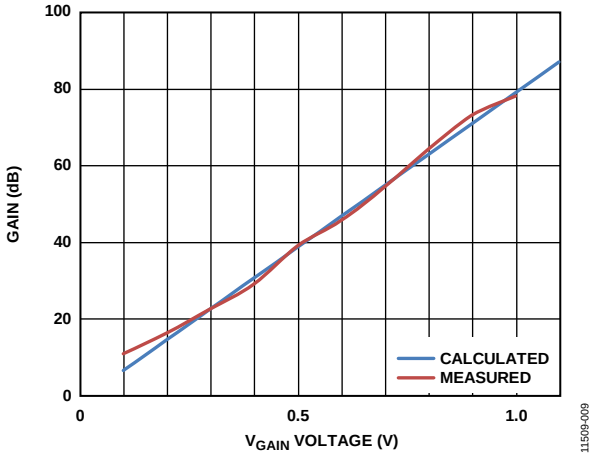

Figure 9. Gain vs. V_{GAIN}, Measured and Calculated with Input Resistors of 210 Ω

Similarly, this adjustment of gain works for larger input resistor values, resulting in an attenuation-to-gain VGA as shown in Figure 10. In this instance, the 210 Ω input resistors are replaced with 41.2 kΩ resistors.

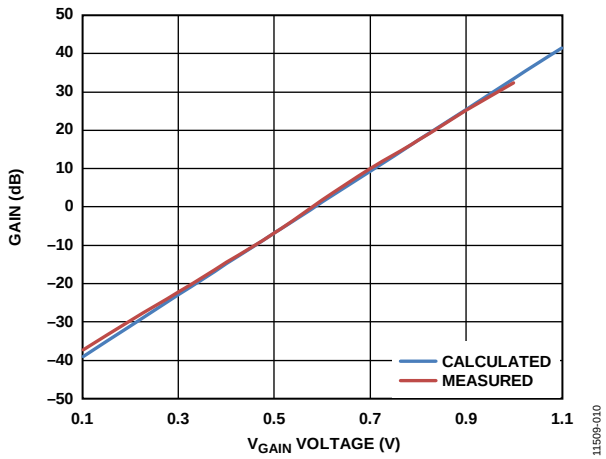

Figure 10. Gain vs. V_{GAIN}, Measured and Calculated with Input Resistors of 41.2 kΩ

In Figure 10, the minimum gain derived from Equation 23 is resolved to −38.7 dB, an attenuation. What this effectively means is that when configured as an attenuator the AD8338 can handle input signals larger than its supply rails. In the measurements taken to produce Figure 10, an input signal of 10 V p-p was injected into the 41.2 kΩ input resistors. In theory, the user could use very high input voltages, so long as the internal transconductance stage's 3 mA input current limit is not exceeded.

Because the gain changes as a function of the input resistance, care should be exercised. If a filter acts as a short, either by a low impedance source or a passive LC filter, then Equation 23 shows that the gain becomes very large. Supposing that the source which is driving the AD8338 has a source resistance of 1 Ω each, the minimum gain will be 53 dB. While no signal will be present, the internal device noise will be gained up by 53 dB.

For systems that are sensitive to input noise, the designer must then shape the inputs in such a way that for frequencies of interest, the inputs appear to be of a specific resistance value. Outside of those frequencies of interest, the inputs appear to be a much larger value. Figure 11 illustrates a general configuration to obtain this behavior.

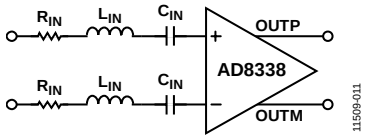

Figure 11. A Tuned Input to Achieve High Input Impedance for Out-of-Band Frequencies While Obtaining a Fixed Low Input Impedance for In-Band Frequencies

Design Example

Suppose that the AD8338 is to be used in a receiver signal chain with an IF Frequency of 10 MHz, where the system impedance is 50 Ω and is single ended (unbalanced). The bandwidth of the signal of interest is 2 MHz wide.

The single-ended system easily couples to the AD8338 with the use of a transformer. Here, at the frequency of interest, the LC networks have an electrical equivalent impedance of a short. The only impedance then seen is the two R_{IN} resistors. Since the internal nodes of the AD8338 inputs appear to be low impedance, the impedance seen by the transformer is 2 R_{IN}. For maximum power transfer, this input impedance should be 50 Ω.

$$2R_{IN} = 50\Omega \quad (28)$$

$$R_{IN} = 25\Omega \quad (29)$$

With R_{IN} set to 25 Ω, the minimum system gain calculated from Equation 23 is

$$20\log\left(\frac{9500}{25}\right) - 26 = 25.6dB \quad (30)$$

In order to prevent a possible instability issue with the AD8338, the INPR and INMR inputs need a dc path when not used. Since this will set the impedance seen by the amplifier for out-of-band signals, a value of 191 kΩ is used. Since this value is used differentially from INMR into INPR, the single-ended gain is calculated with half of this value (95.5 kΩ). Then for out-of-band signals, the minimum gain is

$$20\log\left(\frac{9500}{95500}\right) - 26 = -46dB \quad (31)$$

To shape the input such that signals of interest couple in, and signals outside the band of interest do not, the values of L_{IN} and C_{IN} shown in Figure 11 require careful selection. One measure of choosing these values is by identifying the Q of the resonant circuit, given by Equation 32.

$$Q = \frac{Frequency_{CTR}}{Bandwidth} \quad (32)$$

From the design specifications, the center frequency is 10 MHz, and the bandwidth is 2 MHz. Q is then

$$Q = \frac{10^7}{2\times10^6} \quad (33)$$

$$Q = 5 \quad (34)$$

With Q identified, the impedance values of the L_{IN} and C_{IN} components are quickly calculated relative to the resistor R_{IN}.

$$X_L = 5 \times 2R_{IN} \quad (35)$$

$$X_L = 250\Omega \quad (36)$$

$$L = \frac{250}{2\pi10^7} \quad (37)$$

$$L \approx 3.97\mu H \quad (38)$$

Repeat the same procedure to find the value of C_{IN}.

$$X_C = 5 \times 2R_{IN} \quad (39)$$

$$X_C = 250\Omega \quad (40)$$

$$C = \frac{1}{2\pi10^7\times250\Omega} \quad (41)$$

$$C = 63.7pF \quad (42)$$

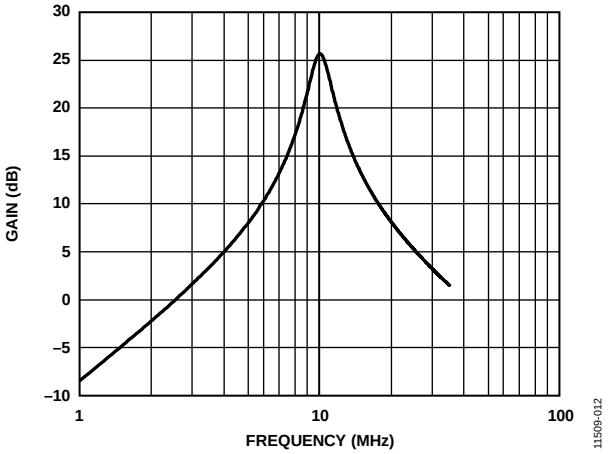

Figure 12. Minimum Gain Calculations Using L = 3.97 µH, C = 63.7 pF

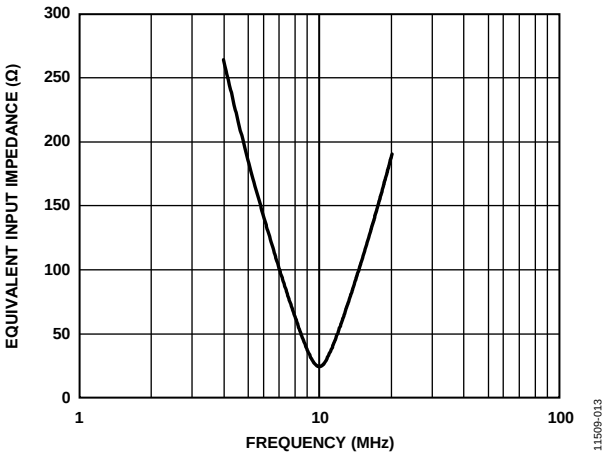

Figure 13. Effective Input Impedance (Single-Ended) over Frequency

As Figure 12 shows, the effective minimum gain for the AD8338 is high for signals of interest, and attenuated for signals outside the band of interest. Additionally, Figure 13 illustrates the effective impedance seen by the coupling transformer. As this impedance increases, less of the incoming energy couples through, improving the rejection of unwanted signals.

A real filter was built for this experiment. It was measured to have a bandwidth of 1 MHz, resulting in a Q of 10. R_{IN} is 25 Ω. From Equation 35 through Equation 38, the resulting L and C values are

- L = 8 µH
- C = 30 pF

Figure 14 shows the measured response of these components. Note that the insertion loss is 2.6 dB.

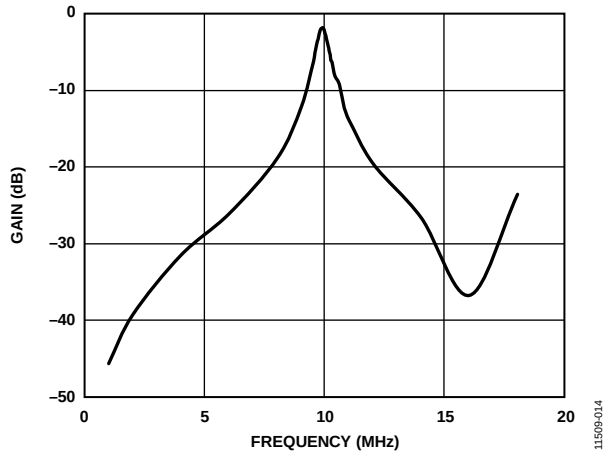

Figure 14. Frequency Response of Filter

Two sinusoidal tones are injected into a power combiner. Their product from the combiner is fed into a 50 Ω termination with the signal levels shown in Figure 15. This signal produces a 20 mV amplitude total output.

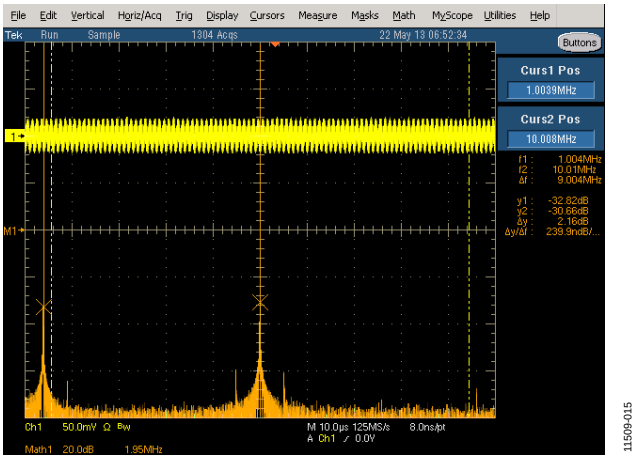

Figure 15. Spectra of the Two Tones. F1 (1 MHz) has a Level of −32.8 dB, F2 (10 MHz) has a Level of −30.7 dB.

Once fed into the filter, these two tones are injected into the AD8338, with a gain of +0 dB (V_{GAIN} = 0.10 V).

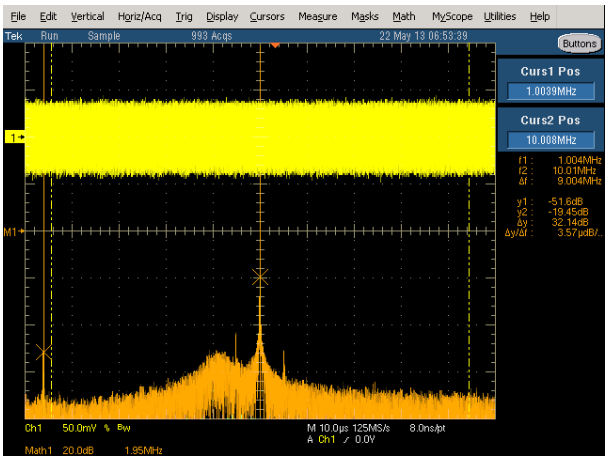

Figure 16. Results of Signal Spectra After the AD8338, with V_{GAIN} = 0.1 V

In Figure 16, the unloaded output of the AD8338 is shown. Note that the unwanted signal is attenuated by 18.8 dB while the signal of interest is gained up 11.3 dB. This demonstrates the gain as shaped by the input filter.

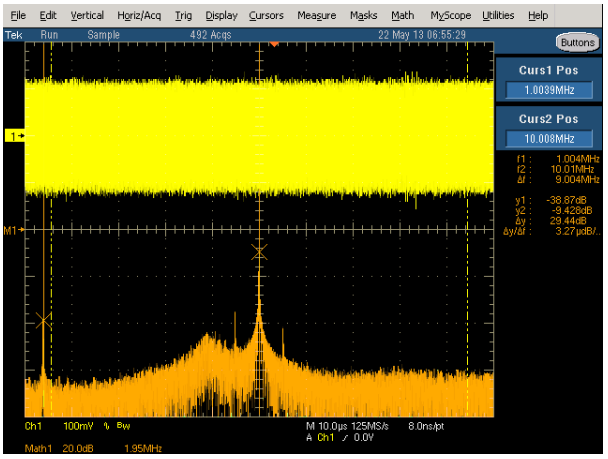

Figure 17. Output of AD8338 with V_{GAIN} = 0.27 (Gain = +13.5 dB)

The results continue as gain is increased. Here the gain has been set to +13.5 dB. The in-band signal has an effective gain of +21.3 dB, while the out-of-band signal has an attenuation of 6.1 dB. The variance of intended gain from what is measured is a function of the losses in the filter, the inputs, and the transformer. Equivalent series resistance (ESR) in both the inductors and capacitors is a function of frequency, which influences the overall behavior of the system as well. If a higher degree of performance is required, silver mica capacitors are highly recommended. Additional improvements to this response can be made through simple filtering in front of the series LC elements in this circuit.

DESIGN EXAMPLE: A VOLTAGE CONTROLLED ATTENUATION-TO-GAIN AMPLIFIER

Figure 18 illustrates the schematic of the attenuation-to-gain amplifier design used to collect the information in Figure 10. This amplifier has been verified over the gain range from GAIN = 0.1 V for an attenuation of −38.7 dB (−37 dB measured), to GAIN= 1.0 V for a gain of +33.2 dB (measured +32.1dB in practice). For large values of attenuation, the input to the amplifier was driven with a differential input of 20 V p-p, or 10 V p-p single ended.

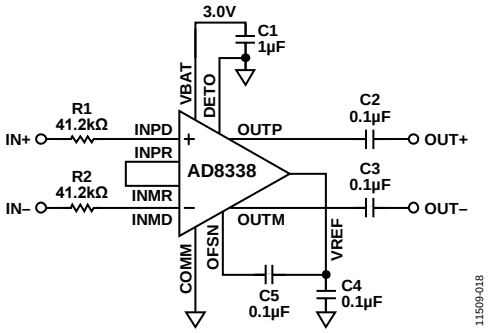

Figure 18. Schematic of the Attenuation-to-Gain Amplifier (MODE, GAIN, and VAGC Pins Not Shown)

This means that for signals of interest, this amplifier can serve as a funnel amplifier for driving an ADC, an adjustable gain automatic gain controller, or any other signal conditioning application, which needs a wide input range.

Table 1. V_{GAIN} vs. Gain, Calculated and Measured

Gain Voltage	Calculated Gain (dB)	Measured Gain
0.1	−38.7	−37
0.2	−30.7	−29.4
0.3	−22.7	−22
0.4	−14.7	−14.4
0.5	−6.7	−1.7
0.6	+1.3	+1.7
0.7	+9.3	+10
0.8	+17.3	+17.2
0.9	+25.3	+25
1.0	+33.3	+32.1

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