

Single-Sideband Upconversion of Quadrature DDS Signals to the 800-to-2500-MHz Band

by Rick Cushing, N17X

INTRODUCTION

Direct digital syntheses (DDS) technology is advancing rapidly, but *direct* synthesis of UHF and microwave output frequencies is not yet practical or economically feasible. Current state-of-the-art commodity DDS ICs—such as the 300-MHz AD9852 Single- and AD9854 Quadrature Complete-DDS chips—offer *usable* outputs to the lower VHF spectrum, approximately 120 MHz. Sampling speed limitations of the DDS and output DAC form the major bottleneck; fundamental DDS output signals must not be greater than one-half the sample frequency. The next generation of high-speed DDS ICs from Analog Devices will challenge those limitations with 900-MHz sample rate and 360-MHz usable fundamental output.

In order to take advantage of DDS attributes at UHF and microwave frequencies, a DDS is commonly integrated with a phase-locked loop (PLL) or upconverted in a mixer. Unfortunately, multiplication using PLLs compromises signal integrity, frequency resolution, and agility. Also, upconverting a DSB (double-sideband) signal to single-sideband at a higher frequency, using a mixer, may require difficult or impossible output filtering as well as a high-quality fixed-frequency local oscillator (LO). Methods used to overcome these shortcomings usually result in the need for multiple PLL or mixer/filter/oscillator stages.

The following is an improved and economical approach to *single-stage* upconversion to the frequencies from 800-to-2500-MHz, using the above-mentioned AD9854 Quadrature Complete-DDS and a new device, the AD8346 Quadrature Modulator, which has phase accuracy to within 1 degree and amplitude balance to within 0.2 dB at 1900 MHz. The upconverted suppressed-carrier, single-sideband signal displays >36-dB typical rejection of LO and

undesired sideband frequencies over the entire frequency range. Moreover, *all* DDS signal qualities are preserved, while the unwanted products of upconversion are minimized. 36-dB rejection is adequate for many applications, and this 4000× suppression of unwanted signal power will greatly reduce output filter complexity or alternatively improve the feasibility of effective filtering in more-demanding applications.

To choose between the upper and lower sidebands, one simply reverses or exchanges the quadrature DDS signals, I for Q and Q for I, at the AD8346 modulator input pins. The AD9854 DDS has a variety of modulation modes (AM, FM, PSK, and FSK) available. This enhances the utility of this application by providing digital and analog communications capability in addition to agile, single-frequency signals.

Upconversion of quadrature DDS signals is just one example of what can be done with the AD8346 Quadrature Modulator. It can in fact upconvert *any* quadrature analog baseband signal (dc to 70 MHz) with similar sideband suppression.

QUADRATURE SSB UPCONVERSION

The AD8346 Quadrature Modulator provides impressive SSB upconversion performance, permitting baseband signals to directly modulate local-oscillator (LO) frequencies from 800 MHz to 2.5 GHz with typically 36 dB rejection of redundant sideband and LO frequencies. The upconverted signal may be frequency-hopped, spread-spectrum or stationary; and unmodulated or wide-band modulated, within the allowable input bandwidth. For upconverting quadrature signals synthesized by DDS, the block diagram in Figure 1 shows how AD9854 output signals would be applied to the AD8346 differential “baseband modulation” inputs for SSB upconversion near the LO frequency.

In quadrature upconversion, two mixers are driven with sine and cosine LOs, which are internally derived from a single-ended high-quality oscillator, provided by the user. The mixers are fed sine and cosine baseband signals (filtered DDS output signals) to be symmetrically upconverted about the fixed LO. The two mixer outputs are summed internally to add in-phase components and reject quadrature components of the mixer outputs. The end result (without additional filtering) is a suppressed-carrier, single-sideband, voltage output at -10 dBm and 50-ohm impedance, at a frequency that is either the sum or difference of the LO and baseband signal, plus suppressed remnants of the LO and opposing sideband.

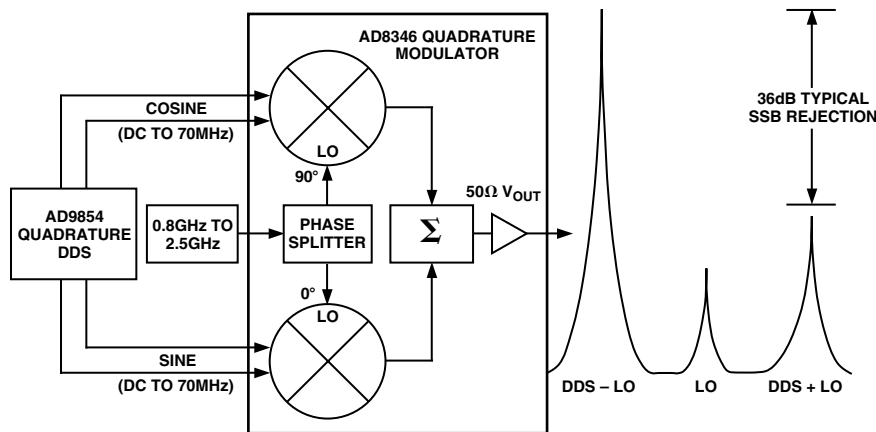


Figure 1. Quadrature DDS SSB Upconversion.

Quadrature modulation, which requires precise phase relationships, is not a new concept. Fifty years ago, one of the first uses of quadrature modulation was to produce single-sideband radio-telephony signals; it was called the “phasing method.” However, the “filter method” came to be preferred because maintaining quadrature phase relationships over appreciable bandwidth is not easily accomplished with *analog* methodology. Both methods were used primarily at low IF frequencies, with the aim of removing the redundant sideband and eliminating the “carrier.”

The AD9854 DDS produces *digitally precise* quadrature output signals (typical accuracy two-tenths of one degree) from dc to >120 MHz, using a 300-MHz clock source. In the example shown in Figure 1, the clock can be derived from the high-quality LO if divided down appropriately. The quadrature phase error of the AD8346 is typically 1 degree over its 800-to-2500 MHz output range. These devices comprise a “chip set” that can serve well in many wideband digital and analog communication schemes, from spread-spectrum to television.

A more complete explanation, including a basic mathematical analysis of analog and digital quadrature modulation and SSB upconversion, is available in an article written by Doug Smith, “Signals, Samples and Stuff: A DSP Tutorial (Part 1)” in the March/April, 1998, issue of *QEX: Forum for Communications Experimenters* magazine. For more information contact the American Radio Relay League, 225 Main Street, Newington, CT 06111, <www.arrl.com/qex.>

To gain a greater appreciation of the merits of quadrature upconversion, it may be instructive to compare two popular methods for generating UHF and microwave DDS-based signals: *DDS/PLL frequency multiplication* and *single-stage mixer upconversion*.

PLL/DDS MULTIPLICATION

PLL multiplication of a DDS signal to UHF and microwave frequencies is easily and economically accomplished, but at a cost: the advantages provided by DDS will be degraded in practically every desirable attribute, including the phase-noise specification, new-frequency acquisition time, frequency resolution and spurious-free dynamic range (SFDR). Combinations of PLL/DDS/mixer/filter that reduce the signal degradation do exist, but the complexity and cost of such multiple-stage implementations may not be tolerable. Figure 2 shows a typical DDS/PLL implementation.

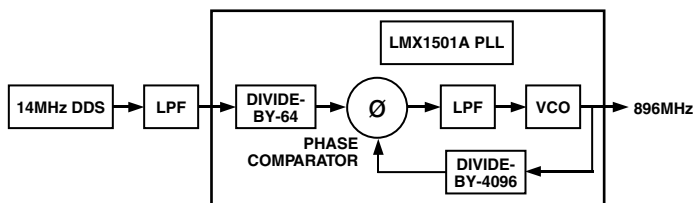


Figure 2. Example of a DDS and PLL integration using an LMX1501A PLL evaluation board and an AD9851 DDS.

PLL output phase noise is an obvious and easily observed phenomenon; its magnification will degrade performance in proportion to the multiplication factor of the PLL (expressed in dB, $20 \log f_{OUT}/f_{IN}$). For example, if the frequency of a DDS signal at 10 MHz is multiplied by 100, to yield an output of 1 GHz from a PLL, the output phase noise within the PLL loop bandwidth will be approximately 40 dB greater than with the original input signal. Furthermore, spurious signals, or “spurs” within the PLL loop bandwidth will be increased by the same amount. This may result in *unacceptable* spur levels that are up to 40 dB greater than those of the DDS input signal.

Spectral plots easily show how the phase noise of a DDS signal suffers after being multiplied by 64 in the PLL circuit in Figure 2. Figure 3 shows the DDS input signal to the PLL at 14 MHz and Figure 4 shows the PLL-multiplied DDS signal at 896 MHz. The wide noise “skirt” is the signature of degraded phase noise.

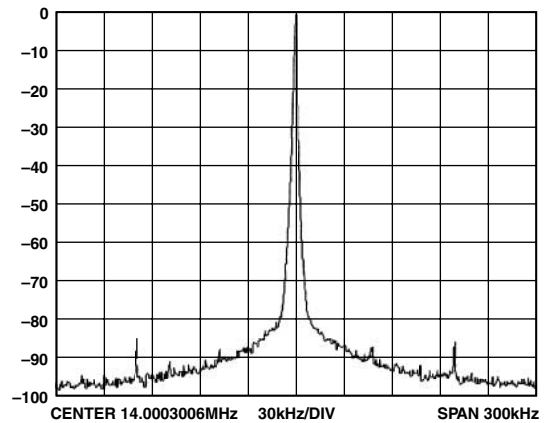


Figure 3. 14 MHz DDS input signal.

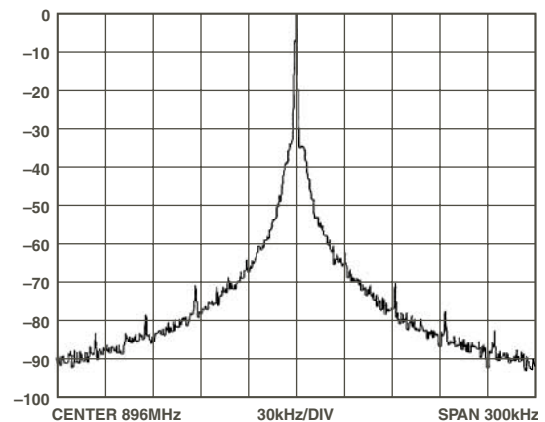


Figure 4. 896 MHz PLL output signal.

To illustrate the effect of PLL multiplication on spur levels, the DDS signal was modulated to produce an abundance of low-level spurs close to the fundamental. Figure 5 shows the modulated DDS signal that was fed to the PLL, while Figure 6 shows how

these spurs within the 30 kHz loop bandwidth of the PLL have been magnified. Note that >60 kHz away from the carrier, spur amplitudes are not affected. The phase noise has not been altered nor have any other parameters been changed.

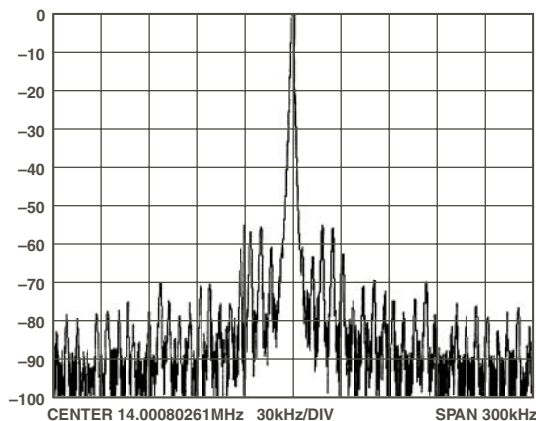


Figure 5. Modulated 14 MHz DDS signal to PLL.

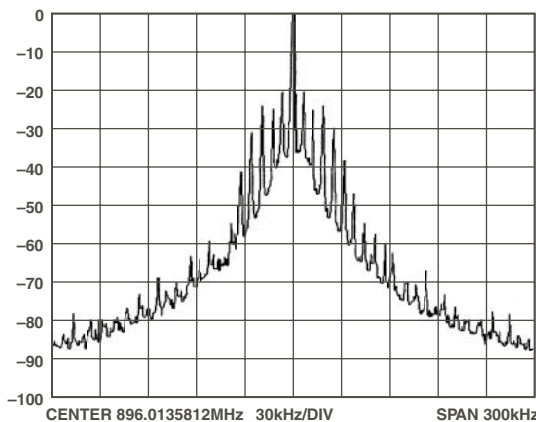


Figure 6. 896 MHz PLL output signal.

In addition to phase noise, timing jitter, and spur-level degradation, many other desirable DDS attributes, including frequency agility and resolution, will be adversely affected with PLL multiplication. Even frequency resolution will become N times worse than the

DDS resolution, and new-frequency acquisition will be limited by the PLL's settling time (which can be as much as 10,000 times greater than that of the DDS).

DDS/MIXER UPCONVERSION

A better option available to the designer is to upconvert a DDS signal to UHF/microwave frequencies using a mixer. Upconverting does not significantly increase either the spur levels or the phase noise. Furthermore, frequency agility and resolution remain unaffected. The largest obstacle to overcome is the presence of the double-sideband (DSB) output: LO + DDS and LO - DDS, and any LO feedthrough that occurs.

Figure 7, showing a 200-MHz region of spectrum of a suppressed carrier (LO), single-upconversion mixer output, demonstrates this problem with upconversion. The two sidebands are 50 MHz apart, with LO feedthrough at a frequency midway between the two at 1.04 GHz. This 50-MHz spread is only 5% of the 1-GHz output frequency. Filtering the signals to remove the unwanted sideband and LO feedthrough will be extremely difficult. If the output frequency is increased to 2 GHz, it may complicate matters to the point where filtering is impractical. To overcome this problem, designers traditionally incorporate multiple stages of mixing and filtering to produce a DSB signal with larger sideband spacing at UHF/microwave that will be more easily filtered but at far greater expense and complexity.

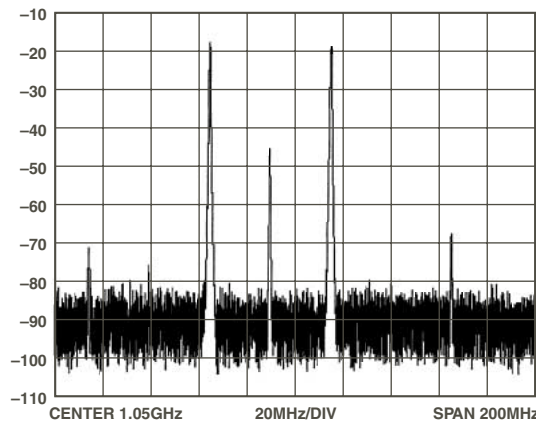


Figure 7. DSB output from typical mixer.

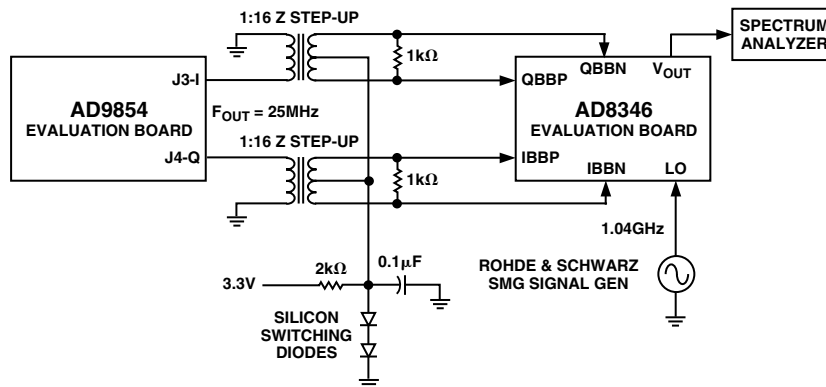


Figure 8. Hookup and modification of Analog Devices evaluation boards for lab evaluation.

DDS UPCONVERSION LAB RESULTS

A quadrature implementation of the SSB upconverter was accomplished in the lab was using the evaluation boards for the AD9854 and the AD8346. Modifications to the AD8346 evaluation board were required to accept the filtered, quadrature, *single-ended* signals provided by the AD9854 evaluation board. The output voltage levels also needed to be increased to suit the AD8346 input requirements. A diagram of the lab hook-up and modifications is seen in Figure 8. Modifications are as follows:

1. Add two 1:16 center-tapped impedance-step-up transformers (Mini-circuits T16-6T) to convert single-ended quadrature signals to differential signals and to provide a 1:4 voltage step-up. Use of the center-tapped secondary allowed a dc offset voltage of 1.2 volts to be added to the differential signals to comply with the AD8346 input-biasing requirements.
2. Add 1000-ohm termination resistors across each transformer output.
3. Add a 1.2-volt dc bias source consisting of two silicon diodes forward-biased from the 3.3 volt supply voltage through a 2000-ohm current-limiting resistor. Connect to center-tap of both I- and Q-channel transformer secondary windings.

Tests of this setup verified the performance expectations conveyed in the AD8346 data sheet when the quadrature input signals from the AD9854 were properly adjusted to compensate for quadrature phase error and I & Q amplitude imbalance. See Figures 9 and 10.

Errors in the I & Q quadrature phase relationship are introduced—*after* the signals exit the AD9854 IC—by the filters, unequal cable and PCB trace lengths, transformer differences, etc. System phase errors cannot be corrected through programming changes of the AD9854. Its outputs are *fixed in accurate quadrature*. Phase errors can be corrected by adjusting cable lengths from the AD9854 to the AD8346 evaluation board. Amplitude inequalities can be corrected using the AD9854's 12-bit, independent sine and cosine (I & Q), digital amplitude multiplier stages.

Figure 9 shows a 200-MHz segment of the output spectrum of the AD8346 centered around 1.05 GHz. The DDS “modulating” upper and lower sideband signals are seen 25 MHz away on either side of the LO at 1.04 GHz. A difference of -40 dB is indicated between the suppressed upper sideband (USB) and the favored lower sideband (LSB) amplitudes. The 40-dB differential equates to a power ratio of about ten-thousand to one. This level of sideband suppression is indicative of approximately 1 degree of input-signal phase mismatch.

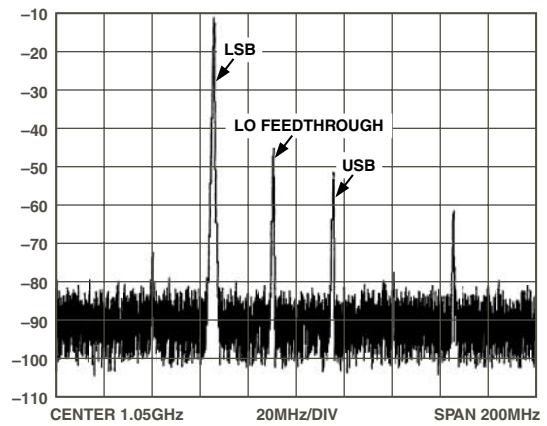


Figure 9. Output spectrum of AD8346 modulator.

A close-in view (Figure 10) of the lower sideband (LSB) at 1.015 GHz shows excellent signal integrity. It is in striking comparison to the PLL-multiplied signal in Figure 4. As noted earlier, the sine and cosine DDS signals to the quadrature modulator can be exchanged to cause the complementary sideband to be favored.

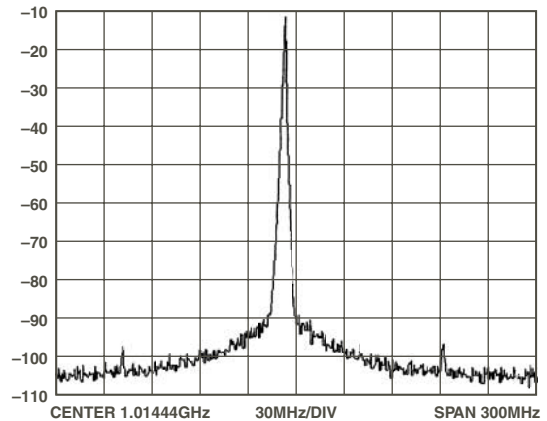


Figure 10. Close-in look at the LSB.

LO feedthrough amplitude (-36 dB) is greater than the suppressed sideband in this setup. LO feedthrough level is not affected by either the phase or amplitude of the DDS I & Q input signals. To reduce the significance of LO feedthrough, the voltage levels of the I & Q input signals should be maximized (1V p-p) at each differential input pin.

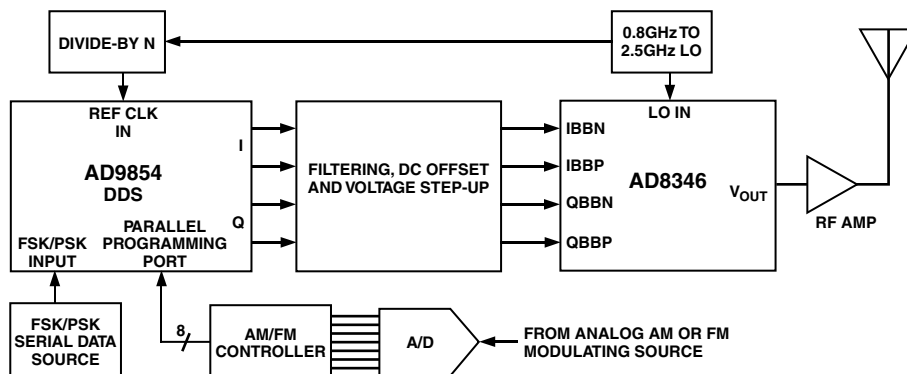


Figure 11. Block diagram depicting the stages needed for an RF exciter producing AM, FM, FSK, PSK modulated signals in the 800 to 2500 MHz frequency band.

CONCLUSION

Quadrature modulation is a well established and economical method of DDS upconversion to UHF and microwave frequencies, without losing any of the desirable attributes of DDS technology or compromising signal quality. The AD8346 quadrature modulator simplifies the process. It is a “natural” match to the AD9854 DDS, with its differential quadrature outputs. With a high-quality LO, UHF and microwave SSB output is readily achievable.

With the AD9854’s variety of modulation modes, this application supports a (nearly) complete AM, FM, PSK, FSK exciter at microwave output frequencies. With minor additional signal processing of the AM suppressed-carrier I & Q DDS outputs, SSB voice or other amplitude modulation schemes become possible. Figure 11 shows how the ICs would be interconnected with external modulating sources and controlling devices to perform communications functions.

The 36-dB (typical) sideband and LO rejection is directly usable in many applications, and output filtering becomes a much less formidable task in more-demanding applications. Appropriate

adjustment of the DDS I & Q signal phase relationship and amplitude balance can increase sideband suppression even further.

Although it was specifically designed to provide the appropriate output signals without the need for multiple DDSs to achieve this function, the AD9854 in the application described here is not the only way to combine DDS and quadrature modulation. Other DDS ICs, such as the AD9850, AD9851 and the AD983x series, might also be used in quadrature pairs. If two DDSs can be synchronized, it is likely that they can be programmed to achieve quadrature outputs using internal phase-offset circuitry. See the DDS Information center at www.analog.com/dds for a complete listing of DDS and digital modulator products, and for access to technical notes and data sheets. It is also worth noting that the AD9854’s independently programmable I & Q output amplitudes make output matching a simple software routine.

The relative simplicity and economy of quadrature DDS SSB upconversion to over 2 GHz should encourage readers to consider adding this technique to their repertoire. It preserves every desirable DDS attribute at microwave frequencies, and at the same time drastically reduces the undesirable redundant sideband of conventional double-sideband-mixer upconversion.