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APPLICATION NOTE

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# A 2.4 GHz WiMAX Direct Conversion Transmitter

by Cecile Masse and Qui Luu

## FEATURES

**Direct conversion transmit chain**
**Tx radio using 5 chips**
**Dual AD9862 MxFE, 14-bit DAC, 128 MSPS, with programmable full-scale current**
**3 GHz quadrature modulator ADL5373**
**2.7 GHz VGA ADL5330 with 50 dB of power control range**
**4 GHz fractional-N synthesizer ADF4153**
**3 GHz RMS power detector AD8362**
**Supports 10 MHz channel bandwidth with 1024-subcarriers OFDM**
**Supports QPSK, 16 QAM, and 64 QAM OFDMA**
**Transmitter output power: 13 dBm maximum, CW**
**EVM 64 QAM OFDM: 1.2% @ −3 dBm output**
**Transmitter noise at 20 MHz offset: −142.5 dBm/Hz @ −1 dBm**
**Precise output rms power control**
**Dual-supply operation: 5 V @ 380 mA, 3.3 V @ 165 mA**

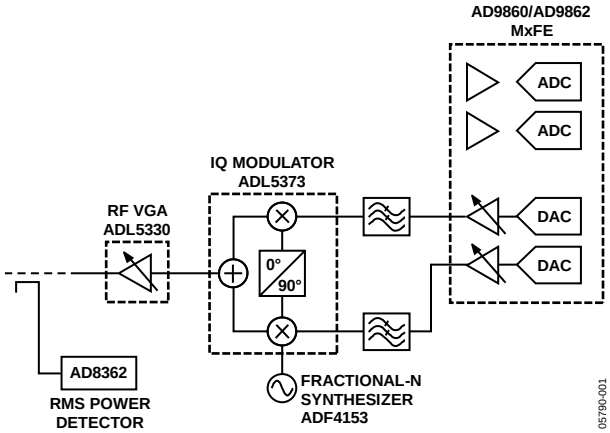


*Figure 1. Direct Conversion Transmitter*

## APPLICATIONS

**WiBro/WiMAX 5 V CPE and base stations**

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# INTRODUCTION

The purpose of this application note is to demonstrate the Analog Devices, Inc. WiMAX 5 V transmit signal chain for applications extending up to 2.7 GHz.

As the wireless communication industry moves toward higher RF frequencies, and higher data rates through wider modulation bandwidths, high performance linear transmit chains are required. WiMAX wireless broadband networks reflect such a trend. Deployment has started in the 2.5 GHz and 3.5 GHz bands for point-to-point and point-to-multipoint fixed applications. Data rates of up to 80 Mbps are achieved using wideband orthogonal frequency division multiplexing (OFDM) modulations.

802.16 WiMAX fixed or mobile standards are based on $2^N$-carrier OFDM modulation: 256 for 802.16d and 512 to 2048 for 802.16e. Each of the $2^N$ subcarriers can be modulated with either a QPSK, a 16 QAM, or a 64 QAM data sequence. The standards also support different signal bandwidths, from 1.25 MHz to 20 MHz to accommodate variable rates, although the current profiles define channel bandwidths from 5 MHz to 10 MHz. The OFDM composite signal envelope amplitude can exhibit significant peaks and valleys, with a modulation depth close to 100% and peak-to-average ratio of about 10 dB. This imposes severe linearity requirements on the transmit chain.

To address these challenges, direct conversion architecture has been chosen. For this particular analysis, a full Tx signal chain, starting from the baseband signal generation, up to the voltage controlled amplifier and power detector functions (but excluding the power amplifier) was evaluated. The primary focus is the wireless broadband (WiBro) frequency band, 2.3 GHz to 2.4 GHz, used in Korea for the deployment of the 802.16d (fixed) and 802.16e (mobile) standards. However, this signal chain may also be used up to 2.7 GHz (see the AD9862, ADL5373, ADL5330, ADF4153, and AD8362 data sheets for performance details).

## ARCHITECTURE

The radio architecture is a direct upconversion, having the following benefits: low number of parts, less mixing product spurs, fewer filters, and lower current consumption.

In addition, the architecture requires only a single upconversion operation, and thus one synthesizer. The large number of subcarriers within the WiMAX OFDM or orthogonal frequency division multiple access (OFDMA) signal actually makes this modulation quite sensitive to phase noise, as each of the N subcarriers is modulated by the phase noise of the local oscillator (LO). For this reason, it is important to minimize the amount of phase error added onto the modulation.

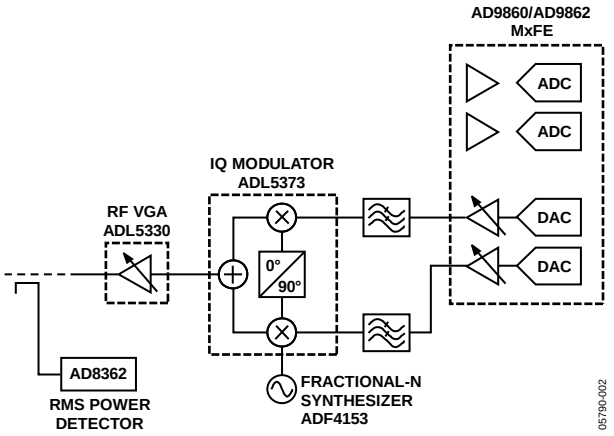


*Figure 2. Direct Conversion Tx Chain*

This architecture includes a transmit DAC, a fixed gain IQ modulator, an LO fractional-N synthesizer, an RF VGA, and an rms power detector. Off-chip, low-pass filters are also required at the DAC outputs to filter the images that lie at multiples of the sampling frequency. The DAC and the synthesizer need a 3.3 V supply, but all other parts run off a 5 V single supply. The specific parts used for the Tx signal chain are as follows:

- AD9860/AD9862, 12-bit/14-bit, 128 MSPS sampling DAC, SNR ≥ 70 dB
- ADL5373, 3 GHz IQ modulator
- ADF4153, 4 GHz LO fractional-N synthesizer
- ADL5330, 2.7 GHz voltage controlled amplifier/attenuator VGA
- AD8362, 2.7 GHz rms power detector

Given the nature of the OFDM signal and the stringent error vector magnitude (EVM) requirements imposed by the very high data rates, these parts have been selected for their linearity and noise performance of up to 2.7 GHz.

The following sections address each of the major functions within this Tx signal chain, with a focus on the system design rationales, implementation, and interfaces.

## ANALOG BASEBAND SIGNAL GENERATION

The Tx DAC is one of the most critical components in this signal chain because it needs to provide the closest to ideal analog signal to be upconverted and amplified. The DAC signal-to-noise ratio (SNR) and sampling rate define the spectral purity and signal quality of the modulated signal driving the IQ modulator.

### *SNR and SFDR*

The chosen Tx DACs for this application are part of the AD9860/AD9862 mixed signal front-end family (MxFE®) and are 12 bits and 14 bits, respectively. They have a maximum sampling rate of 128 MHz. The output of the Tx DACs is a current source, with a programmable peak current between 2 mA and 20 mA. Programming the full-scale current through register writes provides the flexibility of adjusting the peak-to-peak input voltage to the IQ modulator while maintaining the 12-bit/14-bit resolution.

Recommended SNR for this application should be at least 60 dB to be able to meet the spectral mask at maximum power levels and EVM at the lowest power levels (for instance, an SNR of 31.4 dB plus margin is required for a 64 QAM three-quarter OFDM even at the minimum output power at the antenna). Both the 12-bit AD9860 and the 14-bit AD9862 provide better than 70 dB SNR. In some BTS applications, higher SNR is required to meet stringent spectral masks. It is then recommended to use a 16-bit DAC like the AD9779.

In addition, the spurious-free dynamic range (SFDR) within the first Nyquist zone stays constant at −76 dBc whether the signal frequency is at 1 MHz or 6 MHz. This is important, for instance, when dealing with large signal bandwidths like an OFDM 10 MHz WiMAX signal centered at dc.

### *Sampling Frequency*

Depending on the maximum modulation bandwidth, the sampling frequency can be appropriately chosen. For example, a WiBro complex OFDM signal with an 8.75 MHz bandwidth would require a DAC sampling rate , $f_{SAMPLING}$, of at least 2 × 10 MHz or twice the Nyquist minimum (*OFDM modulation sampling frequency* = *n* × *bandwidth* = 8/7 × 8.75e6 = 10 MHz). But all sampling alias would be at n × 20 MHz, which would fall in band for RF frequency bandwidths higher than 20 MHz. These images can only be filtered by the off-chip reconstruction filter at the DAC output.

Good filtering of the DAC images at multiples of the sampling frequency then requires higher order filters. This can be avoided using the interpolation filters, available within the DAC. While the input data rate to the DAC remains the same, the interpolation filters increase the sampling frequency of the DACs. As a result, the images appear further away from the main input signal. Figure 3 and Figure 4 show the effect of enabling the 4× interpolation filters on the AD9860/AD9862.

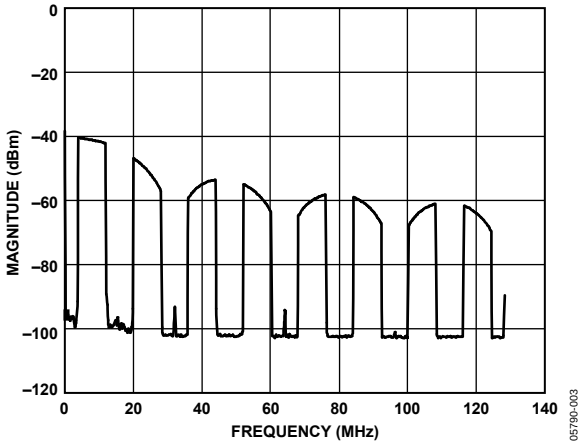


*Figure 3. AD9860/AD9862 Tx DAC Generating an OFDM Signal with 1× Interpolation ($f_{SAMPLE}$ = 32 MSPS, 1× Interpolation)*

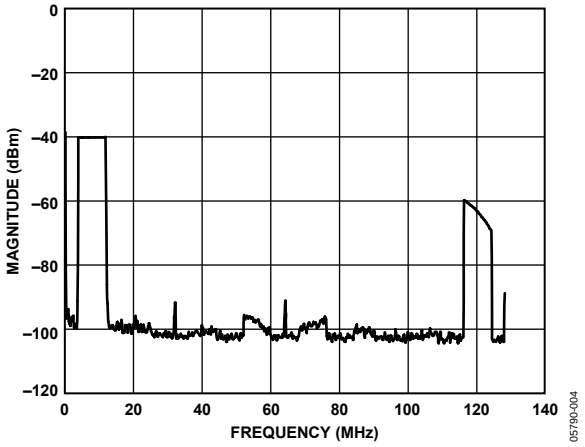


*Figure 4. AD9860/AD9862 TxDAC Generating an OFDM Signal with 4× Interpolation ($f_{SAMPLE}$ = 32 MSPS, 4× Interpolation)*

Therefore, while the Tx digital data are updated at a rate of 20 MHz only, the 4× interpolation filter effectively increases the overall sampling rate to 80 MHz. This allows a simple third-order Bessel LPF at the DAC output (see the IQ Modulator section).

## IQ MODULATOR

### *Modulator AC Drive Level*

The I and Q inputs of the modulator should be driven differentially. For a modulation like WiMAX OFDM with peak-to-average ratios of 10 dB and higher, the peak drive level should be such that there is at least a 10 dB backoff from compression to minimize the distortions. The optimum level is actually determined by minimizing the spectral distortion at the modulator output while maintaining sufficient SNR.

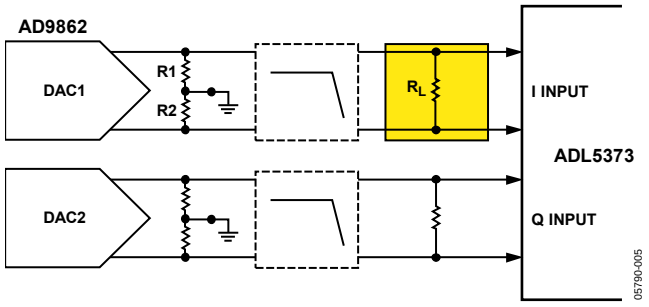


*Figure 5. DAC to IQ Modulator Interface*

The interface between the AD9862 DAC and the ADL5373 modulator is shown in Figure 5.

Resistors R1 and R2 set the dc bias level while Resistor $R_L$ sets the level of the baseband I and Q voltages to the modulator.

The modulator differential input voltage can be calculated from Equation 1 and is both a function of the Resistor $R_L$ and the DAC full-scale current, $I_{DAC}$.

$$V_{diff} = \frac{2 \times I_{DAC} \times R_{DC} \times R_L}{2 \times R_{DC} + R_L} = f(I_{DAC}) = g(R_L) \quad (1)$$
$$R_{DC} = R1 = R2$$

The ADL5373 has a fixed voltage gain. The output level of the modulator can be set by choosing the appropriate input load resistor. As an alternative, a larger resistor can be chosen and the full-scale output current of the DAC can be scaled to the desired drive level.

Optimum drive level to the ADL5373 IQ modulator for an OFDM modulation like WiMAX is 0.650 V p-p ± 10% (see the Finding the IQ Modulator Optimum Operating Point section for more details). At this level, the rms power level out of the modulator is about −12 dBm, providing an optimum trade-off between output power level and spectral quality.

This input voltage can be obtained by using a 50 Ω $R_L$ resistor while driving the modulator with 20 mA of full-scale current.

However, it is common to operate at a given back-off from full scale. As an example, this optimum ac level can also be set by choosing $R_L$ for a high enough peak voltage (200 Ω for 1.3 V p-p, for instance) and by adjusting the DAC output current to about 10 mA (or −6 dBFS). A dc offset then needs to be applied at the connecting point of R1 and R2 to maintain the 500 mV of dc bias level. Note that with this lower full-scale current, the ac dynamic performance of the DAC degrades by about 2 dB.

### *DC Bias Level*

Resistors R1 and R2 set the dc bias level. The recommended level of common-mode voltage is 500 mV.

A value of 50 Ω generates the required 500 mV dc bias for 20 mA of DAC full-scale current, independently of the $R_L$ value.

### *Baseband Filtering*

With the signal being sampled at 80 MHz (20 MHz + 4× interpolation), the requirement for image rejection can be defined. The sample-and-hold action of the DAC is equivalent to a convolution of the sampled waveform by a sin(x) function in the frequency domain.

$$V_{out}(f) = V_{sampled}(f) \times \left( \frac{\sin(\pi fT)}{\pi fT} \right) \quad (2)$$

Figure 3 is a good example of this sampling image shaping effect. As a result, the highest image is usually at 1 × $f_S$, or 80 MHz here.

The level of these sampling images can be calculated using the sin(x)/x function.

Calculated levels are −31.6 dBc and −37.6 dBc at 1 × $f_S$ and 2 × $f_S$ respectively, at a sampling frequency of 80 MHz. The measured levels of these images were actually not very different from these calculated values: −33 dBc and −40 dBc for the first and second images.

The reconstruction filter at the DAC modulator interface is there to provide the modulator with a clean baseband signal, free from images that fall inside the RF bandwidth by up-conversion. Low-pass Bessel structures are ideal for their flat in-band group delay (see Figure 8). A third-order filter with a 3 dB cutoff frequency at 8 MHz provides 50 dB of rejection at 80 MHz, bringing the sampling images down to 80 dBc.

The details of the baseband filter are shown in Figure 6 to Figure 8.

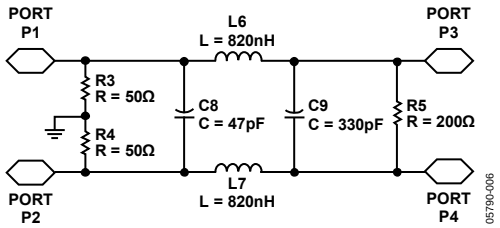


*Figure 6. Baseband Filter Schematic Including Source Resistor and Termination Resistor*

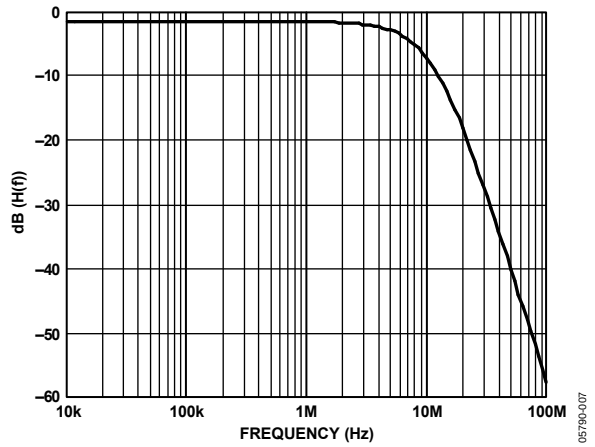


*Figure 7. Baseband Filter Gain Response in Decibels*

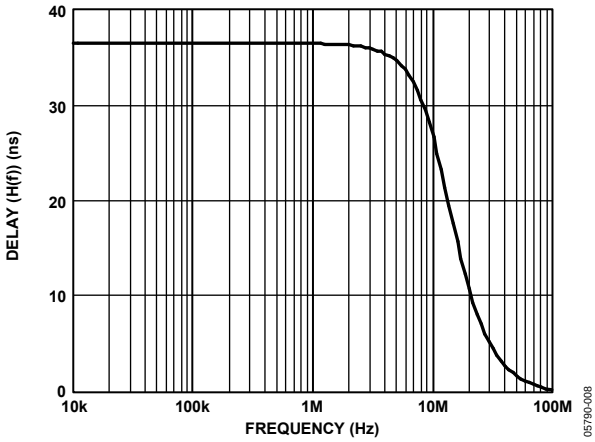


*Figure 8. Baseband Filter Group Delay Response in Seconds*

It is important to consider passive components with the lowest tolerance for this filter, to minimize mismatches between I and Q signal paths.

### *LO Feedthrough and Sideband Nulling*

LO leakage at the output of the modulator comes from different sources:

- DC offsets between I and Q
- DC offsets causing imbalance between the differential signals I and $\overline{I}$ or Q and $\overline{Q}$
- Imperfect LO-to-RF isolation

Usually the most important sources of LO leakage are the unwanted cumulated dc offsets on the baseband signals, between the signal generation and the modulator mixers input.

On the other hand, amplitude and phase mismatches between the I and Q signals and an inaccurate 90° LO phase shifter result in an unwanted upper sideband image. When the Tx DACs are configured for complex outputs, good image rejection at the modulator output is critical because this spur falls inside the channel and cannot be filtered. Phase mismatches cannot be compensated for in this design, but amplitude matching may be achieved through independent gain correction at the DAC level.

Similarly, the AD9862 DACs allow dc offset correction voltages to achieve LO leakage suppression.

I and Q amplitude mismatch correction is achieved by current scaling. There is both a fine and coarse gain control (Register 14 and Register 15) to adjust the full-scale output current of either Tx channel independently. The coarse gain control can be bypassed where no current scaling is done or it can be scaled by 1/2 or 1/11 of the full-scale current. This translates to a −6 dB or −20 dB change in the current. For finer resolution, the fine gain control scales the full-scale currents individually on each leg by ±4%.

For LO suppression, a positive or negative offset can be applied on either the I channel or the Q channel. With a 10-bit accuracy (Register 10 to Register 13), an offset current of up to ±12% or ±2.4 mA for 20 mA full scale can be applied to either differential channel. This is far more than what is usually required for LO nulling.

The gain and offset mismatches are corrected after the analog conversion, therefore maintaining the signal resolution. LO leakage can be suppressed down to 75 dBc at the modulator output and unwanted sideband can be reduced to −60 dBc at room temperature.

Although the WiMAX OFDM signal has no subcarrier at dc, it is important to achieve good dc offset correction to help the demodulator distinguish between the on and off times of the WiMAX burst and to make sure it does not saturate the receiver ADC at low transmitted power.

Figure 9 shows the single sideband spectral characteristic at the IQ modulator output once dc offset and gain calibration have been applied. The unwanted sideband is at −60 dBc and LO leakage at −70 dBc.

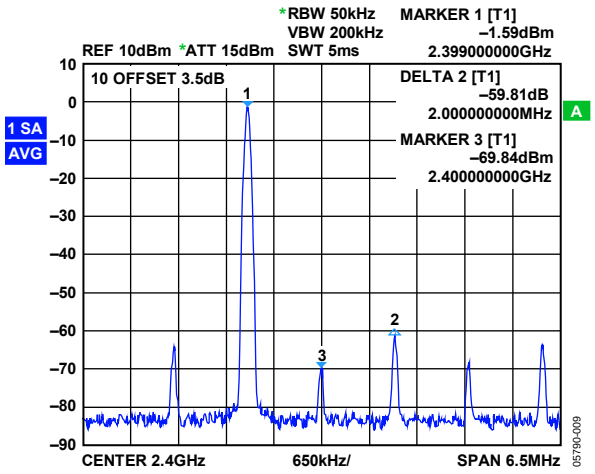


*Figure 9. Single Sideband Spectrum at 2.4 GHz, After DC/Gain Calibration (DAC+IQ Modulator Output)*

### *Finding the IQ Modulator Optimum Operating Point*

Optimum output level for the modulator can be determined by measuring the upconverted signal distortion in the frequency domain. Input voltage at the modulator input is swept such that the output power level varies from −6 dBm to −20 dBm.

The spectral masks are currently being defined but are typically imposed by local regulations for out-of-band emissions. As of today, the Korean WiBro standard provides a specific spectral mask that applies in the 2.3 GHz to 2.4 GHz band, as shown in Figure 10. Other masks have been defined for fixed and mobile radio systems like in the U.S. for deployments in the 2.5 GHz to 2.69 GHz (FCC 04-258).

As an example, Figure 10 shows the characteristics of the WiBro BTS mask, the modulated signal bandwidth being 8.75 MHz.

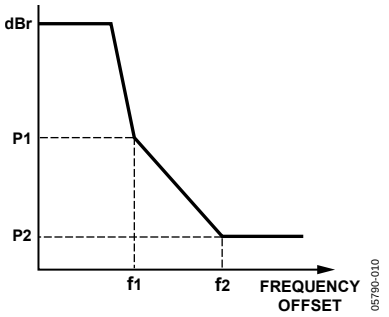


*Figure 10. BTS WiBro Spectral Mask (RBW = 100 kHz)*

The WiBro standard specifies different ACPR requirements depending on the transmitted power at the antenna. Here the requirements are derived for a power level at the antenna of +33 dBm:

- *P1* ≤ −34.5 dBr at *f1* = 4.77 MHz (edge of the main channel)
- *P2* ≤ −52.4 dBr at *f2* = 9.23 MHz (center of the adjacent channel)

Figure 11 shows the modulator spectral performance with a 16 QAM, 256-OFDM signal according to this mask, with the offsets scaled for a 10 MHz OFDM signal. An input drive level has been varied such that the IQ modulator output power ranges from −20 dBm to −6 dBm. An optimum operating point is obtained at about −12 dBm output rms, where the mask is met with more than 20 dB margin.

Figure 12 displays a more generic ACPR characteristic, again for a 10 MHz OFDM signal, where adjacent and alternate powers are compared to the main channel power level. All channel power levels are integrated in a 9 MHz bandwidth and ACP1 and ACP2 are respectively calculated at 10 MHz and 20 MHz offsets from the carrier.

At the first frequency offset (ACP1), as the power level drops, more backoff from the compression and third-order intercept point helps reduce the signal distortion and improve ACPR performance. As the output power drops further, degradation of SNR (due to less signal energy compared to modulator noise floor) is the reason for the dB-per-dB ACPR degradation. At the second frequency offset given by ACP2, there is no spectral regrowth and ACPR basically degrades with decreasing SNR.

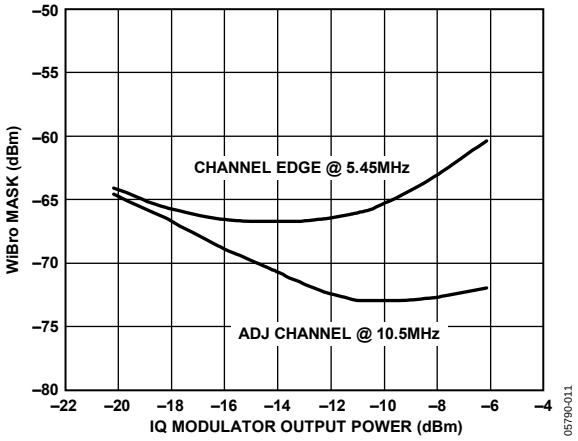


*Figure 11. Modulator Performance According to WiBro Mask, with 16 QAM OFDM Modulation, Function of I and Q Input Voltage (or IQ Modulator Output Power), at 2400 MHz*

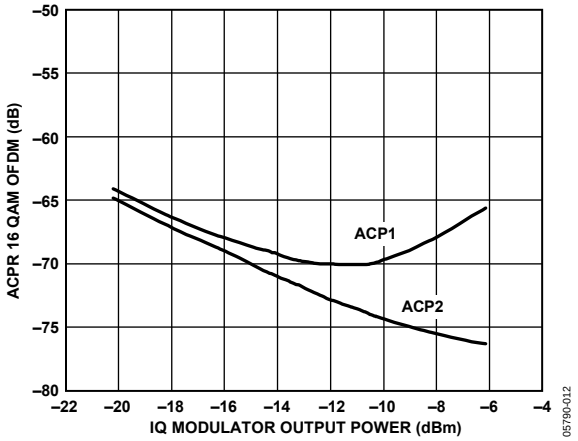


*Figure 12. Modulator Output ACPR with 16 QAM OFDM Modulation, Function of I and Q Input Voltage (or IQ Modulator Output Power), at 2400 MHz*

The EVM performance with a WiMAX OFDM waveform, for the IQ modulator itself, is also quite good at 0.6% rms. Most of it is due to finite upper sideband cancellation as well as second- and third-order intermodulation for each subcarrier that falls within the main channel.

## THE LO SYNTHESIZER

One local oscillator (LO) is required for this direct conversion architecture. The up-conversion from dc to the wanted RF frequency is directly achieved by the IQ modulator. Performances like phase noise, frequency resolution, and settling time dictate the choice of a fractional-N synthesizer for the LO generation.

### *Phase Noise*

With the upconversion, phase noise is superimposed on each of the N subcarriers of the WiMAX OFDM signal when mixed to the local oscillator.

LO phase noise has two effects:

- Random phase rotation for all subcarriers
- Intercarrier interference resulting from the corruption of a given subcarrier by its N-1 noisy adjacent subcarriers.

To help correct for these phase errors that contribute greatly to the degradation of EVM, the OFDM symbol contains eight subcarriers that are modulated with a known training sequence of data. These training subcarriers are called pilot tones and help the receiver track and remove most of the close-in phase noise generated by the LO. However, this only allows the removal of phase changes that are slower than a symbol period, while phase changes that are faster than a symbol period are not tracked and, therefore, affect EVM.

For a 64 QAM modulated OFDM, EVM requirements at the transmitter output are very stringent at 3.1% rms. This is why the PLL loop bandwidth, as well as the total integrated phase error, is critical for the design of this PLL. A total phase error lower than 1°rms has been used as a criteria for choosing a synthesizer.

With integer-N synthesizers, the N divider can be quite high to synthesize >2.3 GHz RF frequencies while allowing for fine resolution. Within the PLL loop bandwidth, both the reference and phase frequency detector (PFD) noise levels are increased by 20 × log(N). It directly degrades the PLL total phase error, which can often be higher than 1°rms.

Fractional-N synthesizers are preferred for their inherent good phase noise. Very small frequency resolution can be achieved while using a higher comparison frequency, therefore helping to reduce the total phase noise. The typical phase noise errors for these fractional-N synthesizers can be <0.5°rms; which is appropriate for this application.

The ADF4153 is a 4 GHz fractional-N synthesizer with three modes available: low noise mode, low noise/low spur mode, and low spur mode. The low noise mode is recommended for narrow-loop filter bandwidths because the loop filter response already attenuates the spurs. This is the case for WiMAX duplex modes that do not require fast locking loops.

For fast loops, spurs are less attenuated because they fall inside the loop bandwidth. In low spur mode, dither is enabled. This randomizes the fractional quantization noise so it looks like white noise, not spurious noise.

### *Synthesizer Frequency Resolution*

The minimum required frequency resolution for the IQ modulator LO is derived from the required channel raster imposed by the 802.16 standard. As of today, the channel raster requirement should be 250 kHz in most cases, and 200 kHz for some specific profiles. This means that the carrier frequency generated by the PLL should be at least a multiple of 250 kHz.

### *Reference Frequency*

The following equations govern how a fractional-N synthesizer is programmed:

$$RF_{out} = [INT + K/MOD] \times [f_{REF}] \quad (3)$$

$$MOD = \frac{f_{REF}}{f_{RES}} \quad (4)$$

where:
$RF_{out}$ is the PLL synthesized frequency.
$f_{REF}$ is the reference frequency, also equal to the PFD comparison frequency in this case.
$INT$ is the integer division factor.
$K$ sets the value of the synthesized frequency fractionality.
$MOD$ is the modulus.
$f_{RES}$ is the PLL frequency resolution.

In fractional-N synthesizers, spurs appear at intervals of the channel spacing (fractional spurs) and possibly also at fractions of the channel spacing (subfractional spurs). Table 1 shows how the value of the modulus affects the location of subfractional spurs.

**Table 1.**

| Conditions | Spur Interval |
|---|---|
| If MOD is divisible by 2, not by 3 | Channel step/2 |
| If MOD is divisible by 3, not by 2 | Channel step/3 |
| If MOD is divisible by 6 | Channel step/6 |
| Otherwise | Channel step |

From Equation 4, the modulus value (MOD) depends on the PFD frequency and channel spacing. The channel spacing is fixed, so if possible the PFD should be chosen such that the modulus value does not produce subfractional spurs.

In addition, the reference frequency should be chosen high enough to reduce the integer INT division ratio (see Equation 3). A reference frequency greater than 10 MHz contributes to the improvement of the PLL phase noise beyond that achievable with an integer-N synthesizer.

### Lock Time

PLL lock time can be critical in the following scenarios:

- In HFDD systems where both frequency duplex and time duplex are used.
- During frequency hopping used to achieve better signal quality, to increase data security, to avoid multipath fading, or to avoid interference.

PLL lock time can be optimized by increasing the reference or comparison frequency, and, if necessary, by increasing the loop bandwidth.

With the ADF4153, a reference frequency or PFD frequency up to 32 MHz can be chosen, or the available frequency doubler can be used to increase the PFD frequency while using a lower frequency reference clock.

The definition of the PLL loop bandwidth is a trade-off between the required settling time, the acceptable phase error, and the spurs level. The larger the loop bandwidth is the faster the lock time, at the expense of higher phase error and spurs level. But if the lock time is not critical, using a narrow-loop bandwidth is recommended for the reasons described in the Phase Noise section.

### Performance

In this particular characterization, the PLL has been designed for a closed-loop bandwidth of about 20 kHz. For a 10 MHz 256 OFDM signal, the symbol duration is 25.6 µs, which corresponds to a subcarrier spacing of 39 kHz. Therefore, the PLL loop has voluntarily been designed slower than the symbol duration such that most of its phase noise can be tracked and removed by the pilot-tracking algorithm. Figure 13 shows the PLL schematic, including the loop filter.

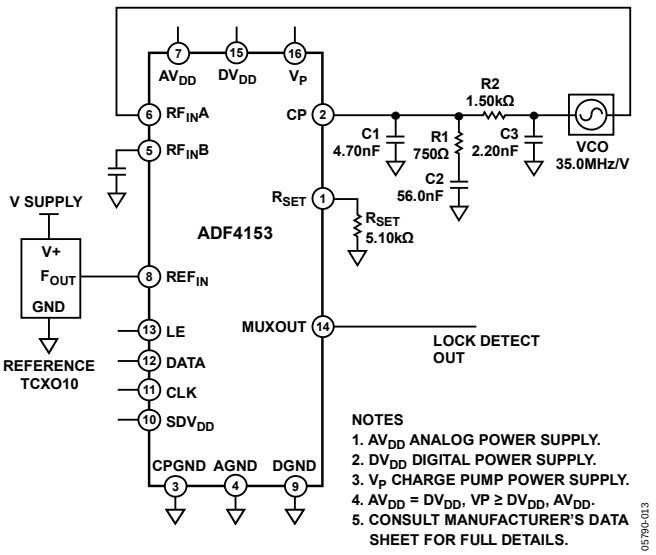


*Figure 13. PLL Loop Schematic*

Figure 14 shows the closed-loop phase noise performance of this PLL.

The VCO is a Sirenza VCO190-2350T(Y), with a tuning sensitivity of 35 MHz/V typical. PLL closed-loop in-band phase noise is −95 dBc/Hz.

The equivalent rms phase error for this design is only 0.35°rms, equivalent to an EVM contribution of 0.6%. The contribution of this fractional-N PLL to the overall EVM performance is given in the Overall System Performance section.

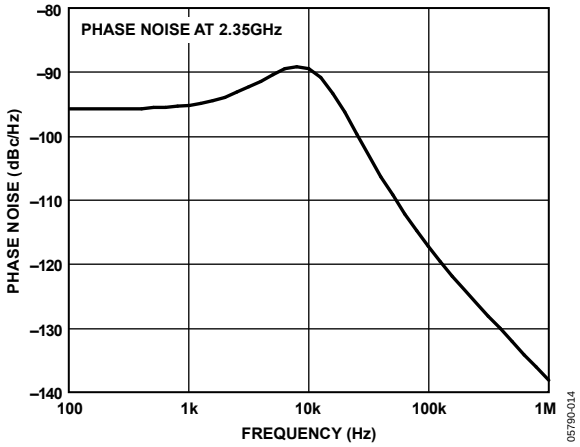


*Figure 14. Closed-Loop Phase Noise Simulation at 2.35 GHz*

## THE VGA AND THE INTERFACE TO THE IQ MODULATOR

Because WiMAX systems can be used for nonline-of-sight applications, gain control of the transmitter is necessary to adjust the output Tx level depending on the channel quality.

The ADL5330 is a high performance VGA, 50 Ω I/O, which provides close to 50 dB of gain control at 2.3 GHz, with a gain control slope of about 60 dB/V. A positive control voltage from 0.5 V to 1.4 V is required to control the gain of the VGA. At $V_{GAIN}$ = 1.4 V, a maximum gain close to 15 dB is achieved. The basic connections for interfacing the ADL5373 IQ modulator with the ADL5330 are shown in Figure 15.

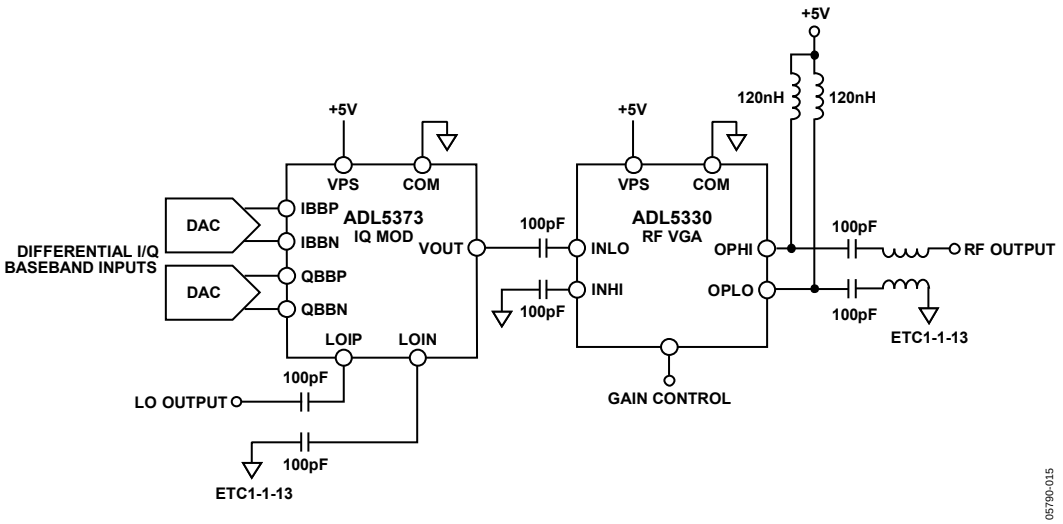


*Figure 15. IQ Modulator and RF VGA Interfaces*

The ADL5373 is designed to drive a 50 Ω load and easily interfaces with the VGA.

If less power is required from the VGA, adding a pad in between the modulator and the VGA is recommended. This helps maintain optimum linearity performance while improving the output noise floor.

For operation in the 2 GHz to 3 GHz bandwidth, using differential-to-single-ended baluns specifically matched in this bandwidth is also recommended. The ADL5330 provides differential input and output. For a single-ended interface, using a balun like the Murata SP-LDZ-49_LDB182G5005G helps to improve the RF gain by at least 1 dB.

## RMS POWER DETECTION

For accurate and fast power control, the AD8362 rms power detector can be used at the output of the power amplifier. This is a high accuracy, wideband rms-to-dc square law detector. The output of this square law function is a positive current that is integrated by both an on-chip capacitance and an external capacitance, CLPF. The resulting voltage is then buffered by a dc-coupled amplifier, which provides output that can be used for measurement and control purposes.

Figure 16 shows an rms power measurement technique through a directional coupler. For practical reasons, it has been placed at the VGA output, but can also be used to detect power levels at the power amplifier (PA) output.

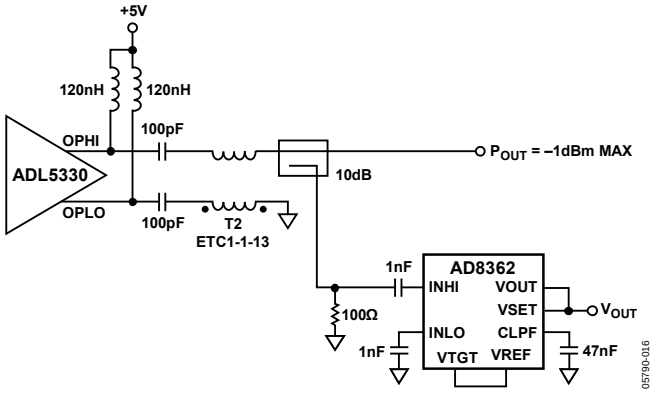


*Figure 16. Power Detection Using the AD8362*

The AD8362 takes either a differential input (for best detection range) or a single-ended input. Because the coupled port of a coupler is unbalanced, the AD8362 has been characterized with a single-ended drive, for all the potential modulations in the 802.16 standard.

An externsal filtering shunt capacitor is required at the output of the square law detector to remove the residual of the signal envelope. For WiMAX signals, a capacitor of 0.1 µF provides a good trade-off between the detection accuracy and settling time. But a smaller capacitor along with a fast sampling ADC can be used for a faster response.

**Table 2.**

| CLPF | Accuracy Within 40 dB | Settling Time |
|---|---|---|
| 0.1 µF | +0.3 dB/−0.5 dB | 160 µs |
| 47 nF | +0.3 dB/−0.75 dB | 78 µs |

The expected measured performance of the power detector is shown in Figure 29 and Figure 30.

Figure 17 shows the power detection error with CLPF = 1 µF and VTG = 0.625 V.

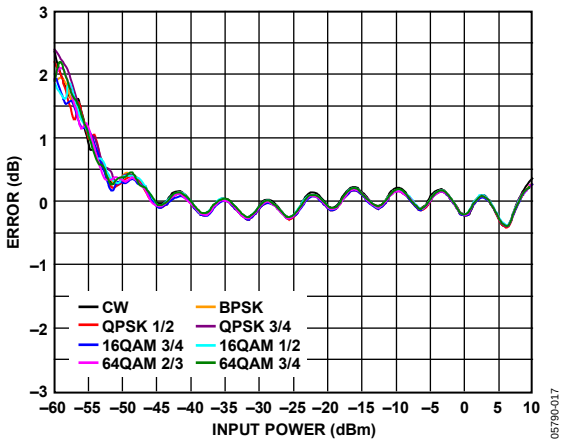


*Figure 17. RMS Power Detector Detection Range and Accuracy for CLPF = 1 µF*

With VTG = 0.625 V (connecting VREF to VTG through a resistive divider) and a smaller CFLT capacitor, similar performances can be achieved with a fast averaging ADC. In such configuration, the RMS detector is completely insensitive to the type of OFDM modulation applied to it. Therefore, no calibration is required, whether a QPSK or a 64 QAM modulates the OFDM subcarriers. Figure 18 shows the power detector settling time for CLPF = 47 nF.

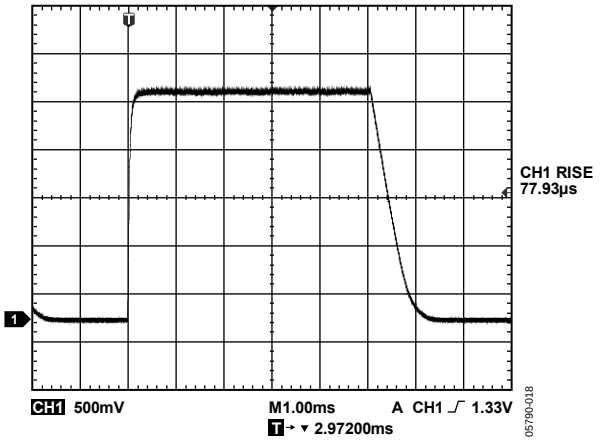


*Figure 18. Power Detector Time Response to a WiMAX Downlink Burst ($T_{SYMB}$ = 25.6 µs), CLPF = 47 nF*

### *Temperature Compensation*

To improve the measurement accuracy of the AD8362 over temperature at 2.35 GHz, a simple temperature compensation scheme can be used. It helps correct for the drift of the detector intercept point of the $V_{DET} = f(\text{Pin})$ characteristic. The whole transfer function tends to drop with increasing temperature, while the slope remains quite stable. Therefore, compensating the drift at a particular input level (for example, −15 dBm) holds up well over the dynamic range (see Figure 20).

The compensation is simple and relies on the TMP36 precision temperature sensor. At 25°C, the TMP36 has an output voltage of 750 mV and a temperature coefficient of 10 mV/°C. The positive temperature coefficient of the TMP36 can directly compensate for the negative temperature coefficient of the detector. The implemented circuit is given in Figure 19. (Note that the VOUT pin of AD8362 is depicted as VDET_OUT to avoid confusion within this figure.) The resistor ratio of R1 and R2 can be calculated so that the corrected VOUT_Comp voltage remains steady over temperature.

The temperature drift of the AD8362 at 2.35 GHz is −0.03 dB/°. It has been measured at a detector input power of −15 dBm.

The following equation shows how of the resistor ratio is calculated:

$$\frac{R2}{R1} = \frac{-\frac{\Delta V_{TM} P}{\Delta T}}{\frac{\Delta V_{DET}}{\Delta T}} = -\frac{10\text{ mV}/^{\circ}\text{C}}{AD8362\ Drift(\text{mV}/^{\circ}\text{C})}$$

The temperature drift of the AD8362 in dB/°C is converted to mV/°C through multiplication by the logarithmic slope of the detector (49.79 mV/dB at 2.35 GHz). In this application, the drift of −0.03 dB/°C is equivalent to −1.51 mV/°C.

Figure 20 shows the measured performance over temperature for the compensated circuit at 2.35 GHz. Note that the compensation factor was chosen to optimize temperature drift in the 0°C to 85°C range. This is consistent with end equipment where performance at low temperatures is less critical.

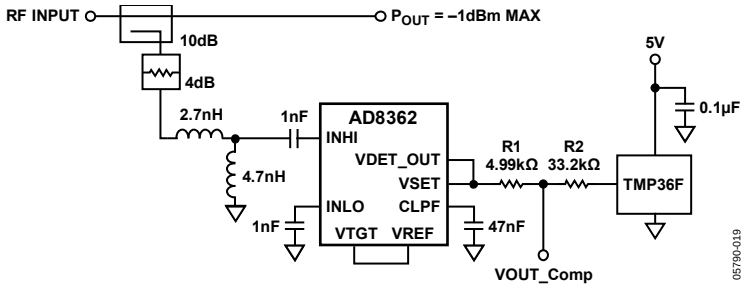


*Figure 19. Power Detection and Temperature Compensation of the AD8362 at 2.35 GHz*

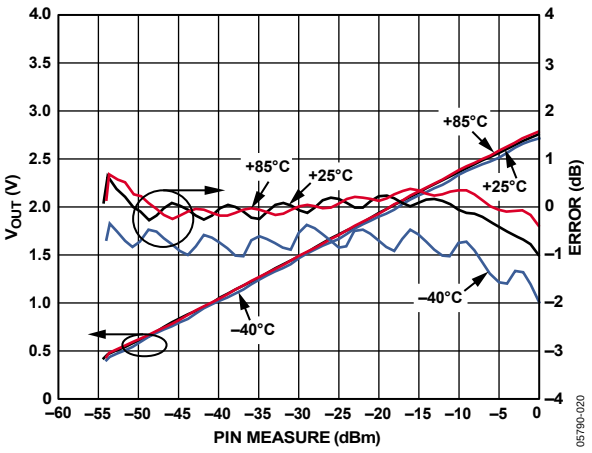


*Figure 20. Output Voltage and Temperature Drift of the AD8362 at 2.35 GHz with External Temperature Compensation*

## OVERALL SYSTEM PERFORMANCE

Table 3 gives a summary of the whole Tx chain performance. The following system performances have been characterized:

- Power control range
- Maximum linear output power
- Gain flatness
- Noise floor
- OP1dB and OIP3
- Power detector accuracy and detection range
- EVM with a WiMAX OFDM signal
- Spectral quality with a WiMAX OFDM signal

The OFDM signal is generated by extracting I and Q vectors off of a WiMAX signal generator. EVM performance was measured using the Agilent 89600 demodulating software.

For an OFDM signal, most of the EVM degradation is caused by the imperfections of the IQ modulator and the phase noise or phase error of the local oscillator. Some of the close-in phase noise modulating the subcarriers after upconversion can be removed by the phase tracking algorithm implemented within the receiver or demodulator.

The contribution of each building block of this transmit chain to EVM at −3 dBm of output power is as follows:

- DAC and IQMOD with ideal LO: *EVM* = 0.6%
- DAC and IQMOD + VGA with ideal LO: *EVM* = 1.02%
- DAC and IQMOD + VGA with Frac-N PLL: *EVM* = 1.21%

The fractional-N PLL used for this reference design has a phase error due to phase noise of 0.35° and only degrades the overall system EVM by 0.2%.

For these characterizations, the IQ modulator output power level was set around its optimum power level at −14 dBm. Then a 3 dB pad was added to drive the Tx VGA.

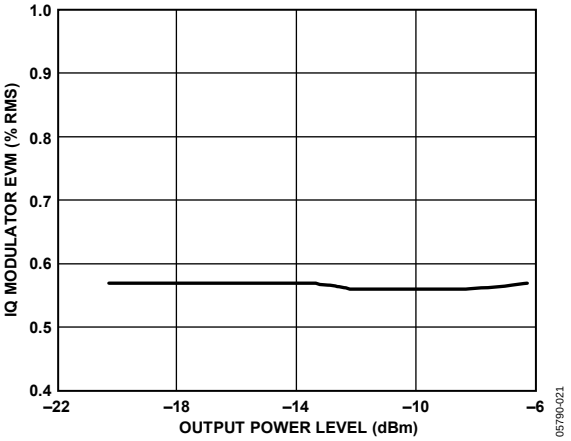


*Figure 21. IQ Modulator EVM in %rms vs. Output Power, 64 QAM OFDM*

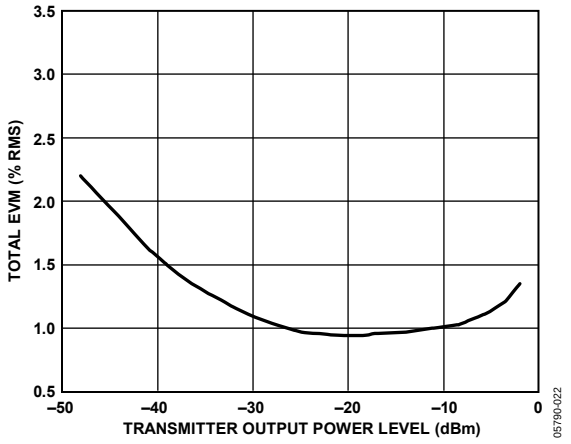


*Figure 22. Signal Chain Total EVM as a Function of the Tx VGA Gain*

With −17 dBm of input power, the VGA can deliver about −3 dBm with a very good EVM performance of 1.2%, as shown in Figure 22.

Figure 22 highlights the exceptional EVM performance of the ADL5373 IQ modulator over a good range of output power levels. Its contribution to the cascaded EVM performance is quite small.

At midpower, the EVM is basically driven by the IQ modulator and the LO synthesizer. As the output power reaches the lowest part of the dynamic range, EVM performance starts to degrade as the signal-to-noise ratio drops.

# TYPICAL PERFORMANCE CHARACTERISTICS

VPS1 = 5 V for the ADL5373, ADL5330, and AD8362 components. VPS2 = 3.3 V for ADF4153 and AD9860/AD9862. Radio frequency band: 2.3 GHz to 2.4 GHz.

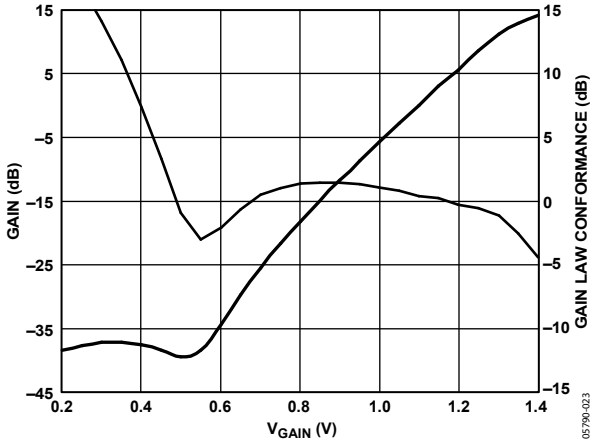


*Figure 23. Power Gain Range for −10 dBm Out of the IQ Modulator, and Gain Law Conformance vs. $V_{GAIN}$ at 2350 MHz*

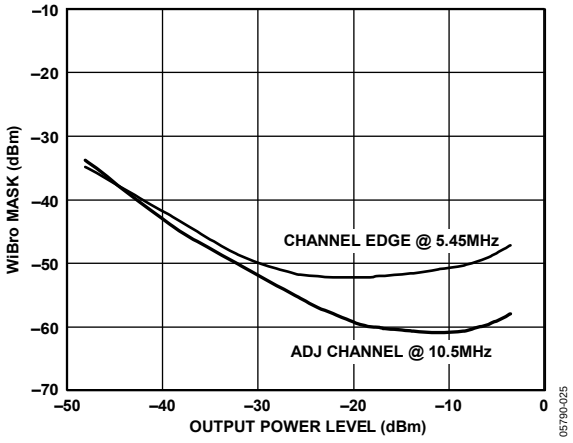


*Figure 25. Transmitter Spectral Quality According to WiBro Mask (64 QAM WiMAX OFDM, 10 MHz BW) Function of Output Power or $V_{GAIN}$ Voltage*

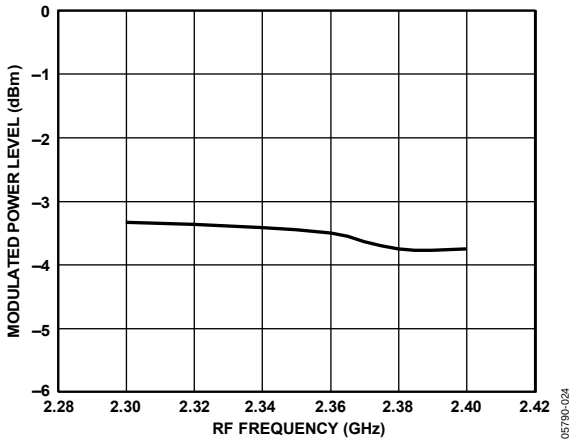


*Figure 24. Modulated Power Level vs. RF Frequency, with a Modulated OFDM Signal*

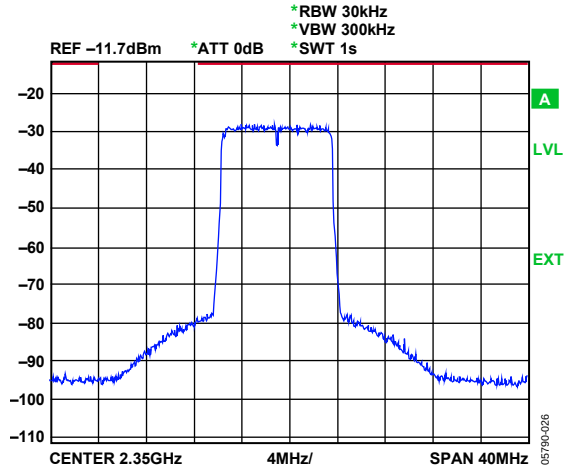


*Figure 26. Transmitter Output Spectrum @ 2.35 GHz (64 QAM WiMAX OFDM, Bandwidth = 10 MHz) at −5 dBm Output Power*

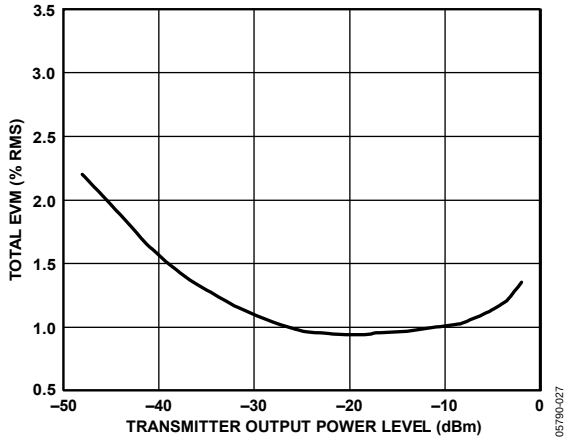


*Figure 27. Transmitter Total EVM for an 802.16 64 QAM OFDM Signal, 10 MHz Signal Bandwidth*

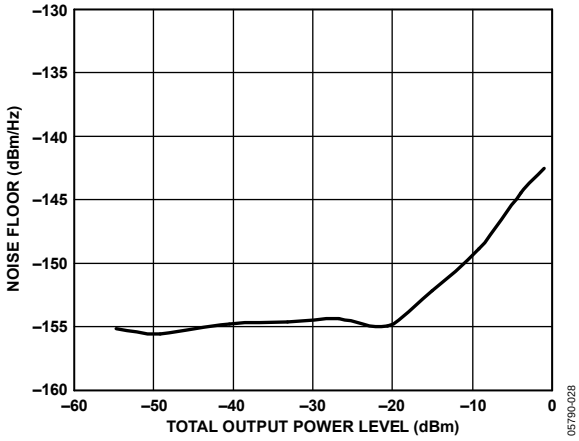


*Figure 28. Transmitter Output Noise Floor vs. Output Power (QPSK, 16 QAM, 64 QAM OFDM Modulated Signal)*

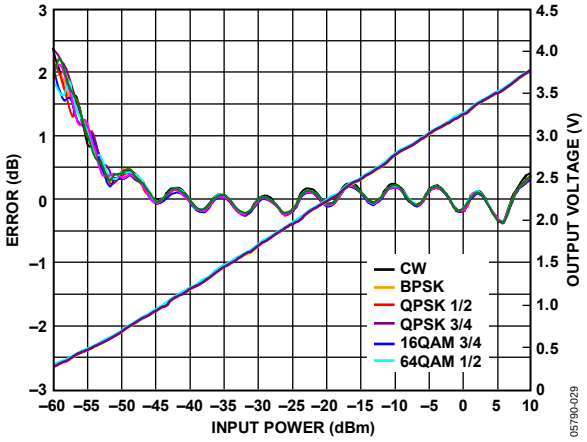


*Figure 29. RMS Power Detector Response and Detection Error vs. Tx Signal Chain Output Power Level for QPSK, 16 QAM, 64 QAM OFDM Modulations*

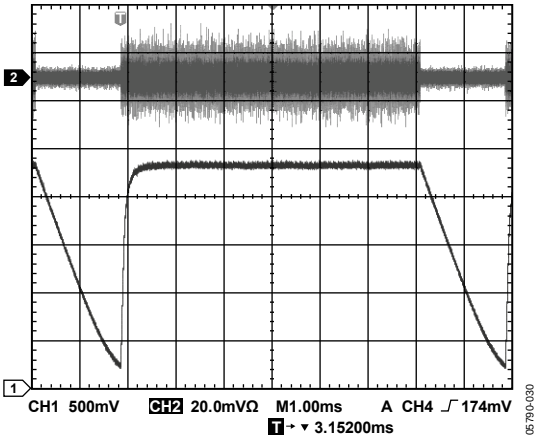


*Figure 30. Power Detector Time Response for a WiMAX Downlink Burst (Long Preamble, FCH, 64 QAM OFDM Data Sequence), $T_{SYMB}$ = 25.6 µs*

# SUMMARY OF MEASURED PERFORMANCE

VPS1 = 5 V (ADL5373, ADL5330, and AD8362). VPS2 = 3.3 V (ADF4153, AD9860/AD9862 DAC). Radio frequency band: 2.3 GHz to 2.4 GHz. Signal bandwidth = 10 MHz. QPSK, 16 QAM, and 64 QAM, 256-subcarriers OFDM modulation.

**Table 3.**

| Parameter | Conditions | Typ | Unit |
|---|---|---|---|
| Maximum Linear Output Power Level | 64 QAM OFDM, EVM = 1.2 % | −3 | dBm |
| Output Power Control Range | @ 2.35 GHz, ±3 dB gain law conformance, VGA input power <−10 dBm | 51 | dB |
| Gain Flatness vs. Frequency | 2.3 GHz to 2.4 GHz band | 0.005 | dB/MHz |
| | Worst case for any BW = 20 MHz | 0.25 | dB |
| OIP3 | @ 2.35 GHz, $V_{GAIN}$[1] = 1.4 V | 19 | dBm |
| OP1dB | @ 2.35 GHz, $V_{GAIN}$ = 1.4 V | 12.4 | dBm |
| Spectral Mask/ACP | RBW = 100 kHz, VBW = 30 kHz | | |
| | 64 QAM OFDM – $P_{OUT}$ = −5 dBm, 10 MHz signal | | |
| | Adjacent channel at 10MHz offset | −55 | dB |
| | WiBro mask first offset @ channel edge | −48.5 | dBr |
| | WiBro mask second offset @ center of adjacent channel | −59 | dBr |
| EVM vs. Gain Control | 64 QAM OFDM, 2.35 GHz | | |
| | $P_{OUT}$ = −3 dBm, $V_{GAIN}$ = high | −38.4 | dB |
| | | 1.2 | % |
| | $P_{OUT}$ = −30 dBm, $V_{GAIN}$ = low | −39.1 | dB |
| | | 1.1 | % |
| Broadband Noise Floor | Offset frequency = 20 MHz, $P_{OUT}$ = −1 dBm or $V_{GAIN}$ = 1.4 V | −142.5 | dBm/Hz |
| | Offset frequency = 20 MHz, $P_{OUT} \leq$ −20 dBm or $V_{GAIN} \leq$ 1 V | −155 | dBm/Hz |
| RMS Power Detection Range | All modulation types, error < ±0.5 dB | 60 | dB |

[1] $V_{GAIN}$ is the ADL5330 gain control voltage.

**Table 4. Power Supply**

| Parameter | Conditions | Typ | Unit |
|---|---|---|---|
| Positive Supply Voltage 1 | | 5 | V |
| Quiescent Current | Total current for the ADL5373, ADL5330, and AD8362 | 380 | mA |
| Positive Supply Voltage 2 | | 3.3 | V |
| Quiescent Current | Total current for the ADF4153, AD9860/AD9862 Tx paths at 80 MSPS | 165 | mA |

# BILL OF MATERIALS FOR MAJOR COMPONENTS

**Table 5. Components Description (Excludes Passives)**

| Component | Function | Vendor | Evaluation Board Part No. |
|---|---|---|---|
| AD9860/AD9862 | Mixed signal front end (ADC and DAC) | Analog Devices, Inc. | AD9860-EB, AD9862-EB |
| ADL5373 | Direct conversion IQ modulator | Analog Devices, Inc. | ADL5373-EVALZ |
| ADL5330 | Voltage-controlled amplifier/attenuator | Analog Devices, Inc. | ADL5330-EVAL |
| ADF4153 | Fractional-N PLL | Analog Devices, Inc. | EVAL-ADF4153EB1 |
| AD8362 | RMS responding power detector | Analog Devices, Inc. | AD8362- EVALZ |


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