Design Circuits with Digitally Controllable Variable Resistors

AD8402/3 dual/quad digital pots set resistance values and ratios remotely

by Walt Heinzer

Here is the first viable cost-effective substitute for trimmers and potentiometers in new designs. This new IC family offers digital control of the variable-resistance function. Basically a set of D/A converters in which resistance—or resistance ratio—is the analog variable, they are in contrast to (but complement) the family of TRIMDACs® (*Analog Dialogue* 24-3, 1990, pp. 16-18), which can be thought of as *buffered potentiometers*. The newer devices are controllable circuit elements—*variable resistors* (VRs) or *unbuffered pots*; for example, they allow users to directly program time constants and filter cutoffs in traditional R-C circuits.

The first of these, the 2-channel 8-bit (256 positions) AD8402 and 4-channel AD8403 (Figure 1), provide standard full-scale resistance values of 10 kΩ, 50 kΩ and 100 kΩ, with ±20% tolerance. A "wiper contact" taps the resistor (R_{AB}) at a point selected by the digital input. The resistance between the wiper and point B is nominally proportional to the stored digital code, and the resistance between the wiper and point A is proportional to its 2s complement (complement + 1 LSB). Requiring +3-V to +5-V single supplies to operate the switches, the devices are programmed by a 3-wire serial data interface that is compatible with many of the standard microcontroller serial buses, including SPI, QSPI and the Intel microcontroller serial data ports.

Ideal for low-power, battery-operated applications, these devices conserve power in several ways. The digital interface circuits use standard static CMOS logic, which dissipates power only during updates; once set, only nanoampere-level leakage currents flow. A digital *shutdown* mode open-circuits the variable resistor, reducing its current to zero. After the shutdown mode is ended, the previous setting is returned if the V_{DD} supply has not been interrupted. Another useful digital function, *midscale reset*, sets the device at mid-range when initially powered up; the controlled signal can then be adjusted up or down to a final value.

The AD8402/3 were designed to allow circuit *resistances* to be controlled remotely with precision. Previously, only currents, voltages, and gains could be controlled digitally (i.e., by DACs). For applications where simple resistance adjustments would be adequate, the use of complete DACs could lead to "overkill" in terms of circuit complexity, space, power, and cost.

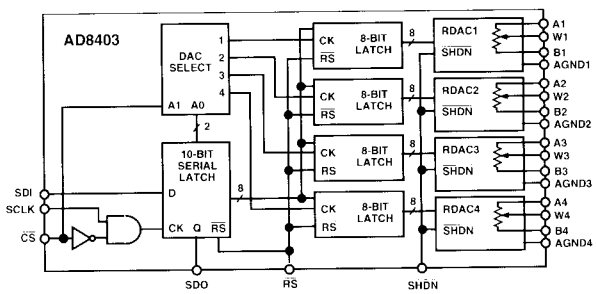

Figure 1. AD8403 Functional block diagram.

As portable circuit designs become ever-more-compact, pots are too big to fit; if used, they are hard to access. The >3-mm height of the smallest trimmers makes them impractical for many compact portable designs—for example, TYPE I PCMCIA-card circuit standards require all components to have a physical height <2 mm. The higher circuit density possible with digitally adjustable IC resistors resolves these space constraints, removes active signals from instrument front panels, reduces wiring costs, and makes it possible to save "front panel" settings in EEPROM.

Thus the digital potentiometer ("RDAC") provides the solution, with its compact 1.5-mm high SO-14 package and 256 settings. It can be located directly at the circuit point requiring adjustment to minimize noise pickup and simplify front-panel wiring. It is free from the problems of shock, vibration, and open-contacts that often disqualify pots. And it is programmable—settings can be saved in system memory for later recall. The three-terminal functionality—full access to both ends of the pot and the wiper—allow it to be employed in simple panning circuits. As a variable resistor, the AD8402/3 can be combined with capacitors for simple programmable time-constant adjustments in standard low-pass and high-pass filters for a variety of applications.

OPERATION

The two principal configurations of the RDAC are the 3-terminal potentiometric divider and the two-terminal rheostat. In Figure 2a, the open-circuit voltage, V_{WB}, is proportional to the digital input value. In 2b (A open), the resistor, R_{WB}, is proportional to the digital input (and is in series with 50-Ω contact resistance).

A few boundary conditions must be satisfied for proper operation of the AD8402/03: All analog signals must remain within the applied single-supply voltage range. For standard pot/divider applications, the wiper output can be used directly, but for low-resistance loads, buffer the wiper with a suitable rail-to-rail op amp, such as the OP291 or OP279, to maintain linearity and provide drive current. For ac signals and bipolar dc adjustments, an offset ground (e.g., a 2.5-V reference) will generally be needed. It must be able to handle any necessary sink and source current for all connected loads and bypass capacitors.

RDAC PARAMETRIC PERFORMANCE

The basic specs used in selecting any variable resistor include *nominal resistance*, *tolerance*, and *temperature coefficient* (TCR/tempco). The AD8402/3 are available in 10-kΩ, 50-kΩ and 100-kΩ standard values with ±20% tolerances. The nominal TCR at midscale is 500 ppm/°C, with a typical long-term drift of 0.1%.

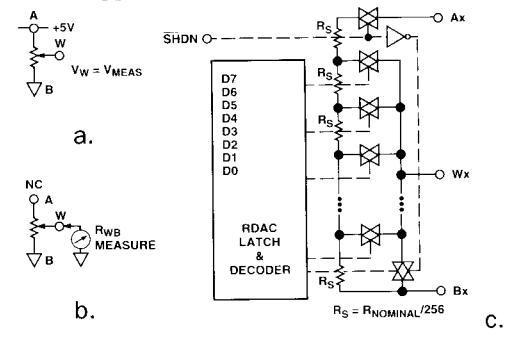

Figure 2. Equivalent circuits. a. Potentiometer divider: 3-terminal connection. b. Rheostat: 2-terminal connection. c. Equivalent RDAC circuit, showing $\overline{\text{SHDN}}$ switches.

In addition, the specs must include *resolution* (256 positions—8 bits), *operating supply range* (+3 to +5 V), and *position linearity*. For potentiometer divider applications, conventional DAC integral and differential nonlinearity specifications (INL and DNL) apply. For the rheostat, (as measured between the wiper and the end terminals), new parameter definitions (and associated test circuitry) were needed to define nonlinearity of the resistance step position value in relation to code. Modeled on INL and DNL, (test circuits are provided on the data sheet) they are:

- **R-INL**, *Resistor position integral nonlinearity*—the worst-case deviation from ideal value over the range from maximum-resistance to minimum-resistance wiper positions.
- **R-DNL**, *Resistor position differential nonlinearity*—compares the actual step change with the ideal, ($R_{WBfull\ scale}/256$) between successive tap positions.

The AC characteristics of the RDACs are dominated by the internal parasitic capacitances and the external capacitive loads. The *–3-dB bandwidth* of the AD8403AN10 (10-kΩ resistors) measures 600 kHz at half-scale as a potentiometric divider. The *total harmonic distortion plus noise* (THD+N) is measured at 0.003% in an inverting op-amp circuit using an offset ground and the rail-to-rail OP279 amplifier (Figure 3 left). *Thermal noise* is primarily Johnson noise, typically 9 nV/$\sqrt{Hz}$ for the 10-kΩ version at f = 1 kHz. *Channel-to-channel crosstalk* measures less than 65 dB at f = 100 kHz. To achieve this isolation, the extra ground pins provided on the package to segregate the individual RDACs must be connected to circuit ground. *Power supply rejection* is typically –35 dB at 10 kHz (care is needed to minimize power supply ripple in high-accuracy applications).

As noted earlier, special attention has been paid to device power consumption. After transient current flows at data changes, the internal logic consumes typical leakage currents of 10 nA at room temperature. The variable resistor will of course dissipate power whenever current is flowing through the wiper and terminals. The shutdown feature will asynchronously open-circuit the device (Figure 2c), stopping power dissipation in the variable resistor when the $\overline{SHDN}$ pin is asserted, without affecting the wiper position setting held in the RDAC latch. After exiting from shutdown, the wiper returns to its previous setting.

Both devices operate over the extended industrial temperature range, –40 to +85°C. The AD8402 is available in 14-pin plastic DIPs and SO; the AD8403 is available in a SOIC-24 package. 10, 50, and 100-kΩ options are designated by the digits at the end of the part number; e.g., AD8402AN10 is a 10-kΩ device in a plastic DIP.* Prices for AD8402/03 in 1000s are $1.66/$2.51.

APPLICATIONS

Figure 3a shows one channel of the AD8402 connected in an inverting wide-range programmable-gain op-amp circuit. The +2.5-V reference serves as an offset "ground", allowing the circuit's output to span a ±2.5-volt range, using the rail-to-rail OP279 amplifier. For gains >1 (code = 80_H), the digital input is increased toward code FF_H; for gains <1, the digital input is decreased toward code 00_H. The plot in 3b shows the wiper settings for a 100:1 range of voltage gain (V/V). Note the ±10 dB of pseudo-logarithmic gain around 0 dB. This circuit is mainly useful for gains from 0 V/V to 4 V/V; beyond this range, the step sizes become very large, and the resistance of the driving circuit can become a significant term in the gain equation.

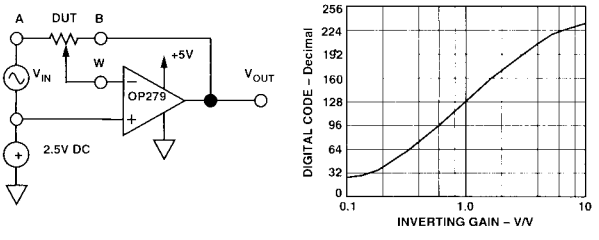

Figure 3. Inverting programmable gain amplifier and plot of settings for gains from 0.1 to 10 (log scale).

*For technical data and/or an AD8402AN10 sample, use the reply card. Circle 3 for data, 4 for sample.

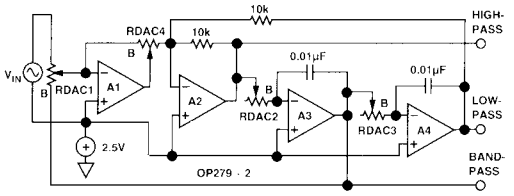

Figure 4. Programmable state-variable active filter.

Active filter: The state-variable filter circuit can simultaneously exhibit low-pass (LP), high-pass (HP), and bandpass (BP) filter characteristics; it is an analog computing circuit solving a second-order differential equation. Digital pots and resistors can be used instead of DACs to program frequency, gain, and Q (Figure 4).[1] The filter circuit uses a +2.5-V virtual ground, which readily allows up to 4-V p-p input and output swing for each stage.

RDACs 2 and 3 set the LP and HP cutoff frequencies—and the BP center frequency. With equal *C*s, they are programmed with equal data (like ganged pots) for best dynamic range. The bandpass gain depends only on RDAC1; then RDAC4 can be used to adjust the Q (which depends on RDAC1, RDAC4, and the ratio of RDACs 2 & 3). Figure 5a shows the measured BP filter response over a range of center frequencies from 2 kHz to 20 kHz. The filter gain response at the BP output is shown in Figure 5b, as RDAC1 adjusts the gain over a range of –20 to +20 dB at a center frequency of 2 kHz. As expected, circuit Q varies with gain. For more detailed reading on the state-variable active filter, see Analog Devices Application Note AN-318.

Adjustable timer: The AD8402, with a capacitor and a comparator, can produce programmable time-delayed switching after a step input. Similarly, the RDAC can be used to improve the accuracy of 555-timer circuits, such as a calibrated one-shot.

The AD8402/3 was designed by James Ashe at ADI's Santa Clara, CA, site.

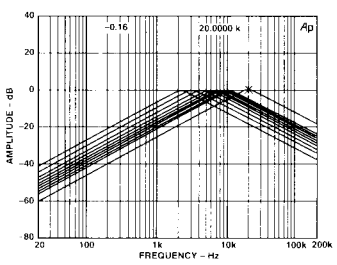

Figure 5a. Bandpass output vs. frequency at unity gain.

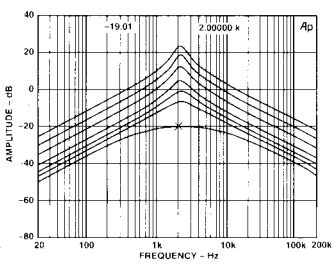

Figure 5b. Bandpass output over a gain-range of 100:1.

[1]See p. 247 ff., *Analog-Digital Conversion Handbook*, 3rd edition, Engineering Staff of Analog Devices, ed. by Daniel H. Sheingold. Englewood Cliffs, NJ: Prentice Hall, 1986. Available from Analog Devices. [use book purchase card]