ANALOG DEVICES

AN-1341
APPLICATION NOTE

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Using the AD8436 True RMS to DC Converter

by James Staley

INTRODUCTION

The AD8436 from Analog Devices, Inc., is a complete true rms measurement system on a chip. It offers designers the greatest flexibility in meeting their application needs, combined with the smallest overall footprint and lowest power available in an off the shelf analog ac measurement front end.

The AD8436 is comprised of three completely independent circuit blocks, as shown in Figure 1. The rail-to-rail field effect transistor (FET) input amplifier, high dynamic range, true zero rms computing core, and precision rail-to-rail output amplifier facilitate measurement systems that operate from high impedance voltage sources in the megohm range. In concert, these three components of the AD8436 deliver highly accurate dc output voltages equivalent to the rms value of applied input voltages at levels near zero and, with appropriate input attenuation, well above its maximum rated input voltage.

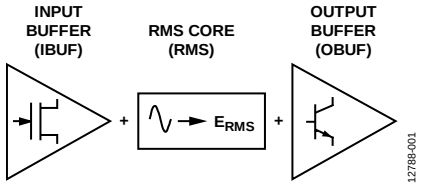

Figure 1. The Three Independent Circuits

Throughout this application note, components that are internal to the AD8436, such as the R_{V-I} and R_{I-V} resistors, are denoted by subscripted text. External components, such as the CAVG, CIN, and CCF capacitors, are denoted by all capital letters to remain consistent with evaluation boards.

GENERAL DESCRIPTION

Referring to Figure 2, the heart of the AD8436 is a true zero, high dynamic range, analog computing core. The design of this core ensures continuous operation from ≤1 mV to 3 V voltage levels. The AD8436 rms core features a higher dynamic range and faster, more consistent response than previous Analog Devices rms to dc converter products.

For applications in which the signal source is sensitive to loading errors, or a boost in gain is required to amplify low level ac signals, the integrated FET input amplifier matches real-world signals to the converter core. There is no need for additional components or space on already crowded printed circuit boards (PCBs).

The precision dc output amplifier for driving low impedance loads optimizes performance between the converter core and the next stage. The output buffer is also configurable as a Sallen-Key or other active filter architecture, further reducing settling time to levels not feasible in other analog or even digital rms to dc solutions.

All of this functionality is available in RoHS compliant, 20-lead LFCSPs and QSOPs.

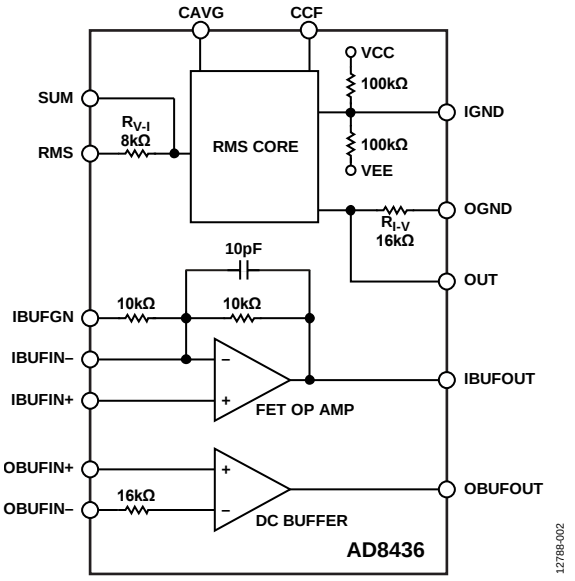

Figure 2. Functional Block Diagram of the AD8436 RMS to DC Converter

SCOPE

This application note is a how-to, in-depth exploration of configuration options of the AD8436, while at the same time striving for clarity. Feedback from engineers is incorporated wherever possible and most of the circuits shown are verified experimentally. Simulations or other forms of vaporware are minimal. Many applications and ideas are inspired by email and questions received from the many AD8436 users.

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REVISION HISTORY

1/15—Revision 0: Initial Version

USING THE CORE

USING THE RMS PIN

For those applications where cost and power consumption are the primary concerns, only the core and two external capacitors (excluding supply filtering) are required for basic ac-to-dc conversion (see Figure 3 and the Single Supply Operation section). Input voltages are typically ac-coupled to the RMS pin via a low leakage capacitor (CIN), such as a metallized polyester or a good quality tantalum capacitor. The applied voltage is converted to current by the 8 kΩ resistor, R_{V-I}, connected to the rms core. The junction of R_{V-I} and the core behaves somewhat like that of an op amp configured as a summing amplifier, with some important exceptions. For additional details, see the Capacitor Selection section and the SUM Pin section where these differences are explained. Because the thin film resistors, R_{V-I} and R_{I-V}, are ratio matched and have ratiometric temperature characteristics, the RMS pin is preferred as the input port for nearly all applications.

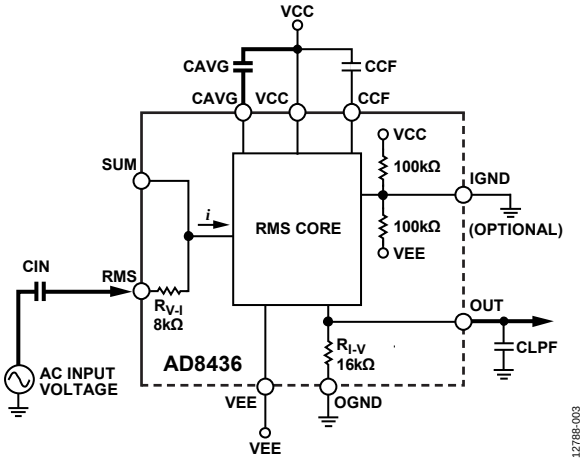


Figure 3. Minimum of Input/Output Connections (Emphasized Lines are the Signal Path)

The input impedance at the RMS pin is the 8 kΩ voltage to current conversion resistor (R_{V-I}), referred to the IGND pin. If the input is provided by a voltage source (that is, ZOUT = 0 Ω) the input amplitude is unaffected by the relatively low 8 kΩ input resistance. Capacitor CIN blocks dc current to and from the core, resulting in negligibly small input referred offset voltages (for example, V_{OS} < ±10 μV). A high voltage capacitor is often used for the CIN capacitor to help protect the AD8436 from hazardous voltages such as ordinary household line voltages. Note that the FET input buffer amplifier (IBUF) easily accommodates voltages from nonzero resistive voltages sources, even those in the megohm range. See the Input and Output Op Amps section for more details.

BASIC AC-COUPLED TRIMMING

For external calibration, increase the value of the internal resistor, R_{V-I}, by inserting a low value metal film resistor between the signal source and the RMS pin (200 Ω shown in Figure 4). Add a small trimmer (RTRIM = 500 Ω in Figure 4) from the OGND pin to ground. The AD8436 is calibrated by adjusting RTRIM with no interaction with V_{OS}.

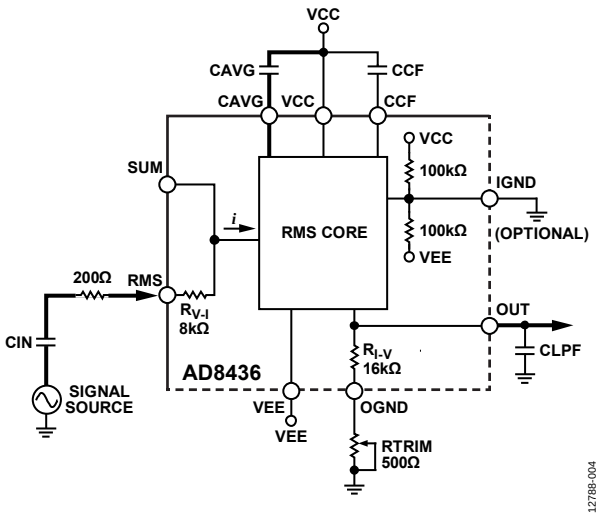


Figure 4. Basic AC-Coupled Calibration

DC COUPLING THE INPUT—CALIBRATION AND V_{OS} TRIM

When the input pin, RMS, of the AD8436 is dc-coupled to the signal source, the combined dc and ac signals are processed as ac + dc (see the SUM Pin—Multiple Input Characteristics section). However, a small dc offset error (V_{OS}) is created from minor dc error sources in the core. The AD8436 is tested for V_{OS} error in production and guaranteed to data sheet specifications (<0.25 mV for the B grade model and <0.5 mV for the A grade and J grade models).

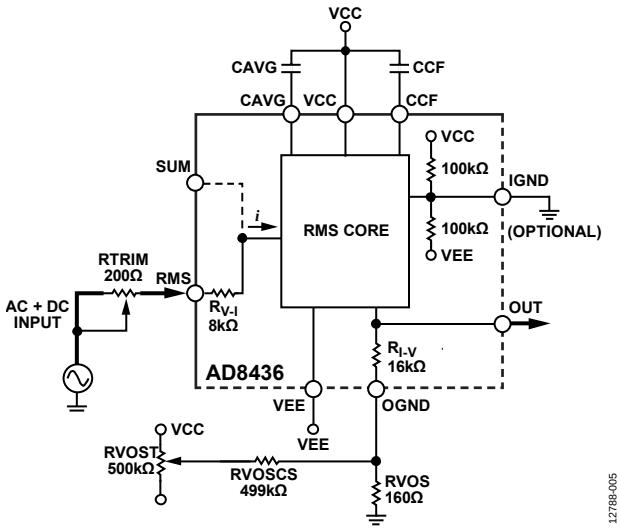


Figure 5. Optional Input Connections for AC + DC Signals, Including Offset Correction and Trim (VCC = +5 V, VEE = −5 V)

Figure 5 shows how to reduce any small V_{OS} error by inserting a small fixed resistor (RVOS = 160 Ω) in series with R_{I-V} from the OGND pin to ground. A current source consisting of the RVOST trimmer with RVOSCS in series with the wiper is connected to the OGND pin. The current source adds or subtracts a small current nulling the offset current. Because the value of R_{I-V} changes with the addition of 160 Ω, Resistor R_{I-V} must be compensated with an external resistor connected between the RMS pin and the signal source. A 200 Ω trimmer provides a more than adequate trim range. To trim the device, remove any input signal and set the dc output at the OUT pin to 0 V using RVOST. Next, apply a 300 mV, 1 kHz test signal to the 200 Ω trimmer and adjust for 300 mV dc at the OUT pin. If there is interaction between the two adjustments, repeat the sequence until the desired result is achieved.

SUM PIN

The SUM pin provides direct access to the rms core, effectively altering the range of usable input voltages. Direct core access is an optional feature unique to the AD8436.

For range shifting applications, increasing or decreasing R_{V-I} optimizes the desired errors over the default range inherent to the embedded 8 kΩ value. Resistors with values less than the internal 8 kΩ at the RMS pin increase the core input current; the opposite result occurs with values greater than 8 kΩ. This method of core scaling is a convenience, obviating external attenuators or amplifiers. When combined with the adjustable gain feature of the on-chip FET input amplifier and scalability of the output voltage, low level voltages convert to greater current levels without degrading settling time, as is the case when using the RMS pin.

When using the SUM pin, one must consider temperature error due to mismatch of the temperature coefficients of R_{V-I} and R_{I-V}. The temperature coefficients of resistance (TCR) of the fabricated silicon chromium (SiCr) resistors used in the AD8436 is <50 ppm. If temperature drift error is important, use resistors with equal TCRs. For low current applications, consider supplementing the 8 kΩ R_{V-I} by adding just enough external resistance to equal the desired value.

SUM Pin—Multiple Input Characteristics

Using separate V to I resistors, multiple voltages can be applied to the SUM pin. However, unlike a typical op amp summing circuit where the output is the arithmetic sum of input voltages, input voltages applied to the SUM pin convert to the residual sum of squares (RSS) of the input voltages. For two rms voltages, V_{RMS1} and V_{RMS2},

$$V_{OUT} = \sqrt{(V_{RMS1})^2 + (V_{RMS2})^2}$$

As an example, if one introduces a dc voltage of 100 mV to a 100 mV, 60 Hz ac voltage to the SUM pin, the dc component does not generate an ac conversion offset at the output (that is, 200 mV). Rather, the result is 141 mV dc.

$$V_{OUT} = \sqrt{(0.1\text{ V ac})^2 + (0.1\text{ V dc})^2} = 0.141\text{ V dc}$$

Fortunately, there is a way to add fixed offset voltages to the output of the AD8436, which is discussed in the DC Matching Devices with Dissimilar Common-Mode Voltages section).

CAPACITOR SELECTION

External capacitors are required to decouple the input (CIN), to compute the mean rms dc (CAVG), and for ripple suppression (CLPF) at the OUT pin. Capacitor CLPF is also used when the AD8436 is configured to yield the average rectified value. The CAVG and CFILT capacitors, in conjunction with the internal 5 kΩ and 16 kΩ charging resistors, directly control the settling time of the converter. Capacitor CCF is a secondary averaging capacitor, and forms the second pole of a passive RC low-pass filter. The 3 dB frequency of Capacitor CCF must be adjusted to no less than 3× the frequency of the primary pole frequency controlled by CAVG.

Input Decoupling Capacitor (CIN)

Capacitor CIN connects to the V to I resistor to form a high-pass filter, referred to IGND (common). The series attenuation of X_C approaches 0 Ω as the input frequency (f) approaches ∞. Or, to put it another way, the capacitor value must increase to accommodate lower frequencies.

A very simple way to calculate the value of CIN is to express the required error in ohms reactance as a percent of R_{V-I}, and then calculate the equivalent capacitance at the required frequency. In this instance, where R_{V-I} is 8 kΩ, the equivalent series resistor for 1% error is R_{ERR} = 80 Ω and the minimum capacitor value is

$$CIN \approx 1/\omega R_{ERR} = 1/2\pi 50 \times 80 = 40\ \mu F$$

The nearest standard value is 47 μF, in which case the capacitive reactance is 68 Ω at 50 Hz, and the error is 0.85%.

Averaging Capacitor (CAVG)

Basic rms to dc conversion requires an external capacitor (CAVG) for providing the mean (or average) value of rms. Use any of the following three methods to select the value of the CAVG capacitor.

Method 1 is an easy graphical method shown in Figure 7. Simply locate the desired frequency and error level on the horizontal and vertical axes and draw lines from these points. Choose or estimate the higher capacitor value where the lines intersect. The orange marks and dashed lines are two examples where the frequencies of interest are 50 Hz and 60 Hz, and the acceptable error is 1%. The nearest standard capacitor value is 2.2 µF for both examples.

Method 2 is an rms error expression from Table 1. Use one of these three empirically derived expressions for a more precise numerical result, then select the next higher standard value capacitor.

Table 1. CAVG vs. Frequency (f) Equations for Three RMS Error Values (Method 2)

RMS Error (%)	CAVG (µF)
0.1	200/f
1	70/f
5	20/f

Method 3 (see Figure 6) is a graphical method displayed as a log-log graph. The orange mark and dashed lines define the point where the desired frequency (50 Hz) and value of CAVG coincide on a log-log plot, whereas the blue diagonal line is the error value (1%). Figure 6 is useful for selecting smaller averaging capacitors for higher frequency applications.

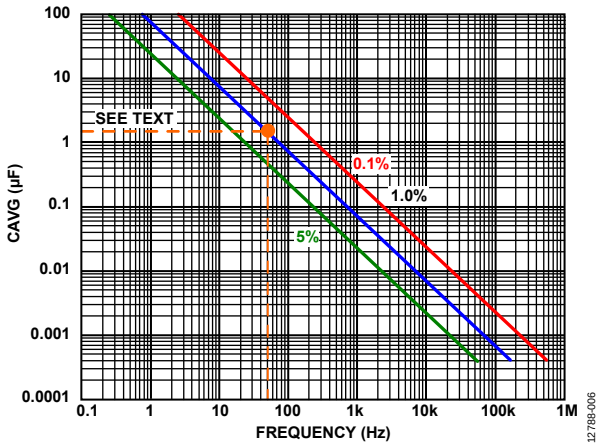


Figure 6. CAVG vs. Frequency for Three Error Values (Method 3)

In terms of circuit topology, the averaging capacitor is placed following the squaring and root extraction cell of the rms core. Its sole function is to store enough charge from each of a succession of the absolute value periods to develop a ripple free dc voltage. The best way to visualize this function is to think of the filter capacitor found in any dc power supply. Because the capacitor is located within the implicit conversion feedback loop, the resulting dc voltage constitutes the rms to dc conversion. For most applications requiring an rms result, the capacitor value needs only to be large enough to average sufficient periods of the input waveform to yield the maximum permissible error at the frequency of interest.

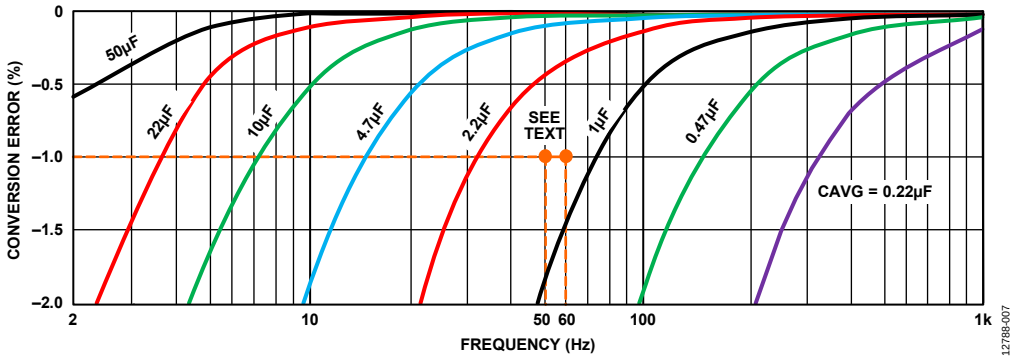


Figure 7. Conversion Error vs. Frequency for Various Values of CAVG (Method 1)

Low-Pass Filter Capacitor (CLPF)

The output impedance of the AD8436 is 16 kΩ referred to ground. Residual ripple errors following rms conversion are most effectively filtered at this point because the voltage source drive charges the capacitor, CLPF, through a 5 kΩ resistor unaffected by drive impedance. The output structure is a current source driving a 16 kΩ resistor that transforms to a voltage source with 16 kΩ resistance. When a capacitor is connected to this point (in this instance, the OUT pin) it becomes a low-pass filter referred to ground. Experiments have shown that a combination of 10 µF for the CAVG capacitor and 3.3 µF for the CLPF capacitor reduces the ripple to <1 mV, peak-to-peak, for a 300 mV rms, 60 Hz sine wave input waveform. Noise and settling time improve with the output buffer configured as a two-pole, Sallen-Key low-pass filter, as shown in the Low Cost, 3-Phase Power Line Monitor—Optimizing Settling Time section.

Crest Factor Capacitor (CCF)

Crest factor errors are not an issue for most sinusoidal applications; however, such errors are important if low duty cycle square waves or pulses are to be measured accurately.

The CCF pin is a node connected to a tap on the 5 kΩ resistor that charges the CAVG capacitor. Connecting a capacitor at this point adds a pole to the rms low-pass filter. The exact value of the CCF capacitor is not critical, but must be <10% of the value of CAVG to ensure the two capacitors behave as a two-pole, RC low-pass filter. A 100 nF filter is used in the AD8436-EVALZ evaluation board and is the default value used for most characterization data.

Capacitor Styles

RMS to dc converter data sheets recommend using high quality capacitors for the CAVG capacitor, but say very little as to what exactly is critical for the application. Legacy Analog Devices data sheets recommend tantalum style capacitors, and these are still a good choice, but today more options are available. The most critical attributes of the averaging capacitor are dc leakage (terminal to terminal resistance) and, to a lesser extent, dielectric absorption (see Figure 30).

Thanks to steady improvements in dielectrics, leading ceramic capacitor manufacturers now offer high temperature surface-mount capacitors (150°C, size 1210) for the automotive market. Capacitance values as high as 47 µF are available. Look for parts with X8L dielectric and high temperature, usually automotive and/or downhole petroleum drilling applications. These capacitors are physically more stable, without the microphonic characteristics exhibited by all other ceramic capacitor dielectrics.

Film capacitors are also suitable for averaging capacitor applications and have shrunk in the past few years; however, many are not suitable for reflow assembly. Users must beware of temperature limitations of the application as well.

OUTPUT CONNECTIONS—CORE

Minimal Output Configuration

The product at the rms core output is in the form of a current at nominally half of the input current and, in turn, converts to a voltage generated across the 16 kΩ resistor, R_{I-V}. The conversion is expressed as follows:

For voltage, the conversion is expressed as

$$V_{OUT(DC)} = e_{RMSIN}$$

For current in amperes, the conversion is expressed as

$$I_{DCOUT} = (I_{RMSIN}/2)\ \text{A}$$

where $I_{RMSIN} = (e_{RMSIN}/8\ \text{k}\Omega)$.

If the output voltage is applied directly to the following stage, the output appears as a voltage source with 16 kΩ series resistance.

Using the R_{V-I} and R_{I-V} Resistors to Scale the AD8436 for Higher or Lower Voltages

The effective range of the AD8436 is a factor of the input and output currents. As an example, consider a nominal input voltage of 300 mV (the specified trim voltage). If the input voltage of interest is 600 mV, one can simply double the resistor values of R_{V-I} and R_{I-V} to double the usable input voltage of the AD8436. The effective range being a factor of the input and output currents is a useful property of the AD8436 in instances where the AD8436 replaces an older rms to dc converter with higher signal levels. It is important to remember that these properties are used to shift the rms to dc voltage amplitudes. The dynamic range is unaffected.

INPUT AND OUTPUT OP AMPS

Referring to Figure 2, the on-chip AD8436 input and output op amps are designed to interface to the rms core. IBUF is a unity gain FET input op amp with a pin-selectable option for 2× gain. The output op amp is a precision bipolar dc amplifier with a 16 kΩ current matching resistor in series with its noninverting input. By adding a few resistors, users can configure either or both op amps over a wide range of gain settings.

FET Input Buffer—Internal Gain Options

The high input impedance input buffer features a metal-oxide semiconductor field effect transistor (MOSFET) input architecture, with a pair of closely matched 10 kΩ resistors for 6 dB of pin-selectable gain. The user has a choice of unity or 6 dB gain settings by simple pin selection, or externally adjustable gain up to 40 dB using a single external resistor.

The unity gain option is shown in Figure 8, whereas Figure 9 shows the pin connections for 6 dB gain. Note the external, 10 MΩ, user supplied resistor required to bias the gate voltage, from the IBUFIN+ pin to the IGND pin.

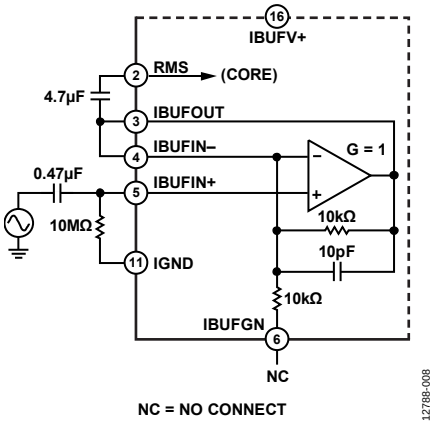


Figure 8. AC-Coupled High Impedance Input Buffer Configured for Unity Gain for LFCSP

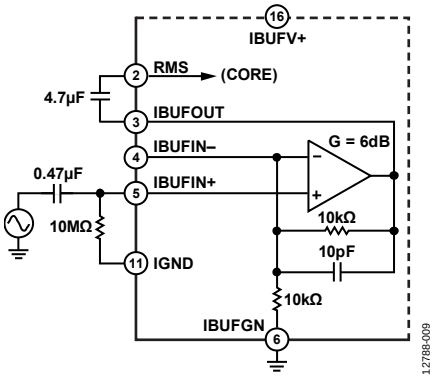


Figure 9. AC-Coupled High Impedance Input Amplifier Configured for G = 6 dB for LFCSP

Embedded across the internal, 10 kΩ feedback resistor is a small capacitor for noise reduction and stability. Figure 10 and Figure 11 show the large signal and small signal bandwidth, respectively, using the 0 dB and 6 dB on-board gain options.

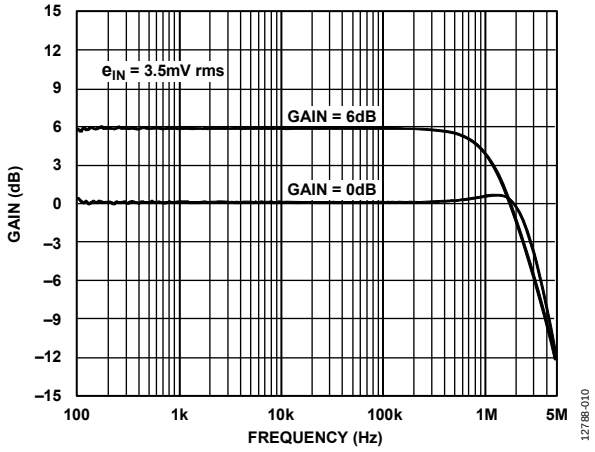


Figure 10. AD8436 FET Input Buffer Small Signal Bandwidth for Both Internal Gain Options

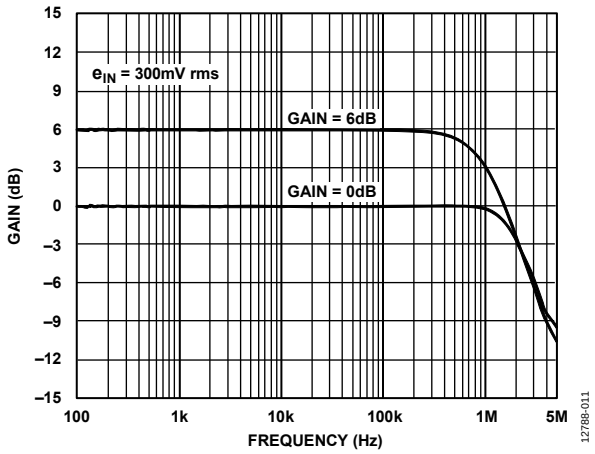
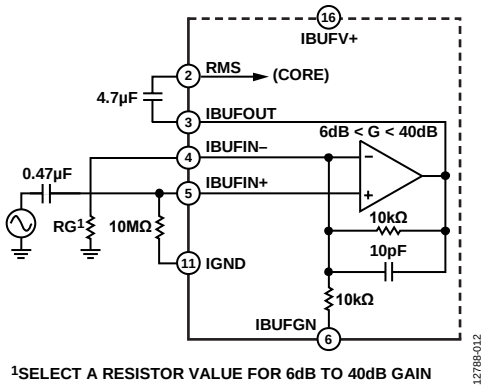


Figure 11. AD8436 FET Input Buffer Large Signal Bandwidth for Gain = 0 dB and 6 dB

Configuring IBUF for Input Gain Greater than 6 dB

The AD8436 can provide gain across a wide range of input voltages and frequencies. A gain value of 10× or 100× extends the usable range of measureable ac voltages down to the tens of microvolts. Larger gain values require a single external resistor connected from the IBUFIN− pin to ground. As with any op amp, the gain conforms to the classic gain bandwidth (GBW) 20 dB/decade relationship. The internal feedback resistor is 10 kΩ, laser trimmed to 1% precision. For gains greater than 6 dB, calculate a new value for the gain resistor, RG (see Figure 12), using a transposition of the noninverting gain equation, G = RFB/RG + 1.

$$RG = \frac{10^4}{G-1}$$



[1]SELECT A RESISTOR VALUE FOR 6dB TO 40dB GAIN

Figure 12. FET Input Buffer Configured for External Gain Adjustment for LFCSP

The bandwidth of the IBUF is more than sufficient for audio and power applications. Table 2 shows five gain values and their corresponding values of RG. Figure 13 shows the resulting corresponding GBW plots.

Table 2. Setting the Gain of the Input Buffer

Gain (dB)	Gain (×)	RG (Calculated)	RG, Nearest 1%	Measured 3 dB Bandwidth (see Figure 13)
0	1	∞	Leave open	2.82 MHz
6	2	10 kΩ	10 kΩ	1.29 MHz
10	3.16	4.1625 kΩ	4.64 kΩ	639 kHz
20	10	1.101 kΩ	1.1 kΩ	160 kHz
40	100	101 Ω	101 Ω	15 kHz

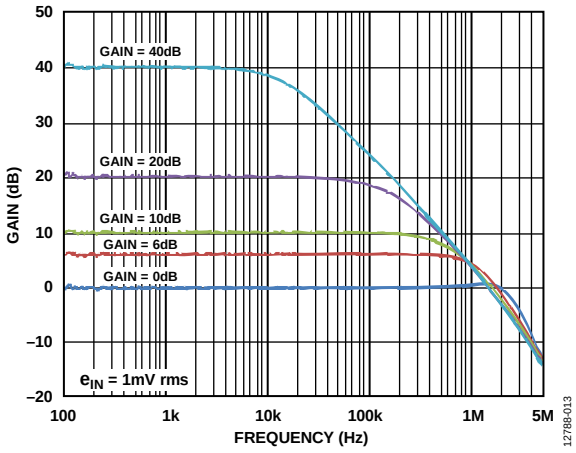


Figure 13. Gain and Bandwidth Options for the FET Input Buffer for Five Values of Gain

The salient feature of a FET input amplifier is the low impact of loading on virtually any real life signal source. Many source circuits utilize resistive dividers to scale high voltages such as utility line or power supply to usable values for measurement purposes. Digital multimeters (DMMs) and other range switching instruments are good examples of such applications. A complete description of all the possible variations in design of DMM front ends is beyond the scope of this document; however, Figure 14 shows a schematic of a front end of such an instrument to illustrate the essential characteristics. A high voltage capacitor (keep safety in mind when selecting a component) protects against unexpected dc voltages. Diode pairs and a small series resistor clamp overvoltages to the supplies, protecting the low voltage rms to dc converter input. Finally, a large resistor network with one or more taps serves to reduce input voltages to within the useable range of the AD8436. Finally, note that the 1 kΩ resistor in the array serves to refer the input to the IGND pin.

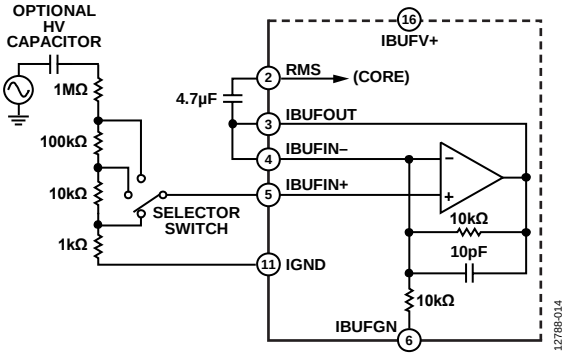


Figure 14. Range Switching for the LFCSP AD8436 FET Input Buffer

Operation of the AD8436 with Very Low Input Voltages

The AD8436 converts input voltages less than 1 mV, but such low voltages result in longer power-up settling. This behavior is caused by the lower input current level available to charge the CAVG capacitor to its operating bias voltage. The power-up time for a 1 mV rms input signal is typically 30 sec and increases with lower input voltages.

In core only applications where power-on delay is an issue, the effect is mitigated by scaling R_{V-I} and R_{I-V} for more current. One approach is to configure the input buffer for gain, thus increasing the core input current for the same applied input voltage. Connecting external resistors to the SUM and OUT pins with appropriately scaled values (less than 8 kΩ and 16 kΩ, respectively) restores the overall gain to unity. Figure 15 shows a suitable configuration with the input buffer configured for 6 dB gain and matching values for the input and output resistors, RIN and ROUT, to optimize temperature stability.

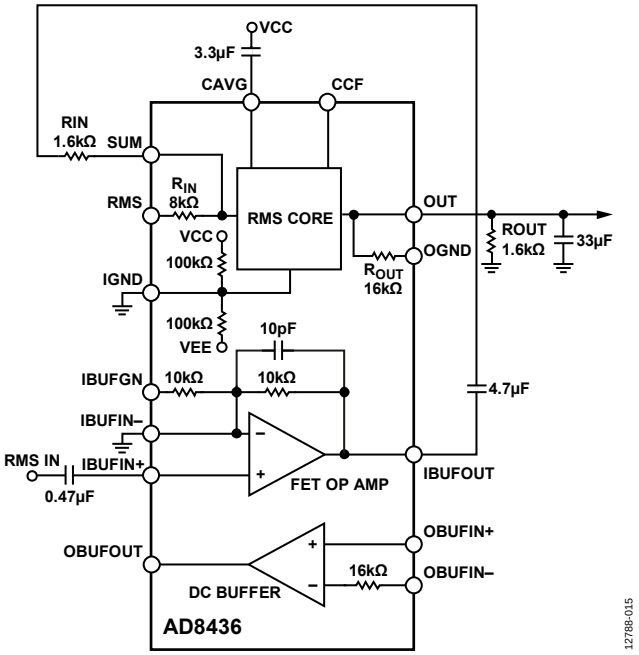


Figure 15. AD8436 Optimized for Low Voltage Input to Enhance the Turn On

It is further recommended to use the minimum necessary value of averaging capacitor to meet the rms error requirement. Then, filter any residual ripple by increasing the value of the CLPF capacitor.

Combining a 5× increase in core input current with the built in 2× gain of the input buffer yields a total of 10× gain overall, reducing the turn on settling time for a 1 mV input from approximately 30 sec to <3 sec. Before using this method, note that this method reduces the maximum usable input voltage, resulting in a tradeoff when implementing this method.

USING THE PRECISION DC OUTPUT BUFFER

Configuring the AD8436 Output Op Amp as a Unity Gain Buffer

As shown in Figure 16, the AD8436 output buffer is a precision bipolar op amp with very low dc offset voltage error. A 16 kΩ resistor from the op amp output to the inverting input nulls any offset voltage created by the bias current from the noninverting input through R_{I-V}, minimizing any offset voltage error.

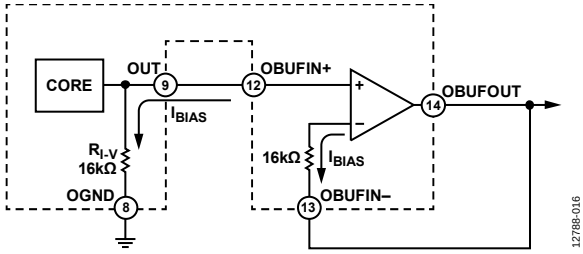


Figure 16. Precision DC Output Buffer Showing Cancellation of the Common-Mode Bias Current Component of V_{OS}

Configuring the AD8436 Precision Output Op Amp for Gain

For applications requiring additional post conversion drive voltage, increase the gain of the output buffer by inserting a totem pole network at the inverting input, as shown in Figure 17. This configuration is useful when the input signal must first be downscaled to avoid overdrive of the core or when an application requires higher dc output. Ensure that the total load resistance is greater than 500 Ω and the resistance of the totem pole gain network is between 10 kΩ and 25 kΩ. Add additional resistance at the noninverting input to compensate for the change in bias current induced V_{OS} resulting from the parallel combined resistance of the output network.

Table 3 shows resistor values and gain results for 3× and 10× gain.

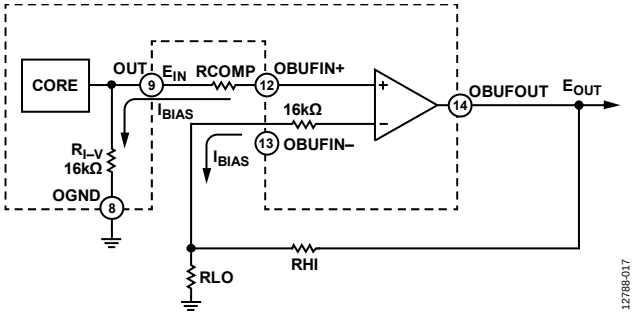


Figure 17. LFCSP AD8436 Precision DC Op Amp Buffer Configured for Greater than Unity Gain

Table 3. External Resistor Values for 3× and 10× Gain

RHI (kΩ)	RLO (kΩ)	RCOMP (kΩ)	Gain, (RHI/RLO) + 1	E_{IN} (V)	E_{OUT} (Calculated)	E_{OUT} (Measured)	Gain (Measured)	Error (%)
6.65	3.32	2.21	3.003×	3.3	9.91	9.91	3.003	0.1
9.09	1	909	10.09×	0.3	3.03	3.03	10.09	0.17

SINGLE SUPPLY OPERATION

The AD8436 is eminently usable with single-supply applications such as handheld DMMs and other small portable instruments. Input signals in these applications are typically referred to 0 V (that is, electrical ground). A matched pair of 100 kΩ resistors connected internally between VCC and VEE provides the midsupply dc reference for the AD8436 circuitry and is user accessible at the IGND pin. The inputs of the RMS and SUM pins are both referred to IGND; however, an external resistor (10 MΩ is recommended) is required between the IBUF+ pin and the IGND pin to bias the FET op amp. A 10 µF decoupling capacitor between the IGND pin and VEE (ground) is recommended.

Minimal Input Connection

Figure 18 shows the basic ac input connection. The CIN capacitor is necessary to isolate the ground referred ac input from the midsupply IGND referred to the RMS pin.

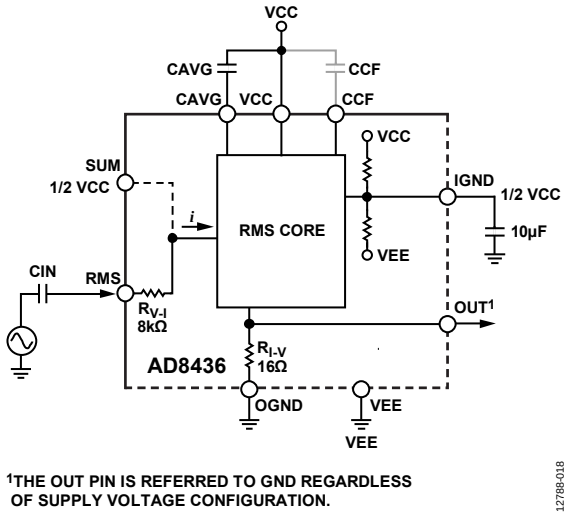


Figure 18. Basic Input Connections with Single Supply

DC Matching Devices with Dissimilar Common-Mode Voltages

Matching the AD8436 devices with dissimilar dc common-mode input devices, such as analog-to-digital converters (ADCs) or pulse-width modulators (PWMs), is not uncommon and requires a means to shift the common-mode voltage of the output of the AD8436 (see the block diagram in Figure 19).

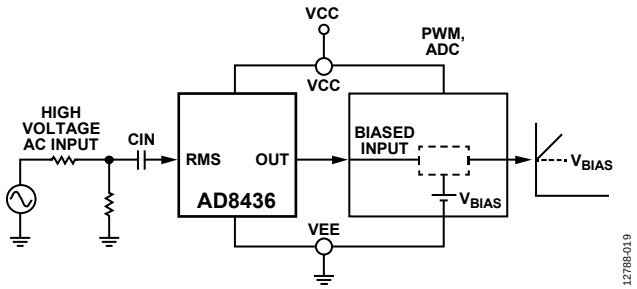


Figure 19. Block Diagram of the AD8436 Driving an External Device Requiring a Fixed DC Input Bias

The most straightforward solution is to offset the AD8436 dc output voltage with an offset enabled amplifier such as a differential or instrumentation amplifier. Figure 20 shows a circuit diagram with an AD8237 instrumentation amplifier configured as buffer and level shifter between the AD8436 and the following device in the signal path. The AD8237 is a low current, single-supply, rail-to-rail in-amp ideally suited for this application. Apply the required offset voltage directly to the reference input and the AD8436 output to the noninverting input of the AD8237. Then, connect the inverting input to ground. A single device accomplishes buffering and level shifting and the input protection to the AD8436 is unaffected.

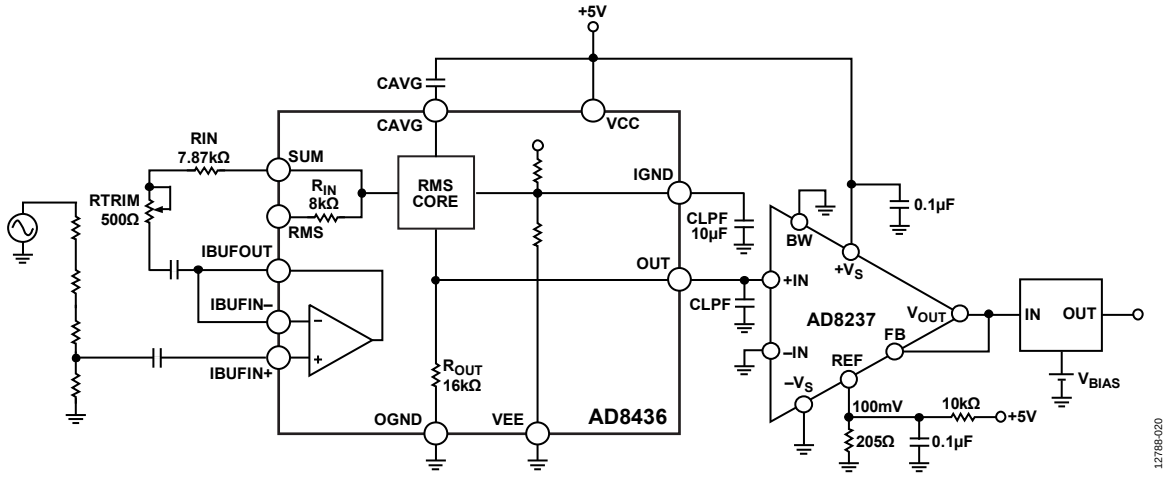


Figure 20. Schematic of AD8436 Configured for Single Supply and a Biased Output Load

AC CURRENT, GROUND FAULT, AND 3-PHASE APPLICATIONS

MEASURING HAZARDOUS CIRCUITS

Configuring a Current Transformer

Monolithic rms to dc converters such as the AD8436 are well suited for current measurements using low cost toroidal current transformers. Toroidal current transformers have existed for a long time in a wide variety of current ranges from milliamperes up to hundreds of amperes.

Shaped like a donut, the transformer primary is one or more turns through the center of a ferromagnetic core wrapped with several hundred turns. The one or more passes of wire in series with the load through the center hole of the toroid is the primary, and the several hundred turns around the core are the secondary. Figure 21 is a schematic of the toroidal current transformer essentials.

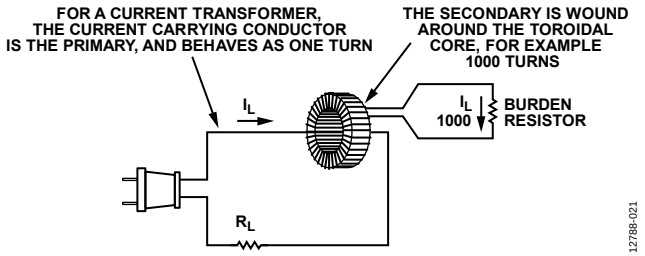


Figure 21. Toroidal Current Transformer Schematic

The AD8436 is the ideal interface for a current transformer because the transformer secondary current must all flow through the burden resistor for maximum accuracy, and the FET input buffer introduces no shunt current path error. Figure 23 shows the circuit of a bench setup for experimenting with current transformers and how best to use them.

The current transformer for the following experiment detects current values down to the milliampere level, has a small center hole (~7 mm), and is accurate to about 80% when used with a 1 kΩ burden resistor. The FET input buffer of the AD8436 introduces no current transformer loading errors and compensates the transformer error with a single 2.4 kΩ external feedback resistor for about 2 dB of gain.

A common 60 W incandescent lamp serves as a useful current load for bench experiments. A Tektronix current probe with scope or power supply monitors current levels, and voltages are measured with Agilent or Fluke secondary standard DMMs. The load current for a 60 W bulb is nominally 0.5 A rms, and the test bulb measured 0.499 A rms.

Detecting Ground Fault Current

The emergence of international stringent safety standards for ac connected equipment is well known. In the USA, UL is a voluntary association that tests electrical safety across a broad range of industries and grants approvals which manufacturers apply to their wares to ensure the buyer that the equipment they are buying has been independently tested for safety.

The IEC is an international organization that establishes safety standards for the European community and is recognized as the gold standard for a host of safety and regulatory limitations.

One of these limits is leakage current, which is the ac line current from any power supplies that can pass through the user when the user is exposed to conductive components of the equipment. Such current leakage is known as ground fault current (or residual current in the European community) and can be lethal. Figure 22 is a schematic of a ground fault current path. Note that ground fault currents are too small to trip the primary protection device, yet large enough to be lethal to human beings. Exterior house wiring in the USA must be equipped with special circuit breakers known as ground fault circuit interrupters (GFCI).

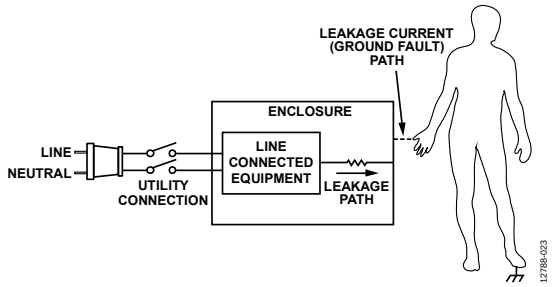


Figure 22. Human Hazard Caused by a Ground Fault Current Path

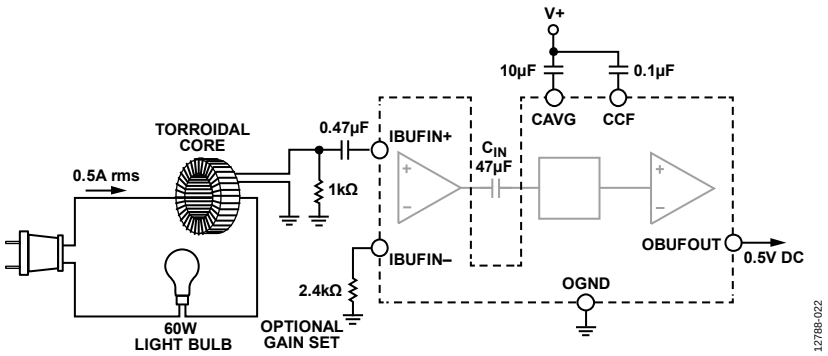


Figure 23. Block Diagram of AD8436 Current Transformer Configuration

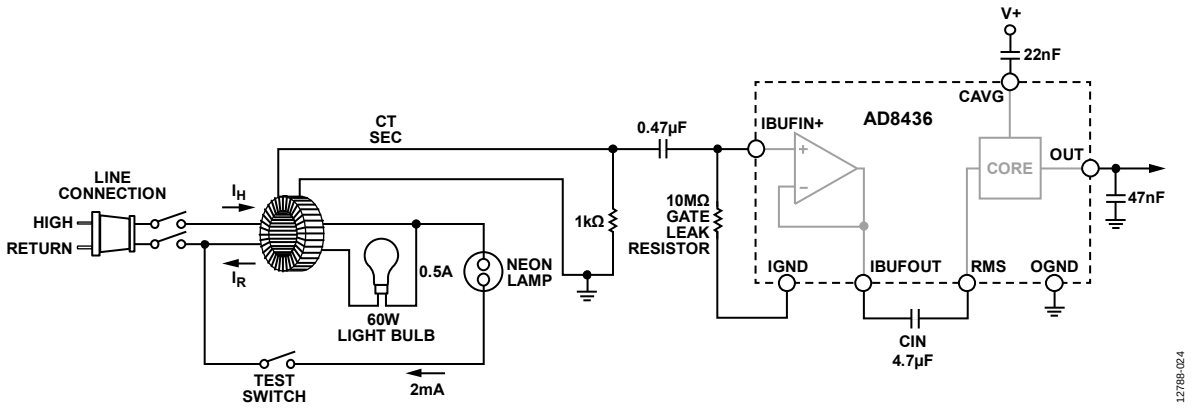


Figure 24. Ground Fault (Residual Current) Test Circuit with the AD8436 Configured as a Precision Full Wave Rectifier (Absolute Value Circuit)

The AD8436 is particularly useful if it becomes necessary to measure or detect these small current values. A common technique is to use a current transformer configured for differential current detection using the source and return currents through the line cord conductors. Under normal circumstances, the current to and from a load are equal and any imbalance in the two are assumed to be caused by current leakage. When a current transformer device is wired for differential, a current appears when none are expected, tripping an alarm. Figure 24 shows a bench experiment testing using the AD8436 to detect ground fault currents.

A small difference current is generated by a neon lamp connected around the toroid to imbalance the load currents through the core center. The neon lamp behaves as a Zener clamp, with no current flowing at low voltages and firing after about 90 V, after which time a very small 2 mA rms current of flows. The small magnitude of the current makes it somewhat difficult to detect.

Figure 25 is a scope shot of the waveforms of interest. Trace 1 is the line voltage across the neon lamp, Trace 2 is the current through the lamp, approximately 2 mA rms, and Trace 3 is the resulting current transformer secondary voltage.

Note that the waveform is a string of transient responses that capture the current transitions when the neon lamps conduct and extinguish, and that the amplitudes are very small, about 2 mV, peak-to-peak, and symmetrical around 0 V. This waveform only describes this particular experiment. The occurrence of hazardous ground fault currents are typically unpredictable because they are caused by component failure or other random events. One solution to this issue is to rectify the pulses and use a comparator with a fixed reference level to detect amplitudes. To demonstrate this solution, the AD8436 is configured as a low level absolute value circuit with superior detector characteristics to create a monopolar pulse train of about 1 mV peak, as seen in Trace 4 in Figure 25.

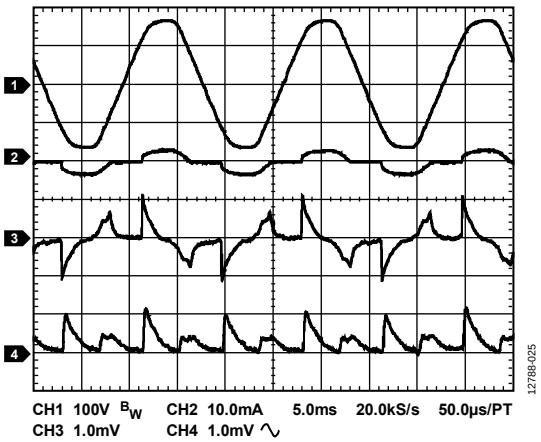


Figure 25. Simulated GFI Experiment Test Circuit Waveforms (see Figure 24); Trace 1: Neon Lamp Voltage; Trace 2: Neon Lamp Current; Trace 3: Current Transformer Load Resistor Waveform; Trace 4: Output of AD8436 Applied to Comparator Input

LOW COST, 3-PHASE POWER LINE MONITOR—OPTIMIZING SETTLING TIME

An internal, high gain driver within the translinear feedback loop design of the AD8436 helps stabilize the settling time across its input dynamic range. The advantage is that the same rms accuracy is achieved with smaller averaging capacitor values than in the prior circuits, but with slightly more ripple. The ripple is easily remedied with an external 2f low-pass filter with shorter time constants. The result is converter applications requiring less overall settling times to accomplish the same conversion accuracies.

Figure 26 (with thanks to the Analog Devices field application staff) shows the phase relationship of a typical European 3-phase power distribution waveform. High voltage rms measurements of utility systems require a high voltage divider with a high input impedance buffer to mitigate loading errors. Depending on the number of phases in the system, one or more rms to dc converters and low-pass filters are selected by a mux and their outputs are converted to digital by sampling with a single ADC (see an example of a multichannel measurement system at the top of Figure 27). The mux and ADC continuously sample all phases well within the period of a single 20 ms power line voltage period.

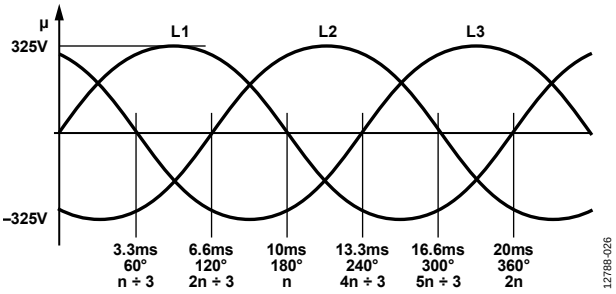


Figure 26. European 50 Hz/3-Phase Utility

However, a single rms to dc converter and low-pass filter are feasible if less frequent data samples over an extended time period are acceptable. Because utility frequencies are 50 Hz to 60 Hz (internationally), and several full cycles are required to produce an rms value, relatively long sampling periods of 1 sec become practical. Thus, a single rms to dc converter and low-pass filter can convert all three phases sequentially by sampling every 0.33 sec, as shown in the bottom of Figure 27.

In this scenario, the 3-to-1 mux is placed ahead of the signal path, followed by the AD8436. Each phase is selected by the mux, whose common output is connected to the IBUFIN+ pin of the AD8436. The FET buffer mitigates divider loading and drives the rms to dc converters. Op amps with moderate bandwidths (~15 MHz) function as two-pole, Sallen–Key low-pass filters with a 3 dB frequency low enough to effectively filter any residual 100 Hz output ripple. Note the dramatic reduction in complexity (and cost) when 3-phase data is collected with a single rms to dc converter. Further savings are possible if the FET input buffers can be configured as Sallen-Key filters; however, the bandwidth may not be sufficient in certain instances.

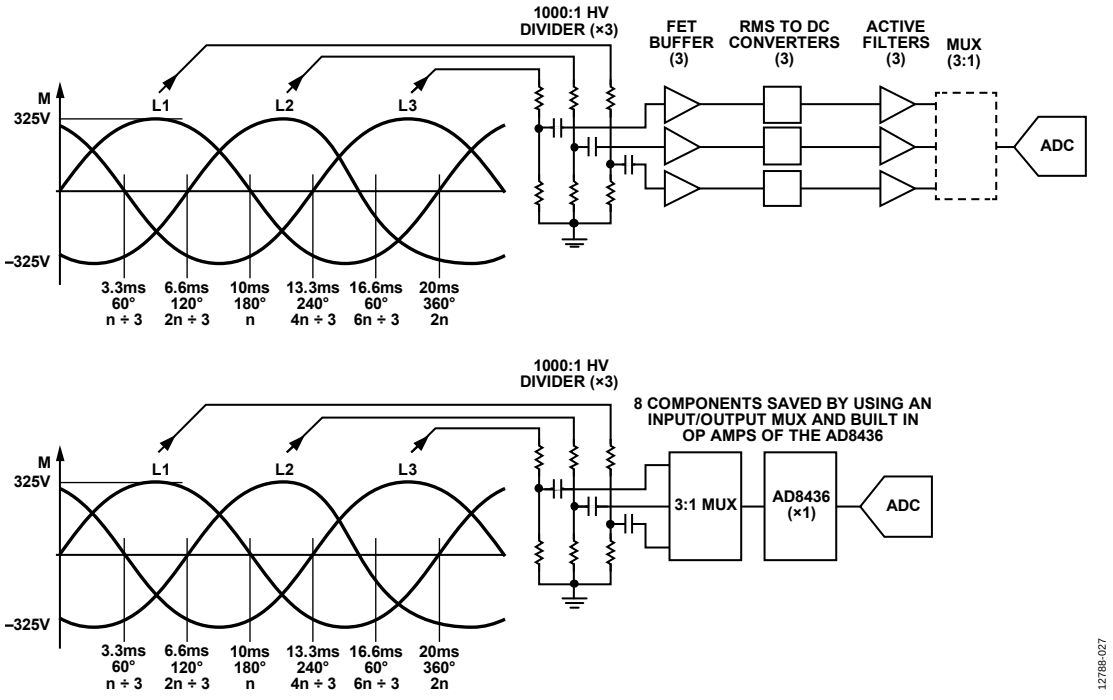


Figure 27. Comparison of Two Methods of Measuring 3-Phase Utility RMS Voltages Using the AD8436

Performance

Figure 28 is a record of test results of the AD8436 configured as shown in the diagram of Figure 29, and using a burst signal to emulate switched samples at the output of a multiplexer (for example, the ADG1604). A 4.8 V dc supply powers the AD8436 and the input and outputs observed on a scope. The AD8436 output buffer is configured as a two-pole, 10 Hz, Sallen-Key low-pass filter, using 2 µF and 1.5 µF capacitors, and an external 8.01 kΩ resistor as shown in Figure 29 (the 16 kΩ input resistor is internal to the device).

The test waveform period is 1 sec (although this can be substantially reduced), with a 16-cycle burst of 50 Hz cycles (20 ms × 16 = 320 ms), of a 252 mV rms sine wave input.

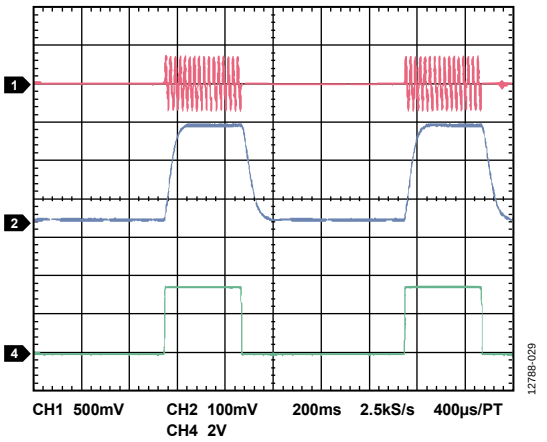


Figure 28. Timing Measurements of the AD8436 Configured for 3-Phase Conversion; Trace 1: Input Burst—16 Cycles, 20 ms per Cycle, 1 sec Period; Trace 2: Output; Trace 3: Timing Reference—Burst Gate (Sync Output of Function Generator)

Direct Connected Power Line Measurements

Line voltages can be measured with a suitable differential amplifier configured with a step-down resistor network such as the AD628. Although efficient in device count and cost, circuitry that is directly connected in any way to power line sources is hazardous to humans and can be used only in galvanically isolated applications. See Technical Article MS-2405, *Simple Circuit Measures the RMS Value of an AC Power Line*, for a complete description of the line voltage measurements.

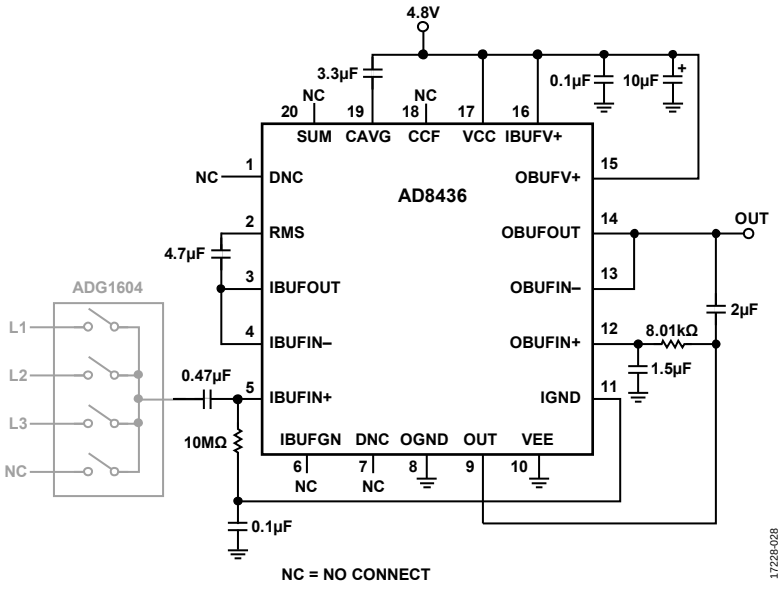


Figure 29. LFCSP AD8436 of High Impedance Input and Precision Output Buffers Configured to Accommodate High Impedance Sources and a Two-Pole, Sallen-Key Low-Pass Output Filter

ERROR SOURCES

The AD8436 is laser trimmed to data sheet specifications; however, careful selection of capacitor styles and scrutiny in PCB layout and assembly are worthwhile, especially for accurate, low level rms to dc conversion levels.

CAVG Pin

Referring to Figure 30, parasitic impedance at the CAVG pin and the capacitor style can both introduce small errors. Any external current diverted from the output path by way of board contamination or capacitor leakage lowers the converted output voltage, introducing a correspondingly negative error. Specify PCB handling procedures applicable for complementary metal-oxide semiconductor (CMOS) devices.

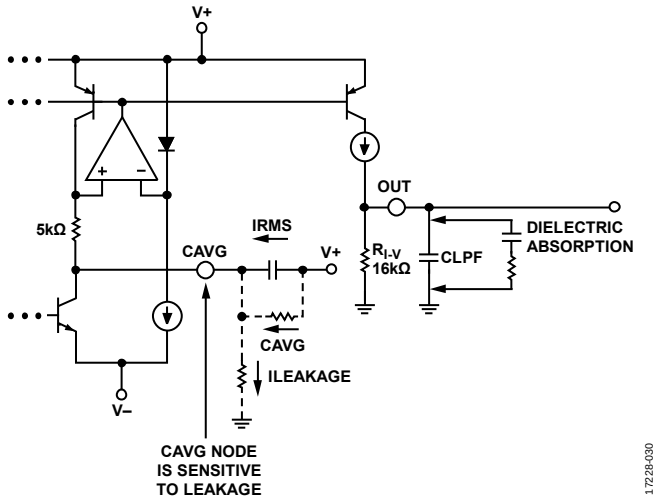


Figure 30. Capacitor and Leakage Errors

CLPF Pin

Referring to Figure 30, the output of the AD8436 is a current source driving the 16 kΩ resistor, R_{I-V}. Capacitors used for low-pass filter applications must have good dielectric absorption qualities; otherwise, error voltages following power-down or temporarily zero level signals can occur. An equivalent error circuit for dielectric absorption is shown in Figure 30.

Conversion Errors

Referring to Figure 31, the AD8436 output includes a few small amplitude, ac and dc error components in addition to the desired output. The ac error is twice the input frequency ripple voltage following averaging, or filtering, at the output and is managed by the judicious choice of the CAVG and CLPF capacitors at the lowest expected operating frequency. Fixed dc errors are compensated by an external offset adjustment; nonlinearities are compensated by external means, either by scaling or by calibration.

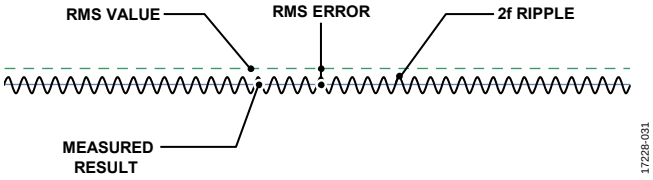


Figure 31. AD8436 Output Components

Referring to Figure 31, the small dc rms error represents the difference between the true rms and the measured dc result. Mathematically, the rms error approaches zero as the averaging capacitor or the frequency values approach infinity. This theoretical convergence is usually ignored as a practical matter, but the log-log representation is useful for sizing averaging capacitors for higher frequency applications. Furthermore, for a higher operating frequency (for example, 100 kHz), some input high-pass filtering in the form of limiting the frequency response using ac coupling may be practical.

In modern ADC or microcontroller applications, the ripple error impact can be quite an issue depending on accuracy and bit resolution. Low supply-voltage converters are quite common, where the references are only 1 V. For a modest 10-bit converter, the LSB weighting is 1 mV, and <500 µV ripple is required for unambivalent sampling.

The dc errors consist of a fixed offset error, which can be calibrated out. The other is caused by nonlinearity of the translinear approach used for the AD8436. Fortunately, it is a very small error over a very large dynamic range; however, if used over an extended range, multiple calibration points may be desired. The core resistor values are trimmed at 300 mV rms input using ±5 V supplies.

PCB PRECAUTIONS

Just a few simple steps can make a big difference in results after selecting the many options offered by the AD8436. Printed circuit and/or other physical properties are worth mentioning here. Any AD8436 board designs need a dedicated ground layer, and benefit from a power layer as well, even if the power layer includes multiple power and signal traces. Empty space in the top and bottom layers filled with copper further improves noise performance. The IBUF of the AD8436 is a FET design, and the LFCSP version of the AD8436 is particularly vulnerable to surface leakage of the board. Fortunately, these effects are well known in the industry and millions of MOSFET applications serve as precedents. For the QSOP model, hand washing using appropriate solvents can suffice; however, machine washing and drying is most effective for the LFCSP model to remove residual salts and flux contamination that may become trapped beneath the package. PCB assembly houses are aware of these issues and are fully equipped to deal with them.

CONCLUSION

The AD8436 offers substantial flexibility, performance, and cost savings advantages over older rms to dc converters and over converters employing various digital schemes. The applications described herein and data reproduced offer solutions to real life situations. Many were based on customer input and feedback.

RELATED LINKS

AD8436 Data Sheet

RMS to DC Converter Application Guide

Rarely Asked Questions (RAQs): Resistors in Analog Circuitry