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APPLICATION NOTE

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Precision Signal Conditioning for High Resolution Industrial Applications

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INTRODUCTION

Industrial measurement and control systems often need to interface to sensors while operating in noisy environments. Because sensors typically generate very small electrical signals, extracting their output from the noise can be challenging. Applying signal conditioning techniques, such as amplification and filtering, can aid in the extraction of the signal because these techniques increase the sensitivity of the system. The signal can then be scaled and shifted to take full advantage of high performance ADCs.

This application note introduces a general-purpose precision signal conditioning front end that can close the gap between sensors and high resolution ADCs. The circuit is analyzed to find its noise contribution, ambient noise rejection, and ability to perform highly sensitive measurements.

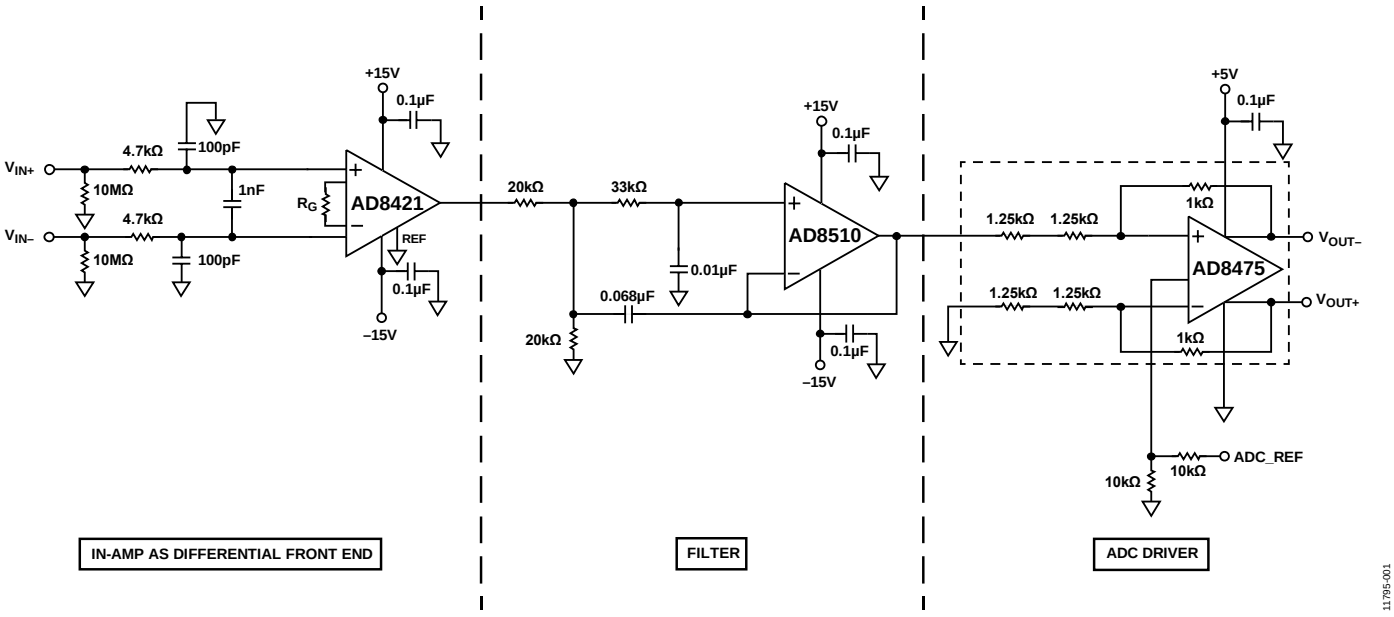

Figure 1. Precision Signal Conditioning Circuit Schematic

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REVISION HISTORY

12/13—Revision 0: Initial Version

PRECISION SIGNAL CONDITIONING CIRCUIT DESCRIPTION

The precision signal conditioning circuit is composed of three main stages: amplification, filtering, and ADC driving. These components provide flexibility with the circuit.

Amplification is done in the first stage using a differential front end. Differential inputs are preferred for their inherent noise rejection characteristics because ambient noise usually appears as a common-mode signal (for example, power line noise and ground loops). This first stage provides a wider input range, adjustable gain, and high common-mode rejection ratio (CMRR) which increases with gain. A filter is used in the second stage; ADC driving is done in the last stage. This final stage accomplishes single-ended to differential conversion, along with shifting and scaling of the output signal to feed into the ADC.

STAGES OF PRECISION SIGNAL CONDITIONING CIRCUIT

A schematic diagram for the precision signal conditioning circuit is shown in Figure 1. The first section of this figure shows amplification accomplished with the AD8421, a low noise instrumentation amplifier which has an input voltage noise density of 3 nV/√Hz. This amplifier enables the system to achieve a common-mode rejection greater than 94 dB when used at unity gain. A single resistor can be used to set different gains. Because of its proprietary pinout and carefully designed architecture, CMRR increases with gain, which is guaranteed to be greater than 140 dB at a gain of 1000. The front-end circuit also includes an RFI filter at its inputs to prevent high frequency noise from corrupting the measurement.

To limit the noise bandwidth and avoid aliasing, filtering is done with the AD8510, a low noise JFET operational amplifier with a voltage noise density of 8 nV/√Hz. The center of Figure 1 shows this device to be configured as a 2-pole Sallen-Key filter with a corner frequency of 460 Hz. This filter passes only the frequencies of interest thus preventing alias frequencies from being sampled by the ADC. The signal from the AD8421 goes into the resistor divider formed by the two 20 kΩ resistors, so that it scales to the inputs of the ADC, which uses a 2.5 V reference. With this divider and the amplifier configured in unity gain, the filter stage is configured in a total gain of 0.5.

The AD8475 is a differential ADC driver configured in a gain of 0.4, as shown in the rightmost portion of Figure 1. It performs single-ended to differential conversion, and features a VOCM pin which allows the user to shift the output signal to an optimal level for the ADC. For this circuit, the output common-mode level is half of the reference voltage used for the ADC. This ensures that the signal going into the ADC has maximum dynamic range. Taking into consideration the gain from the previous stage, the resulting gain of the signal conditioning circuit is 0.2. With this attenuation factor, a usable input range of ±10 V is obtained when the ADC uses a reference of 2.5 V.

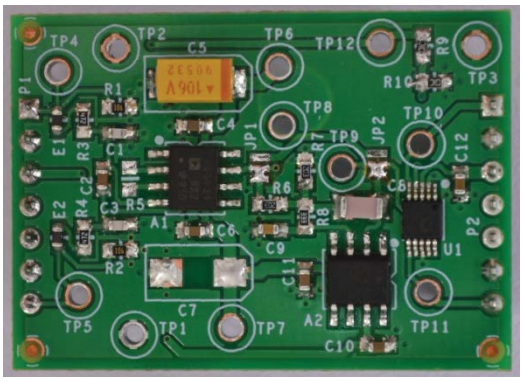

Figure 2. Precision Signal Conditioning Circuit Board

AMPLIFIER NOISE CONSIDERATIONS

In practice, estimating the expected noise contribution of any conditioning circuit allows the user to calculate the effective resolution of the system. Note that the signal conditioning circuit, by nature of its active devices, also contributes some form of noise to the circuit.

As an example, Figure 3 shows a graph of the voltage noise density (referred to input) of the AD8421.

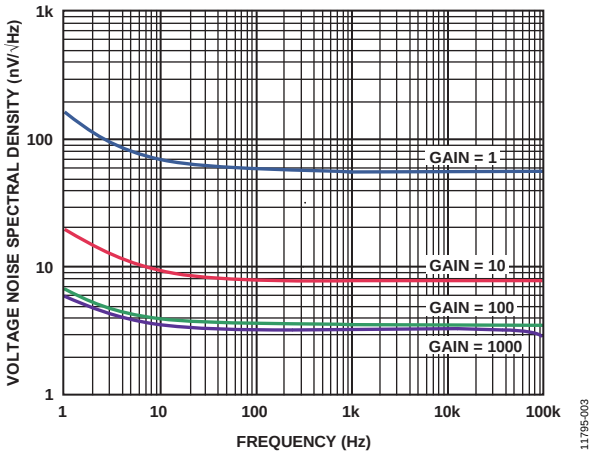

Figure 3. Voltage Noise Density of AD8421

Amplifier noise is generally composed of 1/f noise and wideband noise. The 1/f noise is characterized by a rise in spectral density as the frequency decreases. This noise typically affects low frequencies. An amplifier with a low corner frequency has very low noise at near-dc applications. In contrast, the wideband noise has a constant spectral density over the remaining band of frequencies. When calculating the total noise contribution in the application, the bandwidth of operation should be taken into account. For the AD8421, the corner frequency is at 10 Hz.

From Figure 3, it can also be observed that the noise is affected by the gain used. Instrumentation amplifiers have components of noise at both input and output. When gain is increased, the output noise component scales down by a factor of the gain, resulting in lower overall noise referred to input.

The noise of each component with respect to the other is uncorrelated. Thus, the resultant noise of the circuit is achieved by taking the square root of the sum of their squares, commonly called the RSS (see the MS-2066 Technical Article, *Low Noise Signal Conditioning for Sensor-Based Circuits*, for more information).

Because the dc performance of the circuit is being evaluated, the noise contribution from the amplifiers is dominated by the 1/f noise. The ADC also eliminates the wideband noise, thus it is not taken into account in the calculations. Based on the 0.1 Hz to 10 Hz noise specifications, the noise added referred to output (RTO) for each amplifier is given in Table 1. The AD8421 is assumed to be in a gain state of 1 for all analyses in this section.

Table 1. Total Expected Noise of Precision Signal Conditioning Circuit for an ADC Driver

Part	Typical Noise (μV p-p)	Gain[1]	Noise RTO (μV p-p)
AD8421	2	0.2	0.4
AD8510	2.4	0.4	0.96
AD8475	2.5	1	2.5

[1]Gain is referred from the output of the amplifiers to the input of the ADC.

The total RSS noise expected from the precision signal conditioning circuit is then solved.

$$Noise_{PSC} = \sqrt{0.4^2 + 0.96^2 + 2.5^2}$$

$$Noise_{PSC} = 2.7 \ \mu V \ p-p$$

Interfacing the signal conditioning circuit to a low noise analog-to-digital converter allows one to measure this noise. The AD7195 is a 24-bit sigma-delta ADC, which has an internal PGA. From characterization of the ADC at a reference of 2.5 V, one can observe that the noise contribution of the ADC at an output data rate (ODR) of 10 Hz and an input range of ±19.5 mV is 63 nV p-p (internal PGA gain set to 128). Because this value is two orders of magnitude lower than the calculated front-end noise of 2.7 μV p-p, its contribution is negligible.

This premise can be used to verify the noise from the precision signal conditioning circuit on the actual setup.

Figure 4 shows the signal conditioning circuit interfaced to the AD7195 on a monolithic evaluation board. To measure the system noise, the inputs are shorted and connected to ground. Because noise is random, the peak-to-peak and rms values are measured, the latter being the equivalent of the standard deviation for a Gaussian distribution. These measurements can be collected using the evaluation board software.

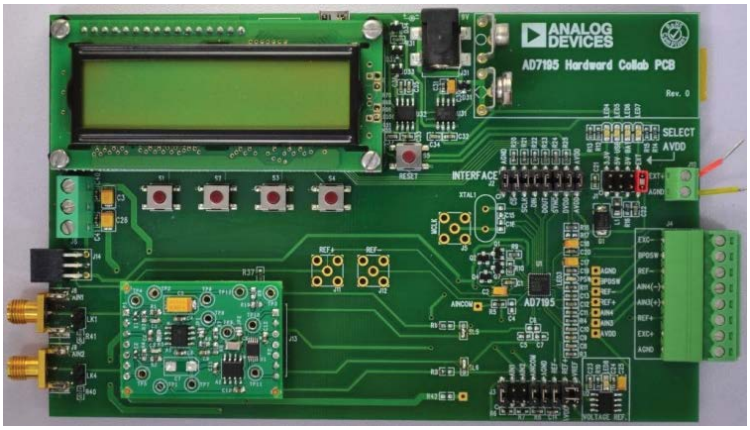

Figure 4. Noise Evaluation Setup

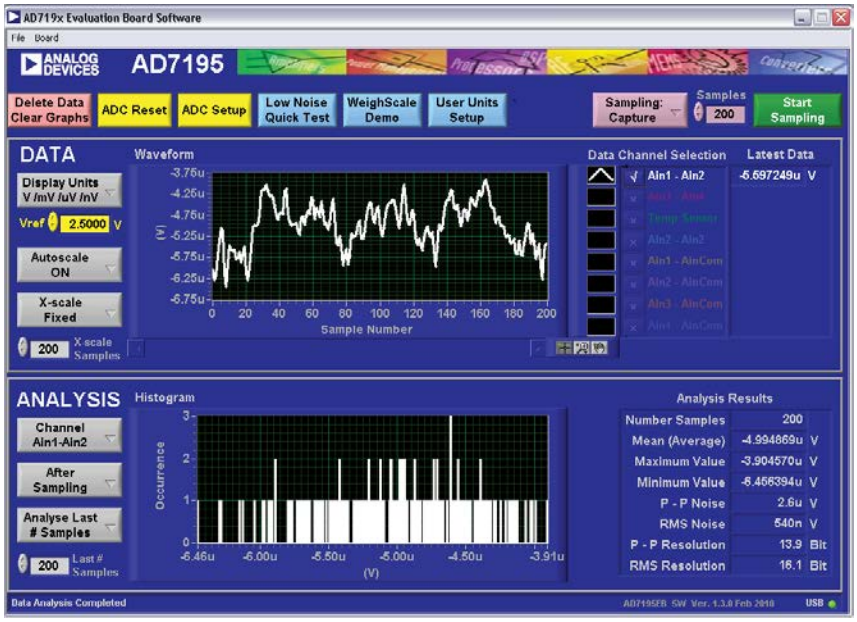

Figure 5. Noise Results at 10 Hz ODR, Internal PGA Gain Set to 128

The noise measurements are shown in Figure 5 where the ADC is set to an internal PGA gain of 128 and an ODR of 10 Hz. Observe that the noise measurement of 2.6 µV p-p is correlated to the calculated value of 2.7 µV p-p. This performance is expected considering that values are estimated using typical specifications.

TOTAL SYSTEM PERFORMANCE

The system sensitivity and effective resolution are determined by the intrinsic noise of the circuit. Noise calculations are applied to predict how the system will behave when the precision signal conditioning circuit is used to drive the AD7195. Since the 0.1 Hz to 10 Hz frequency band is of interest, note that the acquisition time should be 10 seconds for the calculated noise values to be valid.

Systems that can measure very small signals also need to be able to do so in the presence of large interfering signals to be effective. Common-mode rejection is a figure of merit that quantifies this ability, and it is mainly dictated by the front end of the circuit.

Sensitivity

The noise analysis can be applied to determine the sensitivity of the system. When used with an internal PGA gain of 1, the noise of the ADC contributes to the system noise. The expected noise values are shown in Table 2.

Table 2. Expected Noise with Varying Sampling Rate

Output Data Rate (Hz)	Front End (µV p-p)	ADC (µV p-p)	Expected Noise[1] (µV p-p)
10	2.7	1.2	3.0
50	2.7	2.7	3.8
60	2.7	2.7	3.8

[1]Wideband noise between 10 Hz and 50 Hz to 60 Hz is negligible and is not included in computation.

Taking the 10 Hz ODR as an example, noise was measured on the actual setup using the corresponding configurations. The reading of 3.0 µV p-p, as shown in Figure 6, correlates with the calculated value.

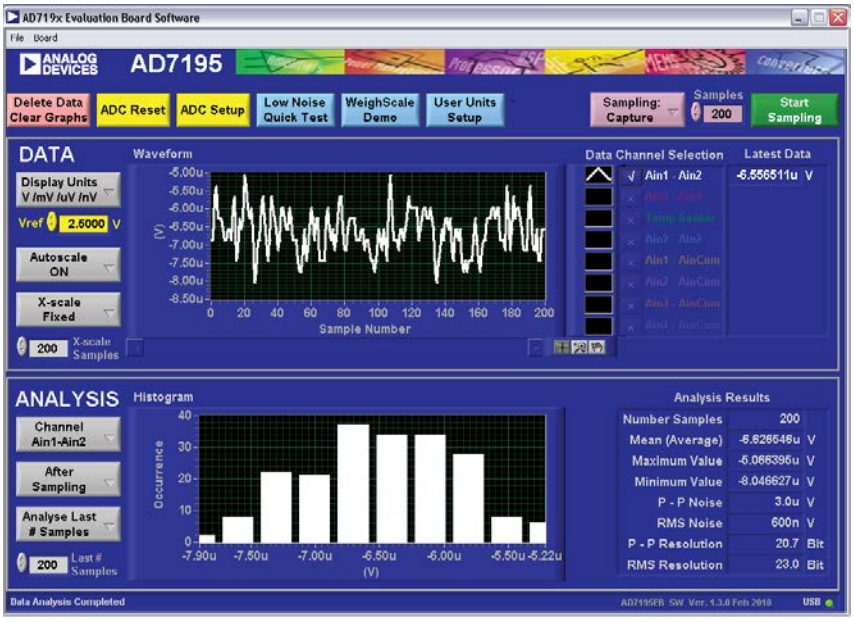

Figure 6. Noise Results at 10 Hz ODR, Internal PGA Gain Set to 1

Following through with the data from the 10 Hz ODR, one could then take the maximum calculated noise and refer it to the inputs of the system to get an idea of its sensitivity, that is, the minimum voltage change that the system will be able to detect. From Table 2,

$$V_{IN-Noise} = \frac{Expected\ Output\ Noise}{Gain}$$

$$V_{IN-Noise} = \frac{3\ \mu V\ p-p}{0.2}$$

$$V_{IN-Noise} = 15\ \mu V\ p-p$$

It can then be predicted that the system will be able to properly resolve a voltage change of 15 µV at its inputs. Because the AD8421 is being used in a gain of 1, this applies to an input range of ±12.5 V.

Using this procedure, it is clear that sensitivity increases with gain. Consider the case where the AD8421 is configured in a gain of 100. At this gain, the input range is ±125 mV, and the total gain of the signal conditioning circuit is 20. The peak-to-peak noise of the AD8421 at a gain of 100 is 70 nV p-p. Including this in the noise calculations for the signal conditioning circuit gives

$$Noise_{PSC} = \sqrt{(0.07 \times 20)^2 + (2.4 \times 0.4)^2 + (2.5 \times 1)^2}$$

$$Noise_{PSC} = 3\ \mu V\ p-p$$

Accounting for the 1.2 µV p-p of noise from the ADC in the calculations, the total expected system noise is 3.2 µV p-p.

The sensitivity of the system can now be calculated.

$$V_{IN-Noise} = \frac{3.2\ \mu V\ p-p}{20}$$

$$V_{IN-Noise} = 160\ nV\ p-p$$

The sensitivity of the system becomes 160 nV p-p at an input range of ±125 mV. This demonstrates how the increased gain of the system also results in an increase in sensitivity.

Noise-Free Resolution

To determine the noise-free resolution that can be achieved with the AD7195, use the following formula:

$$Noise-free\ Resolution = \log_2 \frac{Full-scale\ range}{p-p\ noise}$$

Because bipolar inputs at the ADC are in use, the full-scale range is twice the reference voltage. Substituting this into the previous equation gives

$$Noise-free\ Resolution = \log_2 \left(\frac{2 \times 2.5\ V}{3 \times 10^{-6}}\right)$$

The noise-free resolution, also expressed as effective number of bits (ENOB), is 20.7 bits when the AD8421 is configured in unity gain. When it is configured in a gain of 100, the resolution is almost the same at 20.6 bits.

The same analysis can be done with different sampling rates and gains to achieve an estimate of the system performance. These measurements enable one to assess the capabilities of the circuit with respect to the desired application.

Common-Mode Rejection

The discussions on sensitivity and resolution are indicative of the system performance with respect to the intrinsic noise. A good figure of merit to determine system performance with respect to extrinsic noise is its common-mode rejection.

As the front end of the circuit, the AD8421 dominates the common-mode rejection of the circuit. CMRR is the ratio of the differential gain to the common-mode gain. It can also be expressed mathematically as

$$CMRR\ (dB) = 20logA_{diff}\frac{V_{CM}}{V_{OUT}}$$

where:
A_{diff} is the differential gain.
V_{CM} is the common-mode voltage present at the inputs of the amplifier.
V_{OUT} is the output voltage contribution due to the common-mode voltage.

Assume that an unwanted common-mode voltage induces a 10 V p-p signal at both inputs. The AD8421 has a minimum CMRR of 94 dB at a gain of 1. Given this, one can solve for the contribution of the ambient noise at the input of the AD7195.

$$94\ \text{dB} = 20\log\left[(1)\frac{10\ \text{V p–p}}{V_{OUT}}\right]$$

$$V_{OUT} = 200\ \mu\text{V p–p}$$

One observes an output voltage of 200 µV p-p due to the common-mode noise at the output of the AD8421. The attenuation of the circuit brings this down to 40 µV p-p at the input of the AD7195.

Comparing this to the AD8421 configured in a gain of 100, given the same parameters, the common-mode noise would still be at a 40 µV p-p level at the input of the ADC, but it would have higher sensitivity. This demonstrates how the increased gain and CMRR help increase the sensitivity with respect to extrinsic noise.

After being largely rejected by the front-end CMRR, this common-mode noise, the most familiar source of which is the power line, can be further attenuated by the normal-mode rejection ratio (NMRR) of the AD7195. This is due to its digital filter notches which can be configured to fall on the line frequencies of 50 Hz and 60 Hz. Using its sinc4 filter and an ODR of 10 Hz, the AD7195 guarantees an NMRR greater than 100 dB. The 40 µV p-p common-mode noise contribution would be brought down to less than a nanovolt, thus line noise is effectively rejected by the circuit.

CONCLUSION

The precision signal conditioning circuit allows the user to effectively extract the signal of interest even in noisy environments. Performance parameters, such as sensitivity, effective resolution, and robustness to ambient noise, can be estimated with the consideration of intrinsic noise and common-mode rejection. These merits ultimately determine the system performance and may be used as an aid for the user in the design of industrial applications. The system may be further optimized by using different analog-to-digital converters in the interface.

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NOTES

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