High Temperature, Low Power Operational Amplifier

Known Good Die

AD8634-KGD

FEATURES

Extreme high temperature operation
−40°C to +210°C, tested to +175°C
Rail-to-rail output
Low power: 1.3 mA maximum
Gain bandwidth product: 9.7 MHz typical at A_V = 100
Low offset voltage: 250 μV maximum
Unity-gain stable
High slew rate: 5.0 V/μs typical at 210°C
Low noise: 4.2 nV/√Hz typical at 1 kHz and 210°C

APPLICATIONS

Downhole drilling and instrumentation
Avionics
Heavy industrial
High temperature environments

METAL MASK DIE IMAGE

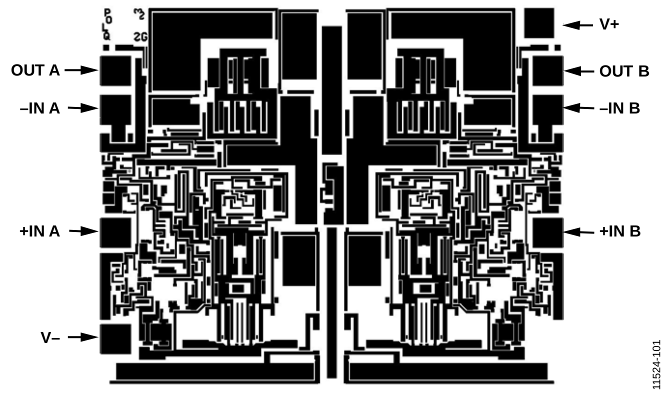

Figure 1.

GENERAL DESCRIPTION

The AD8634-KGD is a precision, 9.7 MHz bandwidth, dual amplifier that features rail-to-rail outputs. The AD8634-KGD is guaranteed to operate from 3 V to 30 V (or from ±1.5 V to ±15 V) and at very high temperatures. The AD8634-KGD is specified and characterized for −40°C to +210°C and is tested at +175°C.

The AD8634-KGD is well suited for applications that require both ac and dc precision performance. The combination of wide bandwidth, low noise, and precision makes the AD8634-KGD useful in a wide variety of applications, including filters and interfacing with a variety of sensors.

Additional application and technical information can be found in the AD8634 data sheet.

The AD8634-KGD is a member of a growing series of high temperature qualified products offered by Analog Devices, Inc. For a complete selection table of available high temperature products, see the high temperature product list and qualification data available at www.analog.com/hightemp.

Rev. 0 **Document Feedback**

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support **www.analog.com**

TABLE OF CONTENTS

REVISION HISTORY

7/14—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS, V_{SY} = ±15.0 V

V_{SY} = ±15.0 V, V_{CM} = 0 V, $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/ Comments	−40°C ≤ T_A ≤ +210°C			Unit
			Min	Typ	Max	
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}				250	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			0.35		µV/°C
Offset Voltage Matching		$T_A = T_{MAX}$			150	µV
Input Bias Current	I_B		−200	−40	+200	nA
Input Offset Current	I_{OS}				30	nA
Input Voltage Range	V_{IN}		−14.5		+14.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −14.0 V to +14.0 V	100	115		dB
Large Signal Voltage Gain	A_{VO}	−13.5 V ≤ V_{OUT} ≤ +13.5 V, R_L = 2 kΩ	100	108		dB
Input Impedance						
Differential				53‖1.1		kΩ‖pF
Common-Mode				1.1‖2.5		GΩ‖pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{CM}	14.8	14.90		V
		R_L = 2 kΩ to V_{CM}	14.0	14.5		V
		R_L = 2 kΩ to V_{CM}, $T_A = T_{MAX}$	14.60	14.75		V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{CM}		−14.95	−14.8	V
		R_L = 2 kΩ to V_{CM}		−14.75	−14.65	V
		R_L = 2 kΩ to V_{CM}, $T_A = T_{MAX}$			−14.65	V
Short-Circuit Current	I_{SC}	V_{OUT} = 0 V, $T_A = T_{MAX}$		+105/−18		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = ±2 V to ±18 V	103	113		dB
Supply Current per Amplifier	I_{SY}	I_{OUT} = 0 mA, $T_A = T_{MAX}$		1.1	1.3	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	3.6	5.0		V/µs
Gain Bandwidth Product	GBP	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 100		9.7		MHz
Unity-Gain Crossover	UGC	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 1		7.0		MHz
−3 dB Closed-Loop Bandwidth	−3dB	V_{IN} = 5 mV p-p, A_V = 1		11.0		MHz
Phase Margin	ΦM			82		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.13		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		4.2		nV/√Hz
Current Noise Density	i_n			0.6		pA/√Hz

ELECTRICAL CHARACTERISTICS, V_{SY} = 5.0 V

V_{SY} = 5.0 V, V_{CM} = 2.5 V, V_{OUT} = 2.5 V, $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/ Comments	−40°C ≤ T_A ≤ +210°C Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}				250	μV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			0.35		μV/°C
Offset Voltage Matching		$T_A = T_{MAX}$			150	μV
Input Bias Current	I_B		−200	−40	+200	nA
Input Offset Current	I_{OS}				30	nA
Input Voltage Range	V_{IN}		0.5		4.7	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0.3 V to 4.7 V	55	60		dB
Large Signal Voltage Gain	A_{VO}	0.5 V ≤ V_{OUT} ≤ 4.7 V, R_L = 2 kΩ	100	108		dB
Input Impedance						
Differential				53‖1.1		kΩ‖pF
Common-Mode				2.8‖2.5		GΩ‖pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{CM}	4.8	4.90		V
		R_L = 2 kΩ to V_{CM}	4.0	4.5		V
		R_L = 2 kΩ to V_{CM}, $T_A = T_{MAX}$	4.60	4.75		V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{CM}		50	200	mV
		R_L = 2 kΩ to V_{CM}		250	350	mV
		R_L = 2 kΩ to V_{CM}, $T_A = T_{MAX}$			350	mV
Short-Circuit Current	I_{SC}	V_{OUT} = 0 V, $T_A = T_{MAX}$		+70/−11		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = ±1.25 V to ±2.75 V	95	100		dB
Supply Current per Amplifier	I_{SY}	I_{OUT} = 0 mA, $T_A = T_{MAX}$		1.0	1.2	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	3.5	5.0		V/μs
Gain Bandwidth Product	GBP	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 100		9.7		MHz
Unity-Gain Crossover	UGC	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 1		7.0		MHz
−3 dB Closed-Loop Bandwidth	−3dB	V_{IN} = 5 mV p-p, A_V = 1		11.0		MHz
Phase Margin	ΦM			82		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.13		μV p-p
Voltage Noise Density	e_n	f = 1 kHz		4.2		nV/√Hz
Current Noise Density	i_n			0.6		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	±18 V
Input Voltage	$V- \leq V_{IN} \leq V+$
Differential Input Voltage[1]	±0.6 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +210°C
Junction Temperature	245°C

[1] For differential input voltages greater than 0.6 V, limit the input current to less than 5 mA to prevent degradation or destruction of the input devices.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PAD CONFIGURATION AND FUNCTION DESCRIPTIONS

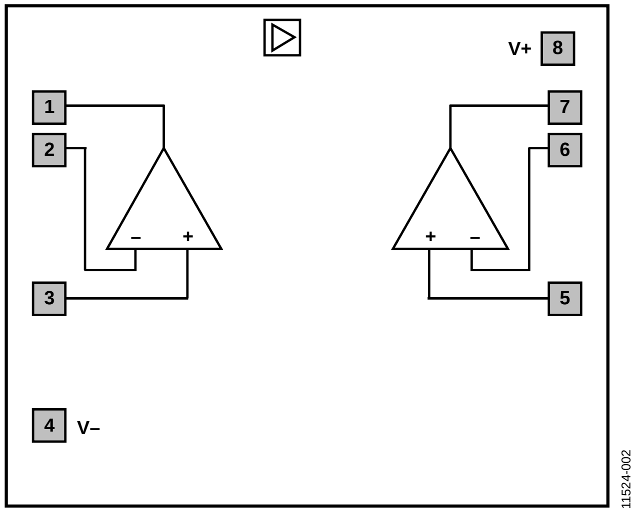

Figure 2. Pad Configuration and Functional Block Diagram

Table 4. Pad Function Descriptions[1]

Pad No.	X-Axis (µm)	Y-Axis (µm)	Mnemonic	Description
1	−566	330	OUT A	Output Pad of Amplifier A.
2	−566	227	−IN A	Inverting Input Pad of Amplifier A.
3	−566	−97	+IN A	Non-Inverting Input Pad of Amplifier A.
4	−566	−377	V− Pad	Negative Power Supply Pad. Substrate is connected to V−.
5	566	−98	+IN B	Non-Inverting Input Pad of Amplifier B.
6	566	227	−IN B	Inverting Input Pad of Amplifier B.
7	566	330	OUT B	Output Pad of Amplifier B.
8	544	456	V+	Positive Power Supply Pad.

[1] Die center is the reference location at 0.0 µm × 0.0 µm. Pad coordinates are to the center of each pad.

OUTLINE DIMENSIONS

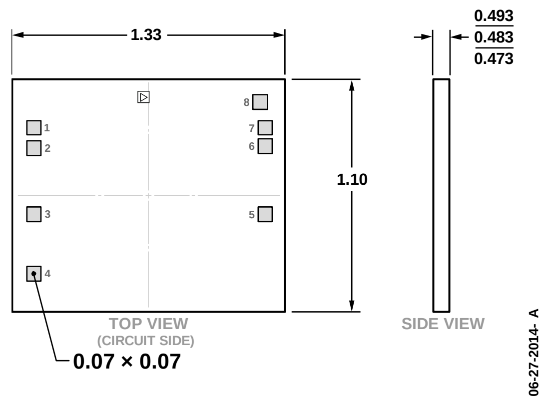

Figure 3. 8-Pad Bare Die [CHIP]
(C-8-3)
Dimensions shown in millimeters

DIE SPECIFICATIONS AND ASSEMBLY RECOMMENDATIONS

Table 5. Die Specifications

Parameter	Value	Unit[1]
Chip Size	1240 × 1020	µm
Scribe Line Width	90 × 90	µm
Die Size	1330 × 1100	µm
Thickness	483	µm
Bond Pad	70 × 70	µm
Bond Pad Composition	1.0 AlSi, 0.5AlCu	%
Backside	V- biased	N/A
Passivation	Oxynitride	N/A

[1] N/A means not applicable.

Table 6. Assembly Recommendations

Assembly Component	Recommendation
Die Attach	Epoxy Adhesive
Bonding Method	Gold Ball or Aluminum Wedge
Bonding Sequence	Bond Pin 1 First

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8634-KGD-CHIP	−40°C to +210°C	8-Pad Bare Die [CHIP]	C-8-3