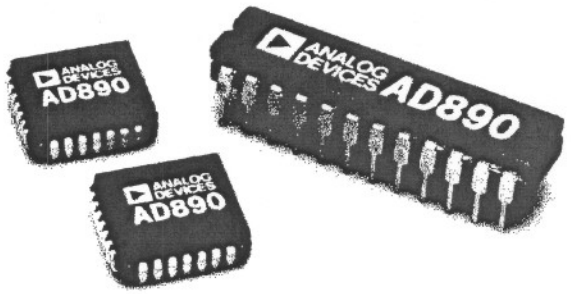
Precision, Wideband Channel Processing Element

FEATURES

- An 80MHz Bandwidth Permitting a 50Mb/s Data Transfer Rate
- A Variable Gain Amplifier with 30dB max Gain and 40dB Control Range
- Two Gain of 4 RF Buffers
- 200Ω Differential Load Drive Capability
- A Pair of Precision Rectifiers
- AGC Level and Threshold Outputs
- An Averaging, High Gain Sample-and-Hold for Accurate AGC Operation
- Typical Gain Drift in Hold Mode: 0.2dB/ms
- Gains Trimmed and Temperature Compensated
- AGC Operation Independent of AGC Level
- Symmetrical AGC Attack/Decay Times
- 1µs AGC Attack/Decay Times Using a 1000pF External Capacitor
- Suitable for Use as an Accurate Video Programmable Gain Amplifier
- Dynamic Clamp Ensures Fast Recovery After Write to Read Transients
- AGC RF Output Level is Internally Preset



PRODUCT DESCRIPTION

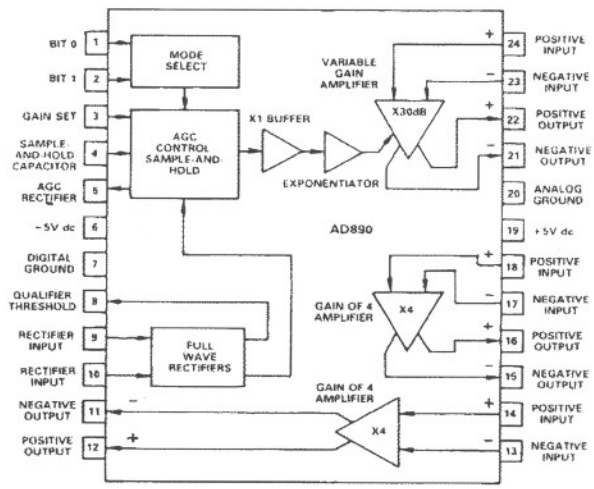
The AD890 is primarily intended for high-performance disk subsystem use and as such it is configured around the classic read channel processing block diagram. It is intended to be connected between the head preamplifier and the qualification circuitry required for digital data recovery. When used with the AD891 rigid disk data qualifier, data transfer rates in excess of 50Mb/s can be processed.

A temperature-compensated AGC loop, with an exponential transfer characteristic, permits optimal settling and allows for predictable performance in the classic single integrator control loop configuration. Fast acquisition and low droop while in the hold mode allow for AGC operation to be performed within the sector header without compromising channel behavior when reading data.

The AD890 processing element has the flexibility to perform both continuous and sampled AGC functions; it is also ideal for embedded, dedicated, or mixed servo applications. Two user-defined filter/equalizer stages may be employed, thus allowing maximum design flexibility. This greatly simplifies the design of the overall channel characteristics. Using the AD890, the designer no longer needs to resort to passive techniques to isolate network functions; this avoids problems of signal loss and interaction. Two low-offset, 100MHz full-wave rectifiers provide the capability to track a 1V peak signal. The rectifier generating the "Qualifier Threshold" output may be used for creating a data qualification level. A second rectifier is used to drive the sample-and-hold circuitry.

The 80MHz bandwidth of the AD890 ensures good phase linearity up to 50MHz. Thus, data transfer rates in excess of 50Mb/s can be supported with good error rates and predictable channel behavior.

The AD890 is available in both a 24-pin, slim-line cerdip package and in a 28-pin PLCC package and is specified to operate over the 0 to 70°C commercial temperature range.



Functional Block Diagram

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West Coast 714/641-9391 Central 214/231-5094 Atlantic 215/643-7790

SPECIFICATIONS (@ +25°C and ±5V dc, unless otherwise noted)

Model	Conditions	AD890J Min	AD890J Typ	AD890J Max	Units
VARIABLE GAIN AMPLIFIER					
Maximum Gain[1]		**29.4**	30.0	**30.6**	dB
±3dB Bandwidth	Up to 26dB Gain Reduction	100			MHz
Input Voltage Noise	0dB Gain Reduction, f = 1kHz		5		nV/√Hz
Input Signal Range	Recommended p-p Differential	10		200	mV
Input Resistance			12		kΩ
Output Impedance			5		Ω
Harmonic Distortion	0dB Gain Reduction		0.15		%
	26dB Gain Reduction		1.5		%
Output dc Level			3.5		V
INPUT CLAMP[2]					
Turn-On Time			30		ns
Turn-Off Time			200		ns
Input Signal Attenuation			35		dB
On-State Input Impedance	Differential		14		Ω
GAIN OF 4 BUFFER					
Nominal Gain		**12.50**	12.75	**13.00**	dB
Gain Variation	T_{min} to T_{max}		±0.25		dB
±3dB Bandwidth		160			MHz
Input Voltage Noise[3]	f = 1kHz		7		nV/√Hz
Input Resistance		100			kΩ
Input Common Mode Range		−1.5		+1.5	V
Output Resistance			10		Ω
Harmonic Distortion	300mV Peak Output, 200Ω Load		0.20		%
Output Signal Level	Recommended p-p Differential		1.3		V
Output dc Level			2.5		V
FULL WAVE RECTIFIER					
Input Signal Level	p-p Differential	0.3		3	V
−3dB Bandwidth	100mV @ 1V Peak Input	100			MHz
dc Offset[4]			10	±20	mV
AGC CONTROL SECTION					
Attack Time	26dB Gain Step – 1000pF C_{SAMPLE}		1.0		µs
	26dB Gain Step – < 50pF C_{SAMPLE}		120		ns
Hold Time	1dB Gain Change – 1000pF C_{SAMPLE}		10		ms
AGC Control Range		**36**	40		dB
AGC Control Sensitivity	Per 20mV Input		1		dB
AGC Control Linearity	26dB AGC Range			±0.5	dB
Set Level Input Range	For Specified Accuracy	**0**		**800**	mV
	Nondestructive Input Range	−0.3		V_{CC}	V
MODE CONTROL SECTION					
TTL Compatible					
V_{IH}		2.0			V
V_{IL}				0.8	V
I_{IH}				100	nA
I_{IL}				2.0	µA
Mode Switching Times				50	ns
POWER SUPPLY REQUIREMENTS					
Rated Performance			±5.0		V
Operating Range		±4.6		±6.5	V
Quiescent Current	T_{min} to T_{max}				
V_{CC}		44	60	76	mA
V_{EE}		18	28	40	mA

NOTES

[1]Gain calibrated in gain set mode with 0 volts applied to the Gain Set Pin.

[2]Clamp operation is specified with a source impedance of 200Ω in series with 0.1µF.

[3]Over the full 100MHz bandwidth of the AD890, the worst-case rms signal-to-noise ratio is 40dB or better with a 40dB AGC range.

[4]Measured using a 4kΩ resistor connected between the Qualifier Threshold Pin and V_{EE}.

Specifications subject to change without notice.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . ±7.5V
RF Gain Stage Differential Input Voltage . . . . . ±5.6V
Storage Temperature Range
AD890JP, AD890JQ . . . . . −65°C to +150°C
Operating Temperature Range[1]
AD890JP, AD890JQ . . . . . 0 to +70°C
Lead Temperature Range (Soldering 60sec) . . . . . +300°C

NOTE
[1]28-pin PLCC package: θ_{JA} = 100°C/W;
24-pin cerdip package: θ_{JA} = 55°C/W.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

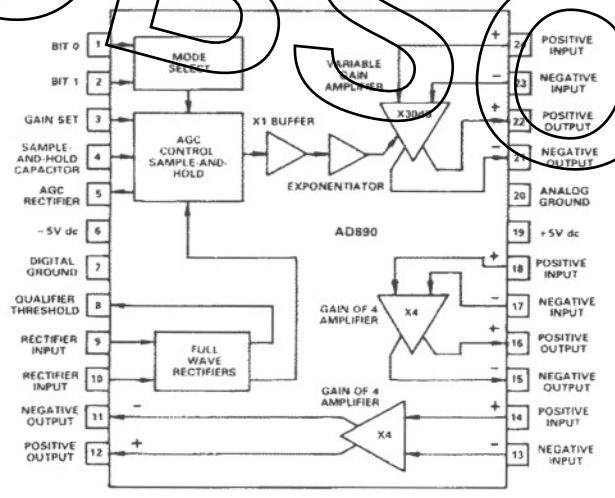
Logic Assignments	Bit 0	Bit 1
AGC Acquire	0	0
AGC Hold	0	1
Gain Set	1	0
Input Clamp	1	1

ORDERING GUIDE

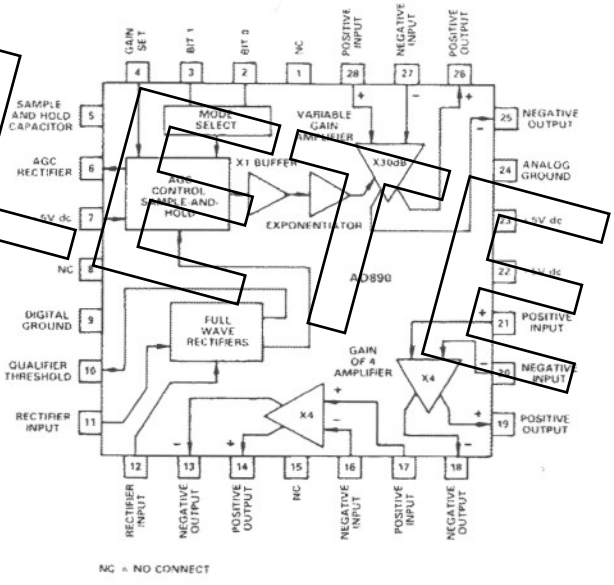
Model	Package	Package Options	Price (10K)
AD890JQ	24-Pin Cerdip	Q-24	$10.00
AD890JP	28-Pin PLCC	P-28A	$ 7.50

CONNECTION DIAGRAMS

24-Pin Cerdip Package



28-Pin PLCC Package

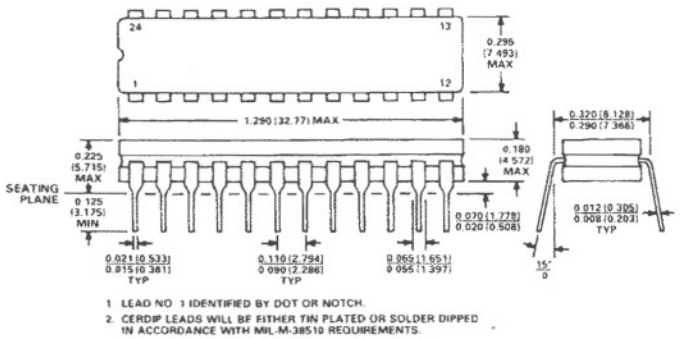


NC = NO CONNECT

OUTLINE DIMENSIONS

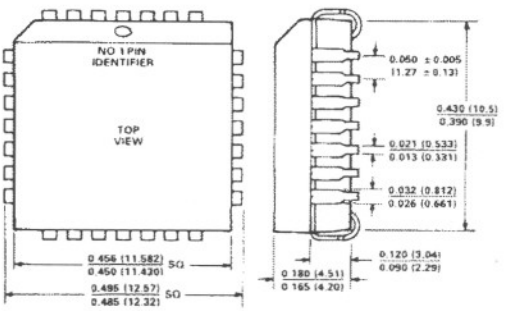
Dimensions shown in inches and (mm).

24-Pin Cerdip Package



1. LEAD NO 1 IDENTIFIED BY DOT OR NOTCH.
2. CERDIP LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

28-Pin PLCC Package



Typical Characteristics @ +25°C with ±5V Supplies

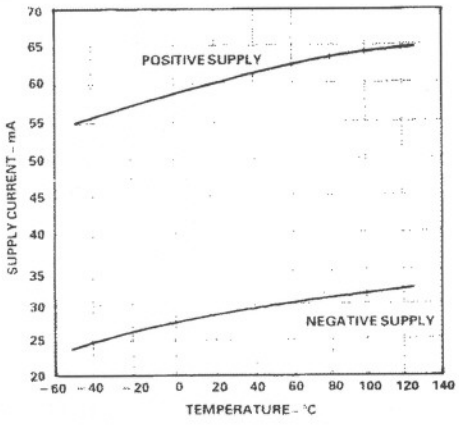


Figure 1. Supply Current vs. Temperature

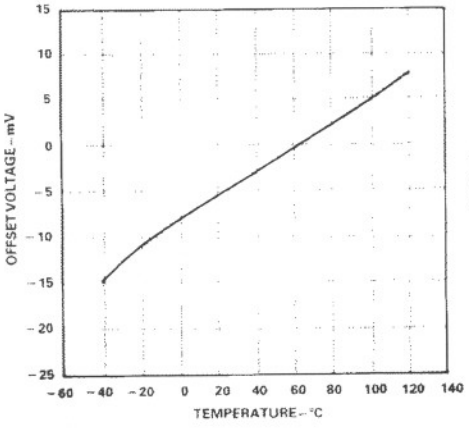


Figure 2. Rectifier Offset vs. Temperature

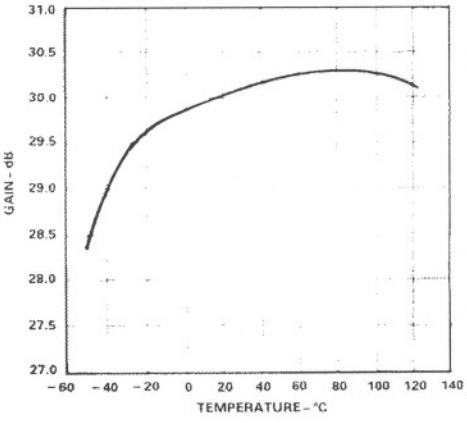


Figure 3. VGA Gain vs. Temperature

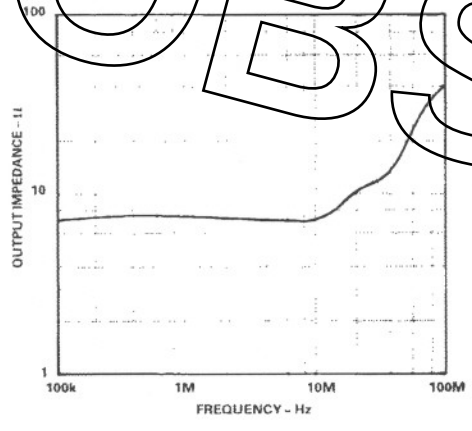


Figure 4. VGA Output Impedance vs. Frequency

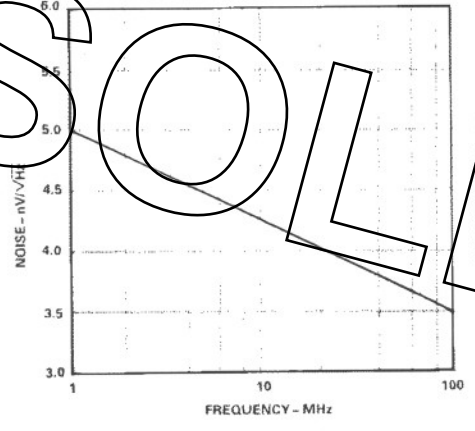


Figure 5. VGA Voltage Noise vs. Frequency

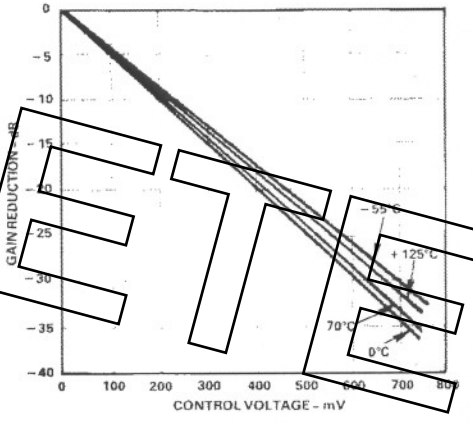


Figure 6. VGA Gain Reduction vs. Control Voltage

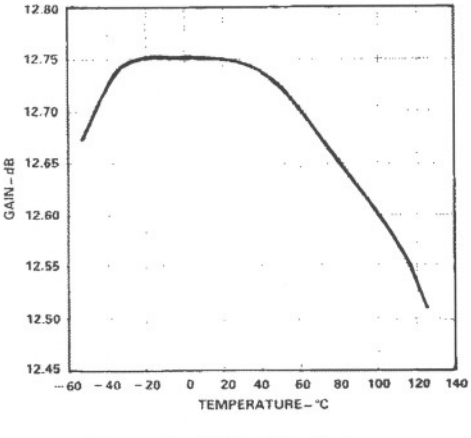


Figure 7. X4 Buffer Gain vs. Temperature

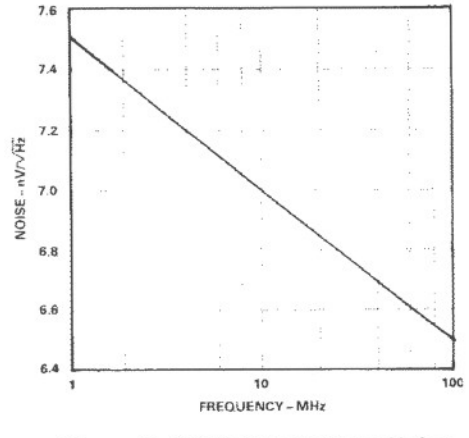


Figure 8. X4 Buffer Voltage Noise vs. Frequency

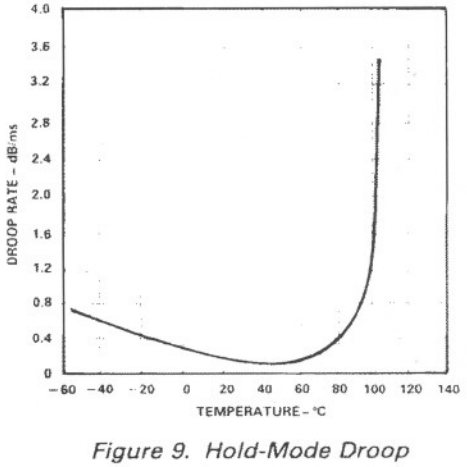


Figure 9. Hold-Mode Droop Rate vs. Temperature

GENERAL LAYOUT REQUIREMENTS

Almost 60dB of total gain is available at 100MHz. Care must be taken to ensure good RF practice in the PC layout to avoid oscillations in the 150MHz-350MHz region. A parallel combination of 0.1μF and 0.01μF ceramic bypass capacitors should be used as close to the supply pins as possible.

Additionally, a single pole RC filter applied at the input of each stage, with a cut off in the region of 100MHz-150MHz, will help avoid oscillation problems. As a general rule, keep the connections to interstage components as short as possible; it is also recommended that any low pass filtering function which may be required by the system be performed between the VGA stage and the first X4 buffer amplifier. A ground plane should be used to surround any interstage components wherever possible. If these simple rules are followed, stable operation should be assured.

BIASING THE RF GAIN STAGES

The VGA Stage

The 30dB variable gain stage is biased at a potential of one diode drop above analog ground. No additional dc bias is required, but ac coupling is necessary. The bias voltage is maintained during normal operation and during operation of the clamp. In order for the clamp to operate correctly with an emitter follower driven input, 50Ω-100Ω resistors should be placed in series with the input coupling capacitors. These resistors can be used in conjunction with a 5.1pF shunt capacitor to limit the input bandwidth to 150MHz. In the case of an open collector driven input with resistive termination, no additional series resistors are required.

The differential outputs have a nominal dc value of 1.5V less than the positive supply. Internal 1300Ω resistors provide bias current to the output emitter followers which operate with 2.7mA nominal current. Output drive can be increased by an additional 2.5mA by paralleling external resistors to either the analog ground or the negative power supply. However, caution should be exercised in order to avoid causing excess dissipation for the package. The recommended output level for the VGA is 300mV p-p differential into 200Ω loads.

The X4 Buffers

The inputs of these stages have no committed dc biasing, and an input bias current path must be provided. This path can normally be supplied via shunt resistors to analog ground which are generally part of the interstage filter termination networks. The inputs can be biased successfully within ±1.5V of analog ground.

Output drive can be increased in a similar manner to that described for the VGA stage. The nominal dc output level is 2.5V with the internal 500Ω load resistors connected to analog ground which provides a nominal standing current of 5mA to the output emitter followers. This current can be increased by up to an additional 5mA by paralleling external resistors to either analog ground or the negative power supply. As before, precautions to limit excessive overall power dissipation apply when steps are taken to increase the output drive capability.

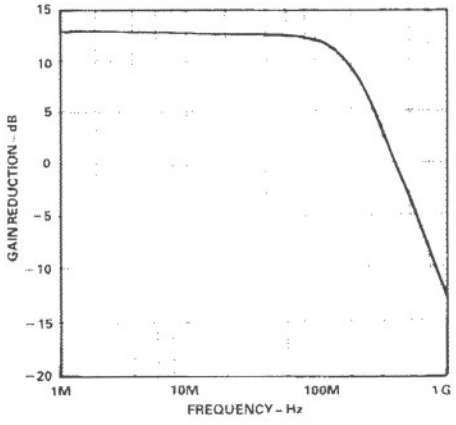


Figure 10. X4 Buffer Frequency Response (100Ω in Series with 1μF Load)

OPERATING THE FULL WAVE RECTIFIERS

The full wave rectifiers consist of two nearly identical stages. Full wave rectification is performed in each stage using two transistors whose emitters are connected together. The inputs to the two full wave rectifiers are biased at one diode drop above analog ground; therefore, ac coupling is recommended. The full wave rectifier outputs – "AGC Rectifier" and "Qualifier Threshold" – are connected directly to these commoned emitters. Thus, the normal output voltage with zero input signal applied is close to analog ground. The "AGC Rectifier" pin allows access to the output of the rectifier which drives the AGC sample-and-hold section of the AD890. The "Qualifier Threshold" pin allows access to the output of the threshold rectifier.

The AGC rectifier has an internal 2kΩ resistive pull-down connected between analog ground and the negative power supply pin. The threshold line has no built in pull-down, in order to allow for a peak hold capability during thresholding. If a well controlled rectifier offset is required, an external 4kΩ pull-down resistor at the "Qualifier Threshold" pin is recommended and will produce a nominal 10mV offset.

THE AGC SAMPLE-AND-HOLD

The AGC sample-and-hold section performs averaging of the input waveform to set the RF average output level to 200mV single ended, or 330mV peak for a sinusoidal signal. Thus, without a peak hold capacitor at the "AGC Rectifier" pin, accurate AGC operation only occurs with sinusoidal input signals. An approximate 2mA pull-down current is permanently present at the "AGC Rectifier" pin, and a capacitor may be added here to provide a degree of peak hold for AGC operation within non-sinusoidal fields. A capacitance value of less than 0.03μF or less per μs of transition spacing is recommended. The addition of the capacitor alters the symmetry of the attack and decay rates of the rectifier, which is otherwise symmetric in operation. In order to ensure that the overall AGC response is the same for both high-to-low and low-to-high input level steps, it is necessary to make the rectifier attack and decay times at least a factor of two less than the AGC response time.

The AGC acquire time is approximately 1μs per 1000pF of hold capacitor. A low leakage variety of hold capacitor, such as a silver mica, is necessary to ensure low droop rates. The "Gain Set" pin should be tied to analog ground if not used, in order to prevent excessive leakage which would otherwise affect the hold performance.

The AGC control potential is present at the "Sample-and-Hold Capacitor" pin. If control over open-loop gain is desired, based on AGC control potentials obtained during trial AGC operations, a FET input op amp should be used to buffer this node in order to avoid disturbing the hold operation.

USING THE AD890 AS A PROGRAMMABLE GAIN AMPLIFIER

The AD890 is ideally suited for use as an accurate video programmable gain amplifier. If the X4 buffers are utilized with the variable gain amplifier, nearly 60dB of total gain is available at frequencies up to 100MHz. The VGA gain and exponentiator scale factors are trimmed with respect to dc control potentials applied to the "Gain Set" pin. In this mode of operation (see Logic Assignments for bit pattern to be applied to the "Bit 0" and "Bit 1" pins), a 0V dc potential applied to the "Gain Set" pin will produce a nominal VGA gain of 30dB. With an additional 12.75dB from each X4 buffer, total nominal gain is 55dB. Each 20mV increment of voltage applied will produce a 1dB reduction in gain. A simple equation can be used to calculate the nominal gain of VGA in this mode:

$$\text{VGA Gain (dB)} = (30 - V_{GAIN\ SET} \times 50)$$

where $V_{GAIN\ SET}$ is in volts.

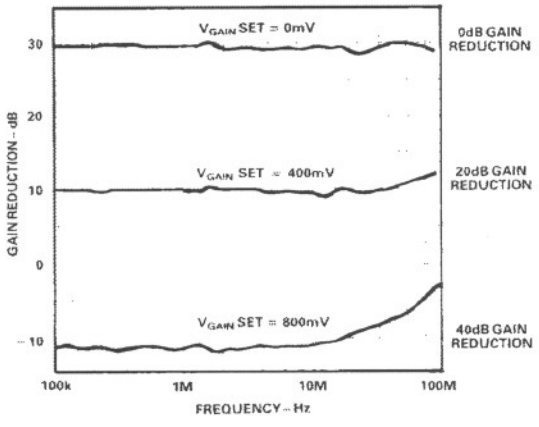


Figure 11. Frequency Response of VGA Gain for Different Gain Set Voltages

OPERATION WITH +5V, +12V SUPPLIES

Operation with +5V (±0.25V) and +12V (±1.2V) supplies is readily achieved. Figure 12 shows the AD890 configured for +5V, +12V operation. The analog and digital grounds must be connected to the +5V line or to an available center tap of the

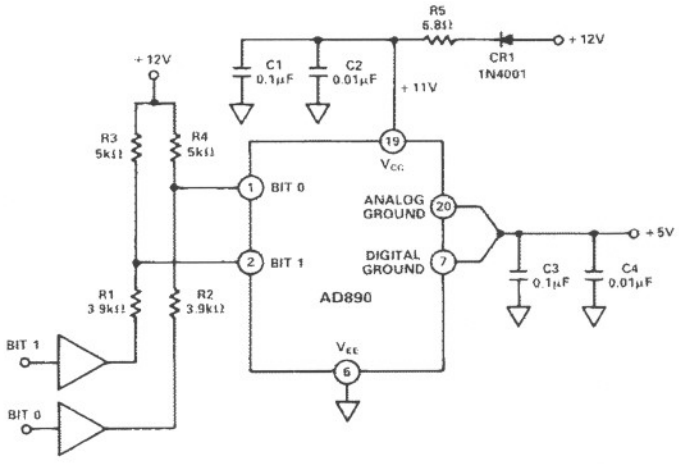


Figure 12. AD890 Connection for +5V, +12V Operation

+12V supply. Thus connected, a current of approximately 30mA will flow in this line under normal operation. The input clamping action occurs with respect to this line, increasing its current by an additional 12mA or so.

Both the +5V and +12V supplies should be RF bypassed to ground with at least two capacitors: values of 0.1μF and 0.01μF are recommended. In addition, some higher level of decoupling capacitance such as 3.3μF value may be desirable. Next, insert a series-connected 6.8Ω 1/4W resistor and 100mA diode in series with the +12V supply. This helps to reduce overdissipation in the chip.

Power supply decoupling should occur on the circuit side of the resistor-diode network. A second diode can be substituted for the 6.8Ω resistor if the voltage difference between the two supplies is greater than 5.6 volts.

Finally, mode control is achieved by using open collector drivers and resistors as shown; 5.1V Zener diodes can be substituted for resistors R1 and R2. Internal diode clamping in the AD890 permits this mode of operation.

The mode switching times will be affected by resistor values chosen; this is due to the RC time constants formed by the resistors in conjunction with the input capacitance of the chip package.

INTEGRATING WITH THE AD891 RIGID DISK DRIVE DATA QUALIFIER

Figure 13 shows a typical application using the AD890 and AD891 connected together to create a 30MHz channel (cerdip connections shown). This circuit includes a 5-pole 30MHz Gaussian-to-6dB transitional filter plus a second-order RLC time domain equalizer. A typical second-order, fully differential, passive delay-line differentiator interface for the AD891 is also included. (For a more detailed description of the delay-line differentiator, see the AD891 data sheet.) The analog and digital grounds should be connected at the power supply common.

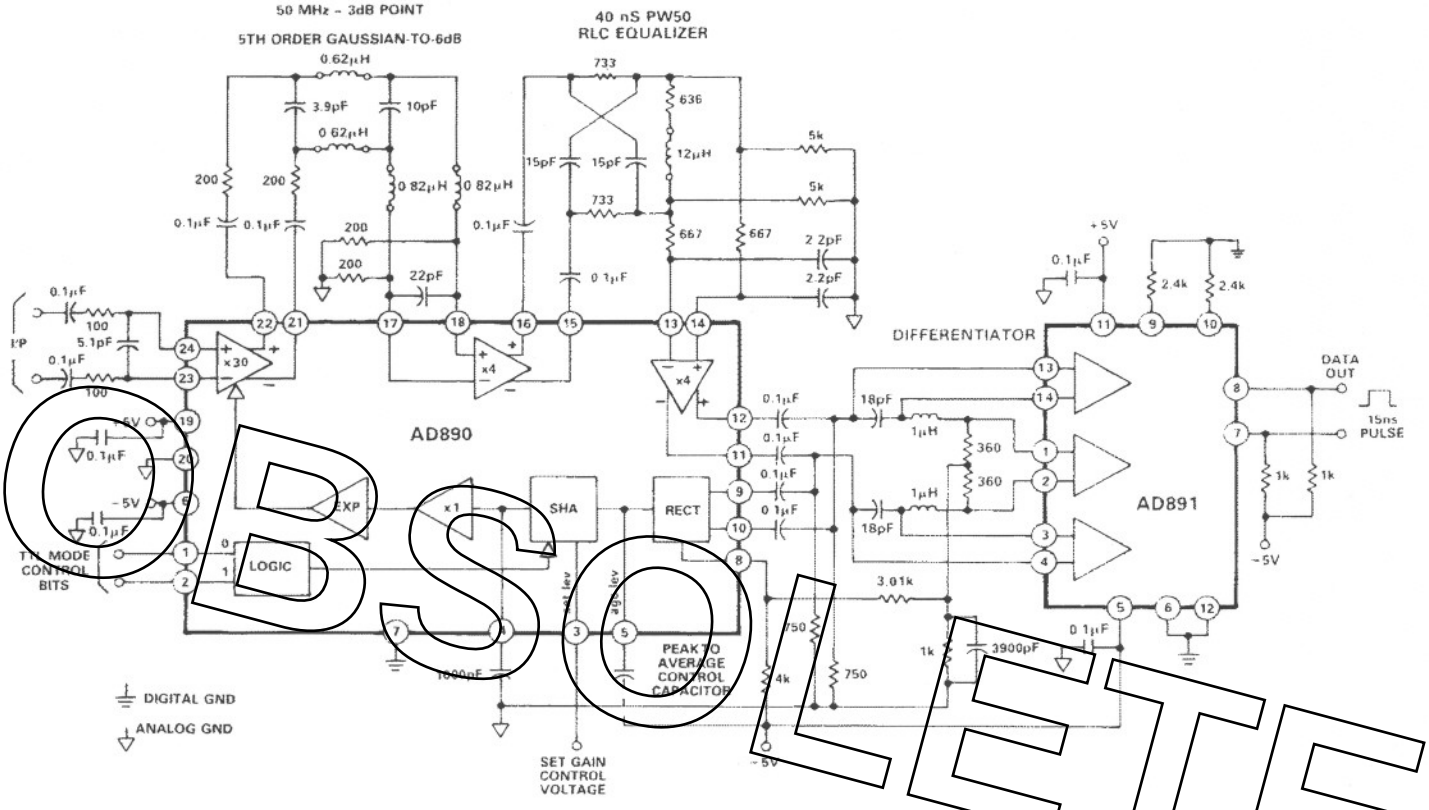


Figure 13. Typical AD890/AD891 Connection for a 30MHz Channel

USING EQUALIZERS WITH THE AD890

The AD890 is ideal for applications where equalization is employed. The X4 buffer output drivers are designed to operate into 200Ω loads, making tapped delay-line designs easy. Sum and differencing of different tap weights can be achieved by simple resistive dividers.

As an alternative, a simple RLC network can be implemented to provide a low-cost, fully differential alternative to the three-tap, tapped delay-line equalizer which often is used for pulse slimming. Essentially, the equalizer shown in Figure 14 consists of an RC lattice, which provides the magnitude characteristic, together with an LR shunt section which acts to define the overall passband group delay and the ratio of minimum to maximum gains within the passband.

The network shown approximates a function of the form:

$$F(\omega\tau) = 1 - k \cos \omega\tau, \text{ where } k = 0.6, \text{ and } \tau = 36\text{ns}.$$

The circuit is optimized for a 120ns transition PW5O. Altering the 953Ω resistor and the 24μH inductor can change both k and τ, permitting cylinder dependent equalization to be performed, thus minimizing problems of overequalization. To alter k, the ratio of the 1.1kΩ and 953Ω resistors should be changed. To alter τ, the reactive element should be scaled proportionally. The equalizer in Figure 13 is optimized for k = 0.6 and τ = 12ns.

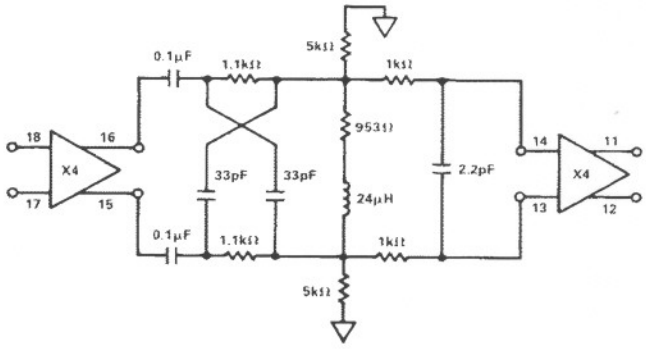


Figure 14. RLC Equalizer

It is important to note the benefits of fully differential (as opposed to single-ended) operation: 1) reduced harmonic distortion due to symmetric operation; 2) improved power supply noise rejection; 3) less insertion loss, allowing for reduced gain and, hence, improved distortion in stages prior to the equalizer.

The magnitude and group delay characteristics of this equalizer are shown in Figures 15 and 16, respectively.

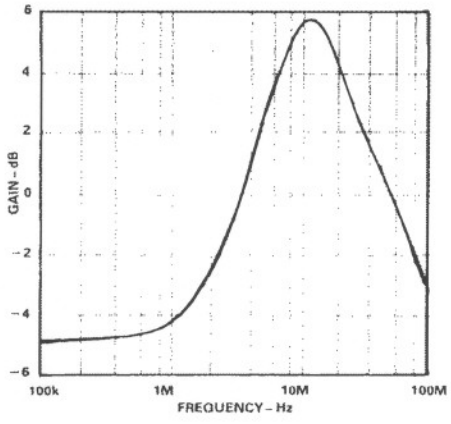


Figure 15. RLC Equalizer Magnitude Response

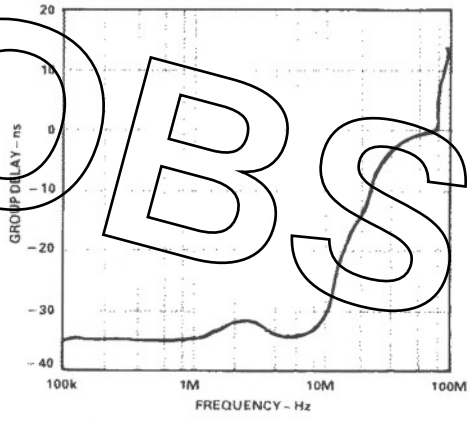


Figure 16. RLC Equalizer Group Delay Response

CHOICE OF LOW PASS FILTER WITH THE RECOMMENDED EQUALIZER

A fifth order, Gaussian-to-6dB transitional filter is recommended for use with the equalizer. Such a low pass filter is shown in Figure 17. Low group delay ripple and high out-of-band rejection make this design work well with the recommended equalizer and the differentiator specified in the AD891 data sheet. The recommended location for the low pass filter is between the VGA and first X4 buffer. The equalizer should be placed between the first and second X4 buffers. This minimizes the potential for oscillations induced by interstage parasitic feedback.

The magnitude and group dealy characteristics of this filter are shown in Figures 18 and 19, respectively.

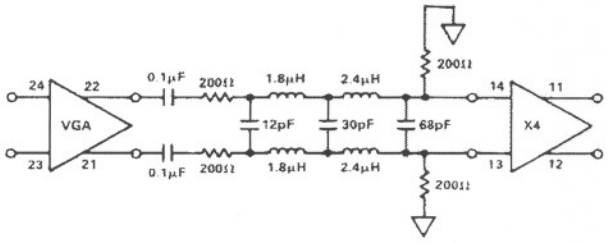


Figure 17. 5th Order Gaussian-to-6dB Transitional Filter

The magnitude and group dealy characteristics of this filter are shown in Figures 18 and 19, respectively.

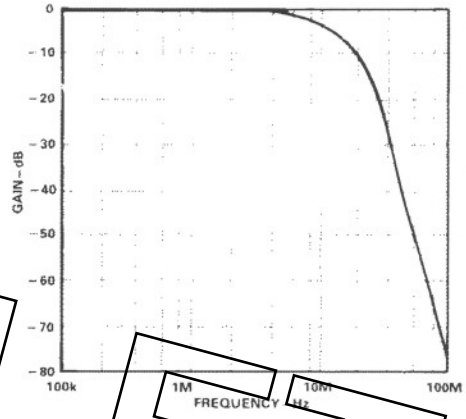


Figure 18. Gaussian Low-Pass Filter Magnitude Response

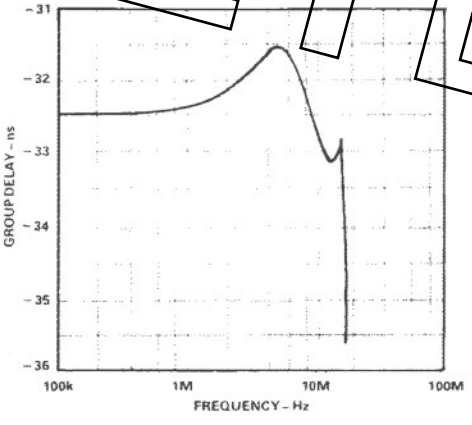


Figure 19. Gaussian Low-Pass Filter Group Delay Response

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