ANALOG DEVICES

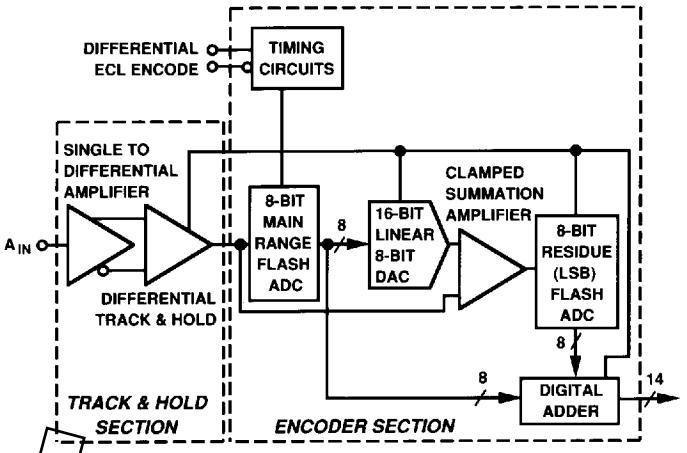
14-Bit, 10 MSPS A/D Converter

AD9014

FEATURES
Sample Rate: 10 MSPS
Spurious Free Dynamic Range: 92 dB @ 2.3 MHz A_{IN}; 88 dB @ 4.3 MHz A_{IN}; 72 dB @ 10 MHz A_{IN}
Low Intermodulation Distortion: −95 dBFS @ 2.3 MHz
SNR: 75 dB
Differential Encode Clock
Complete Subsystem

APPLICATIONS
Radar Signal Analysis
Visible & Infrared Imaging
FFT Spectrum Analysis
Medical Imaging
SIGINT/ECM/EW

AD9014 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9014 is a high performance 14-bit analog-to-digital converter designed to provide extremely wide dynamic range for spectrum analysis and imaging applications. It is a complete subsystem that requires the user to provide only power and an encode clock.

Careful consideration to the design of the converter, along with the development of several custom linear and digital IC building blocks, has resulted in a converter with unsurpassed dynamic range. Sampling at 10 MSPS, the spurious free dynamic range (SFDR) is a function of analog input frequency as shown below:

Analog Input	SFDR
100 kHz	90 dB (min)
2.3 MHz	90 dB (min)
4.3 MHz	86 dB (min)
10 MHz	72 dB (typ)

For the AD9014, DNL is 0.5 LSBs; transient response to 0.01% is 30 ns; full power bandwidth is 50 MHz; and the SNR is 75 dB. These attributes make the AD9014 ideal for applications that require fast sampling of relatively low frequency analog input signals, such as CCD and infrared imaging.

The AD9014 consists of two custom hybrids mounted on a small multilayer PCB. The hybrid differential track-and-hold achieves first order cancellation of the even order harmonics while suppressing common-mode noise. The second hybrid is a digitally corrected subranging A/D encoder that uses two 8-bit flash converters with two bits of overlap correction. Decoupling capacitors have been designed into both hybrids, as well as on the mother board. This onboard decoupling simplifies the task of successfully using the converter.

Each AD9014 is tested at a 10 MSPS encode rate at multiple analog input frequencies. For each input frequency, the FFT testing is repeated for various A_{IN} power levels. This technique verifies that the dynamic performance of the converter is maintained even when low level input signals are being digitized.

Two versions of the AD9014 are available. The AD9014K is intended for applications that require the highest possible spurious free dynamic range performance; the AD9014J is intended for applications where spectral domain information is not as important, such as in imaging. The analog input signal can be applied to the ADC via either an onboard SMA connector or through a pin connected to the connector. Logic is ECL; the encode clock is differential ECL.

Consult Analog Devices about special needs and/or specific applications.

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703 Twx: 710/394-6577
Telex: 924491 Cable: ANALOG NORWOODMASS

AD9014—SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltages ($\pm V_S$) . . . . . ±18 V
V_{CC} Supply Voltage . . . . . +6 V
V_{EE} Supply Voltage . . . . . −6 V
Analog Input Voltage $V_{EE} \leq A_{IN} \leq V_{CC}$
(or whichever is less) . . . . . ±4 V
Digital Input Voltage . . . . . V_{EE} to +0.5 V
Digital Output Current . . . . . 4 mA
Operating Temperature Range . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +150°C

ELECTRICAL CHARACTERISTICS

($\pm V_S$ = ±15 V; V_{CC} = +5 V; V_{EE} = −5.2 V; Encode Rate = 10.0 MSPS unless otherwise indicated)[2]

Parameter (Conditions)	Temp	AD9014J Min	AD9014J Typ	AD9014J Max	AD9014K Min	AD9014K Typ	AD9014K Max	Units
RESOLUTION	Full	14			14			Bits
LSB Weight	Full		0.122			0.122		mV
STATIC ACCURACY								
Differential Nonlinearity	+25°C		0.6			0.5		LSB
	Full		0.6			0.5		LSB
Integral Nonlinearity	+25°C		1.0			0.75		LSB
	Full		1.5			1.0		LSB
No Missing Codes			Guaranteed			Guaranteed		
Gain Error	+25°C		0.2	1.0		0.2	1.0	% FS
Temperature Coefficient	Full		15			15		ppm/°C
Offset Error	+25°C		0.2	1.0		0.2	1.0	% FS
Temperature Coefficient	Full		8			8		ppm/°C
ANALOG INPUT								
Input Voltage Range	Full		±1.0			±1.0		V
Input Resistance	Full		75			75		Ω
Input Capacitance (at SMA connector)[3]	+25°C		7			7		pF
Full Power Input Bandwidth	Full		60			60		MHz
SWITCHING PERFORMANCE								
Conversion Rate[4]	Full			10.00			10.00	MSPS
Pipeline Delay	Full		1			1		Clock Cycle
Output Data Delay (t_{OD})[5]	+25°C		30			30		ns
Aperture Delay	+25°C		4			4		ns
Aperture Jitter	+25°C		1.5			1.5		ps rms
DYNAMIC CHARACTERISTICS[4, 6]								
Transient Response (to 0.01%)	+25°C		30			30		ns
Overvoltage Recovery Time (1.5 × to 0.01%)	+25°C		100			100		ns
Overvoltage Recovery Time (1.5 × to 0.0025%)	+25°C		200			200		ns
Worst-Case Harmonic Distortion[7]								
A_{IN} = 100 kHz	+25°C	−84			−90			dBFS
A_{IN} = 2.3 MHz	+25°C	−84			−90			dBFS
A_{IN} = 4.3 MHz	+25°C	−82			−86			dBFS
A_{IN} = 10 MHz	+25°C		−72			−72		dBFS
Signal-to-Noise Ratio (A_{IN} = 100 kHz)[8]	+25°C		75			75		dB
Signal-to-Noise Ratio (A_{IN} = 2.3 MHz)[8]	+25°C		75			75		dB
Two-Tone Intermodulation								
2.3 MHz & 2.4 MHz (each −7 dBFS)	+25°C	−84			−90			dBFS
ENCODE INPUT[9]			Differential ECL			Differential ECL		
Logic "1" Voltage	Full	−1.1			−1.1			V
Logic "0" Voltage	Full			−1.5			−1.5	V
Logic "1" Current	Full		8			8		mA
Logic "0" Current	Full		8			8		mA
Input Capacitance	+25°C		5			5		pF
Encode Pulse Width	+25°C	10			10			ns
Encode Pulse Width (% of duty cycle)	+25°C			50			50	%

Parameter (Conditions)	Temp	AD9014J Min	AD9014J Typ	AD9014J Max	AD9014K Min	AD9014K Typ	AD9014K Max	Units
DIGITAL OUTPUTS[10]								
Logic "1" Voltage	Full	−1.1			−1.1			V
Logic "0" Voltage	Full			−1.5			−1.5	V
Logic Coding	Full		Offset Binary			Offset Binary		
POWER SUPPLIES								
$+V_S$ Supply Voltage	Full	+14.5	+15.0	+15.5	+14.5	+15.0	+15.5	V
$+V_S$ Supply Current	Full		245			245		mA
$-V_S$ Supply Voltage	Full	−14.5	−15.0	−15.5	−14.5	−15.0	−15.5	V
$-V_S$ Supply Current	Full		130			130		mA
V_{CC} Supply Voltage	Full	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	V
V_{CC} Supply Current	Full		422			422		mA
V_{EE} Supply Voltage	Full	−4.95	−5.2	−5.45	−4.95	−5.2	−5.45	V
V_{EE} Supply Current	Full		980			980		mA
Power Dissipation (Operating)	Full		12.8			12.8		W
Power Supply Rejection Ratio (PSRR)								
$+V_S$ (ΔV_S = ±0.5 V)	+25°C		0.02			0.02		%/%
$-V_S$ (ΔV_S = ±0.5 V)	+25°C		0.01			0.01		%/%
V_{CC} (ΔV_{CC} = ±0.25 V)	+25°C		0.01			0.01		%/%
V_{EE} (ΔV_{EE} = ±0.25 V)	+25°C		0.01			0.01		%/%

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

[2]Cooling air at 500 LFPM applied. Parts must have 30 second warm-up time.

[3]The capacitance seen at the analog input pin of the T/H hybrid is 2.0 pF.

[4]Consult factory regarding availability of units with lower spur levels; units capable of 10.24 MSPS rates are also available.

[5]Measured from rising edge of Encode Command (Pin 16) to instant of final change in data output.

[6]During factory testing, analog input is applied to AD9014 via onboard SMA connector.

[7]Power of the analog input is swept from −1 dBFS to approximately −60 dBFS; and multiple FFTs are taken for "K-grade" parts. The specification is equivalent to the spurious free dynamic range (SFDR).

[8]Including noise and all spurs.

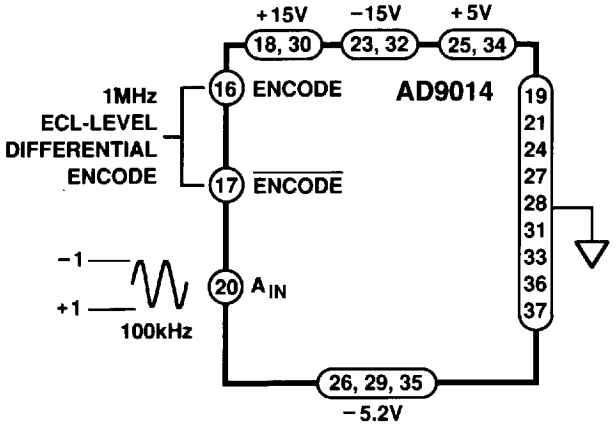
[9]10Kvoltage-level-compatible. Encode inputs have 50 Ω differential terminations.

[10]Each digital output is terminated to −5.2 V through a 2 kΩ resistor with a 1k resistor in series with the output. See diagram elsewhere in data sheet.

ORDERING GUIDE

Model*	Temperature Range	SFDR
AD9014J	0°C to +70°C	84 dB
AD9014K	0°C to +70°C	90 dB

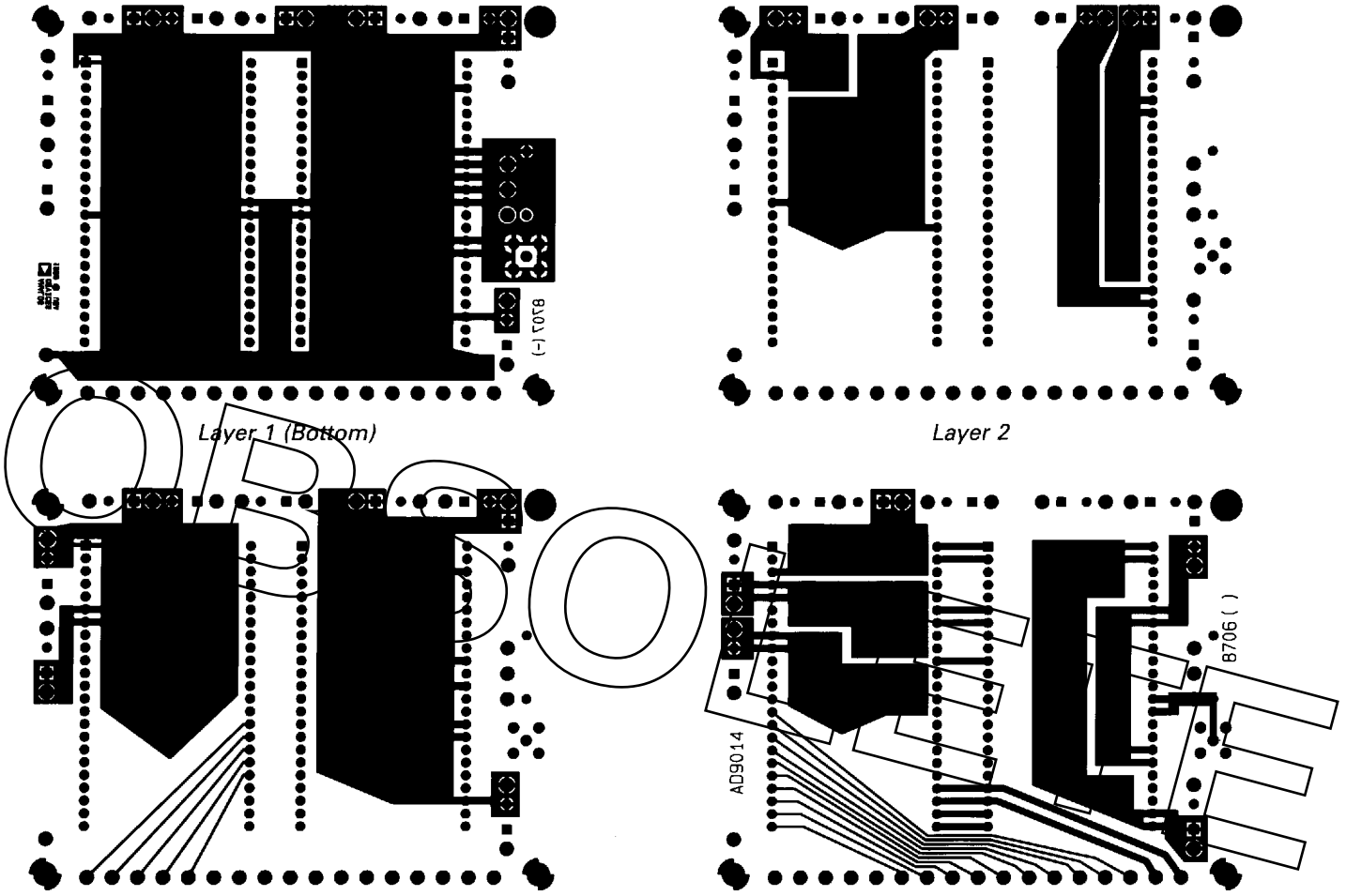
*Add −50 to part number to specify 50 Ω input impedance.



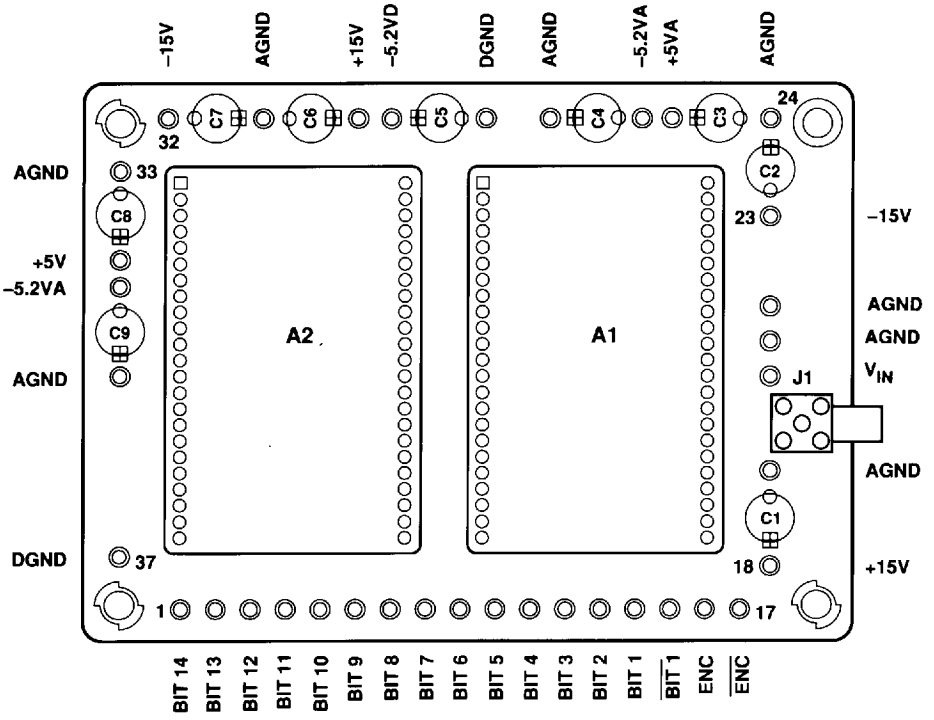
AD9014 Burn-In Circuit

AD9014 PRINTED CIRCUIT BOARD LAYERS

All layers shown from component (top) side.

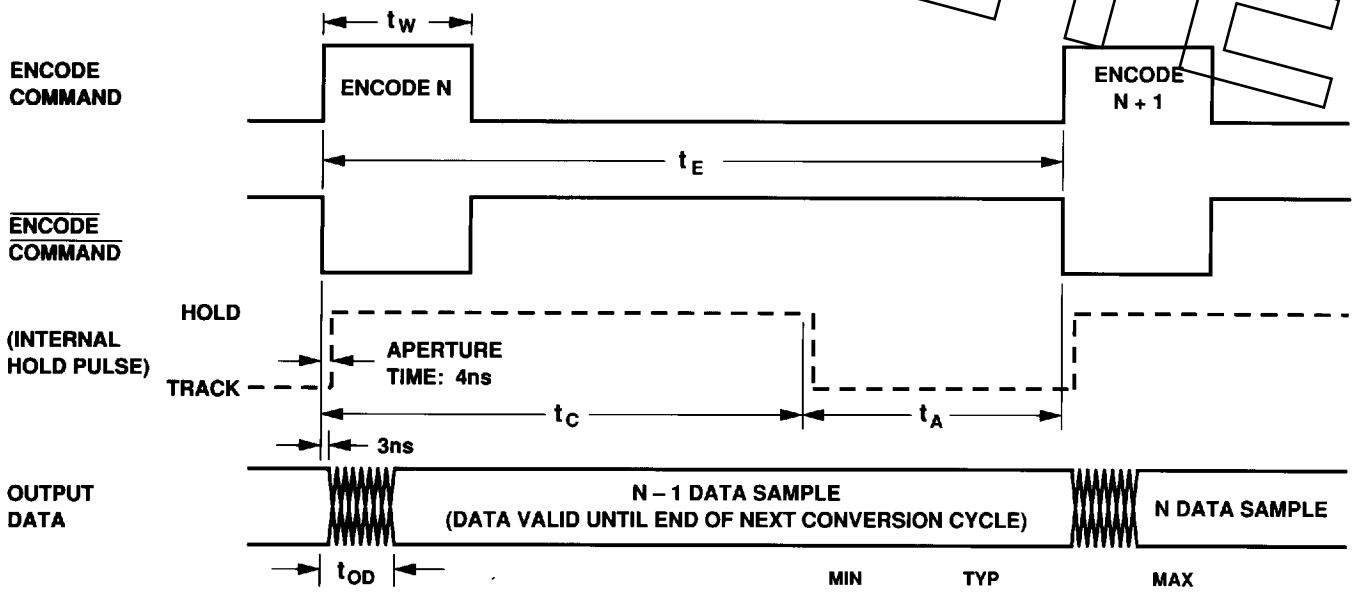


AD9014 PIN CONFIGURATION



AD9014 PIN DESCRIPTIONS

Pin No.	Name	Function
1 through 14	Bit 14 (LSB) through Bit 1 (MSB)	True ECL outputs. Each is internally terminated to −5.2 V through a 2 kΩ resistor and has limited drive capability; a 1 kΩ isolation resistor is connected in series with the output. Additional termination will increase current spikes within the hybrid, and possibly degrade A/D performance. These pins should be interfaced to ECL receivers or latches located as close as possible to the AD9014. Positive full scale is represented by all "1"s. (See equivalent circuit elsewhere in data sheet.)
15	$\overline{\text{Bit 1 (MSB)}}$	Complement of Bit 1 (see above).
16	ENCODE	Differential ECL ENCODE inputs; 50 Ω internal terminations. User-supplied ENCODE command should contain smallest possible amount of jitter for optimum performance.
17	$\overline{\text{ENCODE}}$	
18, 30	+15 V	Analog supply pins; decoupling capacitors included on AD9014 card.
19, 24, 27	AGND	Analog ground; should be connected to low impedance ground plane.
20	A_{IN}	Analog input to AD9014; interface is via either SMA connector or this pin, nominally 75 Ω input impedance. (See equivalent circuit.)
21	AGND	Signal ground reference; should be connected to signal source reference.
22	AGND	Signal ground reference; should be connected to signal source reference.
23, 32	−15 V	Analog supply pins; decoupling capacitors included on AD9014 card.
25, 34	+5 V	V_{CC} analog supply pins; decoupling included on AD9014 board.
26, 35	−5.2 V	V_{EE} analog supply pins; decoupling included on AD9014 board.
31, 33, 36	AGND	Analog ground; should be connected to low impedance ground plane.
29	−5.2 V	Digital V_{EE} supply pin.
28, 37	DGND	Digital ground; should be connected to low impedance ground plane.



		MIN	TYP	MAX
t_W	ENCODE COMMAND PULSE WIDTH	10ns		50% OF DUTY CYCLE
t_E	SPACING BETWEEN ENCODE COMMANDS	100ns		
t_C	CONVERSION TIME		65ns	
t_A	ACQUISITION TIME *		35ns	
t_{OD}	OUTPUT DELAY [DRIVING SINGLE 10K LOGIC GATE ADJACENT TO UNIT (SEE APPLICATIONS SECTION)]		30ns	

*APPLICATIONS WITH SLIGHTLY FASTER SAMPLING RATE (10.24 MSPS) WILL HAVE ACQUISITION TIME WHICH IS APPROXIMATELY 2ns SHORTER

AD9014 Timing Diagram

THEORY OF OPERATION

The AD9014 is a two-step subranging analog to digital converter that provides extremely wide dynamic range performance. Its major system building blocks include a single to differential amplifier; track and hold amplifier; 8-bit main range flash ADC; 16-bit-linear, 8-bit DAC; clamped monolithic summation amplifier; 8-bit residue flash ADC; and digital adder logic.

The AD9014 consists of two custom hybrids mounted on a small multilayered PCB. It was made possible by a judicious combination of innovative design topologies, new custom chips, and mature manufacturing processes including laser trimming of thin-film resistors.

Subranging architecture has been utilized in numerous ADCs and has proven to be an efficient way to obtain wide dynamic range at high sampling rates. Briefly, a single-ended analog input signal is converted to a balanced differential signal that is "sampled and held" by a track and hold amplifier. This held value is then digitized by the main range 8-bit flash A/D converter. The resulting 8-bit word is converted back to an analog value via a 16-bit-linear, 8-bit DAC and is compared to the "held" value via a high accuracy, clamped summation amplifier. The difference of the two signals is then digitized by a second 8-bit flash ADC. In the final step, the two 8-bit words are combined via digital adder logic.

Refer to the block diagram of the AD9014 on the first page of this data sheet. The track and hold hybrid accomplishes two functions. First, the single-ended analog input is converted to a balanced differential signal via an extremely low distortion single to differential amplifier. The 75 Ω input impedance of the AD9014 can be regarded as the feed-forward resistor of this amplifier. Second, the resultant balanced signal is then sampled and held for digitization by the encoder hybrid.

In previous ADCs, the track and hold (T/H) has been the most significant source of harmonic and nonharmonic spurs. To help avoid this in the AD9014, approximately half the power dissipation and one of the two hybrids is dedicated to the track and hold function. A differential T/H architecture is utilized to obtain first order cancellation of the even-order harmonics. The sampling switch (or bridge) is driven by a pair of closed-loop amplifiers to minimize aperture induced harmonics. The acquisition time of the AD9014 is approximately 35 ns.

Differential architecture used in the AD9014 T/H is extended to the encoder section of the AD9014. All circuit elements are differential to minimize the generation of spurs, increase the common-mode noise suppression, and improve performance over temperature.

Two 8-bit flash converters are used to achieve the 10 MSPS encode rate; each converter provides data approximately 8 ns after it receives an encode command. The main range converter provides the MSB information, which is loaded into the digital adder circuits and is also applied to the DAC. The residue converter provides the LSB information. Two overlap or correction bits are utilized in the digital correction logic where the two 8-bit words are combined into the final 14-bit digital output.

In addition to the track-and-hold, the digital-to-analog converter looms as a large contributor of spurs. The DAC in the AD9014 utilizes unique differential diode switching current sources and laser-trimmed thin film resistors. This optimizes the performance of the ADC as a function of temperature and time.

Laser trimmed thin film resistors are inherently stable over time. Any resistor shifts that occur are transparent to the user because each resistor in the network drifts in unison with its matched counterpart. The trimmed DAC settles to 16-bit accuracy in approximately 10 ns.

The output of the DAC is compared to the held dc value via a clamped summation amplifier. This amplifier is set for a gain of 10 V/V and drives the residue 8-bit flash converter. It settles in 35 ns and comes out of overdrive in 5 ns. The settling time of this amplifier is the major factor affecting the maximum sample rate of the AD9014.

The final major source of spurs are the nonlinearities in the two flash converters. Differential nonlinearity (DNL) and integral nonlinearity (INL) errors in the main range converter determine how much of the error correction budget is actually used.

If the INL of the residue converter is sufficiently large, nonlinearities of the main range converter set the DNL of the AD9014 at the digitally compensated subranging points. If the main range converter is sufficiently linear, the DNL of the residue converter sets the overall AD9014 DNL. The flash converters used in the AD9014 are inherently linear; die are screened by probe testing before they are used in the encoder hybrid.

Finally, the two 8-bit digital words from the main range and residue flash converters are latched into a 16-bit register, where they are added to form the 14-bit digital output word. The actual error correction takes place in this adder. If the analog input exceeds positive or negative full scale, the digital output remains, respectively, at all "1" or all "0"; it does not roll over.

USING THE AD9014

The AD9014 A/D converter has been carefully designed to offer users the widest possible dynamic range. Each unit is dynamically tested before it is shipped. Great care has been taken in the design of the AD9014 to simplify its application so that users can easily duplicate the performance measured at the factory.

A well designed, "clean" printed circuit board (PCB) with separate power and ground planes is necessary; a multilayered board is recommended. Wire-wrap techniques often used in prototypes will materially diminish spectral performance. The figure labeled AD9014 Recommended Connections provides details regarding application of the unit.

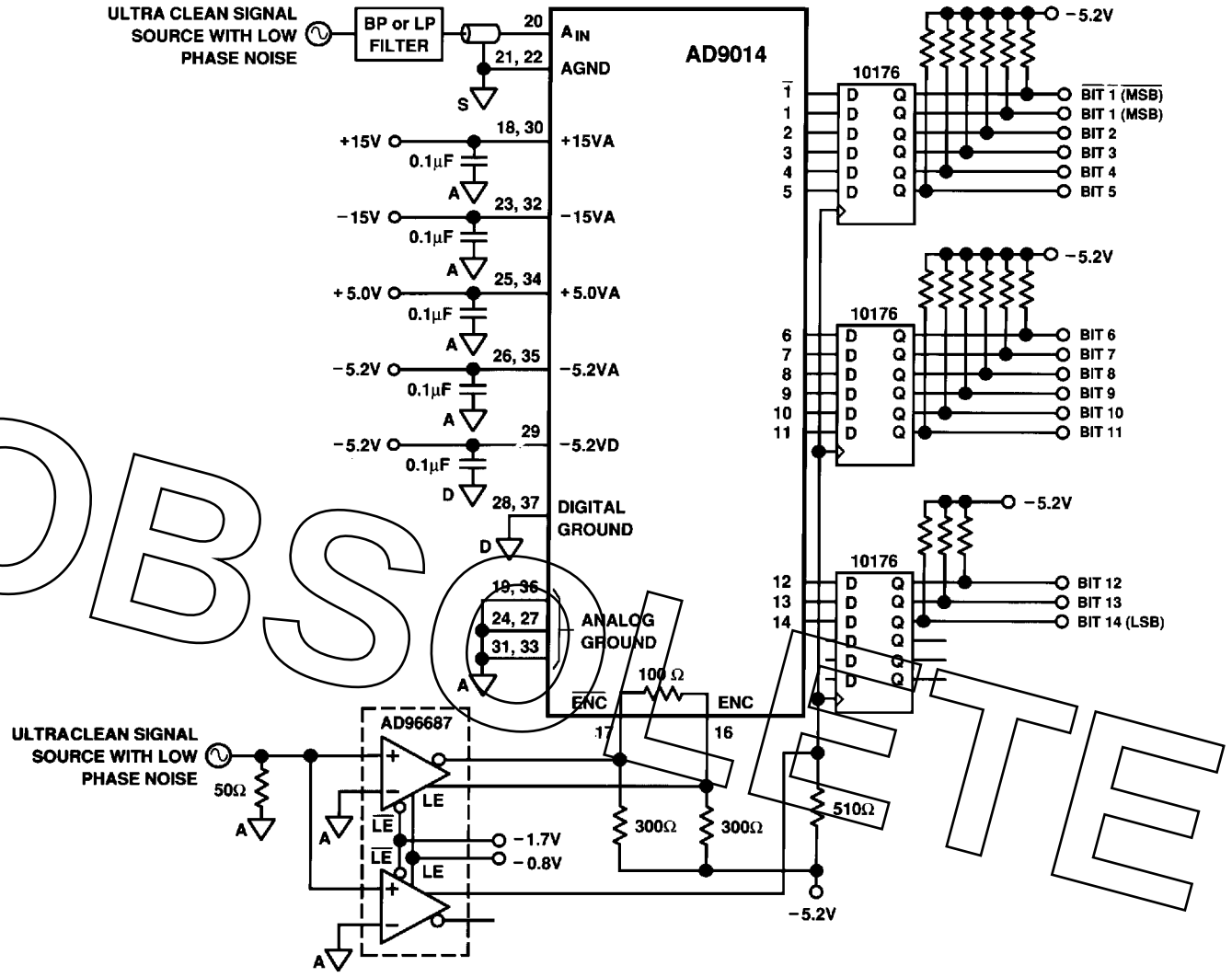
Driving the Differential Encode Input

A differential ECL encode signal is required for the AD9014. This signal should be as "clean" and fast (100K ECL equivalent) as possible, with a minimum amount of jitter.

Excessive jitter on the encode command manifests itself as a wider "skirt" around the analog input fundamental, which degrades the observed SNR and masks information which may be under the skirt. This may not be important in frequency domain applications since the generation of harmonic and nonharmonic spurs is unaffected.

One method of generating a "clean" differential ECL encode signal is to use a spectrally pure low phase noise sine wave to drive an AD96687 ultrafast ECL comparator, as shown in the "AD9014 Recommended Connections" figure on the next page. (Signal generators such as the HP 8642A and Rohde & Schwarz SMHU can be used.)

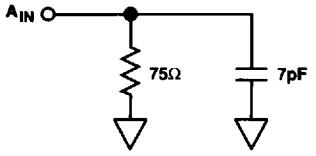
Careful consideration must be given to routing the encode signal. The comparator should be located as close as possible to the AD9014. The inputs to and outputs from the AD96687 should be as short as possible and terminated right at the unit.



AD9014 Recommended Connections

Matching the Analog Input Impedance

As described in the Theory of Operations, the analog input impedance into the track and hold is 75 Ω || 7 pF. This is shown graphically in the figure below.



AD9014 Analog Input Circuit

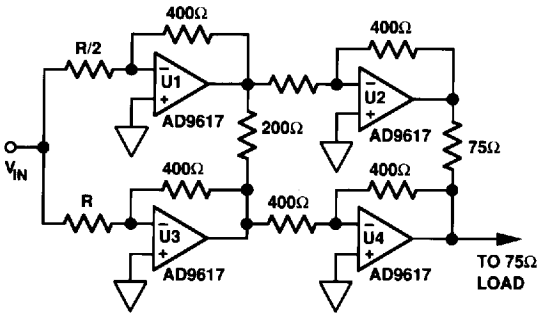
The Analog input signal can be applied to the ADC either via the SMA connector or through Pin 20. The drive source should be matched to the impedance of the ADC. The AD9014 can be set up for a 50 Ω system by soldering the appropriate resistor between Pins 20 and 21. This option will be installed at the factory if "−50" is added to the part number when the order is placed.

Driving the Analog Input

Special care must be taken to ensure that the analog input signal is not compromised before it reaches the A/D converter. Any required filtering should be done as close to the AD9014 as possible, and away from any digital lines.

The full-scale analog input range of the AD9014 is 9 dBm (±1 V into 75 Ω). In many applications, the analog input is at a much lower level and must be amplified to meet the full-scale range of the AD9014. The optimum way to achieve this amplification depends largely on the application.

For frequency domain applications, the circuit shown below is recommended when gain is required. This configuration works well for analog input frequencies through 10 MHz without introducing spurs that degrade the ADC's capabilities. At



Input Impedance = R/3 Gain = $+\frac{400\Omega}{R}$ (V_{OUT} = 2V p–p)

Low-Distortion Drive Circuit for AD9014

2.3 MHz and 2 V p–p output, all spurs generated are less than −100 dBc. The output is configured to drive the 75 Ω input impedance of the AD9014. Note that this circuit will add approximately 6 dB to the noise floor and is not recommended for applications where SNR is crucial.

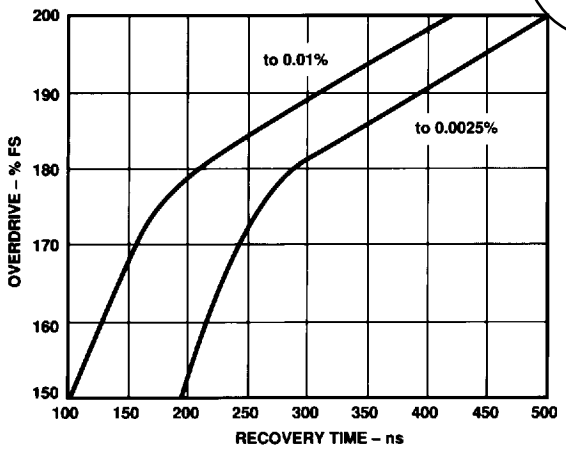
The signal path is through U3 and U4, which are set up in a series inverting configuration to cancel even-order harmonics that are generated when gain bandwidth product diminishes with frequency. U1 and U2 reduce the drive current of U3 and U4, respectively. Since U1 and U2 are set up in gains twice that of U3 and U4, the net effect is that the output stages of U3 and U4 are unloaded. This eliminates the odd-order harmonics generated in the output stages of U3 and U4.

The gain of the overall block is +400 Ω/R, and the input impedance is R/3. The output of the amplifier circuit is set up to drive 1 V peak into 75 Ω.

Overdriving the Analog Input

The analog input can be overdriven by 12 dB (±4 V) without inflicting long term damage to the AD9014. When overdriven, the digital outputs will be either all 1s or 0s depending on whether it is overdriven high or low.

The recovery time from the instant the overvoltage condition is relieved to when the converter begins producing valid data is a function of the amount of overdrive. Results are summarized in the following chart.

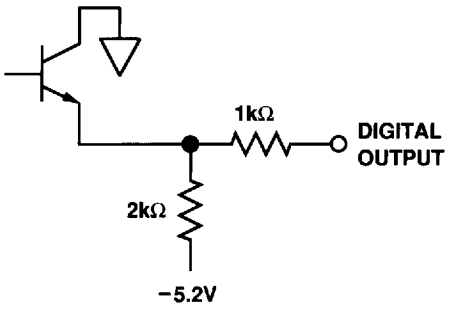


Overvoltage Recovery Time

Collecting the Digital Output Data

Digital data from the AD9014 is ECL compatible. Pull-down resistors are included inside the encoder hybrid; 1 kΩ series resistors are also included to completely isolate the digital outputs from the analog sections of the AD9014. (See "MECL System Design Handbook," Fourth Edition, page 27; printed by Motorola Inc.)

The digital outputs should interface directly to an ECL latch or receiver, located as close to the AD9014 as possible. No external pull-down resistors are required; they are built into the AD9014.

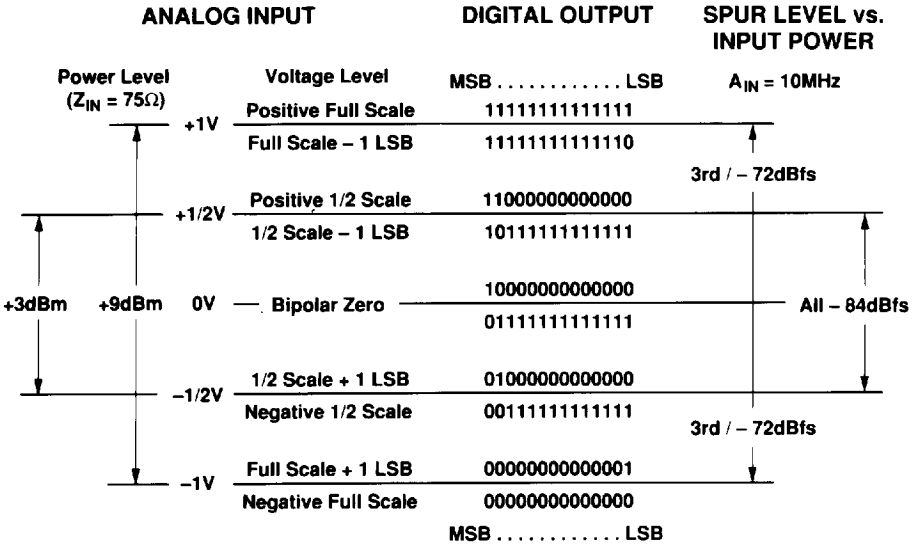


AD9014 Digital Output (One of 15, Including MSB)

Digitizing Super Nyquist Signals

The AD9014 can be used to digitize analog super-Nyquist input signals. For a full-scale analog input of 10 MHz, the third harmonic is typically −72 dBc and is the highest spur. When the analog input power is lowered by 6 dB, the third harmonic drops about 12 dB; all spurs generated by the ADC typically remain below −84 dBFS.

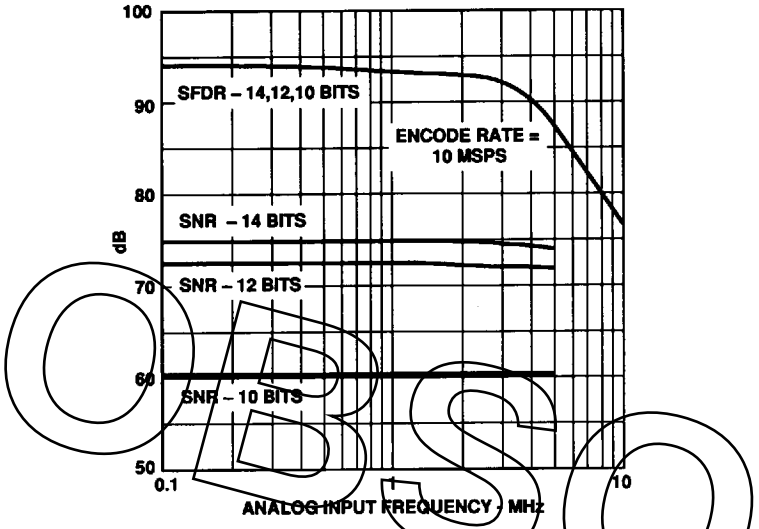
By arbitrarily defining the full-scale power level into the AD9014 to be −6 dBFS or 3 dBm, signals up to 10 MHz can be digitized while maintaining a spurious-free dynamic range of at least 80 dB. In this example, Bits 1 and 2 are used as the overflow signal (see Digital Coding graph below); all 14 bits from the converter must be used, are valid, and should be processed.



AD9014 Digital Coding

Utilizing Fewer than 14 Bits

In some cases it is advantageous to ignore the AD9014's LSBs. As an example, if a previously designed DSP or buffer memory is able to process only 10- or 12-bit words, retrofitting the system using the AD9014 may provide significant improvements.



AD9014 SFDR and SNR vs. Frequency

The spurious free dynamic range (SFDR) of any A/D is a function of the converter linearity, while the "number of bits" of the converter's output affects the level of the noise floor. The level of the internally generated spurs will not rise as bits are omitted, but the noise floor rises for each bit that is dropped. The chart below summarizes the AD9014 SFDR as a function of the number of bits being processed.

Noise Figure Estimates

An estimate of the noise figure of the AD9014 can be calculated from information contained in the specification table. It is defined as the degradation of the signal-to-noise ratio as an analog signal passes through the device.

Since the AD9014 has no gain, the noise figure can be determined by comparing the noise level at the output to the noise at the input. For a 50 Ω system, the input noise can be determined using Boltzmann's Constant, the absolute temperature, and the bandwidth. For a 1 Hz bandwidth at room temperature, this value is −174 dBm/Hz.

The noise level at the output of the AD9014 can be calculated from the specified signal to noise-ratio (SNR) which is 75 dB. Since the full-scale analog input signal is +9 dBm, the noise level at the output of the AD9014 is −66 dBm for the 5 MHz band.

The noise figure can be determined using the following equation:

$$NF = Output\ Noise - 10\ log_{10}\ (BWo/BWi) - Input\ Noise\ Level$$

where BWo = 5 MHz and BWi = 1 Hz

For the AD9014, the noise figure calculates to:

$$NF = -66\ dB - 67\ dB - (-174\ dB) = 41\ dB$$

Third Order Intercept Point

Traditionally, the third order two-tone intermodulation specification of mixers is the most troublesome, since the resultant frequencies are very close to the fundamental signals and are difficult to filter. The differential design of the AD9014 ensures that the generation of two-tone IMD spurs is minimized.

The two-tone IMD intercept point for the AD9014 can be easily estimated for a given frequency if the harmonic suppression of the IMD spur levels is known (or can be measured). As shown in the typical performance section of the data sheet, for 2 dBm (−7 dBFS) analog input tones of 2.3 MHZ and 2.4 MHz, the relevant IMD spurs are located at 2.2 MHz and 2.5 MHz, and are −95 dBm (−102 dBFS).

The following equation can be used to determine the converter's intercept point:

$$Intercept\ Point = [Harmonic\ Suppression/(N-1)] + Input\ Power$$

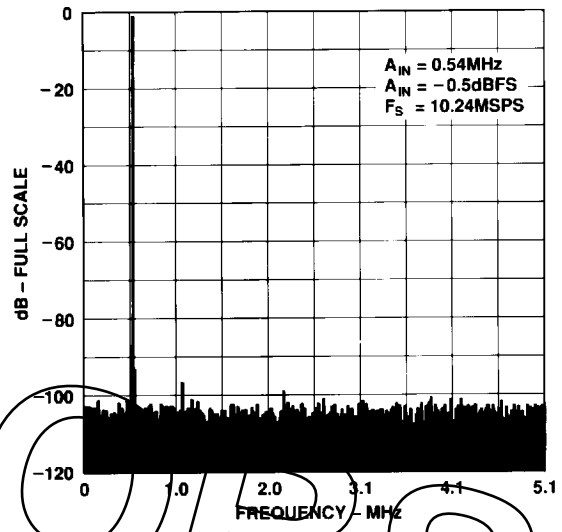
where N = the order of the IMD (3 in this case)

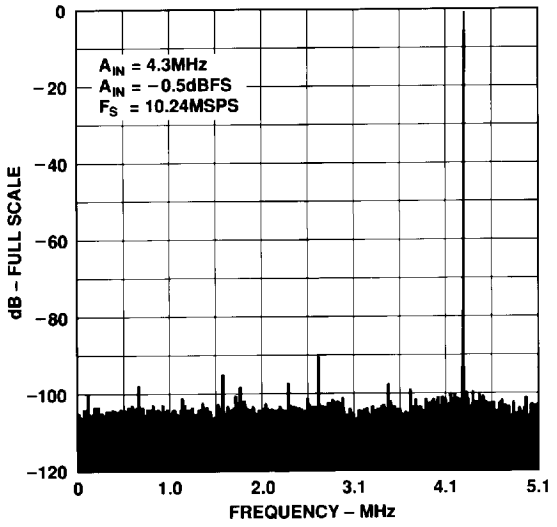
$$AD9014\ Intercept\ Point = 95/2 + 2\ dBm = 49.5\ dBm$$

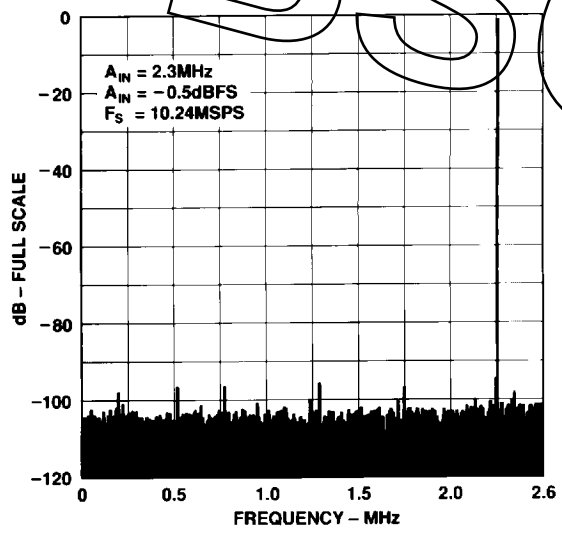
The intercept point for the AD9014 is a measure of the effectiveness of the AD9014's track-and-hold amplifier and is valid over the relevant frequency range and for analog input values within approximately 10 dB of the converter's specified full-scale range. When the analog input level is less than −10 dBFS, the nonlinearities of the encoder tend to dominate and the intercept point concept is invalid.

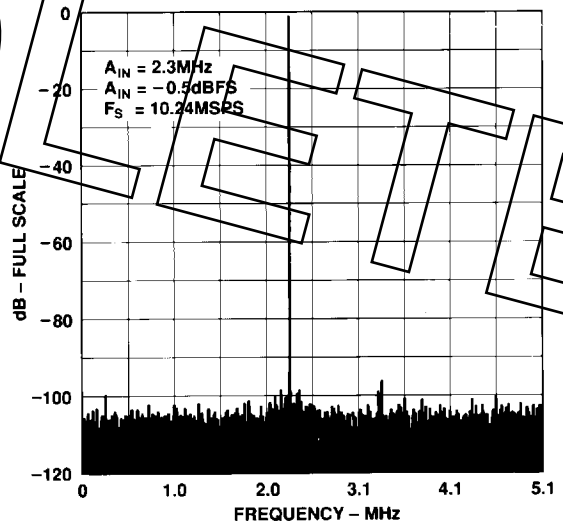
TYPICAL AD9014K SPECTRAL PERFORMANCE

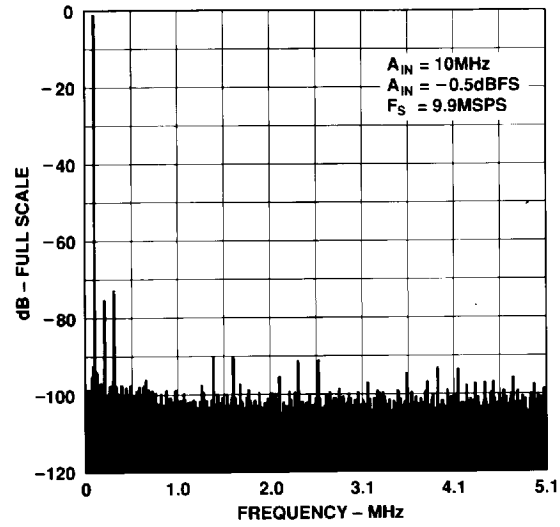
Five-sample average of 8,192-point FFTs; all harmonics are aliased.

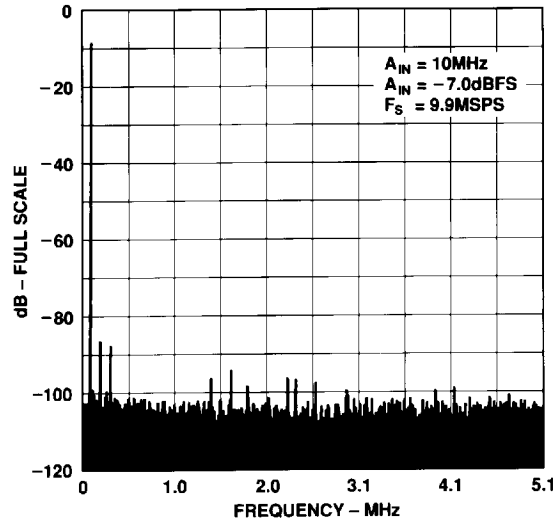


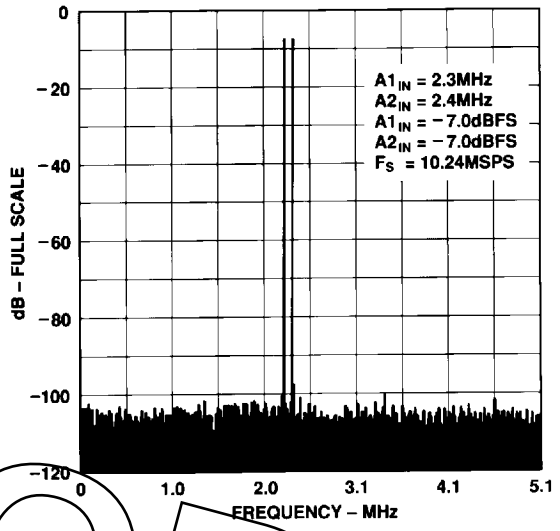


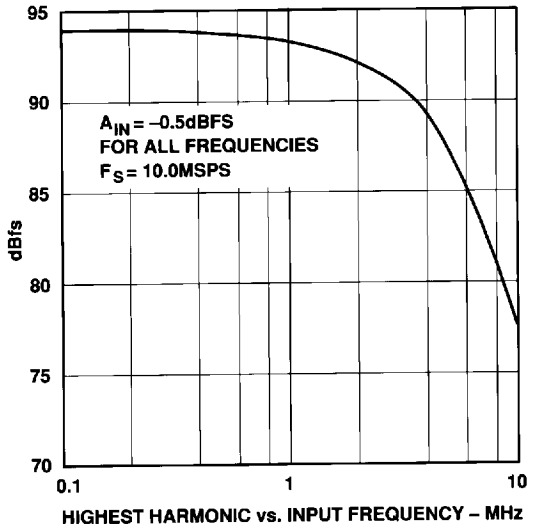




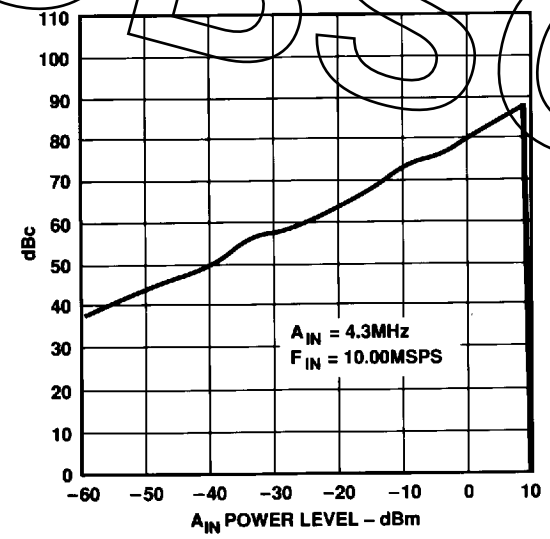


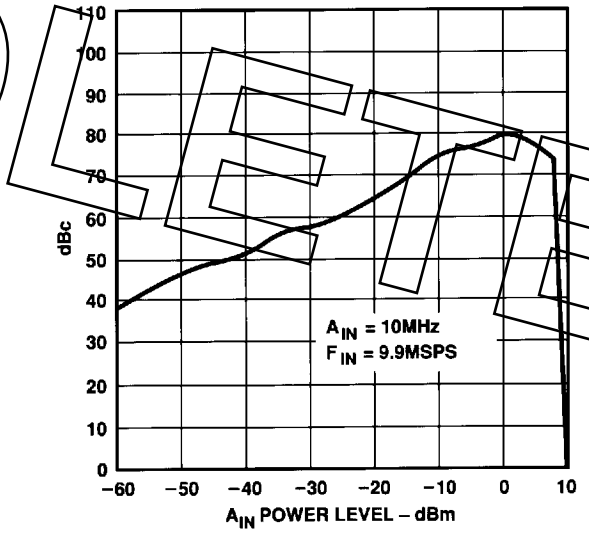


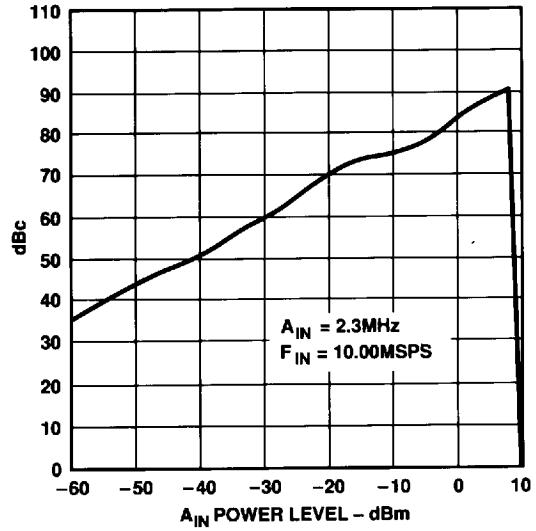


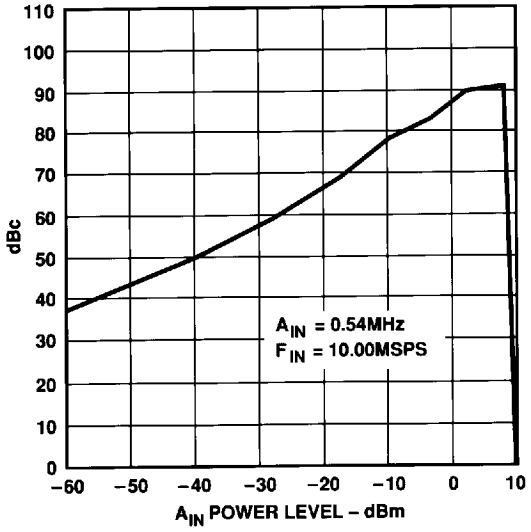


AD9014K TYPICAL PERFORMANCE
SPURIOUS FREE DYNAMIC RANGE (SFDR) VS. INPUT POWER LEVEL



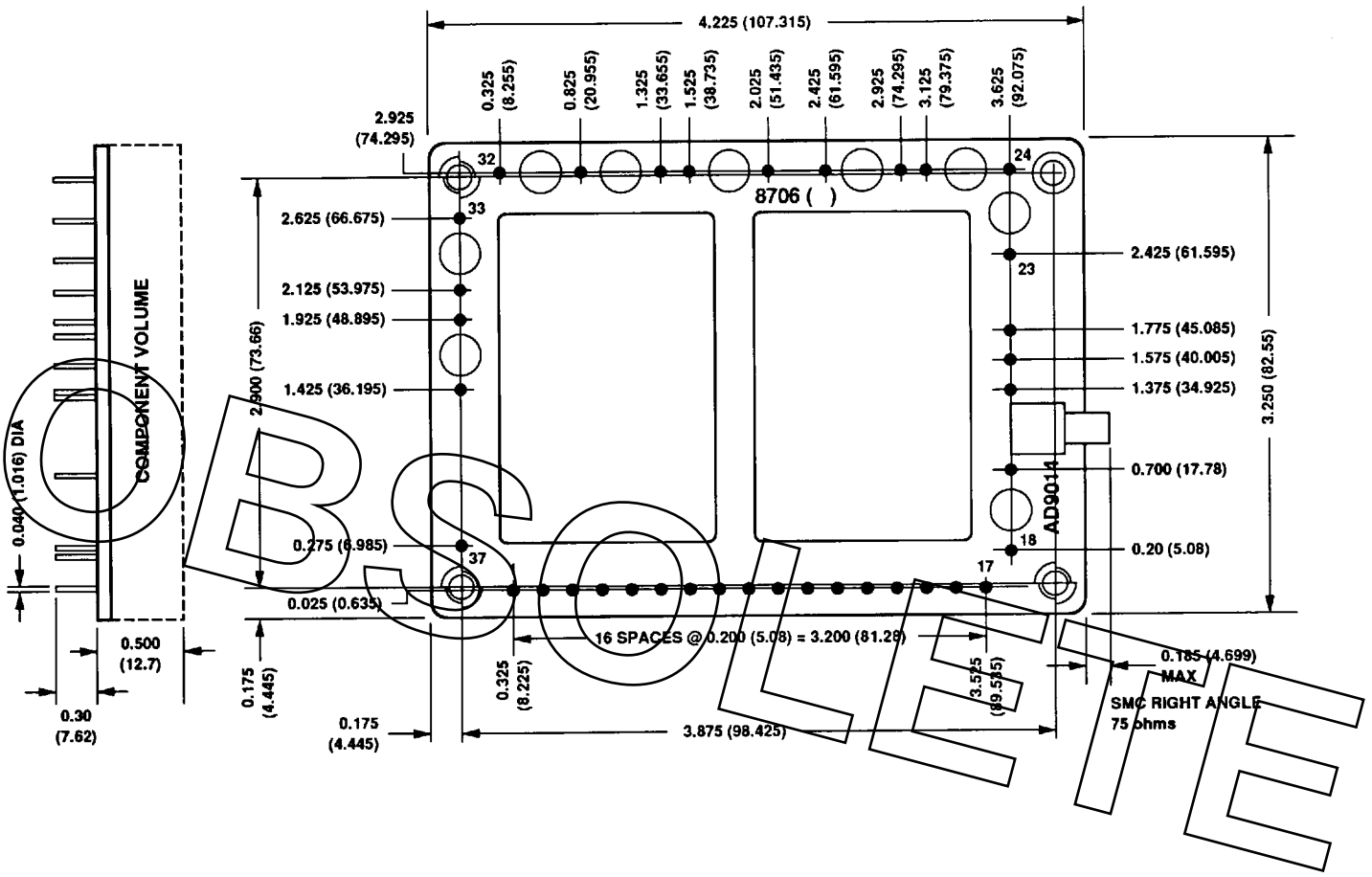






OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



C1459–21–10/90

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