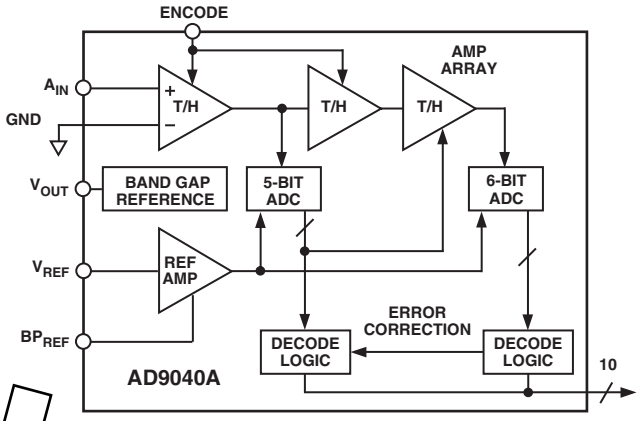
10-Bit 40 MSPS A/D Converter

AD9040A

FEATURES
Low Power: 940 mW
53 dB SNR @ 10 MHz A_{IN}
On-Chip Track-and-Hold, Reference
CMOS Compatible
2 V p-p Analog Input
Fully Characterized Dynamic Performance

APPLICATIONS
Ultrasound Medical Imaging
Digital Oscilloscopes
Professional Video
Digital Communications
Advanced Television (MUSE Decoders)
Instrumentation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9040A is a complete 10-bit monolithic sampling analog-to-digital converter (ADC) with on-board track-and-hold (T/H) and reference. The unit is designed for low cost, high performance applications and requires only an encode signal to achieve 40 MSPS sample rates with 10-bit resolution.

Digital inputs and outputs are CMOS compatible; the analog input requires a signal of 2 V p-p amplitude. The two-step architecture used in the AD9040A is optimized to provide the best dynamic performance available while maintaining low power requirements of only 940 mW typically; maximum dissipation is 1.1 W at 40 MSPS.

The signal-to-noise ratio (SNR), including harmonics, is 53 dB, or 8.5 ENOB, when sampling an analog input of 10.3 MHz at 40 MSPS. Competitive devices perform at less than 7.5 ENOB and require external references and larger input signals.

The AD9040A A/D converter is available in either a 28-lead PDIP or a 28-lead SOIC package. The two models operate over a commercial temperature range of 0°C to 70°C. Contact the factory regarding availability of ceramic military temperature range devices.

PRODUCT HIGHLIGHTS

1. CMOS compatible logic for direct interface to ASICs.
2. On-board track-and-hold provides excellent high frequency performance on analog inputs, critical for communications and medical imaging applications.
3. High input impedance and 2 V p-p input range reduce need for external amplifiers.
4. Easy to use; no cumbersome external voltage references required, allowing denser packing of ADCs for multichannel applications.
5. Available in 28-lead PDIP and SOIC packages.
6. Evaluation board includes AD9040AJR, reconstruction DAC, and latches. Space is available near the analog input and digital outputs of the converter for additional circuits. Order as part number AD9040A/PCB (schematic shown in data sheet).

REV. D

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AD9040A–SPECIFICATIONS

($+V_S = V_D = +5$ V; $-V_S = -5$ V; internal reference: Encode = 40.5 MSPS, unless otherwise noted.)

Parameter (Conditions)	Temp	Test Level	AD9040AJN/AD9040AJR Min	Typ	Max	Unit
RESOLUTION				10		Bits
DC ACCURACY						
Differential Nonlinearity	25°C	I		1.0	2.0	LSB
	Full	VI			2.5	LSB
Integral Nonlinearity	25°C	I		1.0	2.25	LSB
	Full	VI			2.5	LSB
No Missing Codes	Full	VI		Guaranteed		
Gain Error	25°C	I		±0.5	±1.5	% FS
	Full	VI			±2	% FS
Gain Temperature Coefficient[1]	Full	V		±70		ppm/°C
ANALOG INPUT						
Input Voltage Range	25°C	V		2		V p-p
Input Offset Voltage	25°C	I		±2	±25	mV
	Full	VI			±30	mV
Input Bias Current	25°C	I		7	15	µA
	Full	VI			25	µA
Input Resistance	25°C	I	200	350		kΩ
Input Capacitance	25°C	V		5		pF
Analog Bandwidth	25°C	V		48		MHz
BAND GAP REFERENCE						
Output Voltage	Full	VI	2.4		2.6	V
Temperature Coefficient[1]	Full	V		±40		ppm/°C
SWITCHING PERFORMANCE						
Maximum Conversion Rate	25°C	I	40			MSPS
Minimum Conversion Rate	25°C	IV		2	10	MSPS
Aperture Delay (t_A)	25°C	V		1.9		ns
Aperture Uncertainty (Jitter)	25°C	V		7		ps, rms
Output Propagation Delay (t_{PD})[2]	25°C	I	7.5	10	12	ns
	Full	IV	6		14	ns
DYNAMIC PERFORMANCE[3]						
Transient Response	25°C	V		25		ns
Overvoltage Recovery Time	25°C	V		40		ns
Signal-to-Noise Ratio[4]						
f_{IN} = 2.3 MHz	25°C	I	48	54		dB
f_{IN} = 10.3 MHz	25°C	I	47	53		dB
Signal-to-Noise Ratio[4] (Without Harmonics)						
f_{IN} = 2.3 MHz	25°C	I	49	55		dB
f_{IN} = 10.3 MHz	25°C	I	48	54		dB
Signal-to-Noise Ratio[4, 5]						
f_{IN} = 2.3 MHz	25°C	I		56		dB
f_{IN} = 10.3 MHz	25°C	I		55		dB
Signal-to-Noise Ratio[4, 5] (Without Harmonics)						
f_{IN} = 2.3 MHz	25°C	I		57		dB
f_{IN} = 10.3 MHz	25°C	I		56		dB
Second Harmonic Distortion						
f_{IN} = 2.3 MHz	25°C	I	56	67		dBc
f_{IN} = 10.3 MHz	25°C	I	56	65		dBc
Third Harmonic Distortion						
f_{IN} = 2.3 MHz	25°C	I	57	73		dBc
f_{IN} = 10.3 MHz	25°C	I	57	70		dBc
Two-Tone Intermodulation[6] Distortion Rejections	25°C	V		62		dBc
Differential Phase	25°C	III		0.15	0.5	Degrees
Differential Gain	25°C	III		0.25	1.0	%

Parameter (Conditions)	Temp	Test Level	AD9040AJN/AD9040AJR Min	Typ	Max	Unit
ENCODE INPUT						
Logic 1 Voltage	Full	VI	4.0			V
Logic 0 Voltage	Full	VI			1.0	V
Logic 1 Current	Full	VI			±1	μA
Logic 0 Current	Full	VI			±1	μA
Input Capacitance	25°C	V		14		pF
Encode Pulsewidth (High) (t_{EH})[7]	25°C	IV	10		100	ns
Encode Pulsewidth (Low) (t_{EL})[7]	25°C	IV	10		100	ns
DIGITAL OUTPUTS						
Logic 1 Voltage	Full	VI	4.95			V
Logic 0 Voltage	Full	VI			0.05	V
Output Coding				Offset Binary		
POWER SUPPLY						
V_D Supply Current	Full	VI		13	20	mA
$+V_S$ Supply Current	Full	VI		89	110	mA
$-V_S$ Supply Current	Full	VI		87	105	mA
Power Dissipation	Full	VI		0.94	1.2	W
Power Supply Rejection Ratio (PSRR)[8]	25°C	I			±15	mV/V

NOTES
[1]Gain temperature coefficient is for a converter using internal reference; temperature coefficient is for band gap reference only.
[2]Output propagation delay (t_{PD}) is measured from the 50% point of the falling edge of the encode command to the min/max voltage levels of the digital outputs with 10 pF maximum loads.
[3]Minimum values apply to AD9040AJR only.
[4]RMS signal to rms noise with analog input signal 1 dB below full scale at specified frequency.
[5]Encode = 32 MSPS.
[6]Third order intermodulation measured with analog input frequencies of 2.3 MHz and 2.4 MHz at 7 dB below full scale.
[7]For rated performance at 40 MSPS, duty cycle of encode command should be 50% ±10%.
[8]Measured as the ratio of the change in offset voltage for a 5% change in $+V_S$ or $-V_S$.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

I 100% production tested.
II 100% production tested at 25°C and sample tested at specified temperatures. AC testing done on sample basis.
III Sample tested only.
IV Parameter is guaranteed by design and characterization testing.
V Parameter is a typical value only.
VI All devices are 100% production tested at 25°C. 100% production tested at temperature extremes for military temperature devices; guaranteed by design and characterization testing for industrial devices.

ABSOLUTE MAXIMUM RATINGS[1]

$\pm V_S$	±7 V
V_D	7 V
Analog Inputs	$-V_S$ to $+V_S$
Digital Inputs	0 V to $+V_S$
V_{REF} Input	0 V to $+V_S$
Digital Output Current	20 mA
Operating Temperature	
AD9040AJN/AD9040AJR	0°C to 70°C
Storage Temperature	–65°C to +150°C
Maximum Junction Temperature[2] (JN/JR Suffixes)	150°C
Lead Soldering Temp (10 sec)	300°C

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

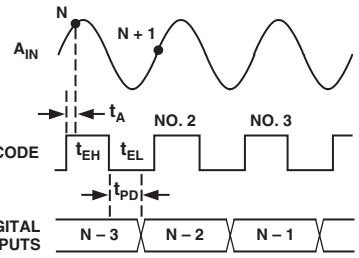
[2]Typical thermal impedances (parts soldered to board):
N Package (PDIP): θ_{JA} = 42°C/W; θ_{JC} = 10°C/W.
R Package (SOIC): θ_{JA} = 47°C/W; θ_{JC} = 10°C/W.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9040AJN	0°C to 70°C	28-Lead PDIP	N-28
AD9040AJR	0°C to 70°C	28-Lead SOIC Package	R-28
AD9040AJR-REEL	0°C to 70°C	28-Lead SOIC Package	R-28

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9040A features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

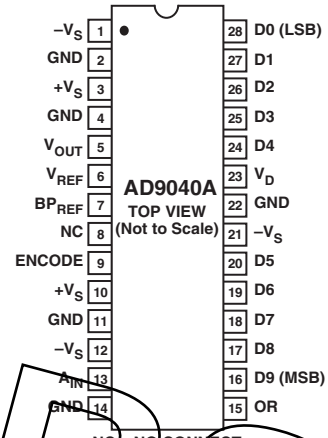


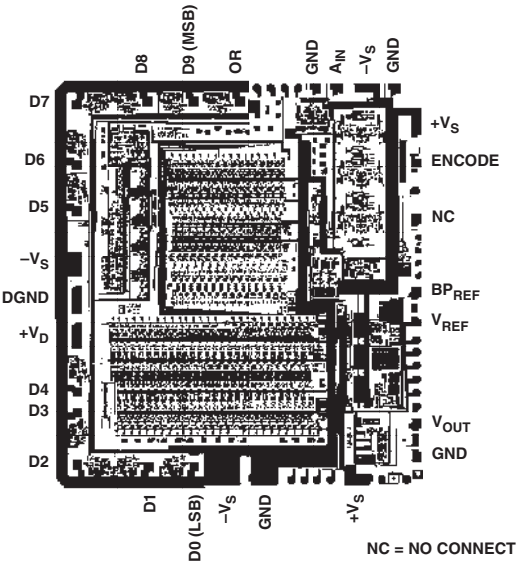
SYMBOL	DESCRIPTION	MIN	TYP	MAX
t_A	APERTURE DELAY		1.9ns	
t_{EH}	PULSEWIDTH HIGH	10ns		100ns
t_{EL}	PULSEWIDTH LOW	10ns		100ns
t_{PD}	OUTPUT PROP DELAY	7.5ns	10ns	12ns

Figure 1. Timing Diagram

PIN CONFIGURATION

PDIP and SOIC





DIE LAYOUT AND MECHANICAL INFORMATION

Die Dimensions	204 mils × 185 mils × 21 (±1) mils
Pad Dimensions	4 mils × 4 mils
Metalization	Aluminum
Backing	None
Substrate Potential	V_S
Transistor Count	5,070
Passivation	Oxynitride
Die Attach (JN/JR)	Epoxy
Bond Wire (JN/JR)	Gold

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1, 12, 21	$-V_S$	5 V Power Supply.
2, 4, 11, 14, 22	GND	Ground.
3, 10	$+V_S$	Analog 5 V Power Supply.
5	V_{OUT}	Internal Band Gap Voltage Reference (Nominally 2.5 V).
6	V_{REF}	Noninverting Input to Reference Amplifier. Voltage reference for ADC is connected here.
7	BP_{REF}	External Connection for (0.1 μF) Reference Bypass Capacitor.
8	NC	No Connection Internally.
9	ENCODE	Encode Clock Input to ADC. Internal track-and-hold placed in hold mode (ADC is encoding) on rising edge.
13	A_{IN}	Noninverting Input to Track-and-Hold Amplifier.
15	OR	Out-of-Range Condition Output. Active high when analog input exceeds input range of ADC by 1 LSB ($< F_S - 1$ LSB or $> +F_S + 1$ LSB).
16	D9 (MSB)	Most Significant Bit of ADC Output; TTL/CMOS Compatible.
17–20	D8–D5	Digital Output Bits of ADC; TTL/CMOS Compatible.
23	V_D	Digital +5 V Power Supply.
24–27	D4–D1	Digital Output Bits of ADC; TTL/CMOS Compatible.
28	D0 (LSB)	Least Significant Bit of ADC Output; TTL/CMOS Compatible.

DEFINITIONS OF SPECIFICATIONS

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between the rising edge of the encode command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Differential Gain
The percentage of amplitude change of a small high frequency sine wave (3.58 MHz) superimposed on a low frequency signal (15.734 kHz).

Differential Nonlinearity
The deviation of any code from an ideal 1 LSB step.

Differential Phase
The phase change of a small high frequency sine wave (3.58 MHz) superimposed on a low frequency signal (15.734 kHz).

Harmonic Distortion
The rms value of the fundamental divided by the rms value of the harmonic.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least square curve fit.

Minimum Conversion Rate
The encode rate at which the SNR of the lowest analog signal frequency tested drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate
The encode rate at which parametric testing is performed.

Output Propagation Delay
The delay between the 50% point of the falling edge of the encode command and the 1 V/4 V points of output data.

Overvoltage Recovery Time
The amount of time required for the converter to recover to 10-bit accuracy after an analog input signal 150% of full scale is reduced to the full-scale range of the converter.

Power Supply Rejection Ratio (PSRR)
The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise Ratio (SNR)
The ratio of the rms signal amplitude to the rms value of noise, which is defined as the sum of all other spectral components, including harmonics but excluding dc, with an analog input signal 1 dB below full scale.

Signal-to-Noise Ratio (Without Harmonics)
The ratio of the rms signal amplitude to the rms value of noise, which is defined as the sum of all other spectral components, excluding the first eight harmonics and dc, with an analog input signal 1 dB below full scale.

Transient Response
The time required for the converter to achieve 10-bit accuracy when a step function is applied to the analog input.

Two-Tone Intermodulation Distortion (IMD) Rejection
The ratio of the power of either of the two input signals to the power of the strongest third order IMD signal.

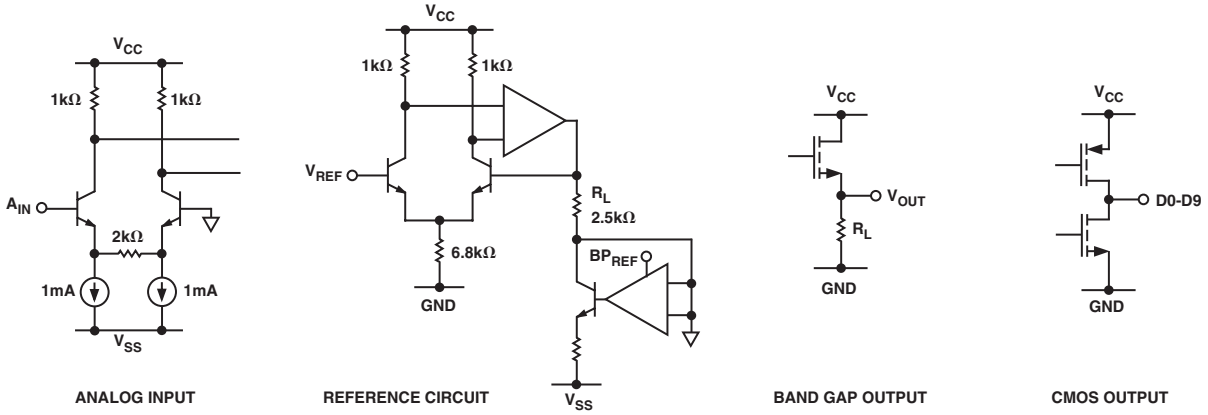
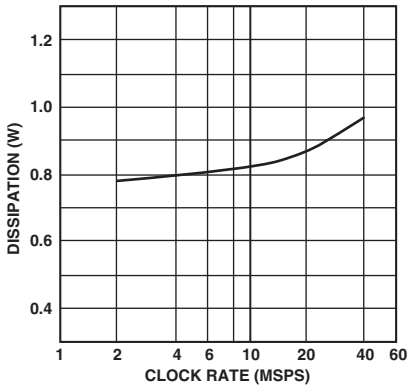
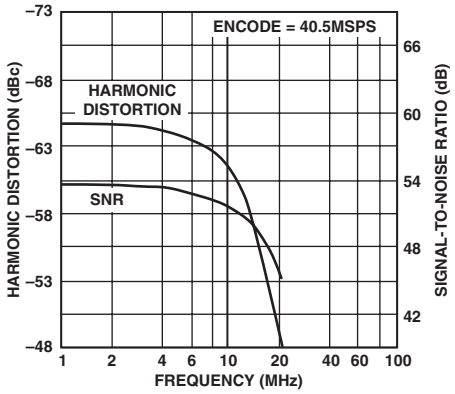


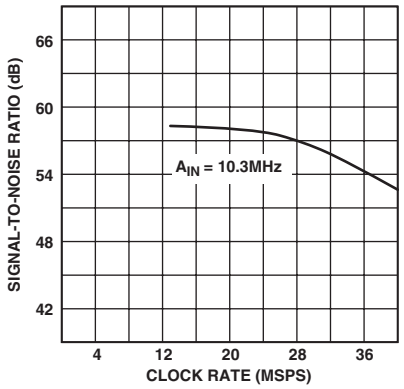
Figure 2. Equivalent Circuits



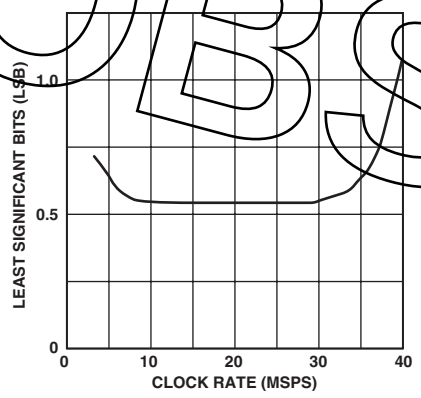
TPC 1. Power Dissipation vs. Clock Rate



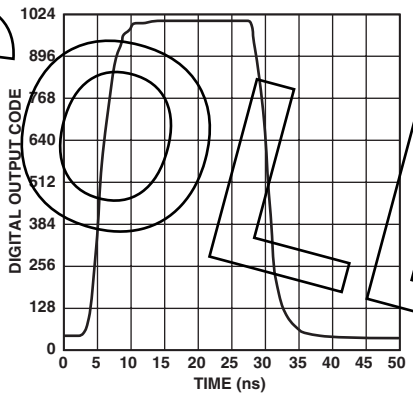
TPC 2. Harmonic Distortion and SNR vs. Analog Input



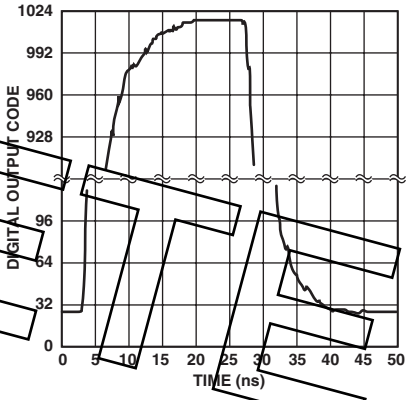
TPC 3. SNR vs. Clock Rate



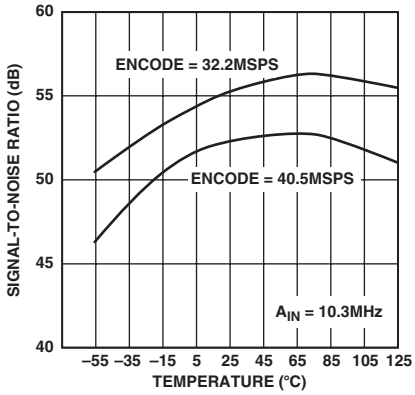
TPC 4. Differential Nonlinearity vs. Clock Rate



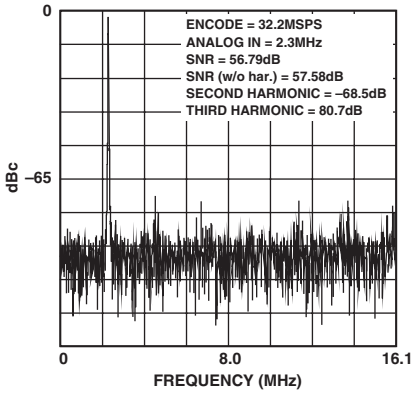
TPC 5. Transient Response



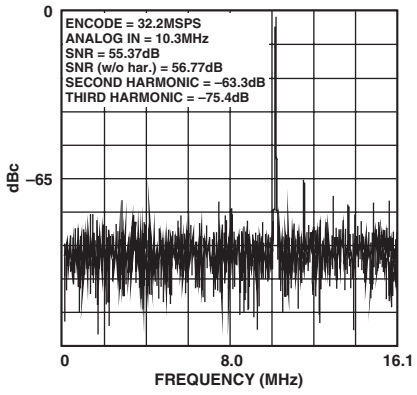
TPC 6. Transient Response (Expanded View)



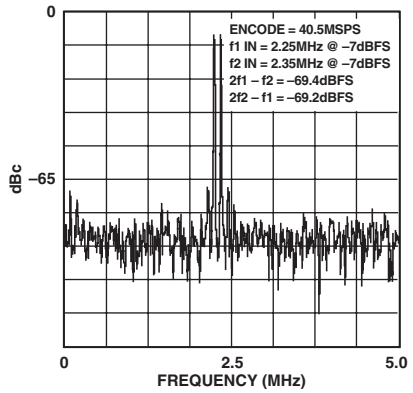
TPC 7. SNR vs. Temperature



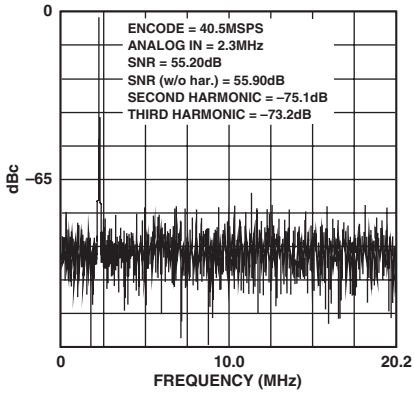
TPC 8. FFT Response



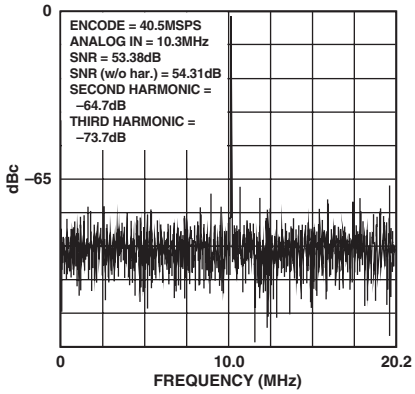
TPC 9. FFT Response



TPC 10. FFT Response



TPC 11. FFT Response



TPC 12. FFT Response

THEORY OF OPERATION

The AD9040A employs subranging architecture and digital error correction. This combination of design techniques ensures true 10-bit accuracy at the digital outputs of the converter.

At the input, the analog signal is applied to a track-and-hold (T/H) that holds the analog value that is present when the unit is strobed with an encode command. The conversion process begins on the rising edge of this pulse, which should have a 50% (±10%) duty cycle. The minimum encode rate of the AD9040A is 10 MSPS because of the use of three internal track-and-hold devices.

The held analog value of the first track-and-hold is applied to a 5-bit flash converter and a pair of internal track-and-hold devices (shown in the Functional Block Diagram as a single unit). The track-and-hold devices pipeline the analog signal to the amplifier array through a residue ladder and switching circuit while the 5-bit flash converter resolves the most significant bits (MSB) of the held analog voltage.

When the 5-bit flash converter has completed its cycle, its output activates 1 of 32 ladder switches; these in turn cause the correct residue signal to be applied to the error amplifier array.

The output of the error amplifier is applied to a 6-bit flash converter whose output supplies the five least significant bits (LSB) of the digital output along with one bit of error correction for the 5-bit main range converter.

Decode logic aligns the data from the two converters and presents the result as a 10-bit parallel digital word. The output stage of the AD9040A is CMOS. Output data are strobed on the trailing edge of the encode command.

The full-scale range of the AD9040A is determined by the reference voltage applied to the V_{REF} (Pin 6) input. This voltage sets the internal flash and residue ladder voltage drops; these establish the value of the LSB. Because of headroom restraints, the full-scale range cannot be increased by applying a higher than specified reference voltage. Conversely, a lower reference voltage will reduce the full-scale range of the converter but will also decrease its performance. An internal band gap reference voltage of 2.5 V is provided to assure optimum performance over the operating temperature range.

USING THE AD9040A

Timing

The duty cycle of the encode clock for the AD9040A is critical for obtaining the rated performance of the ADC. Internal pulsewidths within the track-and-hold are established by the encode command pulsewidths; to ensure rated performance, the duty cycle should be held at 50%. Duty cycle variations of less than ±10% will cause no degradation in performance.

Operation at encode rates less than 10 MSPS is not recommended. The internal track-and-hold saturates, causing erroneous conversions. This track-and-hold saturation precludes clocking the AD9040A in burst mode. The 50% duty cycle must be maintained even for sample rates down to 10 MSPS.

The AD9040A provides latched data outputs, with 2 1/2 pipeline delays. Data outputs are available one propagation delay (t_{PD}) after the falling edge of the encode command (see Figure 1). The length of the output data lines and the loads placed on them should be minimized to reduce transients within the AD9040A; these transients can detract from the converter's dynamic performance.

Voltage Reference

A stable voltage reference is required to establish the 2 V p-p range of the AD9040A. There are two options for creating this reference. The easiest and least expensive way to implement it is to use the (2.5 V) band gap voltage reference which is internal to the ADC. Figure 3 illustrates the connections for using the internal reference. The internal reference has 500 μA of extra drive current that can be used for other circuits.

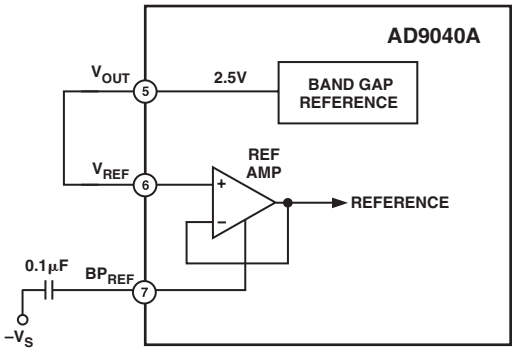


Figure 3. Using Internal Reference

Some applications may require greater accuracy, improved temperature performance, or adjustment of the gain (input range) of the AD9040A, which cannot be obtained by using the internal reference. For these applications, an external 2.5 V reference can be used, as shown in Figure 4. The V_{REF} input requires 5 μA of drive current.

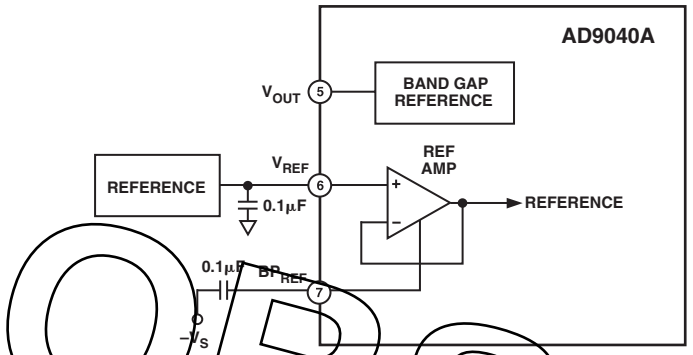


Figure 4. Using External Reference

In applications using multiple AD9040As, slaving the reference inputs to a single reference output will improve gain tracking among the ADCs, as shown in Figure 5.

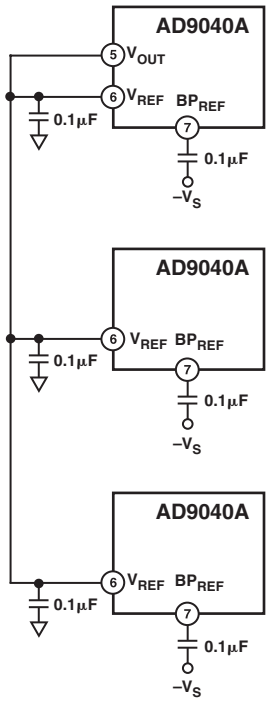


Figure 5. Slaving Multiple AD9040As to a Single Internal Reference

In the Specifications table, the gain temperature coefficient parameter under dc accuracy applies to the ADC when the internal reference is being used. If an external reference is used, its temperature coefficient must be taken into account to determine overall temperature performance.

The input range can be varied by adjusting the reference voltage applied to the AD9040A. By decreasing the reference voltage, the gain can be reduced approximately 10% with no degradation in performance. Increasing the reference voltage increases the gain, but for proper operation, the reference voltage should not exceed 2.6 V.

Time-Gain Control ADC

Ultrasound and sonar systems require an increase in gain versus time. This allows the system to correct for attenuation of return pulses. Figure 6 shows the AD600/AD602 amplifier and the AD9040A ADC configured as a time-gain control analog-to-digital converter. The control voltage ramps from –625 mV to +625 mV, permitting 40 dB of gain-control range. The voltage used for gain control can be either a linear ramp or the output of a voltage-output DAC, such as the AD7242.

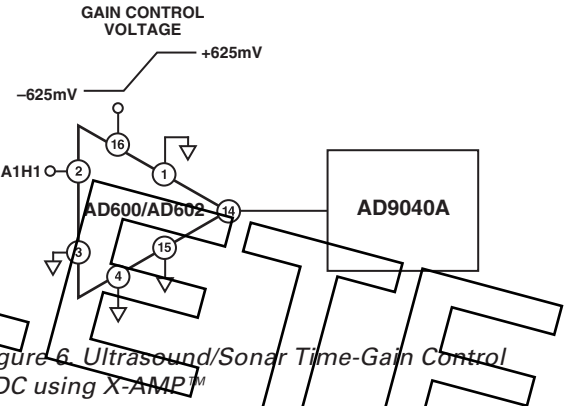


Figure 6. Ultrasound/Sonar Time-Gain Control ADC using X-AMP™

Transient Response

Figure 7 illustrates the method for evaluating ADC transient performance. Two synthesizers are locked in synchronization but tuned to frequencies that are slightly offset from a 2 to 1 submultiple.

One synthesizer clocks a flat pulse network at a frequency of 19.9609375 MHz to provide the analog input signal; the other synthesizer output is shaped to provide a CMOS 40 MHz sampling clock. At the output of the AD9040A, output data reflects an interleaved alias of the input pulse. The repetitive sampling allows the measurement of ADC transient response as shown in the TPCs in this data sheet.

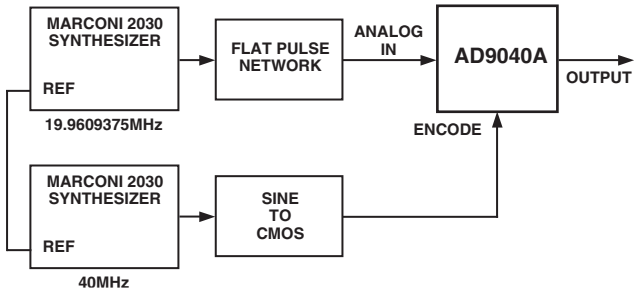


Figure 7. Transient Response Test

Layout Information

Preserving the accuracy and dynamic performance of the AD9040A requires that designers pay special attention to the layout of the printed circuit board.

Analog paths should be kept as short as possible and be properly terminated to avoid reflections. The analog input and reference voltage connections should be kept away from digital signal paths; this reduces the amount of digital switching noise that is capacitively coupled into the analog section. Digital signal paths should also be kept short and run lengths should be matched to avoid propagation delay mismatch. The AD9040A digital outputs should be buffered or latched close to the device (<2 cm). This prevents load transients, which may feed back into the device.

In high speed circuits, layout of the ground is critical. A single, low impedance ground plane on the component side of the board is recommended. Power supplies should be capacitively coupled to the ground plane with high quality chip capacitors to reduce noise in the circuit. Multilayer boards allow designers to lay out signal traces without interrupting the ground plane and provide low impedance ground planes. In systems with dedicated analog and digital grounds, all grounds of the AD9040A should be connected to the analog ground plane.

The power supplies of the AD9040A should be isolated from the supplies used for external devices; this reduces the amount of noise coupled into the ADC. The digital 5 V connection of the device (V_D, Pin 23) powers the digital outputs and should be connected to the same supply as $+V_S$ (Pins 3 and 10). Connecting V_D to a system digital supply may couple noise into the device. Sockets limit dynamic performance and are not recommended for use with the AD9040A.

EVALUATION BOARD

The evaluation board for the AD9040A (AD9040A/PCB) provides an easy and flexible method for evaluating the ADC's performance without (or prior to) developing a user-specific printed circuit board. The two-sided board includes a reconstruction DAC and digital output interface and uses the layout and applications suggestions outlined above. It is available from Analog Devices at nominal cost.

Generous space is provided near the analog input and digital outputs to support any additional signal processing components the user may wish to add. This prototyping area includes through-holes with 100-mil centers to support a variety of component additions.

Input/Output/Supply Information

Power supply, analog input, clock connections, and reconstructed output (RC OUTPUT) are identified by labels on the evaluation board. Operation of the evaluation board should conform to the following characteristics.

Table I. Evaluation Board Characteristics

Parameter	Typical	Unit
Supply Current		
+5 V	250	mA
–5.2 V	300	mA
A_{IN}		
Impedance	51	Ω
Voltage Range	±1.0	V
CLOCK		
Impedance	51	Ω
Frequency	40	MSPS
RC OUTPUT		
Impedance	51	Ω
Voltage Range	0 V to –1 V	V

Analog Input

Analog input signals can be fed directly into the device under test input (A_{IN}). The A_{IN} input is terminated at the device with a 51 Ω resistor.

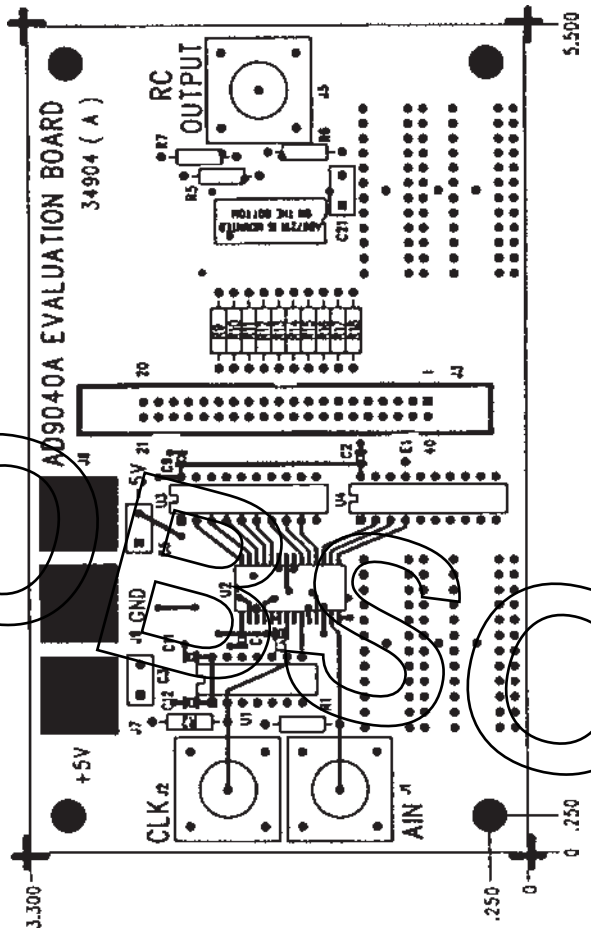


Figure 8. PCB Top View

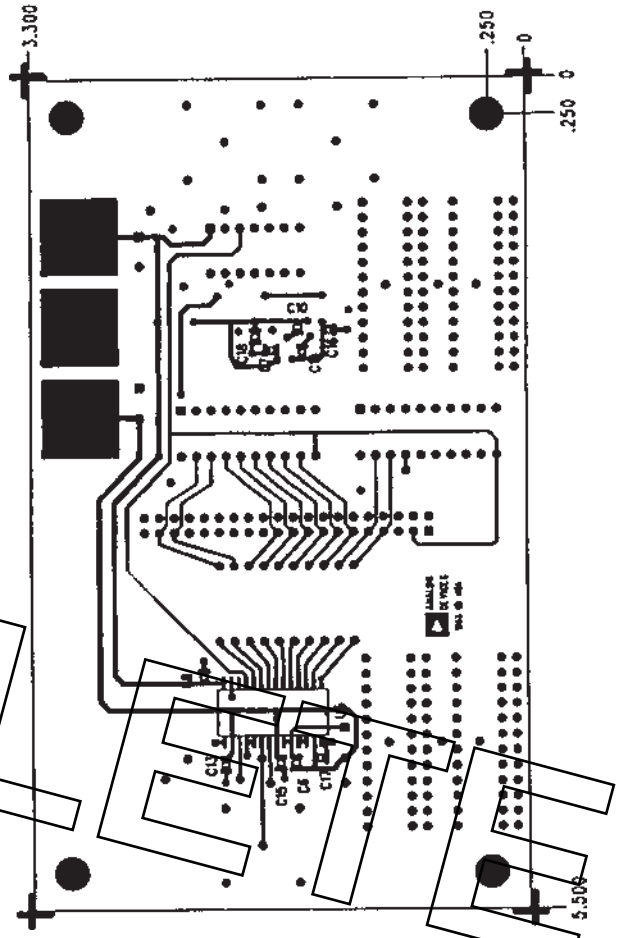


Figure 9. PCB Bottom View

DAC Reconstruction

The AD9040A evaluation board provides an onboard AD9721 reconstruction DAC for observing the digitized analog input signal. The AD9721 is terminated into 51 Ω to provide a 1 V p-p signal at the output (RC OUTPUT).

Output Data

The output data bits are latched with a CMOS 74AC574 that drives a 40-pin connector (AMP p/n 102153-9). The data and clock signals are available on the connector per the pin assignments shown on the schematic of the evaluation board (see Figure 10). Output data are available on the falling edge of the clock.

Table II. Digital Coding

Analog Input	Voltage Level	Out-of-Range	Digital Output
			MSB . . . LSB
+1.002 V	*Positive Full Scale* + 1 *LSB*	1	1111111111
+1 V	*Positive Full Scale*	0	1111111111
	Full Scale – 1 *LSB*	0	1111111110
+1/2 V	*Positive* 1/2 *Scale*	0	1100000000
	1/2 *Scale* – 1 *LSB*	0	1011111111
0 V	Bipolar Zero	0	10000000000
		0	01111111111
–1/2 V	1/2 *Scale* + 1 *LSB*	0	0100000000
	Negative 1/2 *Scale*	0	0011111111
–1 V	*Full Scale* + 1 *LSB*	0	0000000001
	Negative Full Scale	0	0000000000
–1.002 V	*Negative Full Scale* – 1 *LSB*	1	0000000000

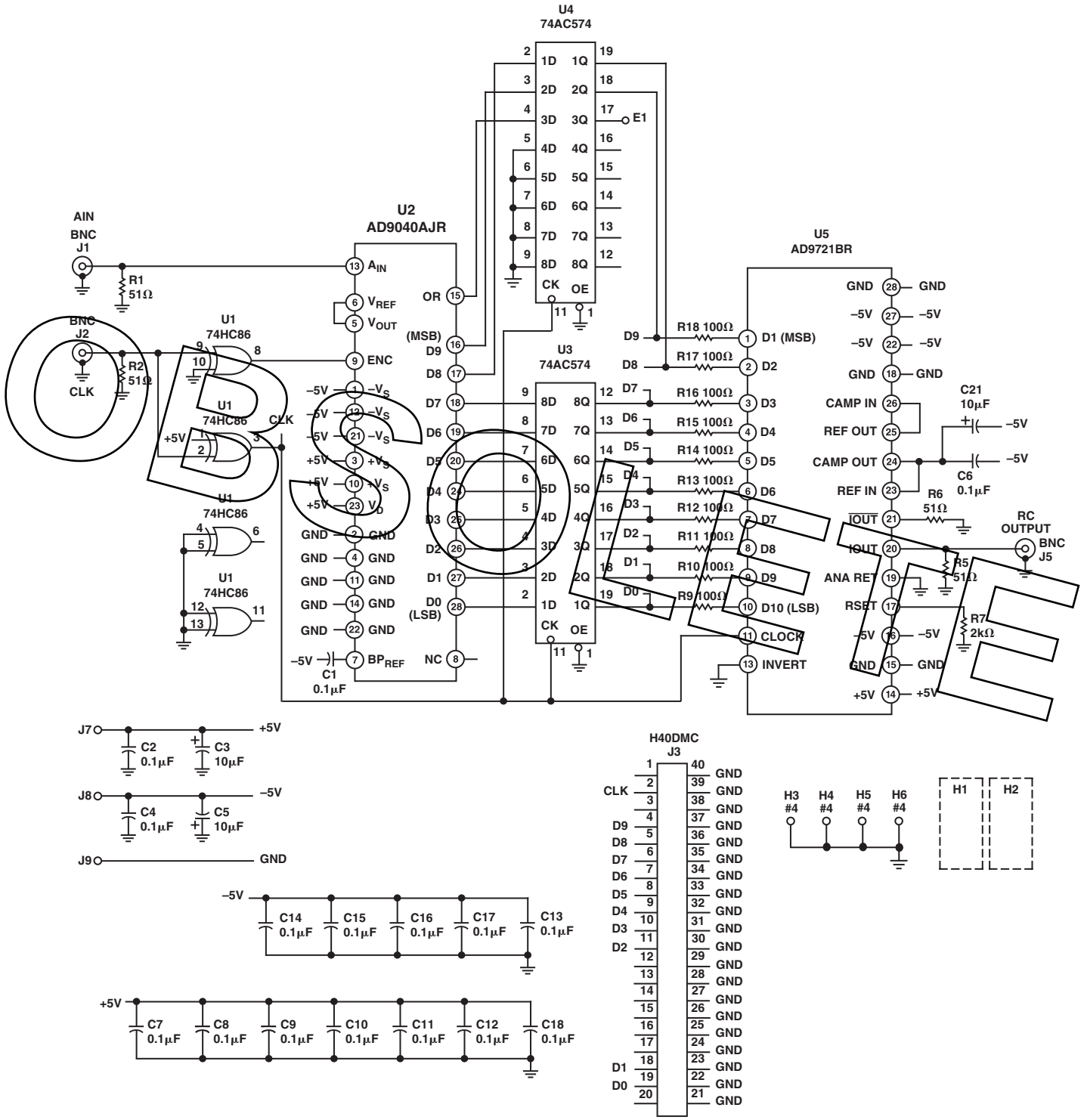
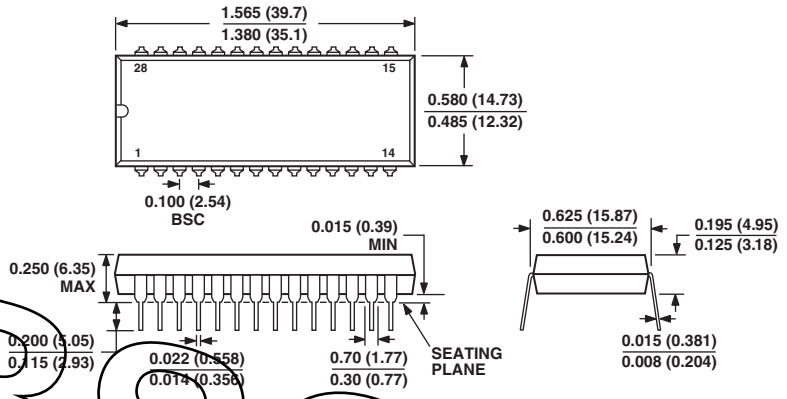


Figure 10. PCB Schematic

OUTLINE DIMENSIONS

28-Lead Plastic Dual In-Line Package [PDIP]
(N-28)

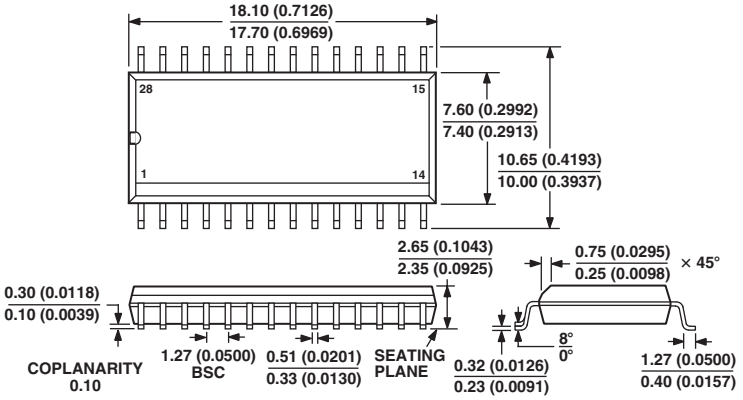
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-011AB
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

28-Lead Standard Small Outline Package [SOIC]
Wide Body
(R-28)

Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-013AE
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Revision History

Location	Page
5/03—Data Sheet changed from REV. C to REV. D.	
Edits to SPECIFICATIONS	2
Edits to ORDERING GUIDE	4
Updated OUTLINE DIMENSIONS	14
2/02—Data Sheet changed from REV. B to REV. C.	
Edits to Specifications	2

C00553–0–5/03(D)