AN-1214
APPLICATION NOTE

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

High CMRR Circuit for Converting Wideband Complementary DAC Output to Single-Ended Without Precision Resistors

CIRCUIT FUNCTION AND BENEFITS

Traditional methods for converting wideband DAC complementary current outputs to a single-ended signal are to either use a center-tapped transformer or a single op amp in a differential-to-single-ended configuration. However, the transformer low frequency nonlinearities may limit its use near dc; and the operational amplifier approach requires closely matched resistors to provide dc common-mode rejection, load impedance, and gain matching between the complementary DAC outputs. Errors in the matching will produce errors at the final output. This circuit uses the AD8130 differential receiver amplifier to generate a simple differential-to-single-ended translation without the use of expensive precision resistors, thereby providing higher accuracy with fewer components.

An added benefit of the AD8130 is its industry-leading ac common-mode rejection (70 dB at 10 MHz). This feature can be used to reject noise between the DAC digital ground plane and the receiver analog ground plane—a common problem in this type of mixed-signal application.

CIRCUIT DESCRIPTION

Table 1. Devices Connected/Referenced

Product	Description
AD8130	Differential receiver amplifier
AD9117	Dual, low power, 14-bit, 125 MSPS DAC

This circuit utilizes the AD9117, a 20 mA complementary current output, low power, 14-bit, 125 MSPS, dual TxDAC® digital-to-analog converter, and the AD8130, a low cost 270 MHz differential receiver amplifier.

The AD9117 full–scale output current can be adjusted from 4 mA to 20 mA by changing the resistor value between FSADJI or FSADJQ and ground. In this example, the internal resistor option is enabled and set to 1.6 kΩ to provide 20 mA maximum current output. This configuration requires writing 0b10100000 to register IRSET and QRSET of the AD9117. The complementary current outputs are terminated with external 49.9 Ω

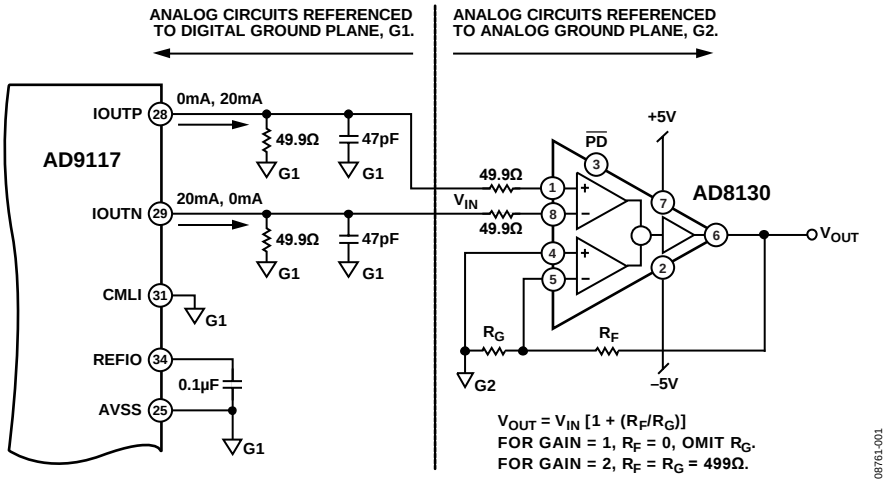

Figure 1. High Speed TxDAC Differential-to-Single-Ended Conversion Using AD8130 Receiver (Simplified Schematic: All Connections and Decoupling Not Shown)

resistors to create a differential voltage. With a full-scale digital input swing, the voltage developed across each of these resistors is 180° out of phase with respect to each other and varies between 0 V to 1 V, thereby providing a peak-to-peak differential output voltage of 2 V. A 47 pF capacitor is placed in parallel with these load resistors to provide a 68 MHz first order reconstruction filter and attenuate images outside the Nyquist bandwidth. The two 49.9 Ω resistors in series with the AD8130 input pins improve the overall distortion performance of the circuit. The common-mode output pins, CMLI and CMLQ, can be used to provide additional offset but are not used in this example and are connected to ground.

The AD8130 is an ideal complementary product, since it has a large balanced input impedance allowing an easy conversion of the differential input into a single-ended format and has excellent ac common-mode rejection, as shown in Figure 2.

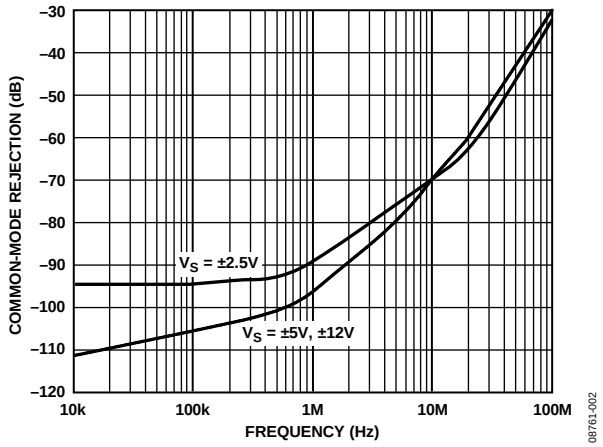

Figure 2. AD8130 Common-Mode Rejection

The AD8130 bandwidth is 270 MHz, which supports DAC output frequencies generated by the AD9117 up to about 40 MHz at the maximum update rate of 125 MSPS.

The AD8130 is set up in this example with a gain of 1 (R_F = 0, omit R_G). However, the gain can be adjusted by simply changing the ratio R_F/R_G. The power supply is set to ±5 V, but if additional swing is needed at the output, it can be increased up to ±12 V.

Headroom issues relating to the DAC and the op amp must be considered in this circuit for proper operation. The DAC output voltages need to be kept within their compliance range to avoid distortion introduced by the internal circuits. With the DAC V_{DD} = 3.3 V and V_{CM} = 0 V, the AD9117 outputs must be less than ±1 V, which is achieved by having 49.9 Ω loads resistors and a full-scale current of 20 mA. With a 1 kΩ load at the output of the amplifier, the AD8130 requires a supply voltage headroom of 1 V; therefore, the output swing cannot be more than ±4 V with ±5 V supplies.

Harmonic distortion is an important criteria in this design. Figure 3 and Figure 4 show measured 2nd and 3rd harmonic distortion of the total circuit (AD9117 + AD8130), as well as the harmonic distortion of the AD9117 by itself. Measurements were taken with the gain of the AD8130 set for 1 (R_F = 0, R_G omitted).

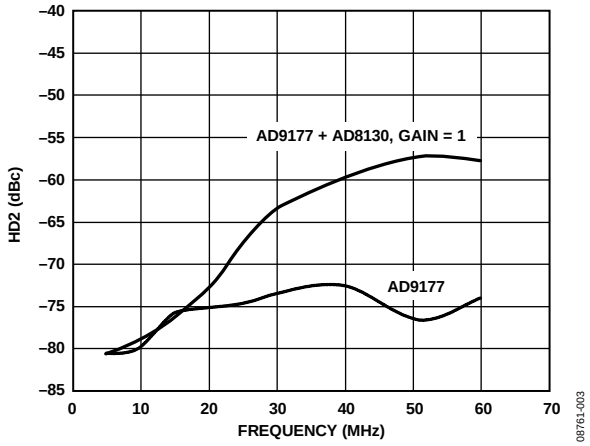

Figure 3. Second Harmonic Distortion of the Circuit, Gain = 1

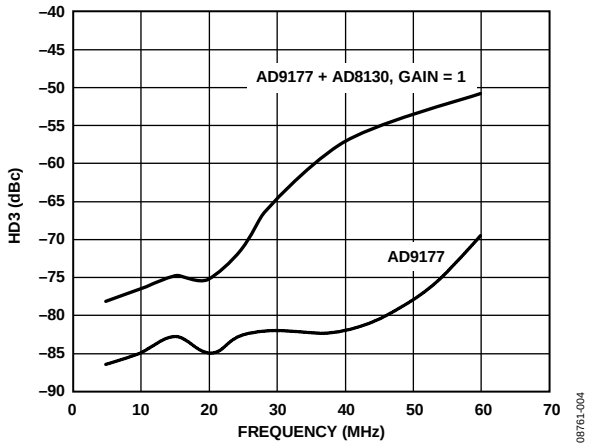

Figure 4. Third Harmonic Distortion of Circuit, Gain = 1

If faster rise/fall time is needed for time domain applications, the reconstruction filter cutoff frequency can to be increased by reducing the capacitor value. However, the 270 MHz bandwidth of the AD8130 limits the rise/fall time and settling time compared to the intrinsic performance of the AD9117 DACs. The circuit can still settle within 3 DAC updates at 125 MSPS.

The 0.1 µF capacitor decouples the AD9117 internal reference. A low inductance 0.1 µF ceramic decoupling capacitor (not shown in Figure 1) should be connected to V_{DD} very close to the AD9117.

The AD8130 output voltage offset can be adjusted to values different from 0 V and independently from the amplifer gain by connecting Pin 4 of the AD8130 and R_G (shown as G2 on Figure 2) to an offset voltage (V_{OFF}). In this configuration, V_{OFF} appears at the output with unity gain, while the AD8130 gain remains at $1+R_F/R_G$.

Excellent layout, grounding, and decoupling techniques must be utilized in order to achieve the desired performance from the circuits discussed in this note. As a minimum, a 4-layer PCB should be used with one ground plane layer, one power plane layer, and two signal layers.

All IC power pins must be decoupled to the ground plane with low inductance multilayer ceramic capacitors (MLCC) of 0.01 µF to 0.1 µF (this is not shown in the figures for simplicity). Follow the recommendations on the individual data sheets for the ICs and Tutorial MT-101.

COMMON VARIATIONS

Other TxDAC ICs, such as the AD9707, AD9717, AD9767, or AD9744, can be used in this configuration as long as the output frequency is kept within the bandwidth capability of the AD8130.

LEARN MORE

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND,"* Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

Data Sheets and Evaluation Boards

AD8130 Data Sheet

AD8130 Evaluation Board

AD9117 Data Sheet

AD9117 Evaluation Board

REVISION HISTORY

4/13—Rev. 0 to Rev. A

Changed Document Title from CN-0142 to AN-1214 ..... Universal

1/10—Revision 0: Initial Version

AN08761-0-4/13(A)