ANALOG DEVICES

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SINGLE EVENT EFFECTS TEST REPORT AD9246S

July 2016

Radiation Test Report	
Product:	AD9246S
Effective LET:	80 MeV-cm^2/mg
Fluence:	1E7 Ions/cm^2
Die Type:	58035330
Facilities:	Lawrence Berkeley National Laboratory
Tested:	April 2016

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Test Report for Single Event Effects (SEE) Testing of the AD9246S 14-Bit 125 MSPS Analog to Digital Converter

Customer PO Number: 45533851

Aeroflex RAD Job Number: 15-0727

Part Type Tested: 5962R1422701VXA, AD9246S 14-Bit 125 MSPS Analog to Digital Converter

Lot Number/Date Code: D/C: 1601, TL# E286400.2, REL#: E282619.

Quantity of Parts for Testing: 10 units received, SN# 2, 3, 4, 7, 8, 10, 11, 14, 36, and 39. Four parts for Single Event Latchup (SEL) testing, three parts for Single Event Upset/Transient (SEU/SET) testing.

Referenced Test Standard(s) and Applicable Documents: ASTM F1192 and EIA/JESD57.

Electrical Test Conditions: Supply currents were recorded before, during, and after heavy ion exposure and monitored for any change at one second intervals. The analog to digital conversion was monitored during heavy ion exposure for transients.

Bias Conditions: All devices-under-test (DUT) was biased during heavy ion irradiation using custom bias boards using the bias conditions listed in Section 2.1. See the figures and schematics in Appendix B for the details of the custom bias boards.

Test Software / Hardware: Custom VISA control and monitor software was used for all test operations. The test setup is shown in Figure 2-2 while the test equipment and calibration dates are shown in Appendix C, Table C-1.

Ion Energy and LET Ranges: Multiple ions from the 10 MeV/n ion beam with linear energy transfers (LETs) between 2 and 80 MeV-cm^2/mg were used for all testing. The 10 MeV/n Xe beam has a minimum range of 90 μm in silicon to the Bragg peak, the shortest range ion used for this test.

Heavy Ion Flux and Maximum Fluence Levels: Testing was conducted with ion fluxes between 10^2 and 10^5 ions/cm^2. For single event latch-up (SEL), the beam shutter was closed when either the DUT experiences a current latch-up or when the fluence has reached 10^7 ions/cm^2. For SEU/SET testing, the beam was shut off when 100 transients have been recorded or when the fluence reached 10^6 ions/cm^2.

Facility and Radiation Source: Lawrence Berkeley National Laboratories (LBNL) located in Berkeley, CA, using the 88" Cyclotron and the 10 MeV/n cocktail.

Irradiation Temperature: For SEU/SET testing, the devices were at ambient temperature of approximately 25°C. For SEL testing, the devices were tested at 125˚C ±5 ˚C.

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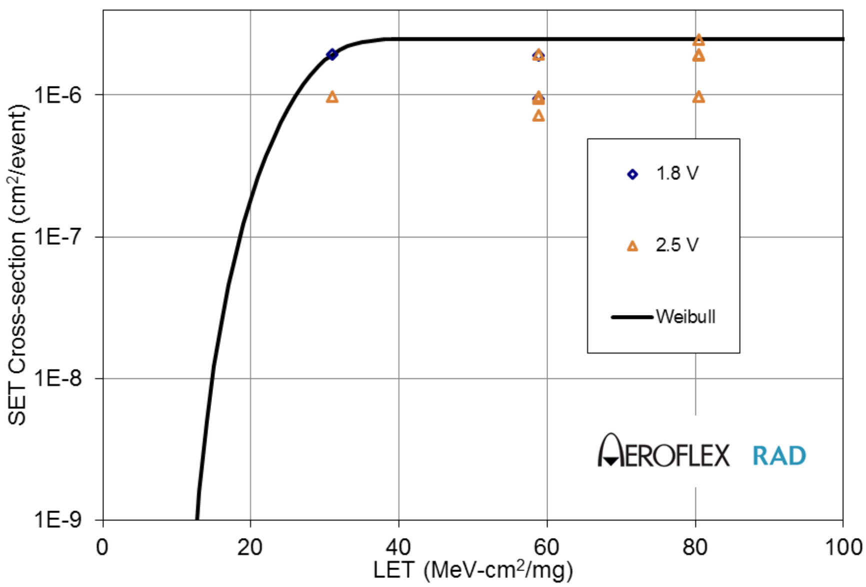
Executive Summary

The Analog Devices AD9246S was tested for Single Event Effects (SEE) with heavy ion irradiation on 4/1/2016 at Lawrence Berkeley National Laboratory.

No latchup (SEL) or other destructive SEE was observed at or below 80 MeV-cm^2/mg on any of the four devices tested at a temperature of 125°C with AVDD=1.9V and DRVDD = 3.6V.

No configuration register upsets (SEUs) were observed at or below 80 MeV-cm^2/mg under all conditions.

Maximum SET cross-section observed was < 2.5x10^{-6} cm^2/event at LET of > 80 MeV·cm^2/mg at ambient temperature of ~25°C) with AVDD=1.7V and DRVDD = 1.8 V and 2.5 V. The figure below shows the cross-section data and a Weibull curve with parameters Shape=4, Width=19, Saturation=2.5x10^{-6}, and Onset=10 for reference.



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1.0. Introduction and Test Objectives

It is well known that heavy ion exposure can cause temporary or permanent damage in electronic devices. The damage can occur through various mechanisms including SEL, single event burnout (SEB), single event gate rupture (SEGR) and single event dielectric rupture (SEDR). These SEEs can lead to system performance issues including degradation, disruption and destruction. Additionally SEU/SET effects, while not destructive in nature, can also have deleterious effects on systems. This test report details the SEL and SEU/SET testing performed on the AD9246S 14-Bit 125 MSPS Analog to Digital Converter for Analog Devices. The two test standards used to guide this testing are ASTM F1192 and EIA/JESD57. The AD9246S 14-Bit 125 MSPS Analog to Digital Converter will be irradiated at LBNL using the 10 MeV/n beam which will provide a sufficient range in silicon while meeting the LET requirements.

All DUTs were de-lidded prior to testing and all exposures took place from the top surface providing a distance to the active layer in silicon of approximately 5 to 10 µm. See the photograph in Appendix A for a sample of a de-lidded device-under-test.

The objective for SEL testing is to determine the threshold for latch-up in the device under worst case temperature and voltage conditions up to an LET of 80 MeV-cm^2/mg. For the SEL testing, the devices will be irradiated to a maximum fluence of 10^7 ions/cm^2 at a temperature of 125°C.

The objective of the SEU/SET test is to provide an expected transient event rate for a given LET and to also provide some statistics regarding the nature (magnitude and duration) of these transients. The transient cross section of the part will be generated for a minimum of five (5) LET's ranging between 2 MeV-cm^2/mg and 80 MeV-cm^2/mg until one of the following conditions have been met: a maximum fluence of 10^6 ions/cm^2, 100 events have been recorded, or a statistically significant number of events have been recorded (i.e. less than 100 events at low flux). The reason for the last measurement scenario (less than 100 events at low flux) is to minimize the possibility of counting single transient events multiple times since the duration of a single event is unknown. By recording a smaller but statistically significant number of events long exposure times at low fluxes can be avoided.

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2.0. Radiation Test Circuit, Setup, Parameters, Conditions, and Procedures

For SEE testing the AD9246S was configured as shown in Figure 2-1. The schematics for the test board are located in Appendix B. For SEU/SET testing, the noisy lower output bits of the AD9246S were masked. Any SEU/SET transients exceeding the mask level were captured.

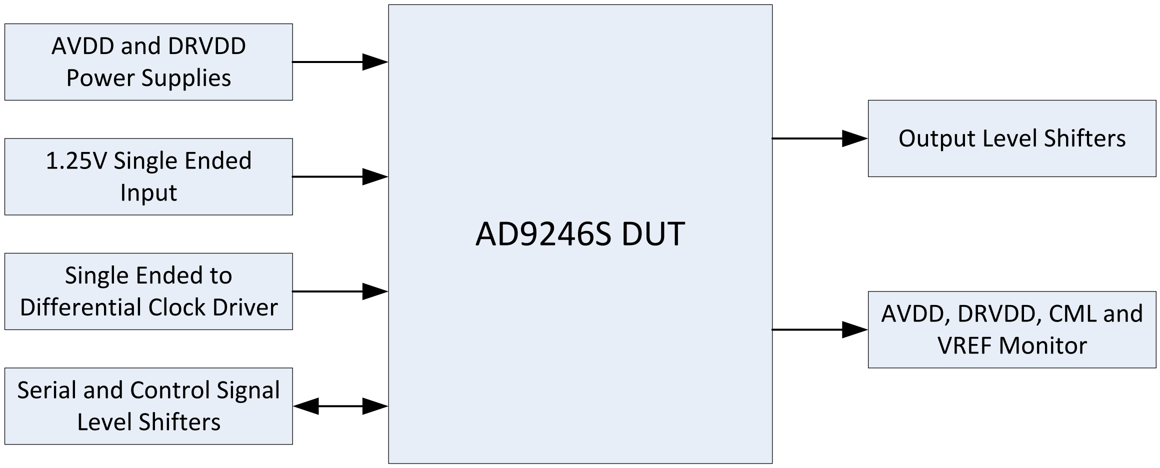

Figure 2-1. Block Diagram of the AD9246S 14-Bit 125 MSPS Analog to Digital Converter SEE Test Circuit.

The SEE test setup for the AD9246S, which includes the memory test motherboard and a 9246S DUT daughterboard, is shown in Figure 2-2. The Keithley 2420 and 2410 Source Meters provide the AVDD and DRVDD supply voltages and also measure the associated currents. The Keithley 2425C Source Meter provides the voltage for the test side of the level shifters. The Housekeeping Power Supply provides +/-5 volts and +24 volts to the memory test motherboard. The Agilent 34970A Data Acquisition Unit with the Agilent 34901A Multiplexer Plug-in provides the capability to measure the AVDD and DRVDD voltages at the daughterboard. The Shutter Status Monitor is simply a TTL signal used to indicate when the shutter is open and provides a reference signal for the data logging. The laptop personal computer (PC) controls the test equipment and records the test data.

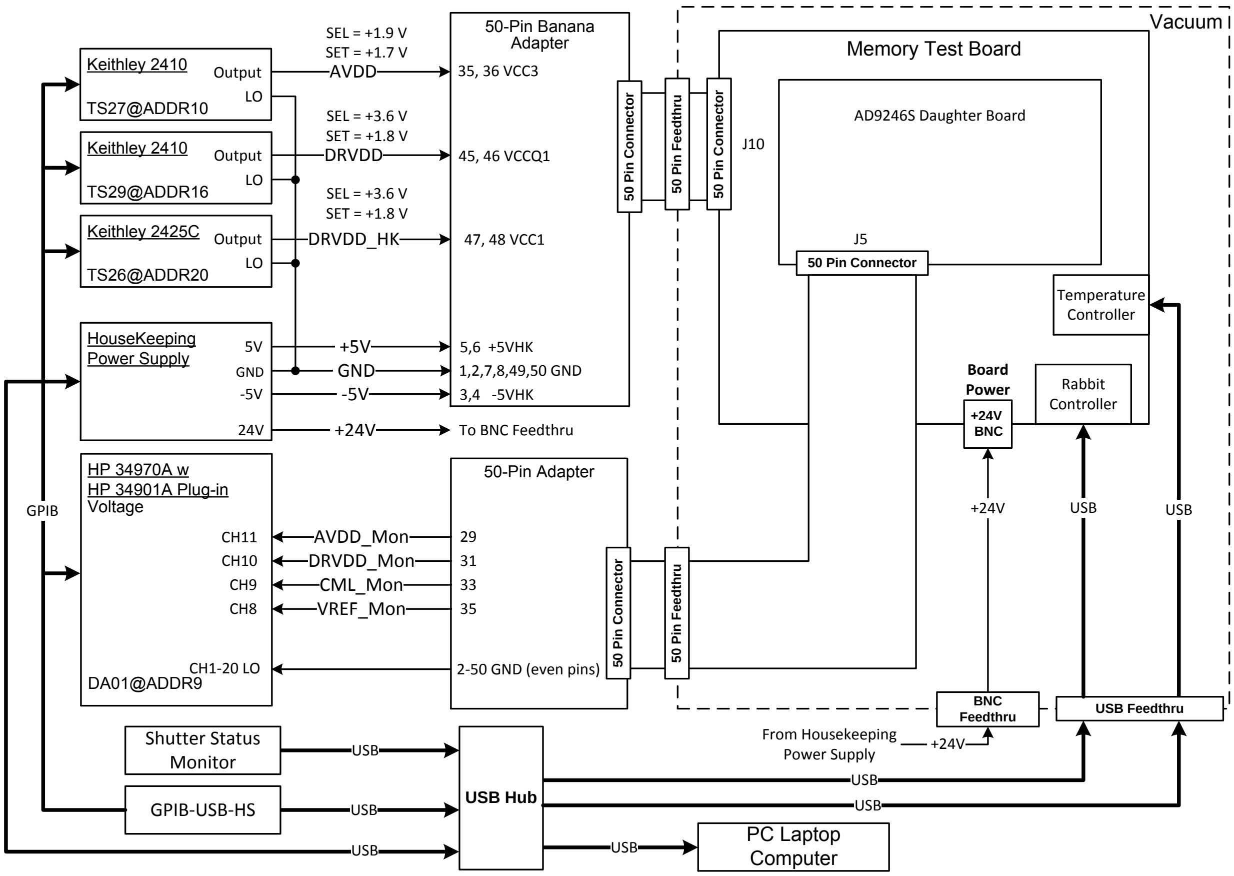

Figure 2-2. AD9246S 14-Bit 125 MSPS Analog to Digital Converter SEE Test Setup.

2.1. Test Parameters

Most of the measured electrical parameters were the same for the SEL and SEU/SET tests. Parameters measured at approximately one second increments during both the SEL and SEU/SET tests include:

1. The DUT temperature
2. The positive analog supply voltage, AVDD, at the DUT
3. The positive analog supply current
4. The positive digital supply voltage, DRVDD, at the DUT
5. The positive digital supply current
6. Beam shutter status

Additional parameters monitored during SEU/SET testing include:

1. The voltage reference, VREF, from the DUT.
2. The common-mode bias level, CML, from the DUT.

In the test circuit these two signals, VREF and CML, have a significant amount of bypass capacitance on their respective lines which would not allow fast transient responses to be observed; therefore, these signals were recorded by the Agilent 34901A multiplexer and monitored for coarse changes in voltage only.

The supply voltages, DUT temperature, and ion fluence for the SEL and SEU/SET testing were as follows:

	SEL	**SEU/SET**
DUT Temperature	125°C	ambient
AVDD	+1.9 V	+1.7 V
DRVDD	+3.6 V	+2.5V or +1.8 V
DRVDD_HK	+3.6 V	+2.5V or +1.8 V
Max. Fluence	10^7 ions/cm^2	10^6 ions/cm^2 or 100 events
Trigger Level	N/A	Three sigma times the noise band

Note: AVDD, DRVDD and DRVDD_HK will be adjusted at the DUT board to meet these voltage levels.

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2.2. Test Conditions

The signals monitored and recorded during the test were routed approximately twenty feet via coaxial cable to the control room. Table 2-1 lists the ions, angles, and LETs used to characterize the SEE response of the AD9246S devices.

Table 2-1. Ions Used for SEL and SEU/SET Characterization

Ion	Angle (Degrees)	LET ($MeV \cdot cm^2/mg$)
Argon	0	9.7
Copper	0	21.2
Krypton	0	30.9
Xenon	0	58.8
Xenon	43	80.4

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2.3 SEL Test Procedure

During the heavy ion exposure the supply currents of the AD9246S were monitored and recorded at approximately 1-second intervals. The current limit for the AVDD power supply was set to 400 mA and the current limit for the DRVDD and DRVDD_HK power supplies was set to 100 mA.

The following general SEL test procedure was used:

1. Power up the DUT and wait for it to attain the desired test temperature.
2. Select the desired ion and incidence angle for an effective LET of 80 MeV-cm^2/mg.
3. Turn on the ion beam, observe/monitor/log device current.
4. If no latch up occurs and the fluence reaches 10^7 ions/cm^2, it's considered a passing run.
5. If the test passes, run the remaining DUTs at the same effective LET beginning at step 1. At least one run should be with the current limit removed.
6. If no latch up or destructive events occurs on any runs, the SEL test is done.
7. If the DUT latches up, it's considered a failing run.
8. Shut off the beam and attempt to recover to initial current levels by first reprogramming the DUT registers. If that fails, power down the DUT.
9. Reapply power to the DUT and check the currents levels and check for a destructive latch.
10. Proceed with SEL characterization

SEL characterization:

11. Perform a run at max supply voltages, max temperature at an effective LET of approx. 10 MeV-cm^2/mg. A "run" is essentially steps 3, 4, 7, 8, and 9 above.
12. If the run passes, repeat the run at an effective LET of approx. 10 MeV-cm^2/mg higher than the previous run.
13. Repeat step 12 until a run fails.
14. If a run fails, lower the supply voltages by 10% and repeat the run at the same effective LET.
15. If run passes at a the lower supply voltages, continue stepping the effective up as in step 12.
16. If a run fails, go back to step 14. That is, lower the supply voltages by 10% and repeat the run.
17. Continue until a run fails with the supply voltages at their minimum values or an effective LET of 80 MeV-cm^2/mg is reached.
18. Once the SEL threshold level is determined, run the remaining DUTs at the highest effective LET and highest supply voltages in which no latch is observed. At least one run should be with the current limit removed.

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2.4 SEU/SET Test Procedure

During the heavy ion exposure the supply currents of the AD9246S were monitored and recorded at approximately 1-second intervals. The current limit for the AVDD power supply was set to 400 mA and the current limit for the DRVDD and DRVDD_HK power supplies was set to 100 mA.

The following general SEU/SET test procedure was used:

1. Power up the DUT.
2. Select the desired ion and desired angle of incidence.
3. Turn on the ion beam while observing, monitoring and logging the power supply currents and recording the transients.
4. Turn off the beam when either the specified number of transients is recorded or the fluence reaches 10^6 ions/cm^2.
5. Repeat the procedure beginning at step 2 until the DUT has been irradiated across the desired range of LETs (2 MeV-cm^2/mg to 80 MeV-cm^2/mg).
6. Test the remaining DUTs.

During heavy ion exposure the transient responses of the DUT were captured by the Xilinx Spartan 6 field programmable gate array (FPGA) when the SEU/SET level exceeds three sigma of the noise band.

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3.0. SEE Test Results

The AD9246S 14-Bit 125 MSPS Analog to Digital Converter was tested for single event effects at the LBNL Cyclotron Facility using their 88-Inch Cyclotron and the 10 MeV/n cocktail on April 1, 2016.

3.1. SEL Test Results

During SEL testing, the power supplies were set to the following voltages: AVDD = +1.9V, DRVDD = +3.6V, DRVDD_HK = +3.6V. The DUT temperature was controlled to 125°C (±5 °C) for DUT serial numbers 39, 7, 11, and 36. Table 3-1 lists the run and test conditions as well as the result of the run. With the SEL test conditions, at no point did any of the four DUTs experience a latch-up condition.

Table 3-1. AD9246 SEL Run Log.

Run	SN	Ion	Effective LET (MeV·cm^2/mg)	Effective Fluence (ion/cm^2)	Temp (°C)	Results
63	39	Xe@43°	80.4	1.01E+07	125	No Latch-up
85	7	Xe@43°	80.4	1.02E+07	125	No Latch-up
95	11	Xe@43°	80.4	1.02E+07	125	No Latch-up
105	36	Xe@43°	80.4	1.01E+07	125	No Latch-up

The nominal AVDD current at 125°C was approximately 226 mA. The nominal DRVDD current at 125°C was approximately 10 mA. Appendix E illustrates the SEL current plots. Figure 3-1 illustrates a representative SEL current plot for AVDD and Figure 3-2 illustrates a representative SEL current plot for DRVDD.

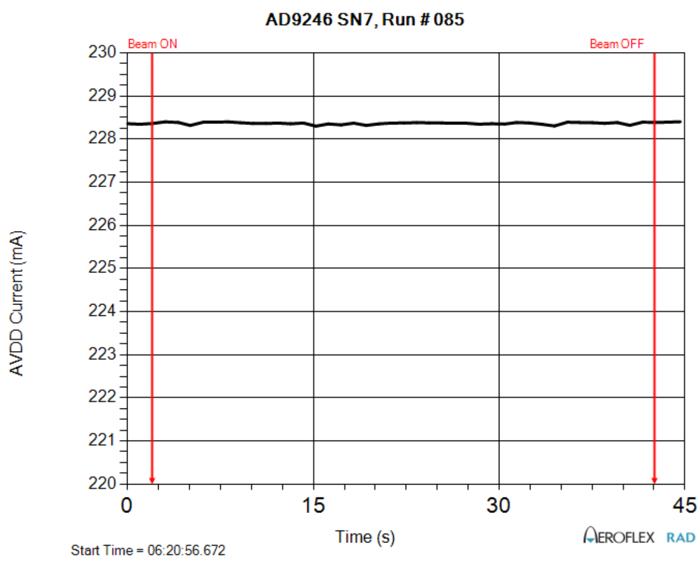

Figure 3-1. AD9246 SN7, Run #85, DUT AVDD Current (mA).

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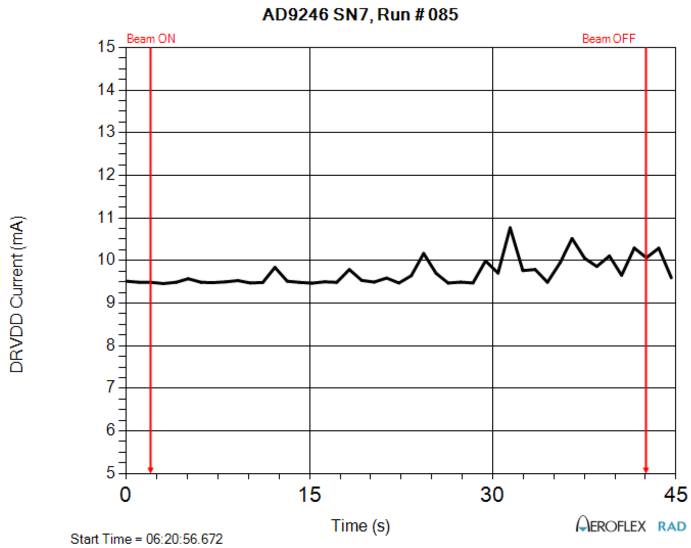

Figure 3-2. AD9246 SN7, Run #85, DUT DRVDD Current (mA).

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3.2. SET Test Results

SET testing was performed using the power supplies set to the following voltages:

AVDD = +1.7V,
DRVDD = +2.5V or +1.8V.

The DUT temperature was not controlled, but it was monitored. No anomalous temperatures were observed. The DUT currents were also monitored, Appendix F illustrates the SET current plots.

The least significant bits reflecting the board and facility noise were removed from the comparison by applying a digital mask to the output of the ADC. For all SET testing, the bottom six (6) bits were masked (i.e., the data were ANDed with 0x3FC0.) This represents about a ½ mV of noise given a 2 V input range. The digital output was sampled 64 times to determine the expected value from the ADC.

Table 3-2 lists the runs for each of the DUTs tested. The table contains the run number, serial number, ion@incident angle, effective LET, effective fluence, DRVDD voltage, register configuration, number of sample errors, number of events, and the event cross section.

The number of sample errors is the total number of errors observed in a run. This includes all consecutive sample errors that are caused by a single event. The number of events reflects the number of heavy ion interactions and is the value used to calculate the event cross-section.

During some of the SET testing runs, the configuration registers used values other than the default values, such as the output driver of 1.8 volts and the two's compliment output data configuration. During runs 65 and 94, no SETs were observed.

Table 3-3 shows the amplitudes of the errors seen by AD9246S serial numbers 39, 7, 11, and 36. With the six least significant bits (LSBs) masked, most of the errors were either 1-bit or 2-bit errors above the data mask. Anomalous behavior was observed in runs 92, 94, and 103. In run 92, LET = 80.4 MeV-cm^2/mg, two events occurred, one at sample 439472315 and one at sample 634331638, where the output indicated full scale (0x3FFF) and the over range (OR) bit was asserted. In run 94, LET = 80.4 MeV-cm^2/mg, one error occurred where the output indicated almost full scale (0x1FFF) and the OR bit was asserted. In run 103, LET = 80.4 MeV-cm^2/mg, the DCO signal froze for 160 ns (i.e., eight consecutive input clock periods). Appendix G illustrates the SET error plots.

Figure 3-3 shows the plot of the observed cross-sections. Given the small number of upsets observed, the shape of the data is difficult to determine. However, a Weibull curve with parameters: Shape=4, Width=19, Saturation=2.5x10^{-6}, and Onset=10 is given for reference.

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Table 3-2. AD9246 SN39 SET Run Log.

Run	SN	Ion	Effective LET (MeV-cm^2/mg)	Effective Fluence (ions/cm^2)	DRVDD Voltage (Volts)	Register Configuration	Sample Errors	Events	Cross Section
64	39	Xe@43	80.4	1.03E+06	2.5	Default	4	2	1.94E-06
65	39	Xe@43	80.4	1.02E+06	2.5	Twos Compliment	6	5	4.90E-06
66	39	Xe@43	80.4	1.02E+06	1.8	Output Drive = 1.8V	0	0	0.00E+00
67	39	Xe@0	58.8	1.03E+06	2.5	Default	3	2	1.94E-06
68	39	Xe@0	58.8	1.04E+06	1.8	Output Drive = 1.8V	5	2	1.92E-06
69	39	Kr@0	30.9	1.03E+06	2.5	Default	0	0	0.00E+00
70	39	Kr@0	30.9	1.03E+06	1.8	Output Drive = 1.8V	0	0	0.00E+00
71	39	Cu@0	21.2	1.04E+06	2.5	Default	0	0	0.00E+00
72	39	Cu@0	21.2	1.04E+06	1.8	Output Drive = 1.8V	0	0	0.00E+00
73	39	Ar@0	9.7	1.03E+06	2.5	Default	0	0	0.00E+00
74	39	Ar@0	9.7	1.04E+06	1.8	Output Drive = 1.8V	0	0	0.00E+00
75	7	Ar@0	9.7	1.04E+06	2.5	Default	0	0	0.00E+00
76	7	Ar@0	9.7	1.03E+06	1.8	Output Drive = 1.8V	0	0	0.00E+00
77	7	Cu@0	21.2	1.04E+06	2.5	Default	0	0	0.00E+00
78	7	Cu@0	21.2	1.04E+06	1.8	Output Drive = 1.8V	0	0	0.00E+00
79	7	Kr@0	30.9	1.03E+06	2.5	Default	0	0	0.00E+00
80	7	Kr@0	30.9	1.02E+06	1.8	Output Drive = 1.8V	0	0	0.00E+00
81	7	Xe@0	58.8	1.05E+06	2.5	Default	1	1	9.52E-07
82	7	Xe@0	58.8	1.05E+06	1.8	Output Drive = 1.8V	1	1	9.52E-07
83	7	Xe@43	80.4	1.03E+06	2.5	Default	1	1	9.71E-07
84	7	Xe@43	80.4	1.03E+06	1.8	Output Drive = 1.8V	0	0	0.00E+00
86	11	Xe@0	58.8	1.39E+06	2.5	Default	1	1	7.19E-07
87	11	Xe@0	58.8	1.03E+06	1.8	Output Drive = 1.8V	0	0	0.00E+00
88	11	Kr@0	30.9	1.02E+06	2.5	Default	0	0	0.00E+00
89	11	Kr@0	30.9	1.03E+06	1.8	Output Drive = 1.8V	0	0	0.00E+00
90	11	Cu@0	21.2	1.03E+06	2.5	Default	0	0	0.00E+00
91	11	Cu@0	21.2	1.04E+06	1.8	Output Drive = 1.8V	0	0	0.00E+00
92	11	Xe@43	80.4	1.21E+06	2.5	Default	3	3	2.48E-06
93	11	Xe@43	80.4	1.03E+06	1.8	Output Drive = 1.8V	1	0	0.00E+00
94	11	Xe@43	80.4	1.04E+06	2.5	Twos Compliment	2	2	1.92E-06
96	11	Xe@43	80.4	1.04E+06	2.5	Default	2	2	1.92E-06
97	36	Xe@0	58.8	1.03E+06	2.5	Default	1	1	9.71E-07
98	36	Xe@0	58.8	1.05E+06	1.8	Output Drive = 1.8V	0	0	0.00E+00
99	36	Kr@0	30.9	1.03E+06	2.5	Default	1	1	9.71E-07
100	36	Kr@0	30.9	1.03E+06	1.8	Output Drive = 1.8V	2	2	1.94E-06
101	36	Cu@0	21.2	1.02E+06	2.5	Default	0	0	0.00E+00
102	36	Cu@0	21.2	1.03E+06	1.8	Output Drive = 1.8V	0	0	0.00E+00
103	36	Xe@43	80.4	1.02E+06	2.5	Default	8	1	9.80E-07
104	36	Xe@43	80.4	1.02E+06	1.8	Output Drive = 1.8V	0	0	0.00E+00

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Table 3-3. AD9246 SN39 Error Amplitudes.

Run	SN	Effective LET	# of bits masked							
			13	12	11	10	9	8	7	6
		(MeV-cm^2/mg)	0x1000	0x3000	0x3800	0x3C00	0x3E00	0x3F00	0x3F80	0x3FC0
64	39	80.4	0	0	0	0	0	0	0	4
65	39	80.4	0	0	0	0	0	0	0	6
66	39	80.4	0	0	0	0	0	0	0	0
67	39	58.8	0	0	0	0	0	0	0	3
68	39	58.8	0	0	0	0	0	0	0	5
69	39	30.9	0	0	0	0	0	0	0	0
70	39	30.9	0	0	0	0	0	0	0	0
71	39	21.2	0	0	0	0	0	0	0	0
72	39	21.2	0	0	0	0	0	0	0	0
73	39	9.7	0	0	0	0	0	0	0	0
74	39	9.7	0	0	0	0	0	0	0	0
75	7	9.7	0	0	0	0	0	0	0	0
76	7	9.7	0	0	0	0	0	0	0	0
77	7	21.2	0	0	0	0	0	0	0	0
78	7	21.2	0	0	0	0	0	0	0	0
79	7	30.9	0	0	0	0	0	0	0	0
80	7	30.9	0	0	0	0	0	0	0	0
81	7	58.8	0	0	0	0	0	0	0	1
82	7	58.8	0	0	0	0	0	0	0	1
83	7	80.4	0	0	0	0	0	0	0	1
84	7	80.4	0	0	0	0	0	0	0	0
86	11	58.8	0	0	0	0	0	0	0	1
87	11	58.8	0	0	0	0	0	0	0	0
88	11	30.9	0	0	0	0	0	0	0	0
89	11	30.9	0	0	0	0	0	0	0	0
90	11	21.2	0	0	0	0	0	0	0	0
91	11	21.2	0	0	0	0	0	0	0	0
92	11	80.4	0	2	2	2	3	3	3	3
93	11	80.4	0	0	0	0	0	0	0	1
94	11	80.4	0	1	1	1	1	1	2	2
96	11	80.4	0	0	0	0	0	0	1	2
97	36	58.8	0	0	0	0	0	1	1	1
98	36	58.8	0	0	0	0	0	0	0	0
99	36	30.9	0	0	0	0	0	0	0	1
100	36	30.9	0	0	0	0	0	0	0	2
101	36	21.2	0	0	0	0	0	0	0	0
102	36	21.2	8	8	8	8	8	8	8	8
103	36	80.4	0	0	0	0	0	0	0	0
104	36	80.4	0	0	0	0	0	0	0	0

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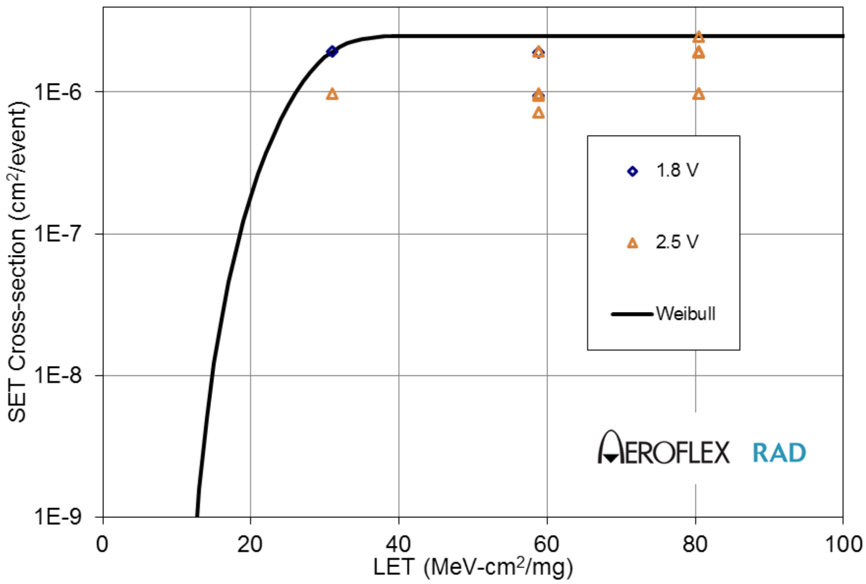

Figure 3-3. AD9246 SET cross-section and Weibull curve with parameters Shape=4, Width=19, Saturation=2.5x10^{-6}, and Onset=10.

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4.0 Summary/Conclusions

The Analog Devices AD9246S was tested for Single Event Effects (SEE) with heavy ion irradiation on 4/1/2016 at Lawrence Berkeley National Laboratory.

No latchup (SEL) or other destructive SEE was observed at or below 80 MeV-cm^2/mg on any of the four devices tested at a temperature of 125°C with AVDD=1.9V and DRVDD = 3.6V.

No configuration register SEUs were observed at or below 80 MeV-cm^2/mg under all conditions.

Maximum SET cross-section observed was < 2.5x10^{-6} cm^2/event at LET of > 80 MeV·cm^2/mg at ambient temperature of ~25°C) with AVDD=1.7V and DRVDD = 1.8 V and 2.5 V.

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Appendix A: Photographs of Sample Device-Under-Test

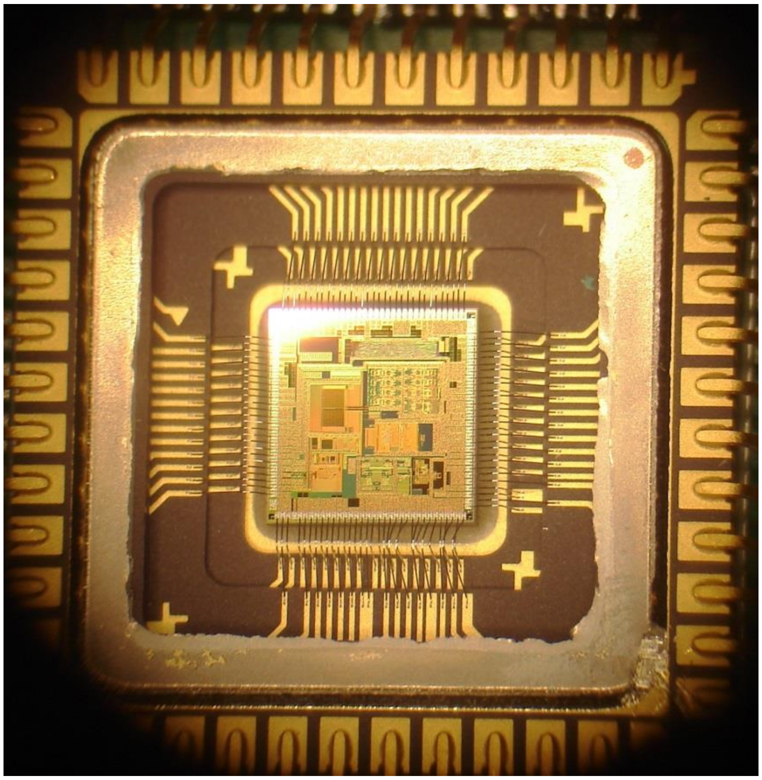
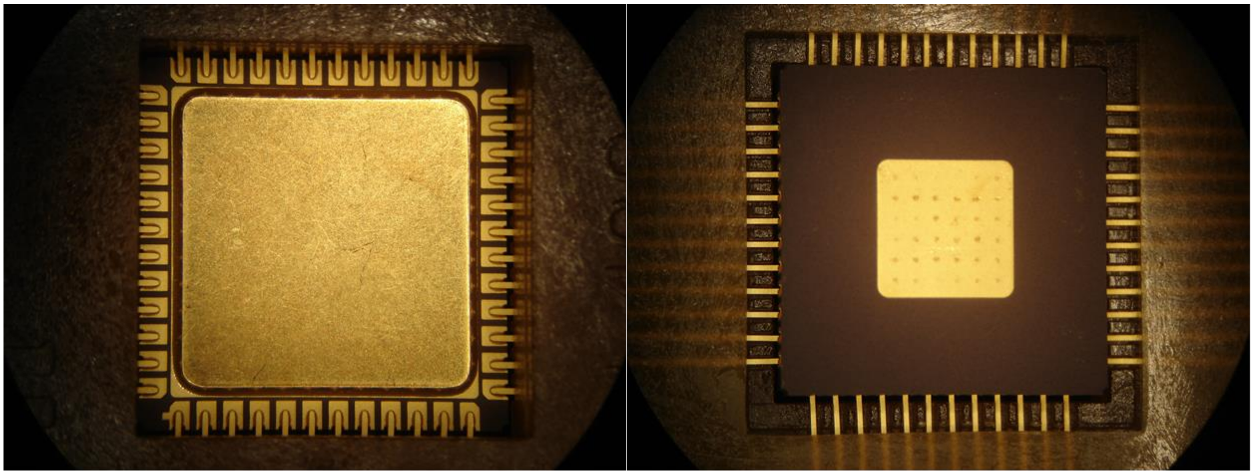


Figure A-1. Delidded AD9246S 14-Bit 125 MSPS Analog to Digital Converter



Units are unmarked. Serial numbers are written in pencil on the plastic carriers

Figure A-2. AD9246S 14-Bit 125 MSPS Analog to Digital Converter as Received

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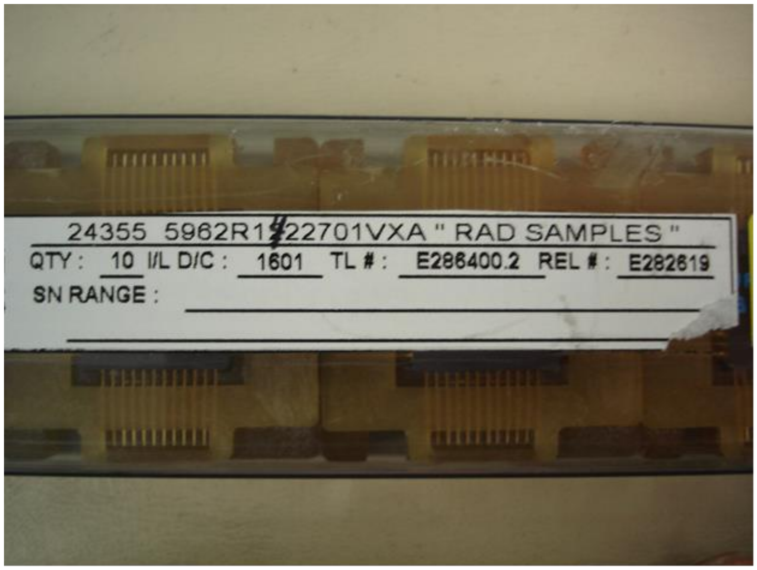

Figure A-3. AD9246S 14-Bit 125 MSPS Analog to Digital Converter Package Label

Appendix B: Photograph of the Test Boards and Electrical Schematics.

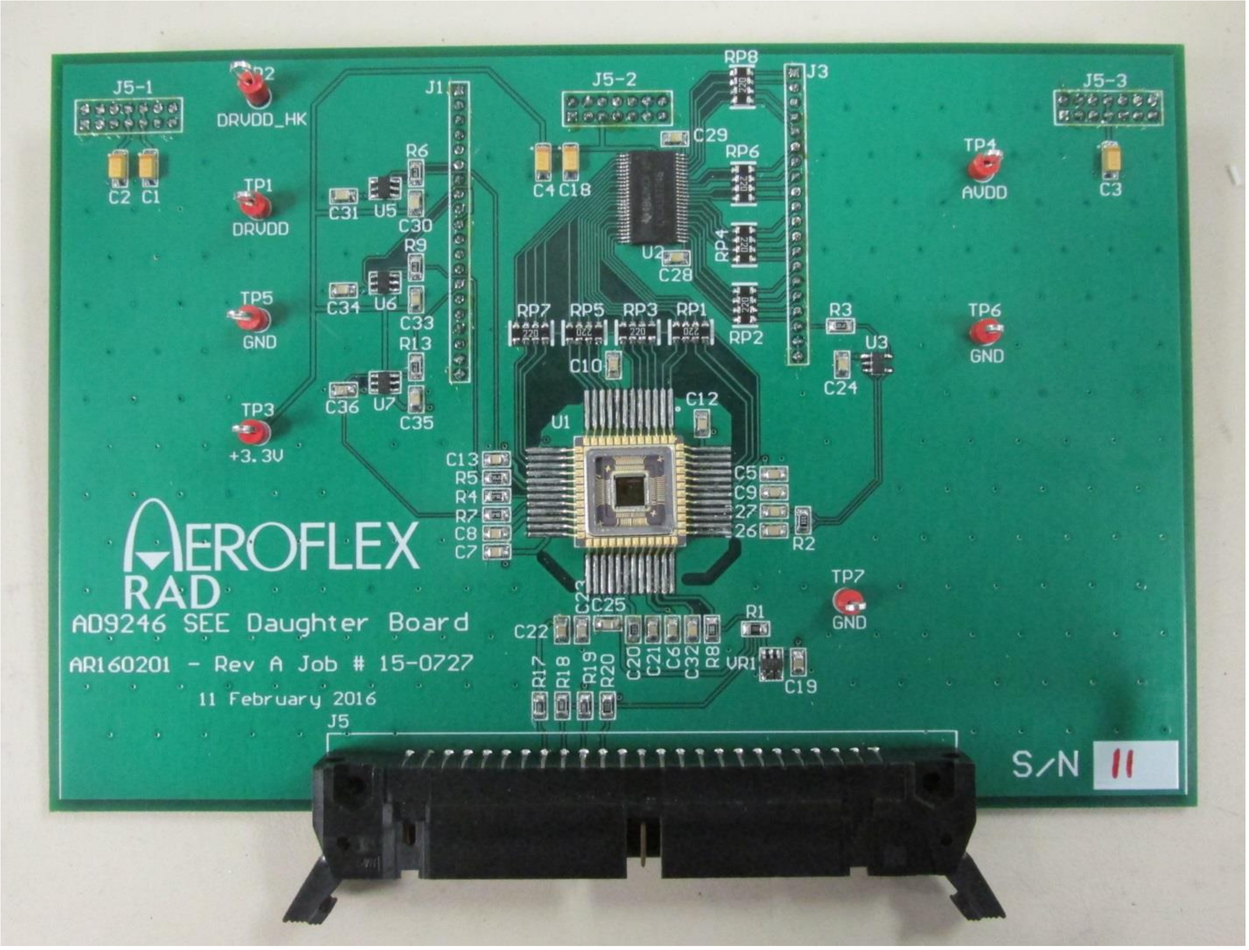

Figure B-1. Photo of the AD9246S 14-Bit 125 MSPS Analog to Digital Converter Daughterboard

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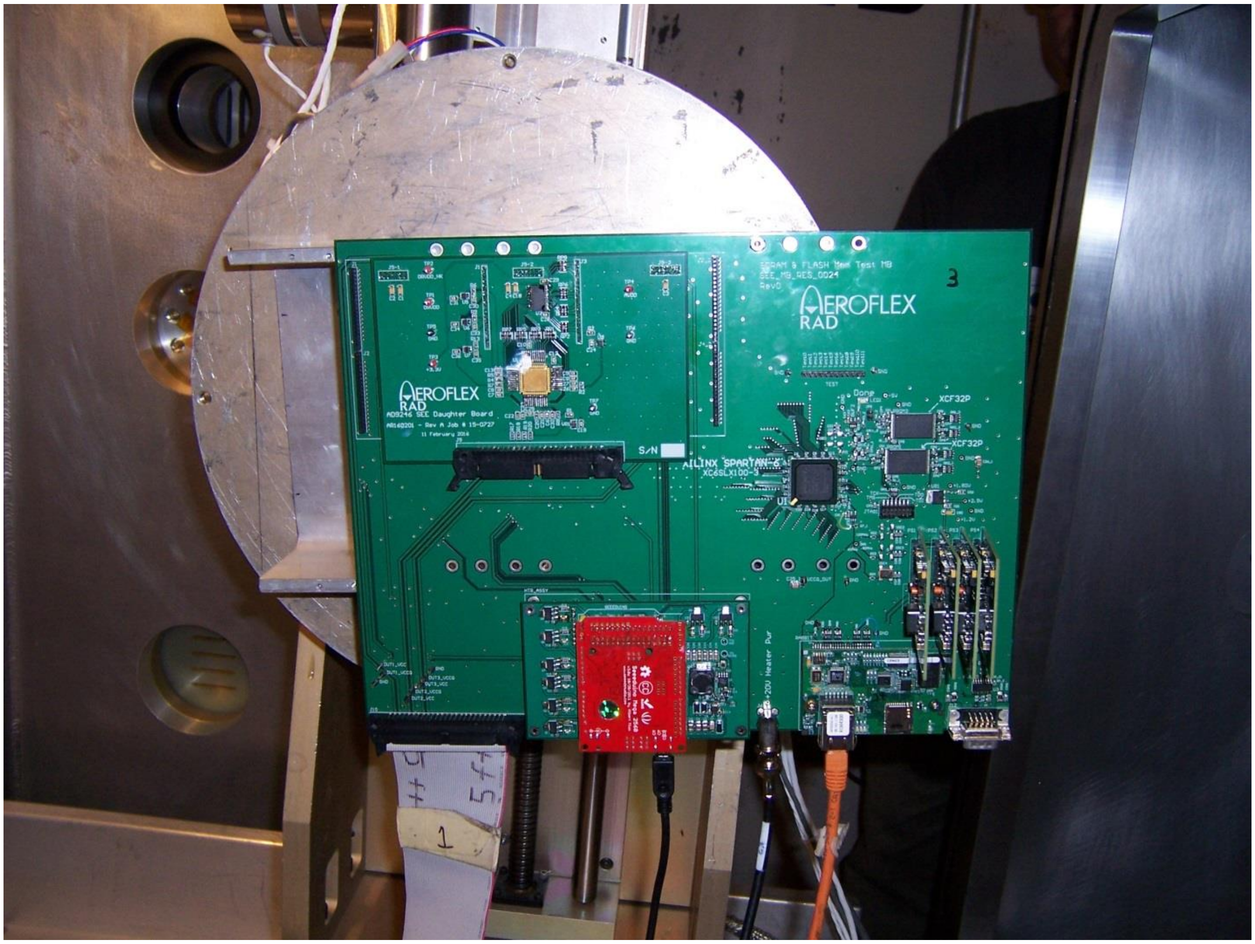

Figure B-2. Photo of the AD9246S Test Setup in the Vacuum Chamber

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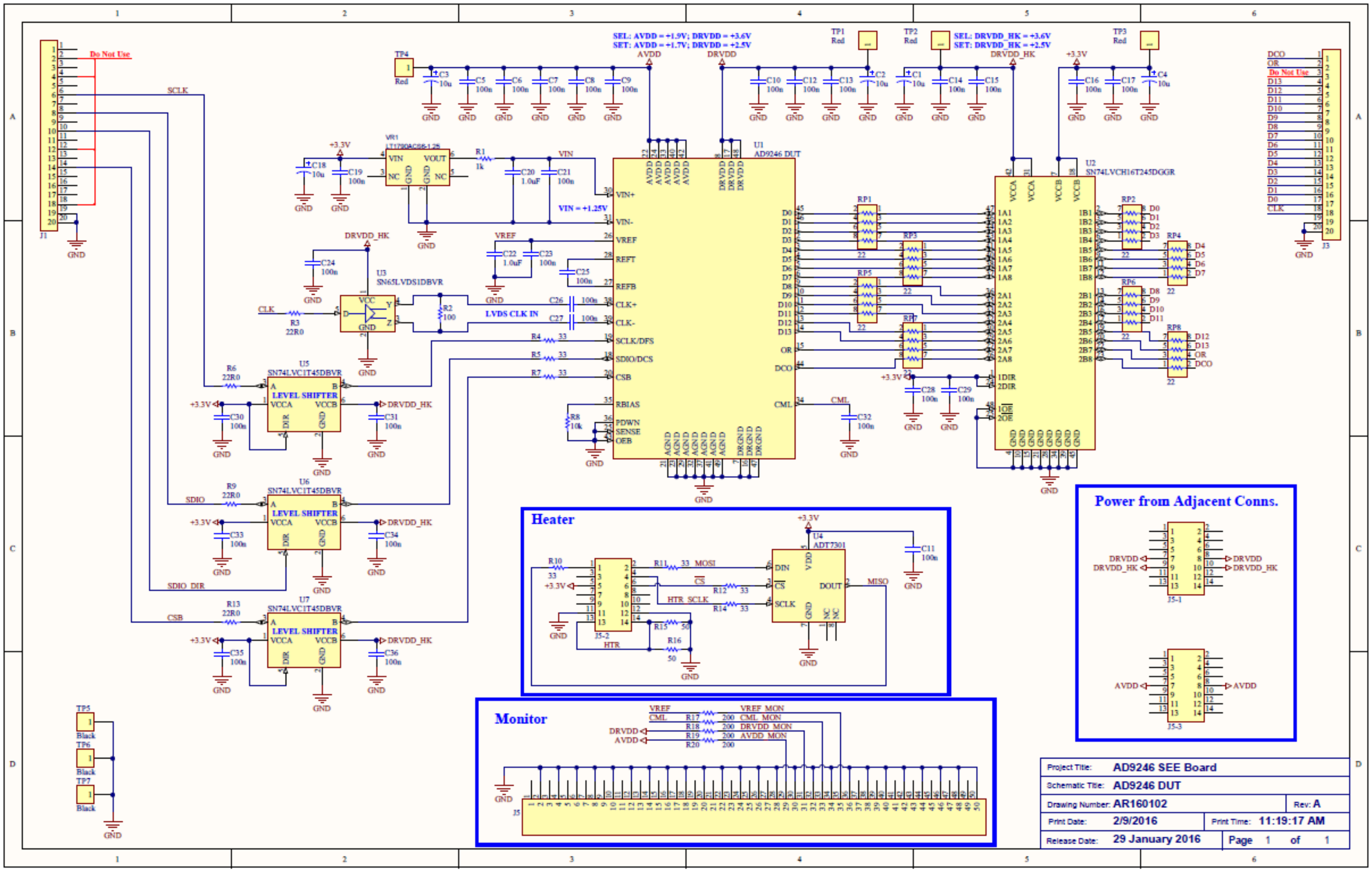

Figure B-3. AD9246S 14-Bit 125 MSPS Analog to Digital Converter Daughterboard Schematic

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Appendix C: Equipment List

Table C-1 lists the equipment typically used during the testing as well as the calibration dates and the date the calibration is due.

Table C-1. Test Equipment List and Calibration Dates.

Equipment	**Entity Number**	**Calibration Date**	**Calibration Due**	**Purpose**
Keithley 2410 Source Meter	TS29	07/14/2015	07/14/2016	DRVDD, Power Supply and Current Measurement
Keithley 2420 Source Meter	TS27	04/15/2015	04/15/2016	AVDD, Power Supply and Current Measurement
Keithley 2425C Source Meter	TS26	06/05/2015	06/05/2016	DRVDD_HK Power Supply
Agilent 34970A Data Aquistion Unit	DA01	08/25/2015	08/25/2016	DUT Voltage Measurements
Agilent 34901A Multiplexer	MP01	08/25/2015	08/25/2016	DUT Voltage Measurements
Fluke 115 True RMS Multimeter	HM17	07/01/2015	07/01/2016	Voltage Measurements
Housekeeping Power Supply		NA	NA	+/-5 Volt, +/-12 Volt and +24 Volt Power Supplies
Fluke 51II Thermometer	TM03	07/31/2015	07/31/2016	Sensor Temperature Calibration
Thermocouple	TC17	02/04/2016	02/04/2017	Sensor Temperature Calibration

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Appendix D: Single Event Effects Apparatus

The single event effects testing discussed in this test report was performed at the Lawrence Berkeley National Laboratories (LBNL) Cyclotron Facility using their 88-Inch Cyclotron. For the single event transient testing performed at LBNL the devices was placed in the Cave 4B vacuum chamber aligned with the heavy ion beam line. The test platter in the vacuum chamber has full horizontal and vertical alignment capabilities along with 2-dimensional rotation, allowing for a variety of effective LETs for each ion. For SEE testing Lawrence Berkeley National Laboratories provides the dosimetry via a local control computer running a Lab View based program. Each ion is calibrated using five photomultiplier tubes (PMTs). Figure D-1 shows an illustration of the LBNL facility, including the location of Cave 4B, where the heavy ion SEE testing takes place. Table D-1 shows the beam characteristics available at LBNL.

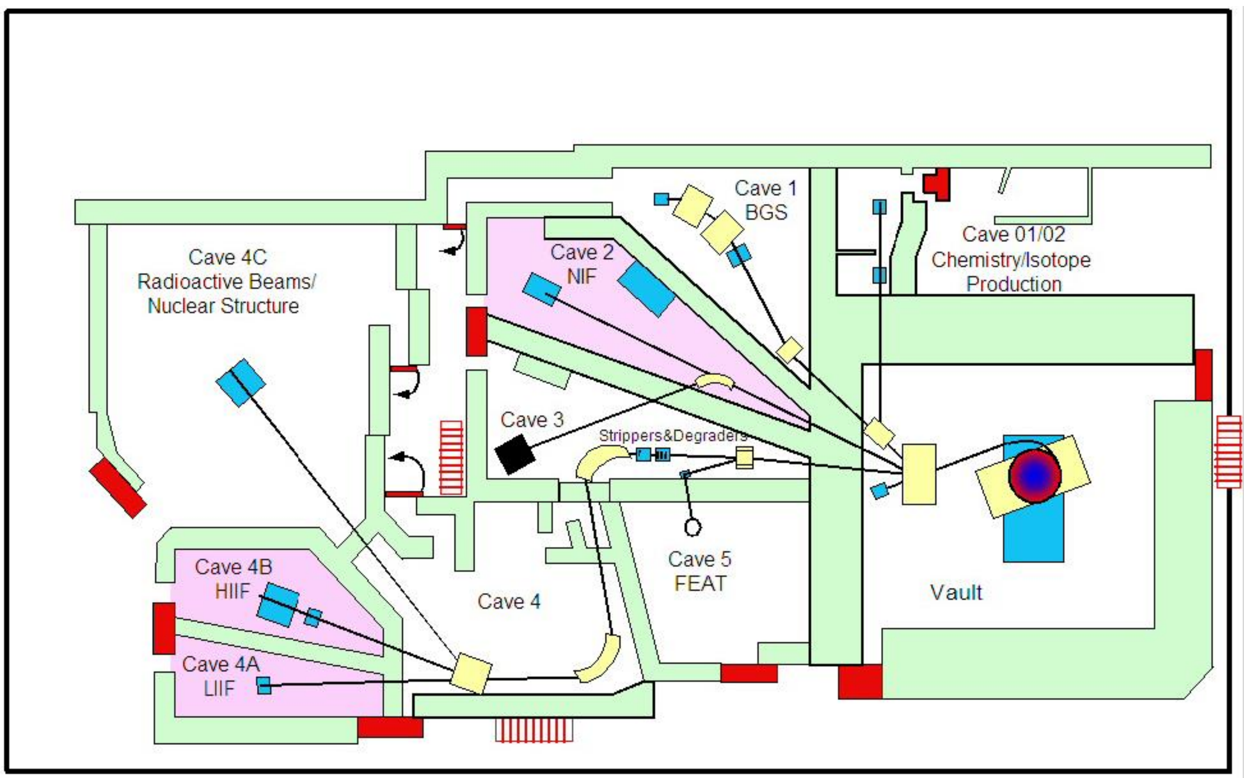

Figure D-1. Pictorial Layout of the LBNL 88" Cyclotron Facility

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Table D-1. Ions and LETs Typically Available During SEE Testing.

Ion	Cocktail (MeV/nuc)	Energy (MeV)	Z	A	Chg. State	% Nat. Abund.	LET 0° (MeV/(mg/cm²))	LET 60° (MeV/(mg/cm²))	Range (µm)	Method
B	4.5	44.90	5	10	+2	19.9	1.65	3.30	78.5	MIVOC
N	4.5	67.44	7	15	+3	0.37	3.08	6.16	67.8	Gas
Ne	4.5	89.95	10	20	+4	90.48	5.77	11.54	53.1	Gas
Si[1]	4.5	139.61	14	29	+6	4.67	9.28	18.56	52.4	Gas
Ar	4.5	180.00	18	40	+8	99.6	14.32	28.64	48.3	Gas
V	4.5	221.00	23	51	+10	99.75	21.68	43.36	42.5	Probe
Cu	4.5	301.79	29	63	+13	69.17	29.33	58.66	45.6	Probe
Kr	4.5	387.08	36	84	+17	17.3	38.96	77.92	48.0	Gas
Y	4.5	409.58	39	89	+18	100	45.58	91.16	45.8	Probe
Ag	4.5	499.50	47	109	+22	48.161	58.18	116.36	46.3	Probe
Xe	4.5	602.90	54	136	+27	8.9	68.84	137.68	48.3	Gas
Tb	4.5	724.17	65	159	+32	100	77.52	155.04	52.4	Probe
Ta	4.5	805.02	73	181	+36	99.988	87.15	174.30	53.0	Probe
Bi	4.5	904.16	83	209	+41	100	99.74	199.48	52.9	Oven
B	10	108.01	5	11	+3	80.1	0.89	1.78	305.7	MIVOC
O	10	183.47	8	18	+5	0.2	2.19	4.38	226.4	Gas
Ne	10	216.28	10	22	+6	9.25	3.49	6.98	174.6	Gas
Si[1]	10	291.77	14	29	+8	4.67	6.09	12.18	141.7	Gas
Ar	10	400.00	18	40	+11	99.6	9.74	19.48	130.1	Gas
V	10	508.27	23	51	+14	99.75	14.59	29.18	113.4	Probe
Cu	10	659.19	29	65	+18	30.83	21.17	42.34	108.0	Probe
Kr	10	906.45	36	84	+24	57	30.23	60.46	113.1	Gas
Y	10	928.49	39	89	+25	100	34.73	69.46	102.2	Probe
Ag	10	1039.42	47	107	+29	51.839	48.15	96.30	90.0	Probe
Xe	10	1232.55	54	124	+34	0.1	58.78	117.56	90.0	Gas
N	16	233.75	7	14	+5	99.63	1.16	2.32	505.9	Gas
O	16	277.33	8	17	+6	0.04	1.54	3.08	462.4	Gas
Ne	16	321.00	10	20	+7	90.48	2.39	4.78	347.9	Gas
Si[1]	16	452.10	14	29	+10	4.67	4.56	9.12	274.3	Gas
Cl	16	539.51	17	35	+12	75.77	6.61	13.22	233.6	Natural
Ar	16	642.36	18	40	+14	99.600	7.27	14.54	255.6	Gas
V	16	832.84	23	51	+18	99.750	10.90	21.80	225.8	Probe
Cu	16	1007.34	29	63	+22	69.17	16.53	33.06	190.3	Probe
Kr	16	1225.54	36	78	+27	0.35	24.98	49.96	165.4	Gas
Xe	16	1954.71	54	124	+43	0.1	49.29	98.58	147.9	Gas
N	30	425.45	7	15	+7	0.37	0.76	1.52	1370.0	Gas
O	30	490.22	8	17	+8	0.04	0.98	1.96	1220.0	Gas
Ne	30	620.00	10	21	+10	0.27	1.48	2.96	1040.0	Gas
Ar	30	1046.11	18	36	+17	0.337	4.87	9.74	578.1	Gas

[1]By Special request

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Appendix E: SEL Current Plots

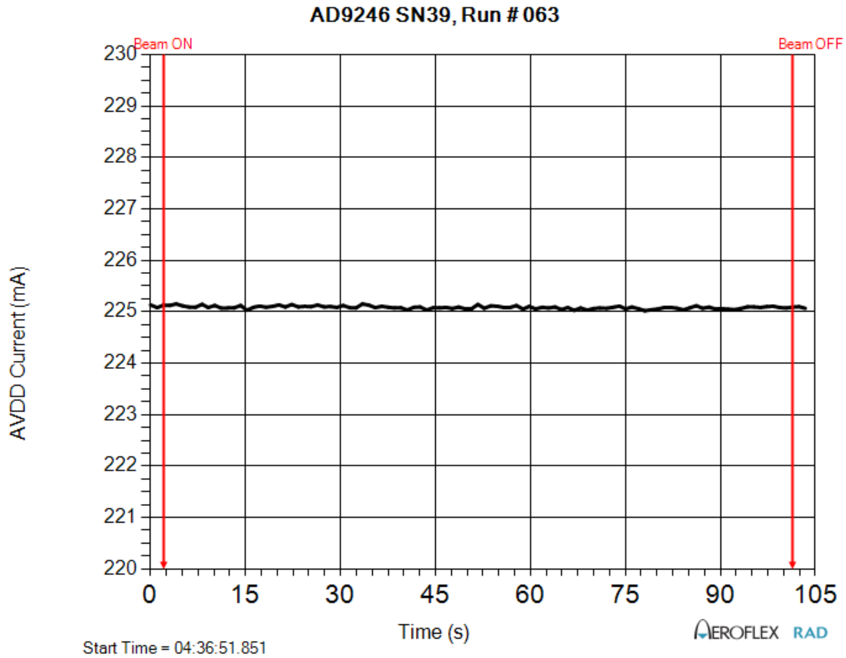

Figure E-1. AD9246 SN39, Run #63, DUT AVDD Current (mA).

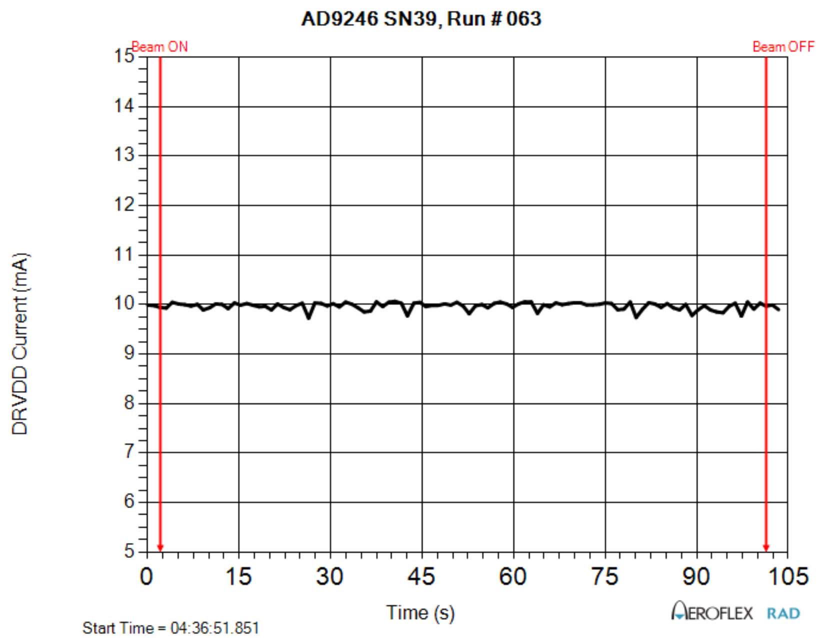

Figure E-2. AD9246 SN39, Run #63, DUT DRVDD Current (mA).

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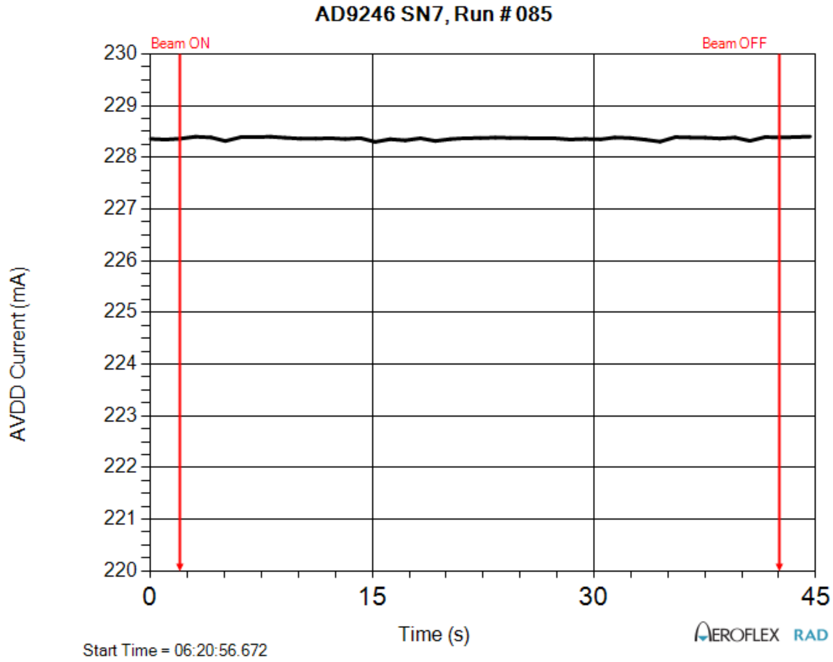

Figure E-3. AD9246 SN7, Run #85, DUT AVDD Current (mA).

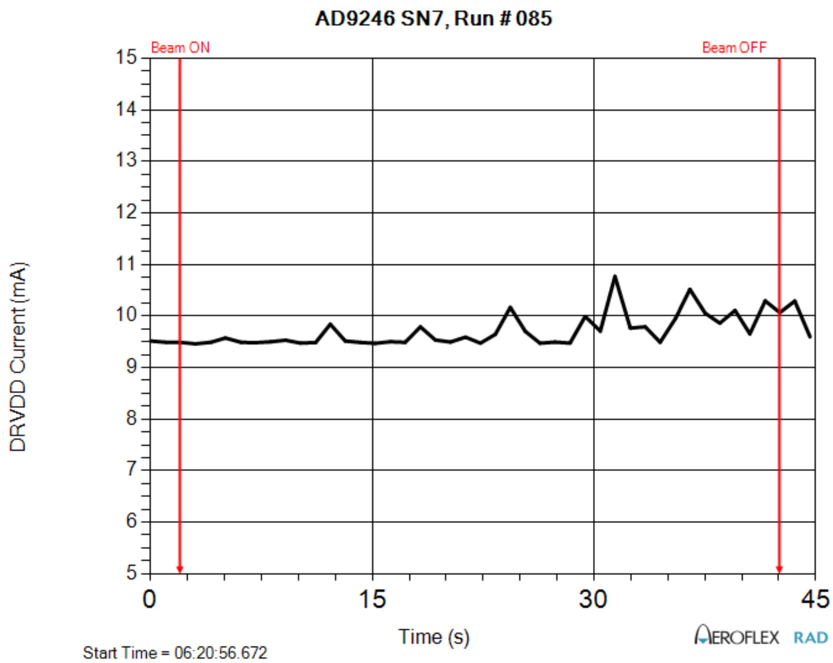

Figure E-4. AD9246 SN7, Run #85, DUT DRVDD Current (mA).

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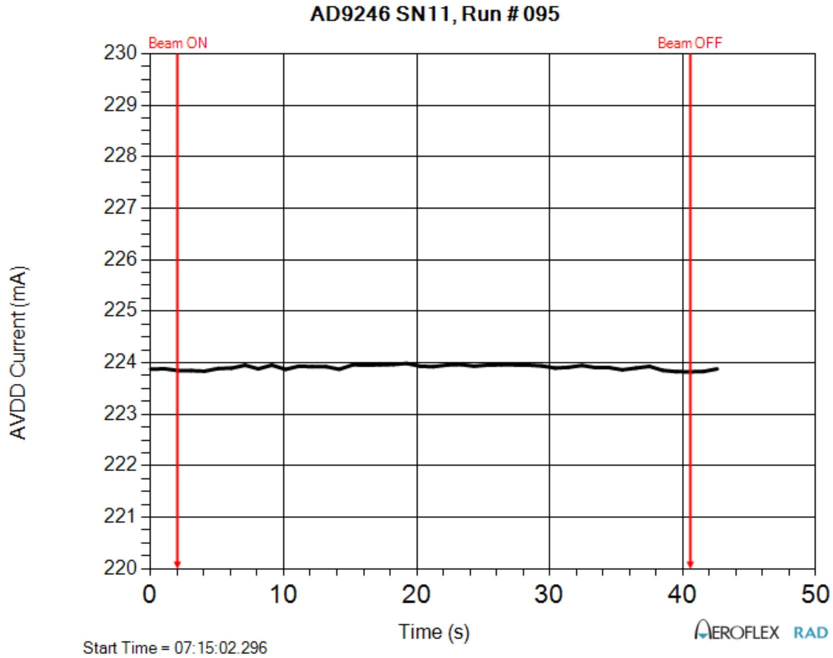

Figure E-5. AD9246 SN11, Run #95, DUT AVDD Current (mA).

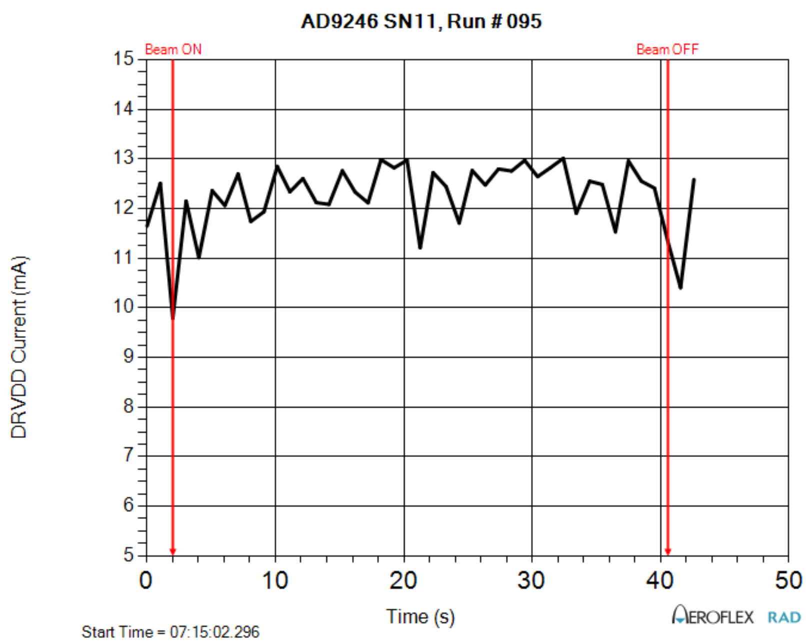

Figure E-6. AD9246 SN11, Run #95, DUT DRVDD Current (mA).

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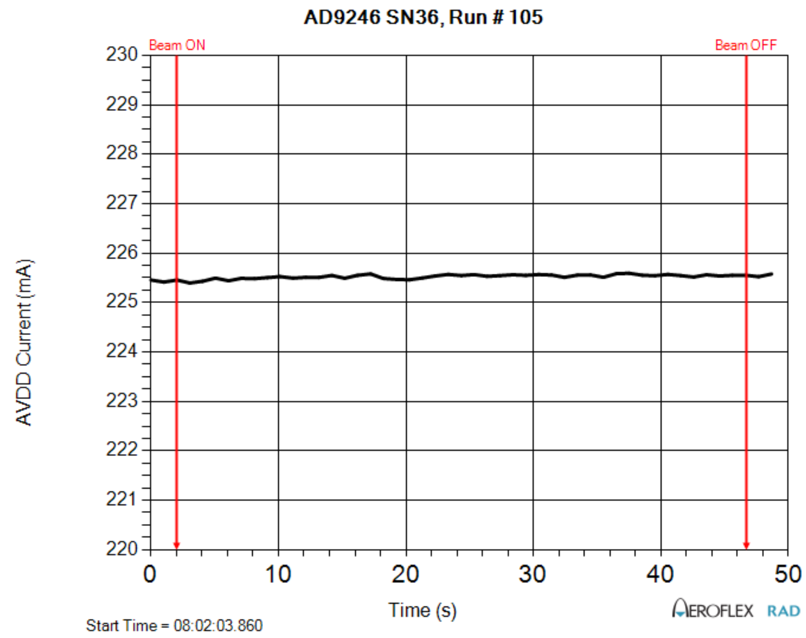

Figure E-7. AD9246 SN36, Run #105, DUT AVDD Current (mA).

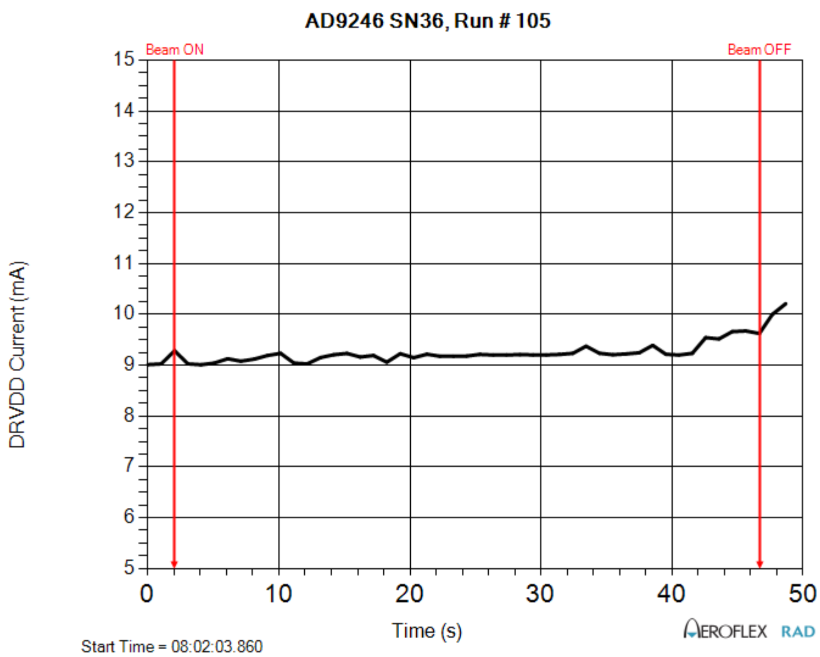

Figure E-8. AD9246 SN36, Run #105, DUT DRVDD Current (mA).

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Appendix F: SET Current Plots

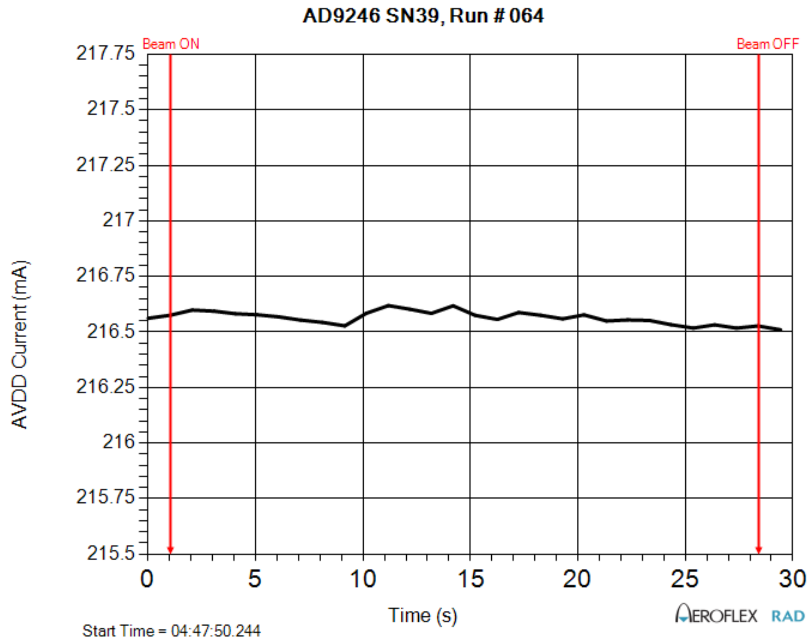

Figure F-1. AD9246 SN39, Run #64, DUT AVDD Current (mA).

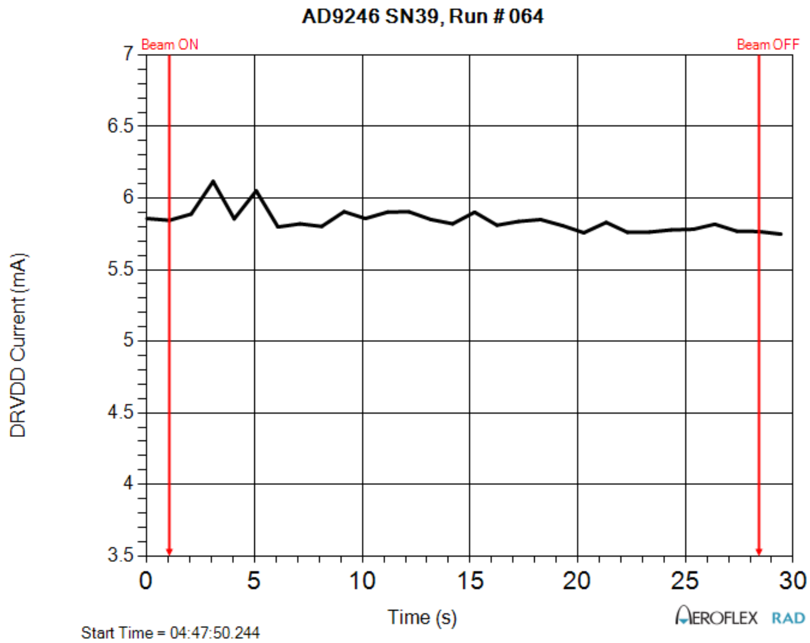

Figure F-2. AD9246 SN39, Run #64, DUT DRVDD Current (mA).

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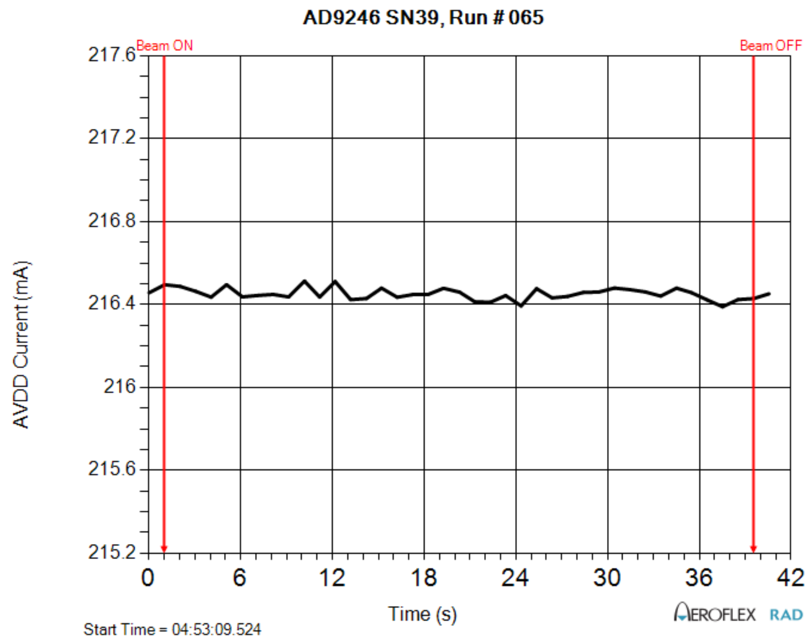

Figure F-3. AD9246 SN39, Run #65, DUT AVDD Current (mA).

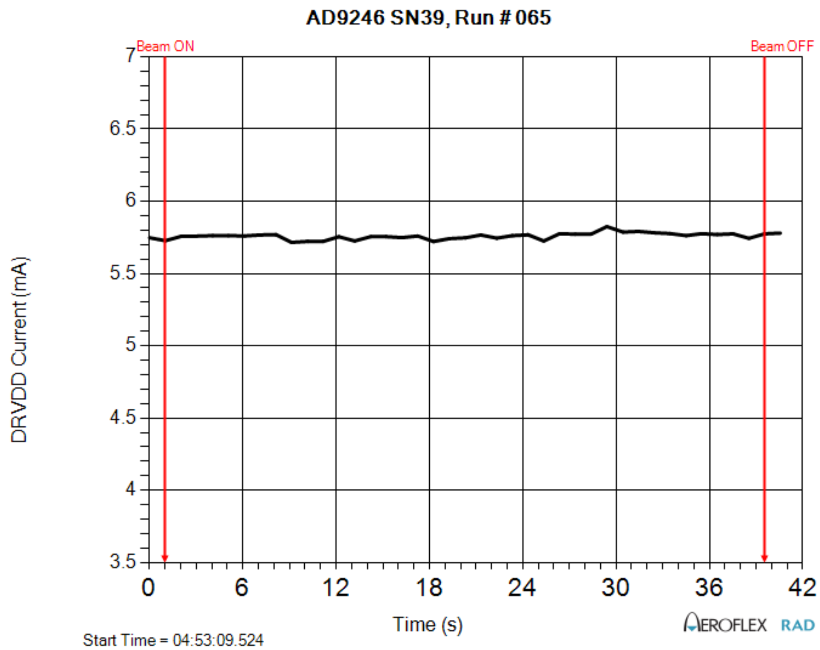

Figure F-4. AD9246 SN39, Run #65, DUT DRVDD Current (mA).

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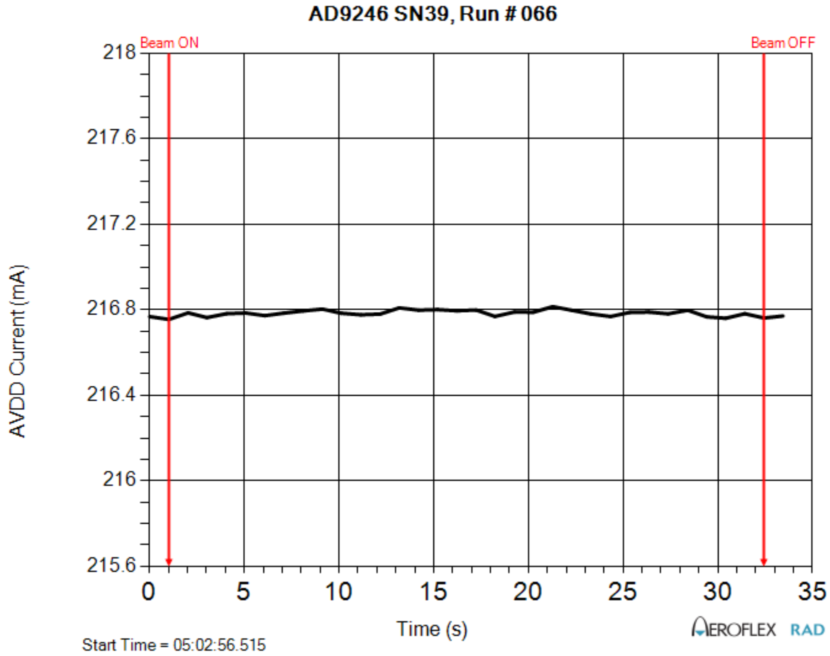

Figure F-5. AD9246 SN39, Run #66, DUT AVDD Current (mA).

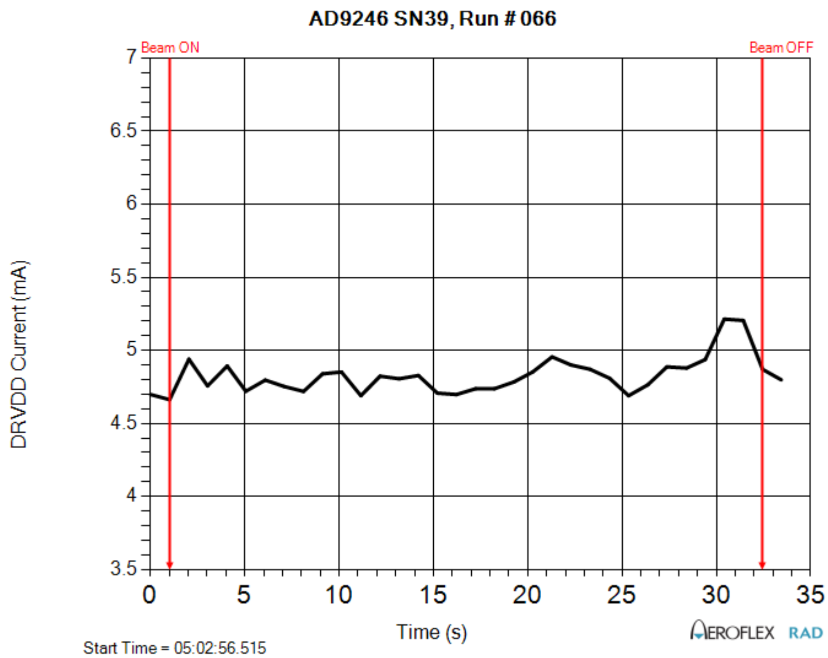

Figure F-6. AD9246 SN39, Run #66, DUT DRVDD Current (mA).

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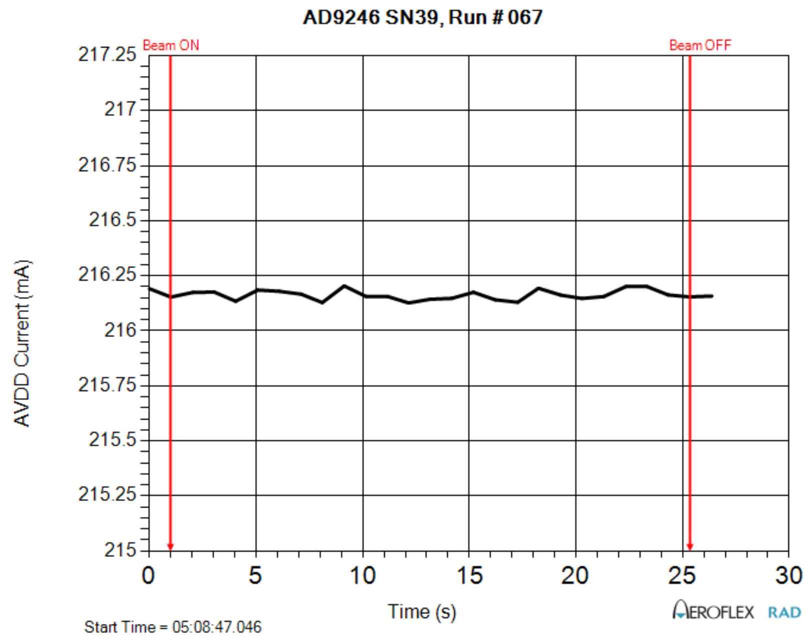

Figure F-7. AD9246 SN39, Run #67, DUT AVDD Current (mA).

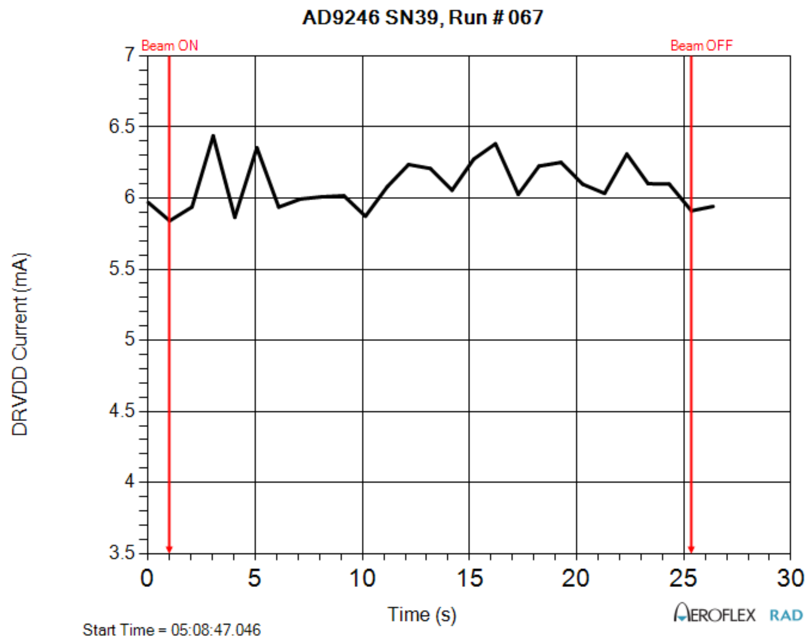

Figure F-8. AD9246 SN39, Run #67, DUT DRVDD Current (mA).

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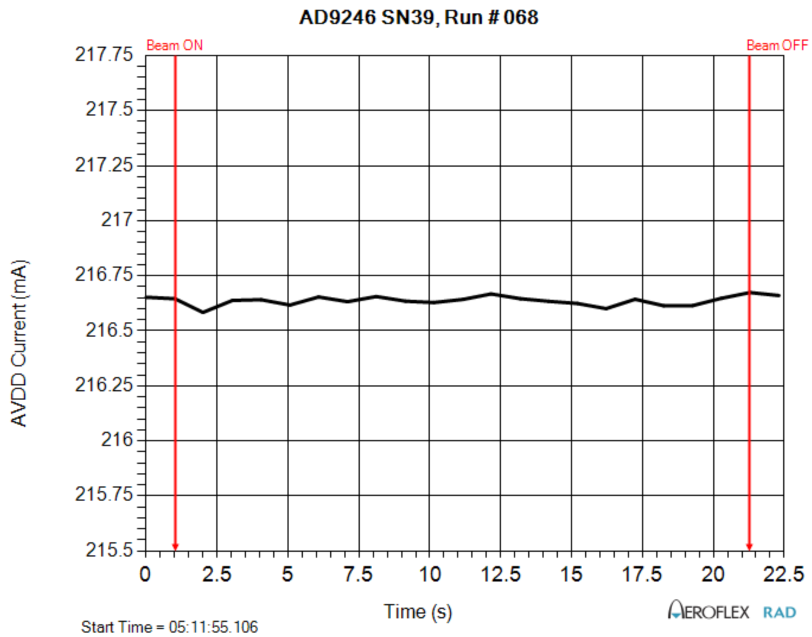

Figure F-9. AD9246 SN39, Run #68, DUT AVDD Current (mA).

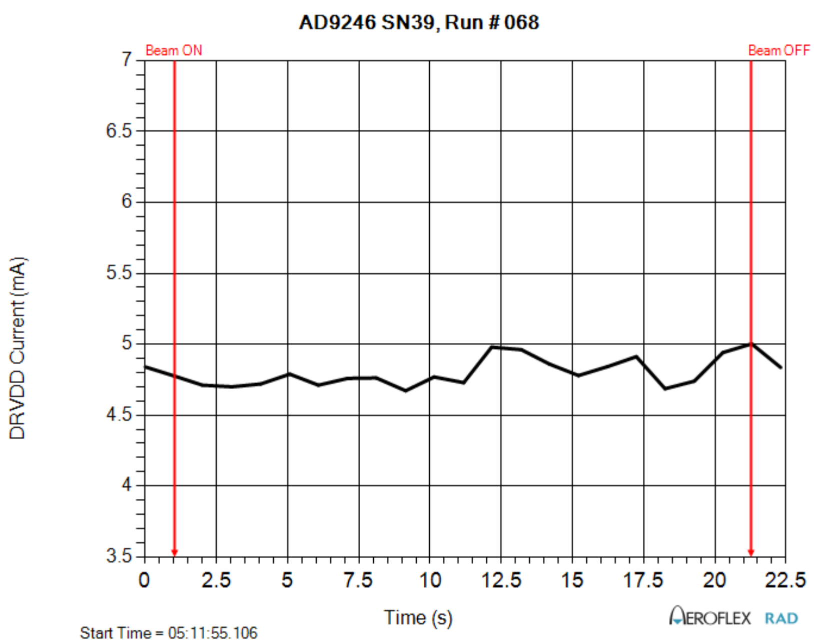

Figure F-10. AD9246 SN39, Run #68, DUT DRVDD Current (mA).

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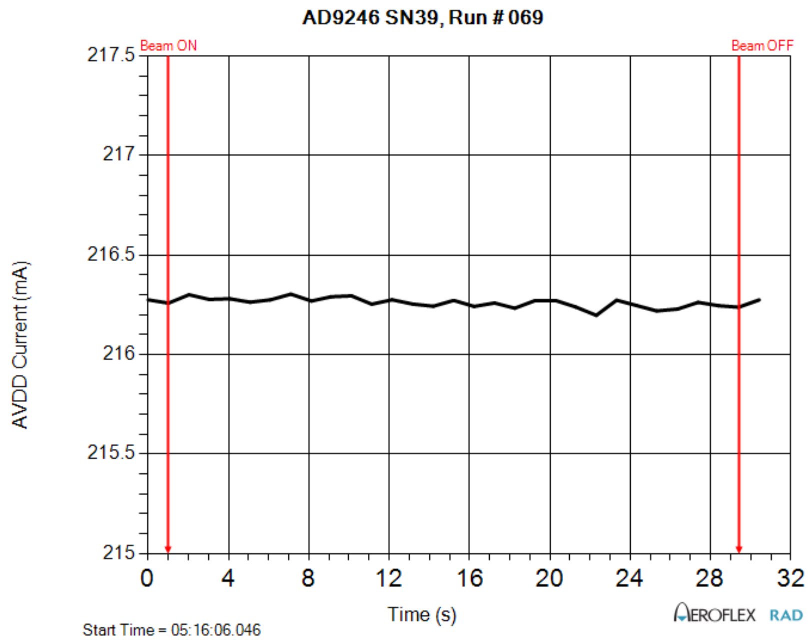

Figure F-11. AD9246 SN39, Run #69, DUT AVDD Current (mA).

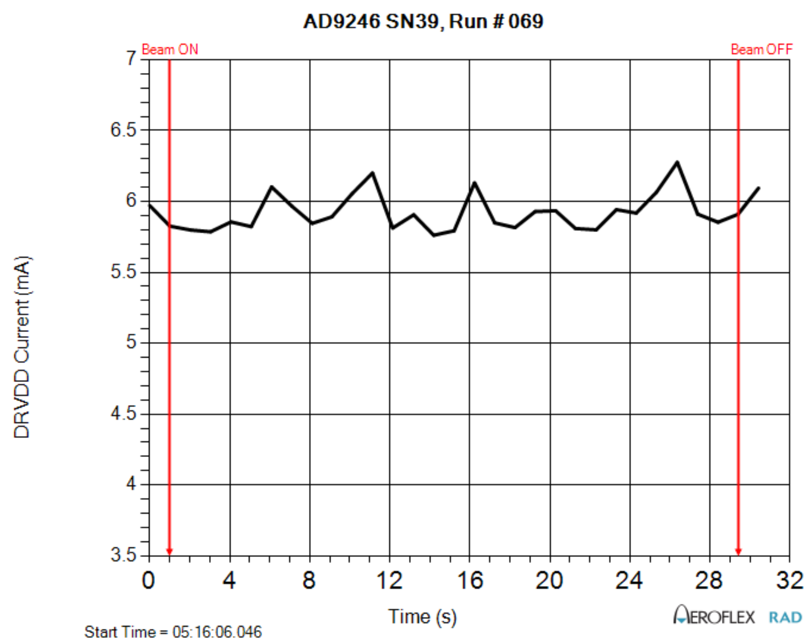

Figure F-12. AD9246 SN39, Run #69, DUT DRVDD Current (mA).

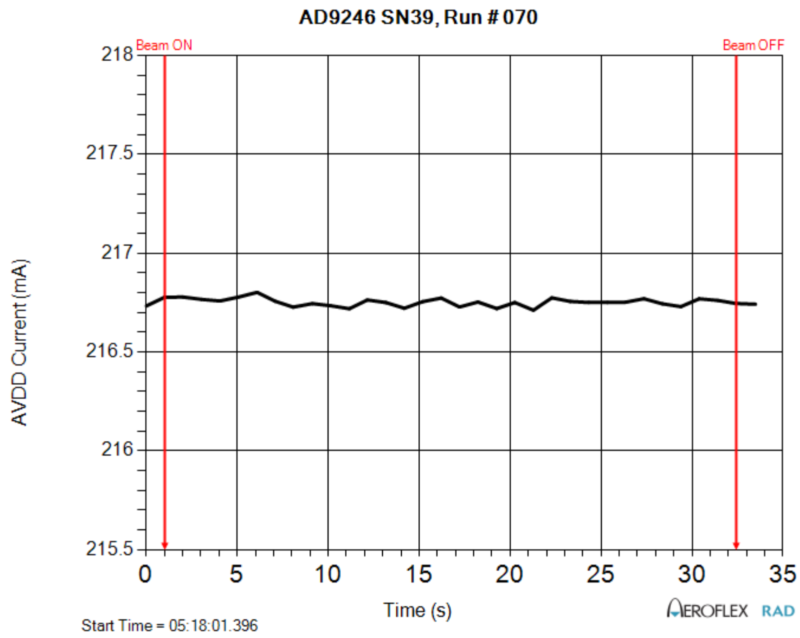

Figure F-13. AD9246 SN39, Run #70, DUT AVDD Current (mA).

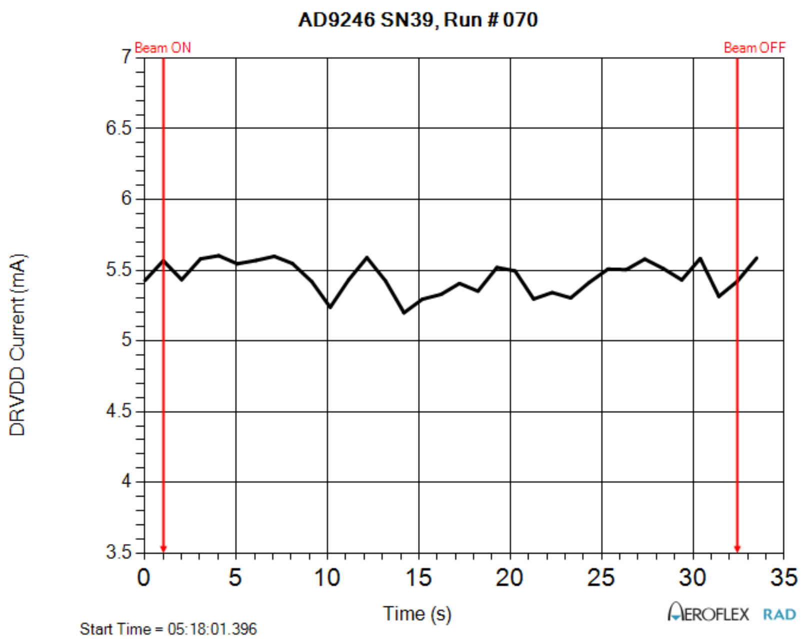

Figure F-14. AD9246 SN39, Run #70, DUT DRVDD Current (mA).

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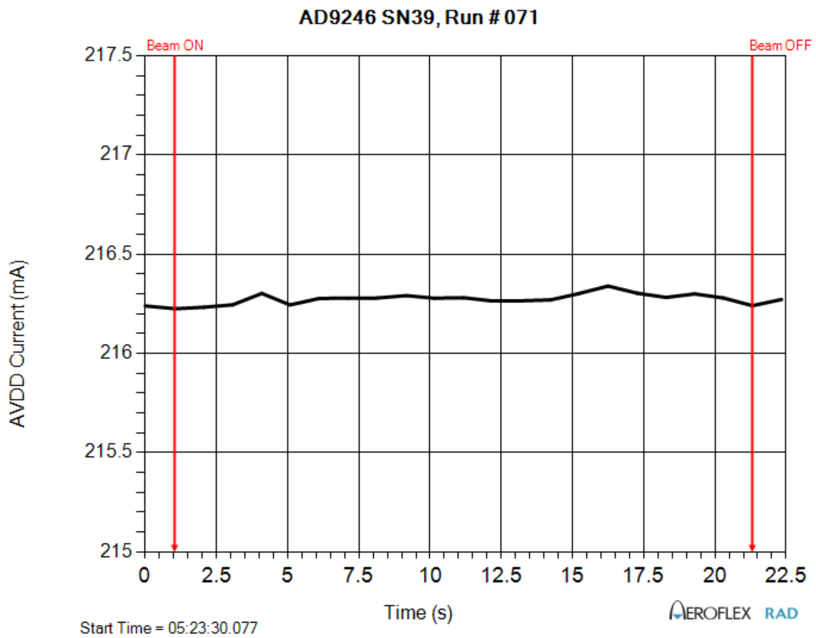

Figure F-15. AD9246 SN39, Run #71, DUT AVDD Current (mA).

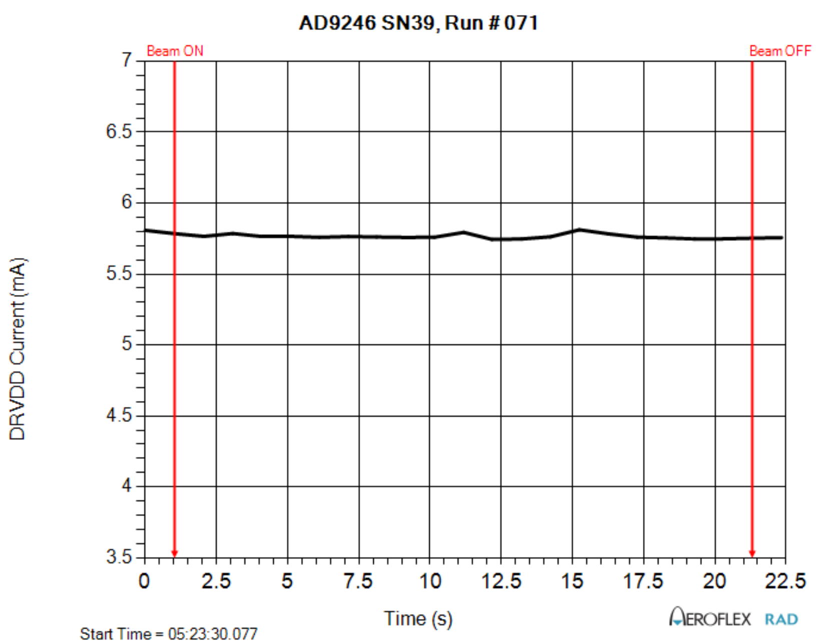

Figure F-16. AD9246 SN39, Run #71, DUT DRVDD Current (mA).

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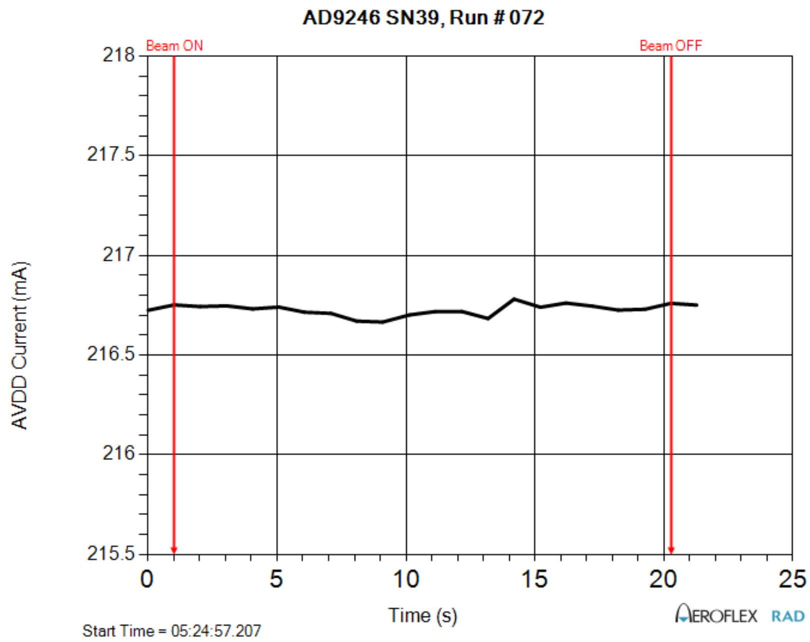

Figure F-17. AD9246 SN39, Run #72, DUT AVDD Current (mA).

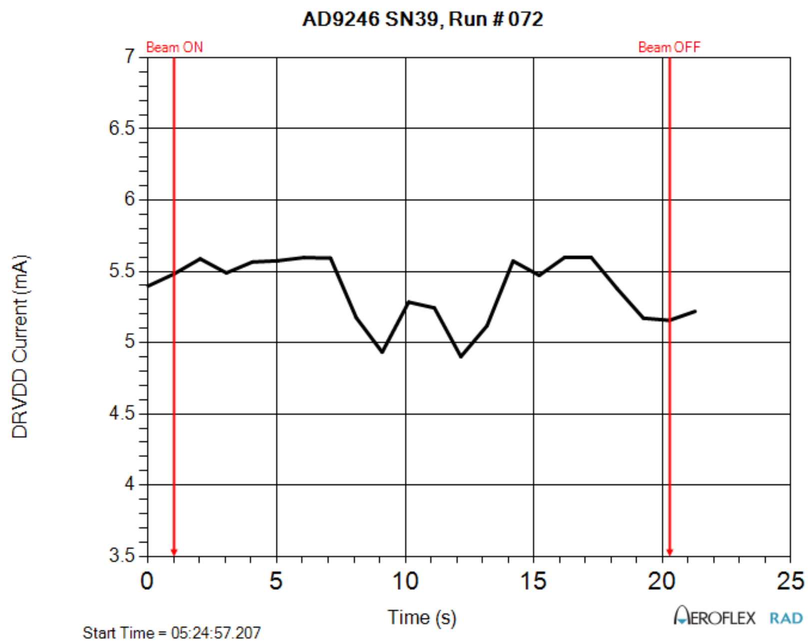

Figure F-18. AD9246 SN39, Run #72, DUT DRVDD Current (mA).

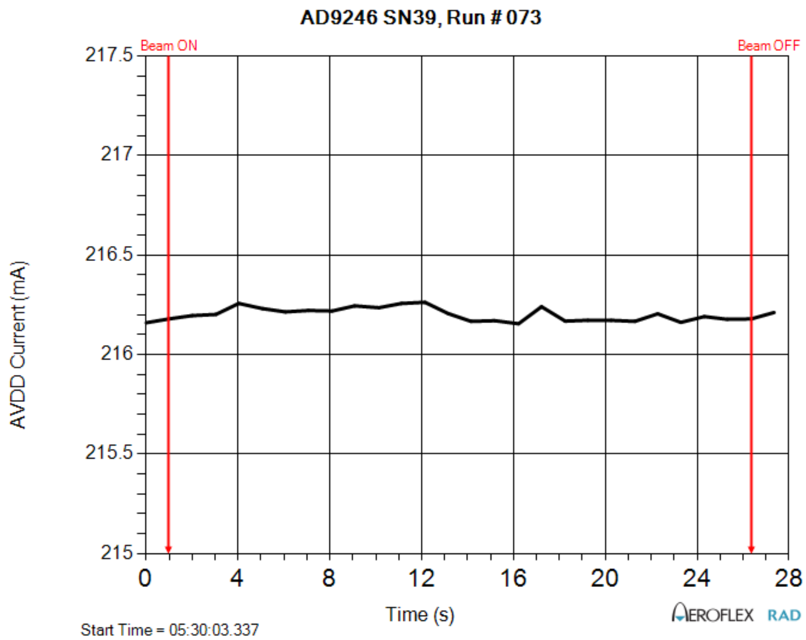

Figure F-19. AD9246 SN39, Run #73, DUT AVDD Current (mA).

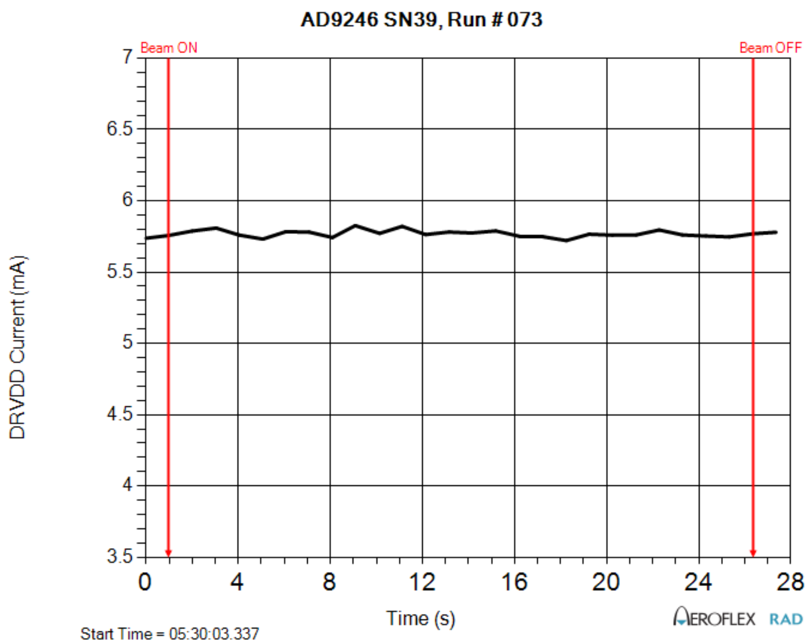

Figure F-20. AD9246 SN39, Run #73, DUT DRVDD Current (mA).

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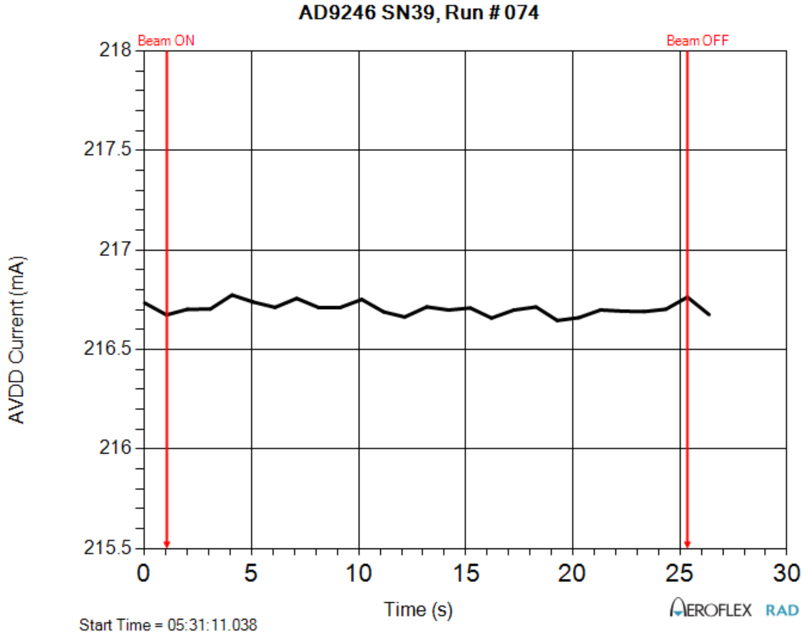

Figure F-21. AD9246 SN39, Run #74, DUT AVDD Current (mA).

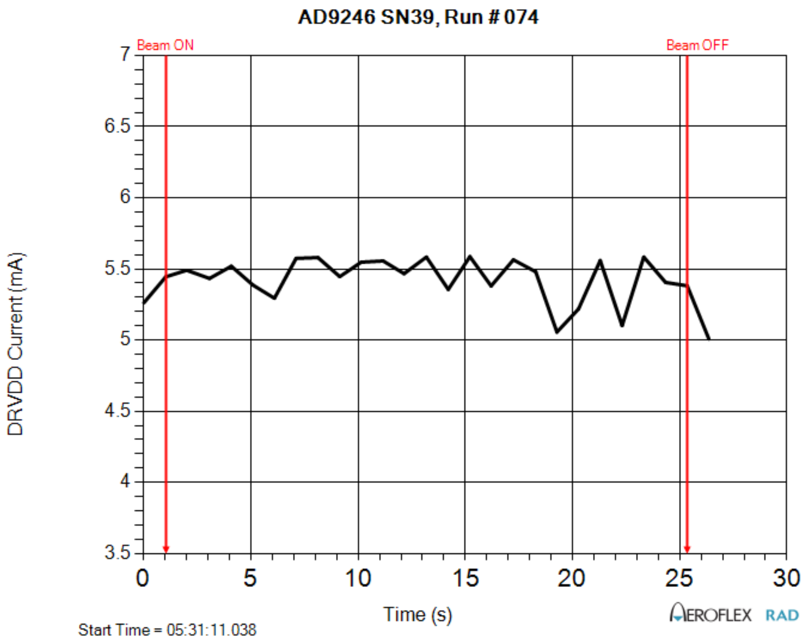

Figure F-22. AD9246 SN39, Run #74, DUT DRVDD Current (mA).

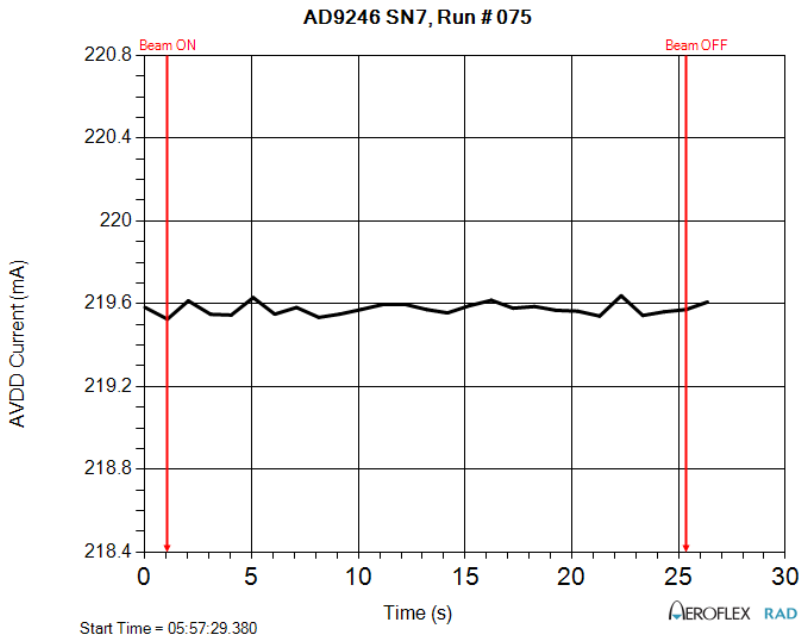

Figure F-23. AD9246 SN7, Run #75, DUT AVDD Current (mA).

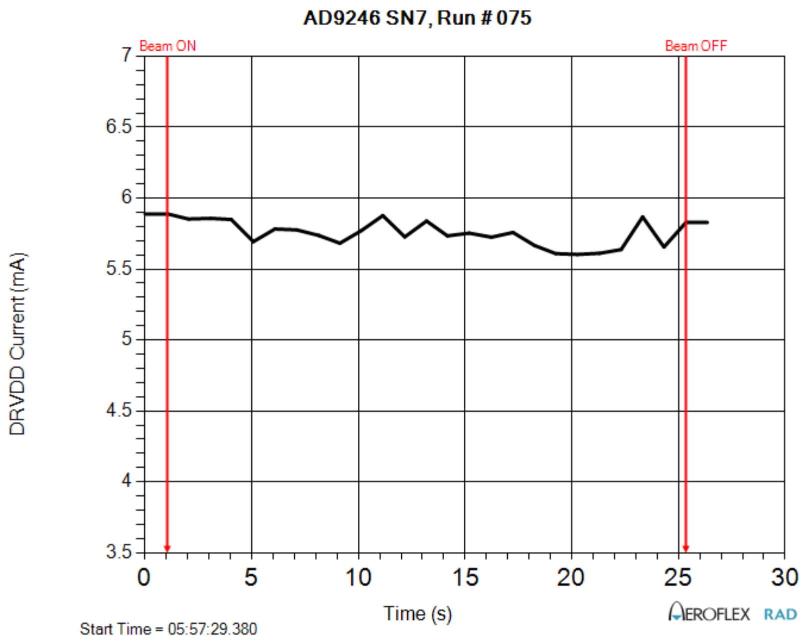

Figure F-24. AD9246 SN7, Run #75, DUT DRVDD Current (mA).

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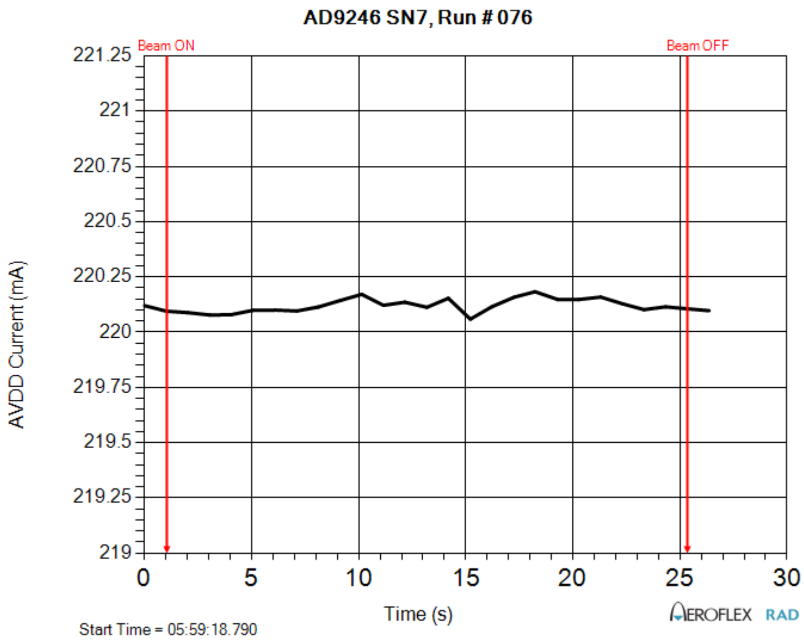

Figure F-25. AD9246 SN7, Run #76, DUT AVDD Current (mA).

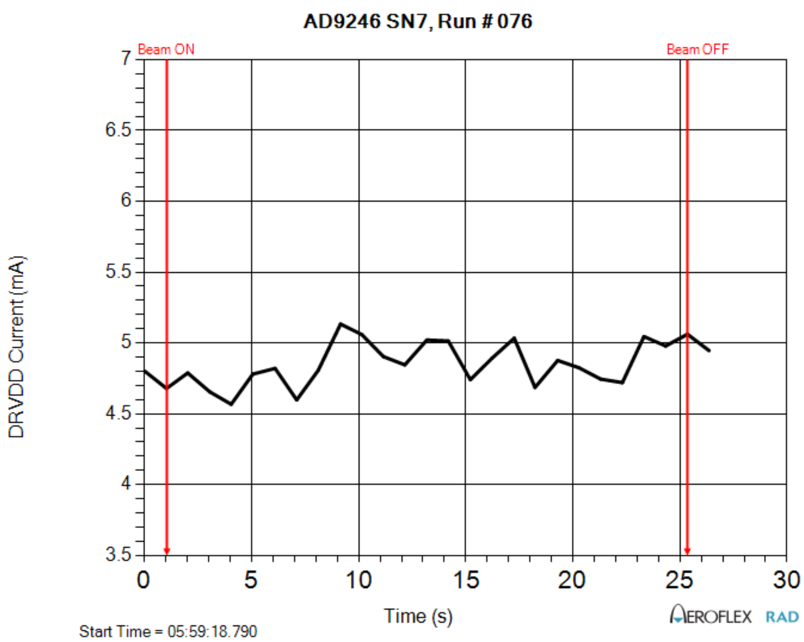

Figure F-26. AD9246 SN7, Run #76, DUT DRVDD Current (mA).

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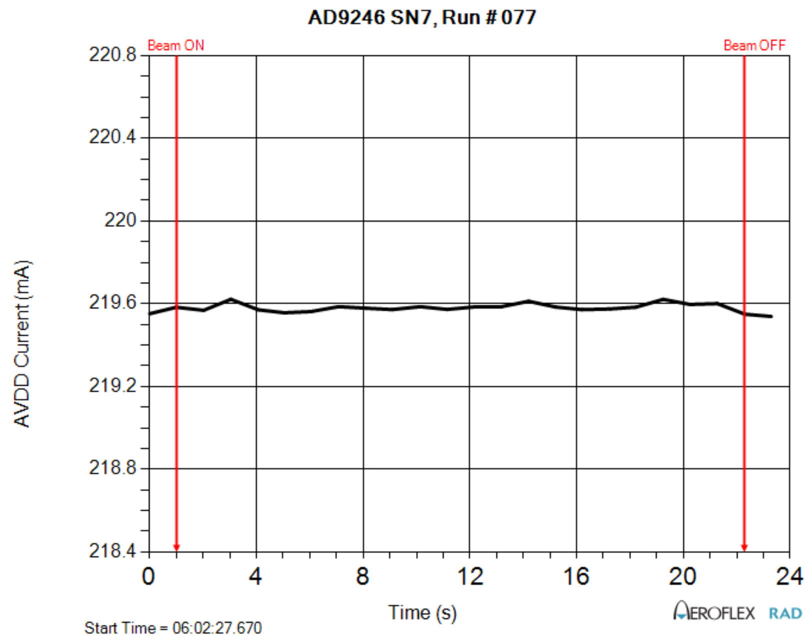

Figure F-27. AD9246 SN7, Run #77, DUT AVDD Current (mA).

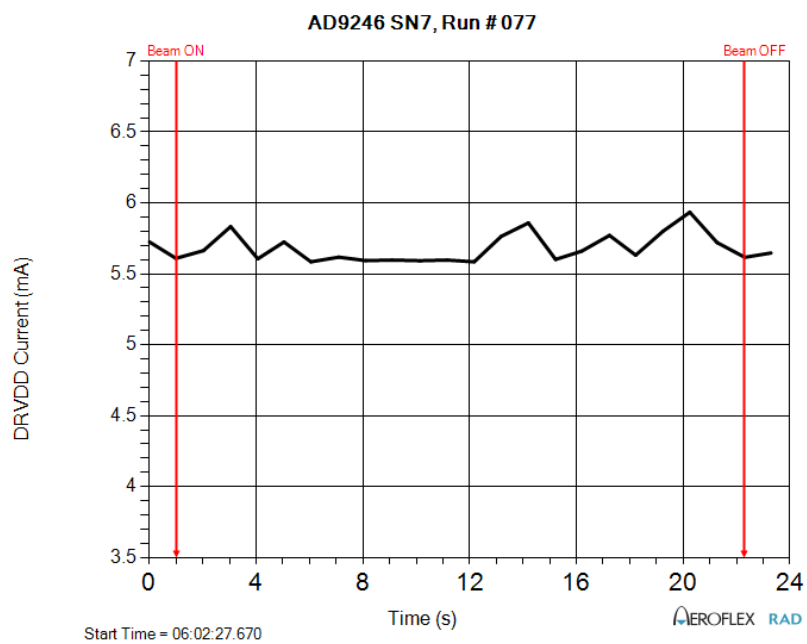

Figure F-28. AD9246 SN7, Run #77, DUT DRVDD Current (mA).

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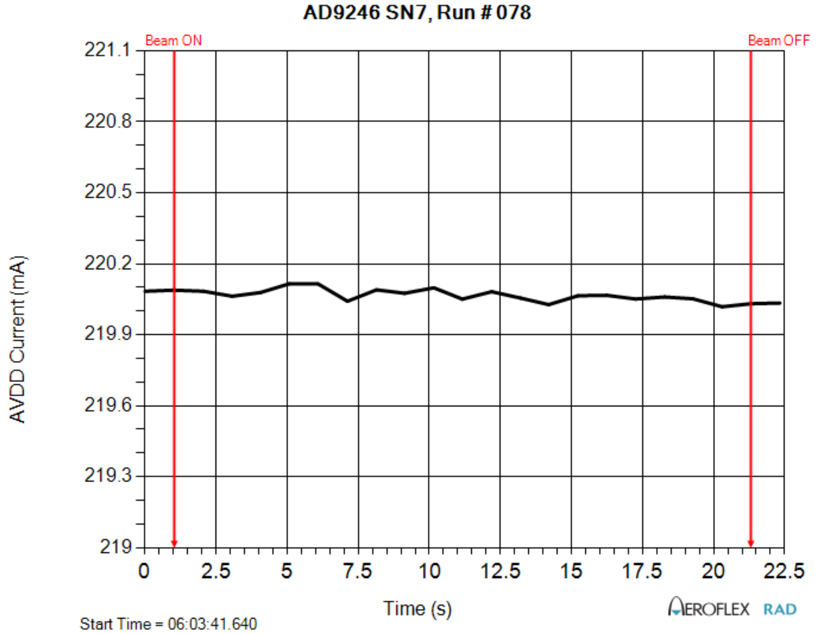

Figure F-29. AD9246 SN7, Run #78, DUT AVDD Current (mA).

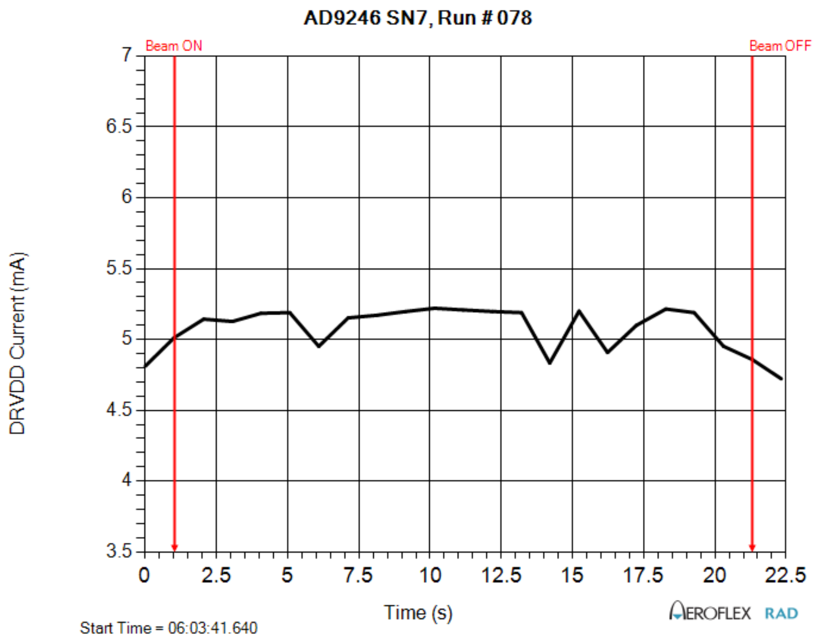

Figure F-30. AD9246 SN7, Run #78, DUT DRVDD Current (mA).

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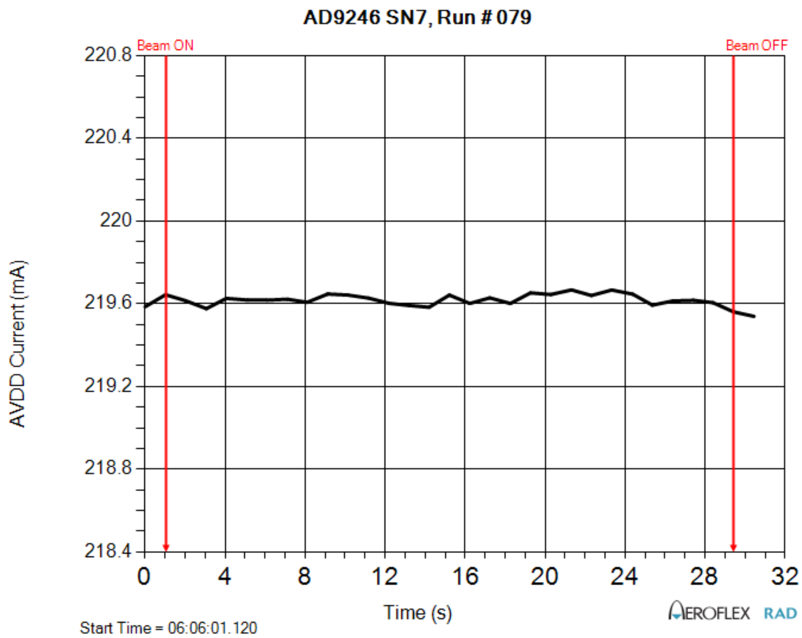

Figure F-31. AD9246 SN7, Run #79, DUT AVDD Current (mA).

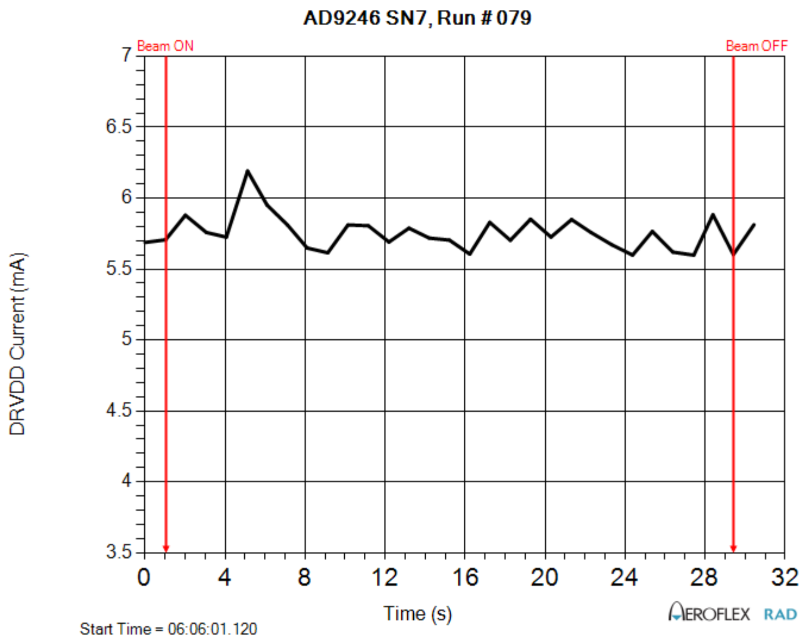

Figure F-32. AD9246 SN7, Run #79, DUT DRVDD Current (mA).

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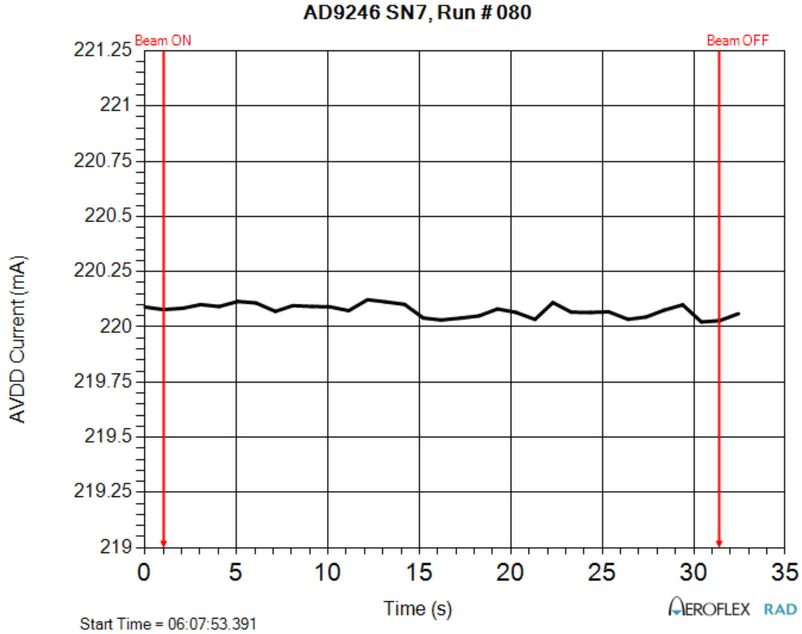

Figure F-33. AD9246 SN7, Run #80, DUT AVDD Current (mA).

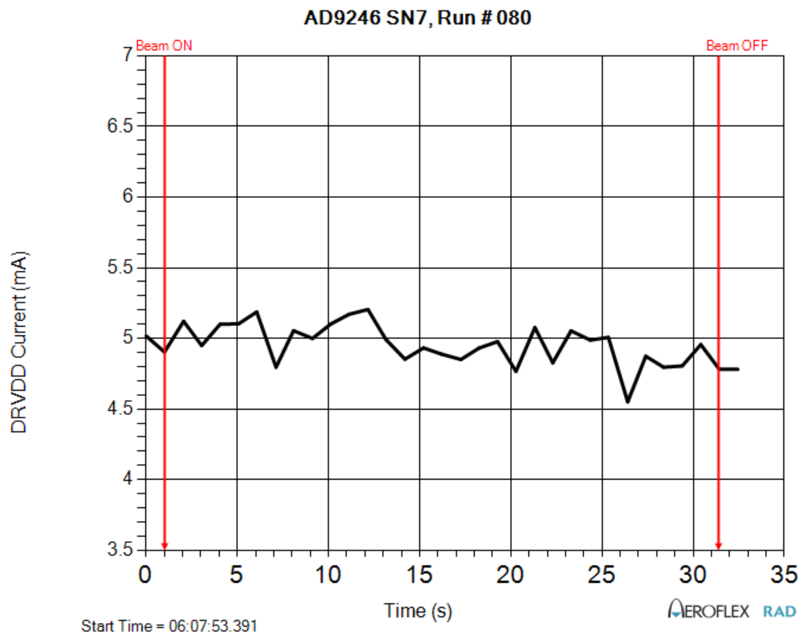

Figure F-34. AD9246 SN7, Run #80, DUT DRVDD Current (mA).

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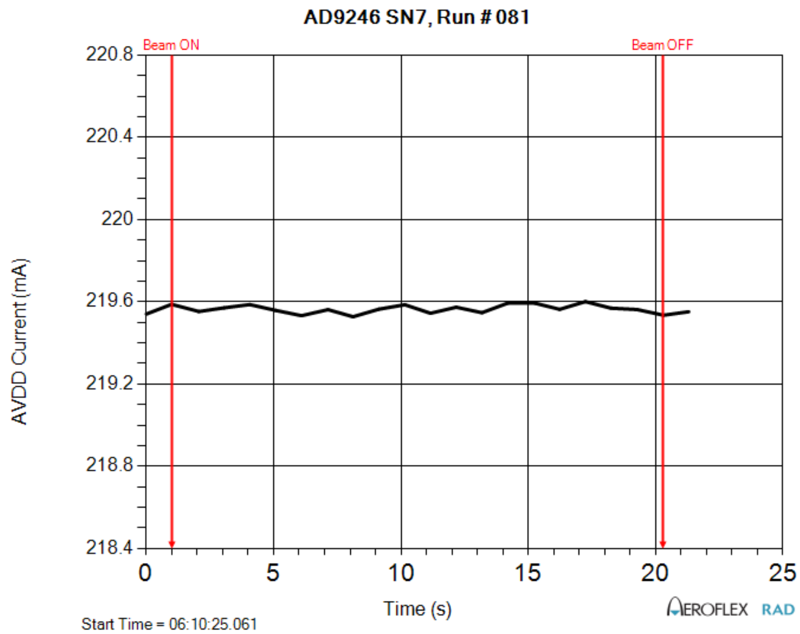

Figure F-35. AD9246 SN7, Run #81, DUT AVDD Current (mA).

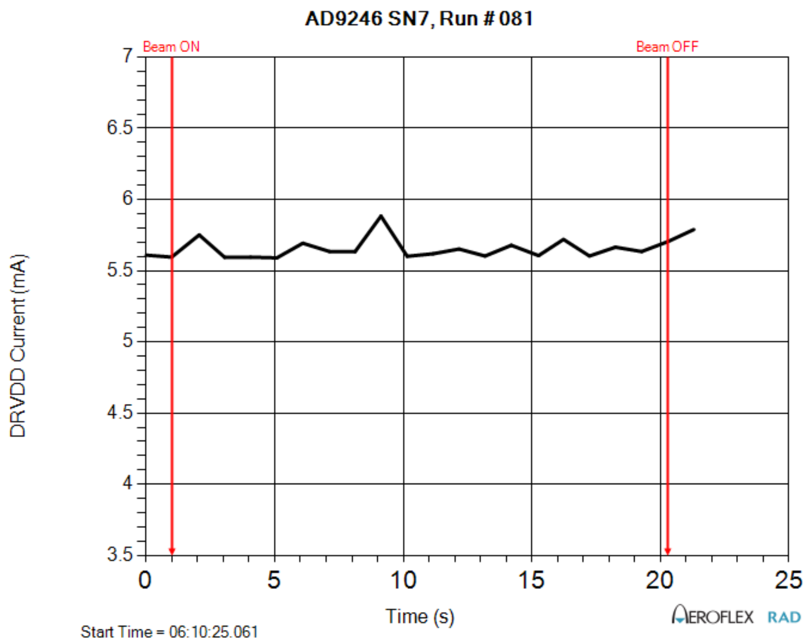

Figure F-36. AD9246 SN7, Run #81, DUT DRVDD Current (mA).

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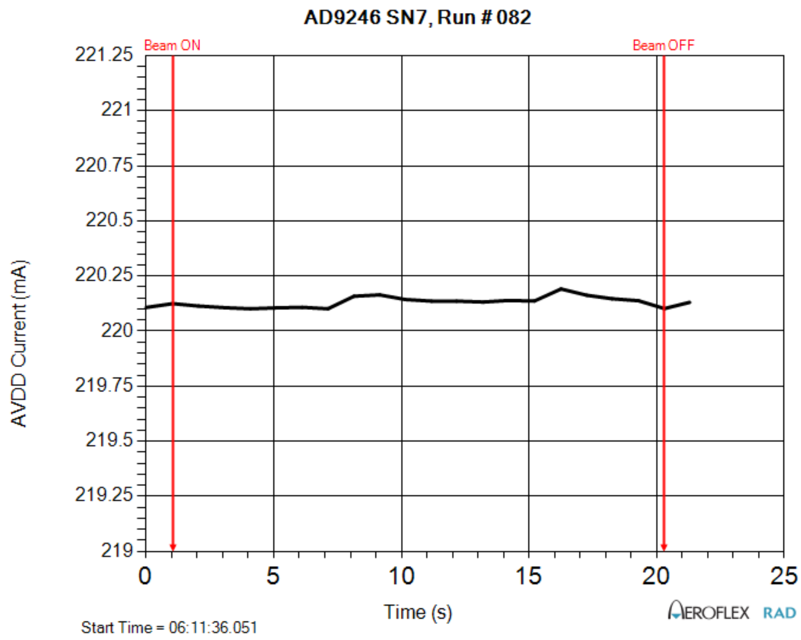

Figure F-37. AD9246 SN7, Run #82, DUT AVDD Current (mA).

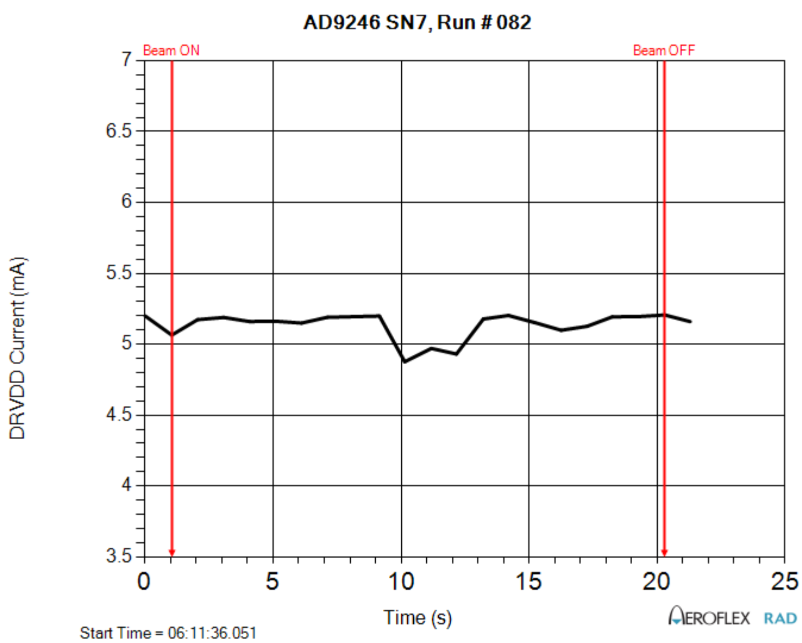

Figure F-38. AD9246 SN7, Run #82, DUT DRVDD Current (mA).

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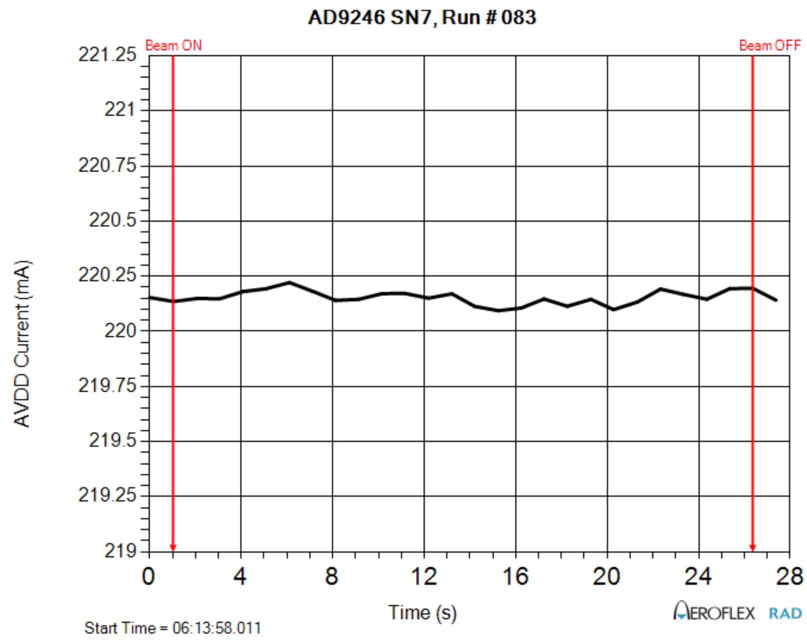

Figure F-39. AD9246 SN7, Run #83, DUT AVDD Current (mA).

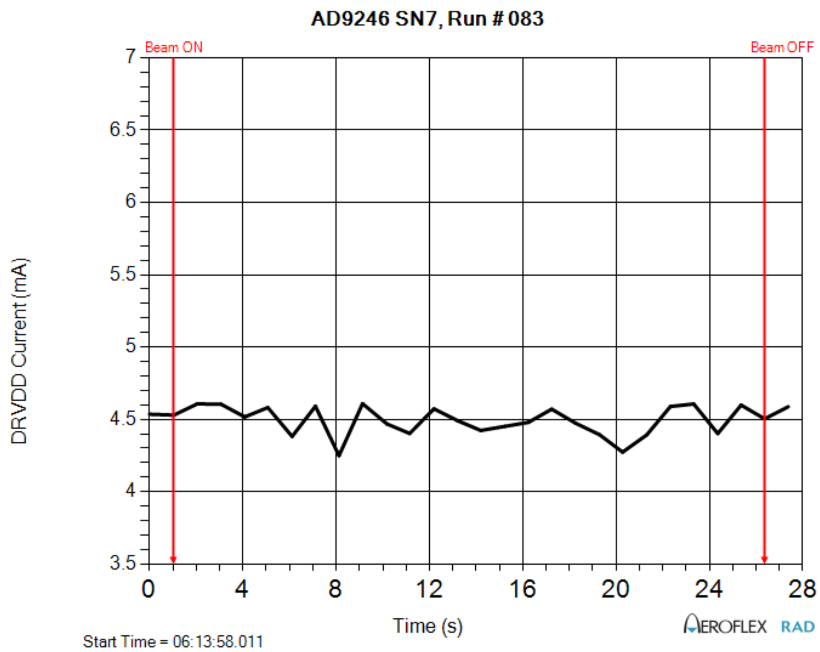

Figure F-40. AD9246 SN7, Run #83, DUT DRVDD Current (mA).

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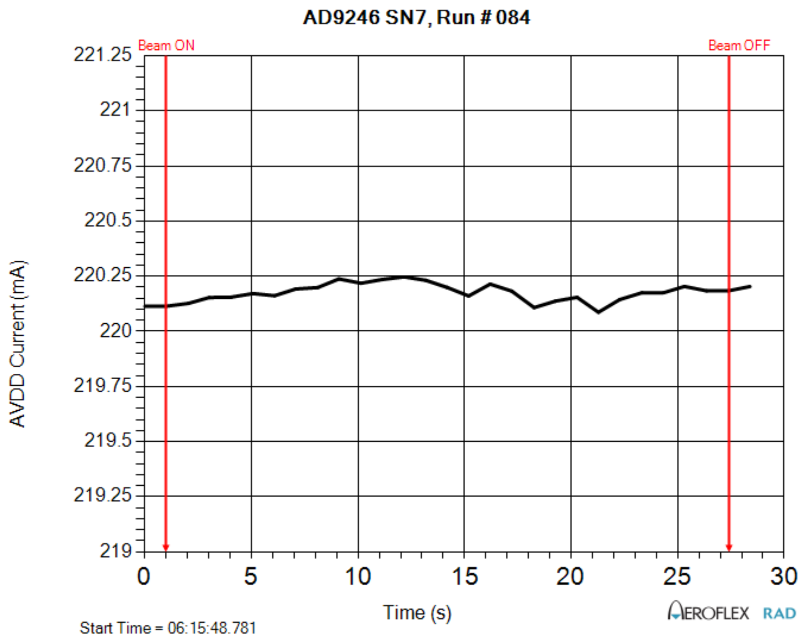

Figure F-41. AD9246 SN7, Run #84, DUT AVDD Current (mA).

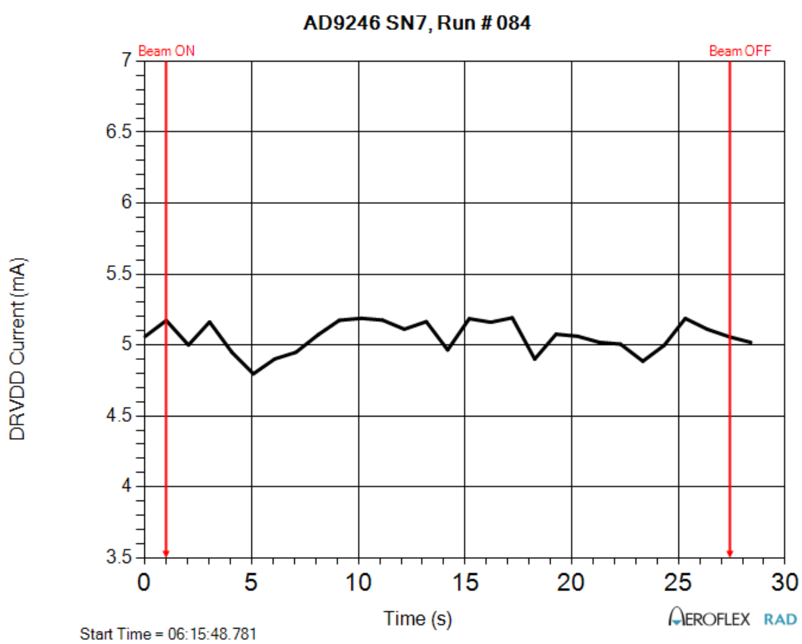

Figure F-42. AD9246 SN7, Run #84, DUT DRVDD Current (mA).

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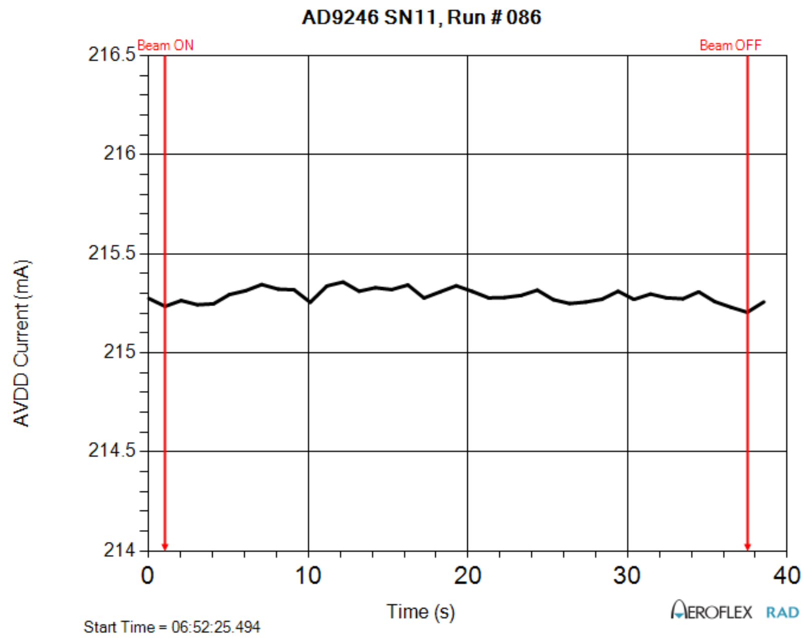

Figure F-43. AD9246 SN11, Run #85, DUT AVDD Current (mA).

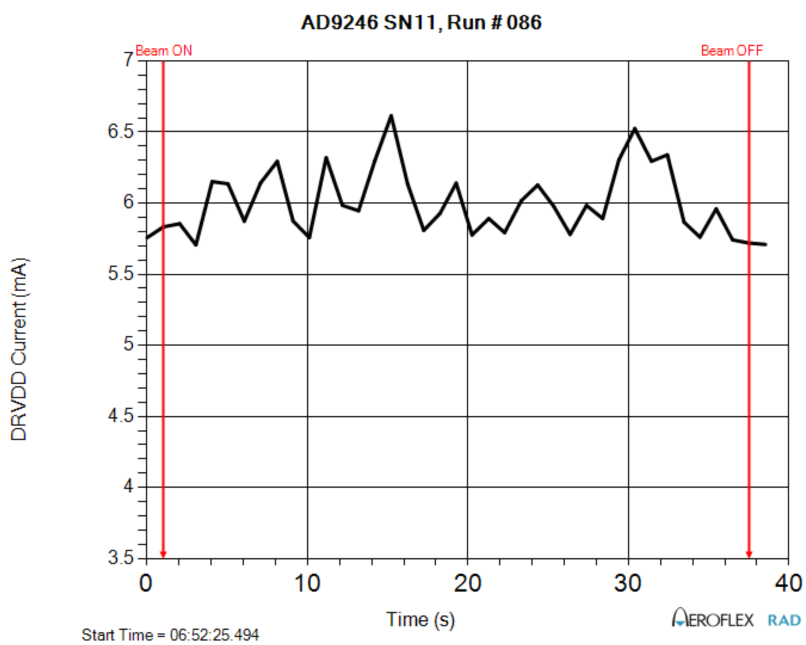

Figure F-44. AD9246 SN11, Run #85, DUT DRVDD Current (mA).

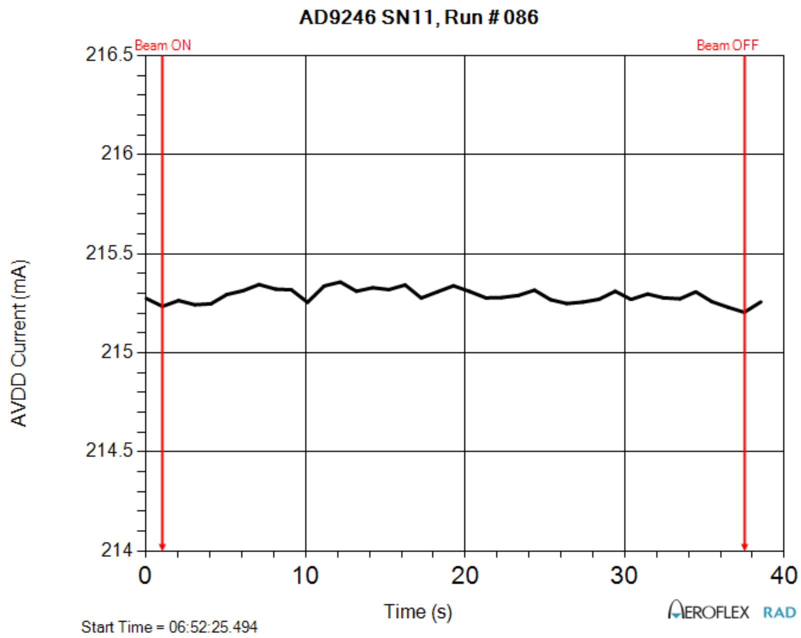

Figure F-45. AD9246 SN11, Run #86, DUT AVDD Current (mA).

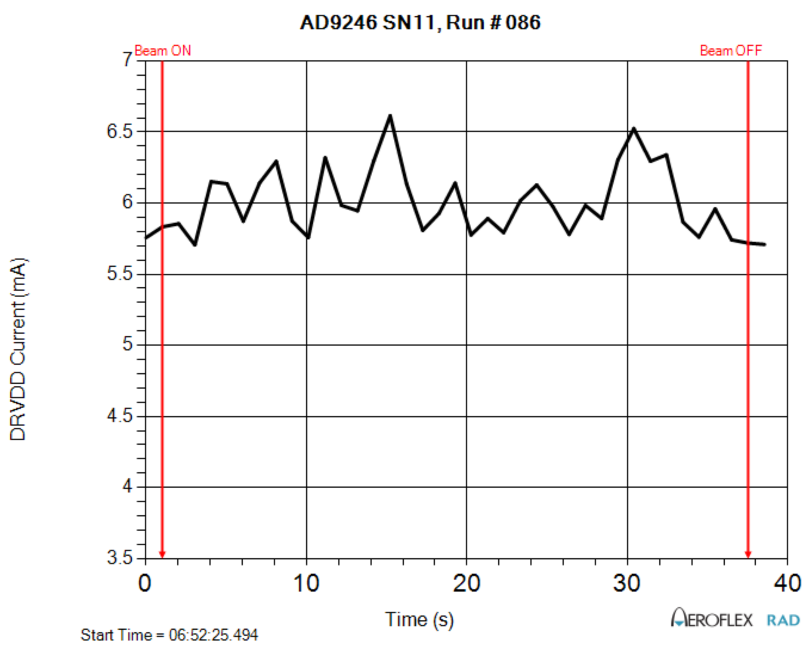

Figure F-46. AD9246 SN11, Run #86, DUT DRVDD Current (mA).

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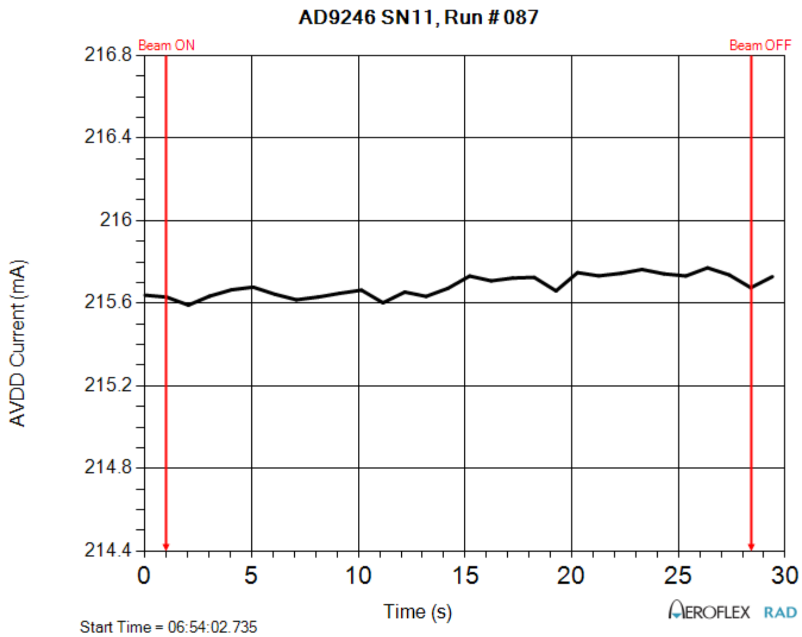

Figure F-47. AD9246 SN11, Run #87, DUT AVDD Current (mA).

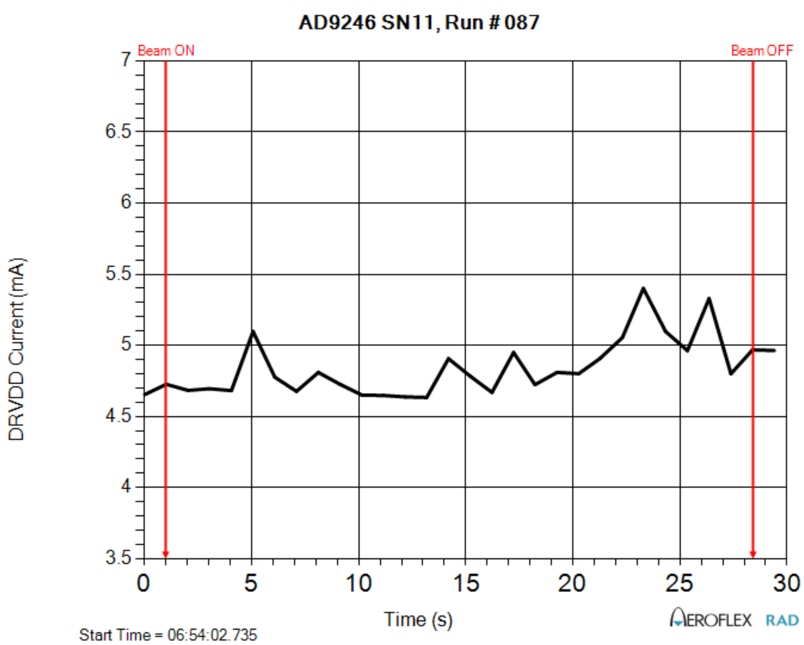

Figure F-48. AD9246 SN11, Run #87, DUT DRVDD Current (mA).

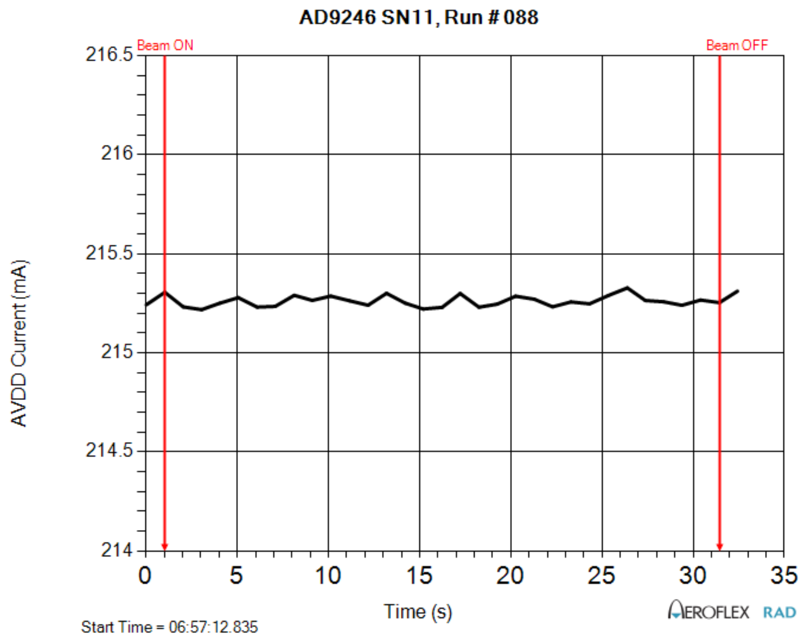

Figure F-49. AD9246 SN11, Run #88, DUT AVDD Current (mA).

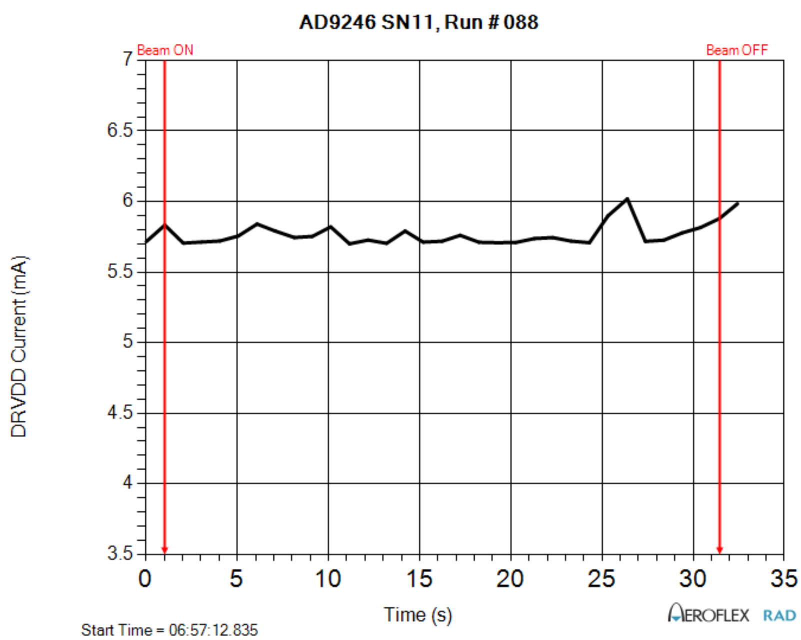

Figure F-50. AD9246 SN11, Run #88, DUT DRVDD Current (mA).

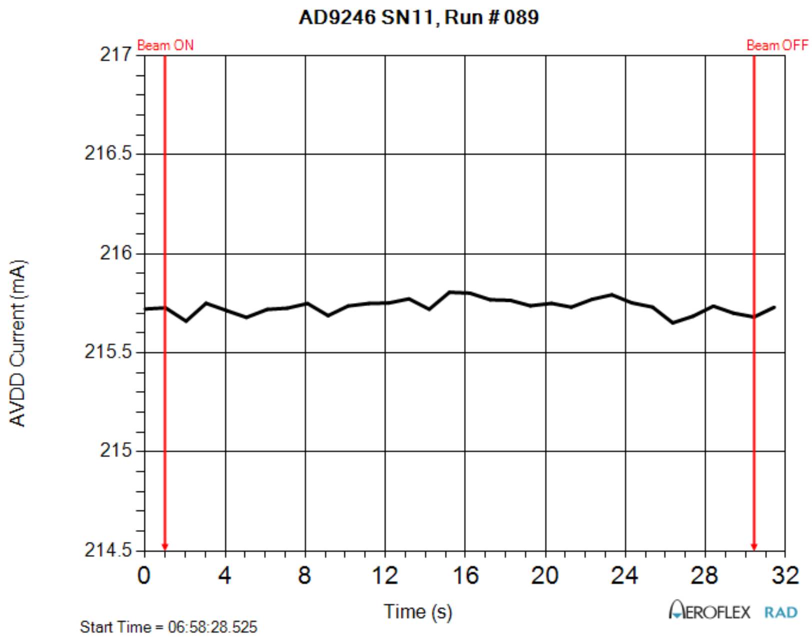

Figure F-51. AD9246 SN11, Run #89, DUT AVDD Current (mA).

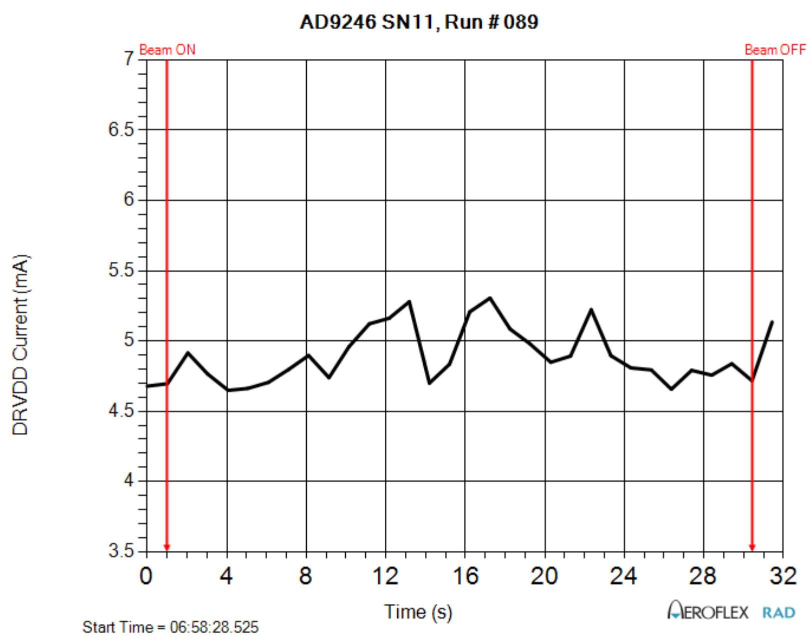

Figure F-52. AD9246 SN11, Run #89, DUT DRVDD Current (mA).

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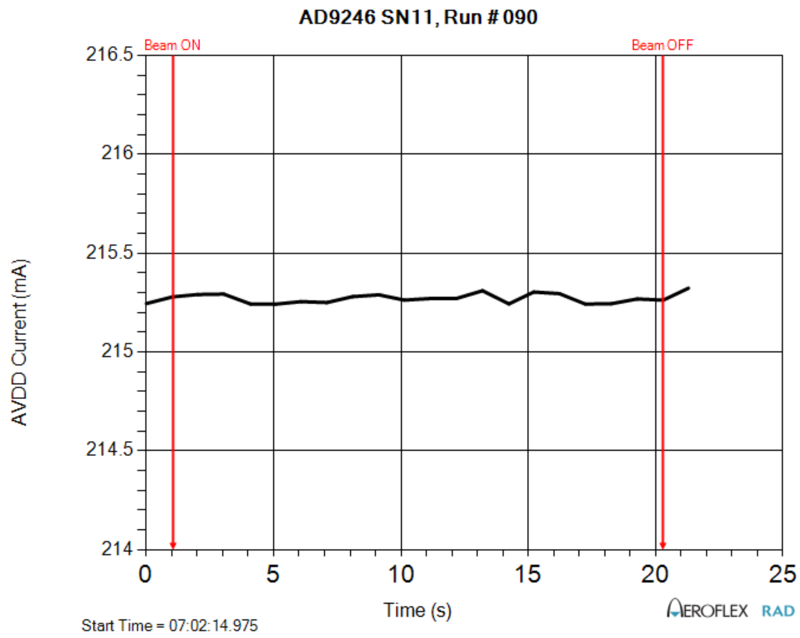

Figure F-53. AD9246 SN11, Run #90, DUT AVDD Current (mA).

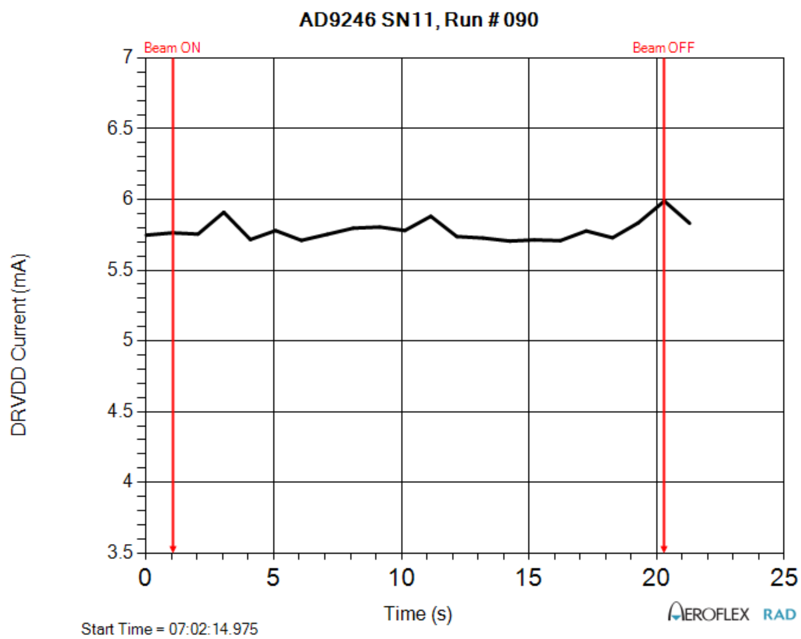

Figure F-54. AD9246 SN11, Run #90, DUT DRVDD Current (mA).

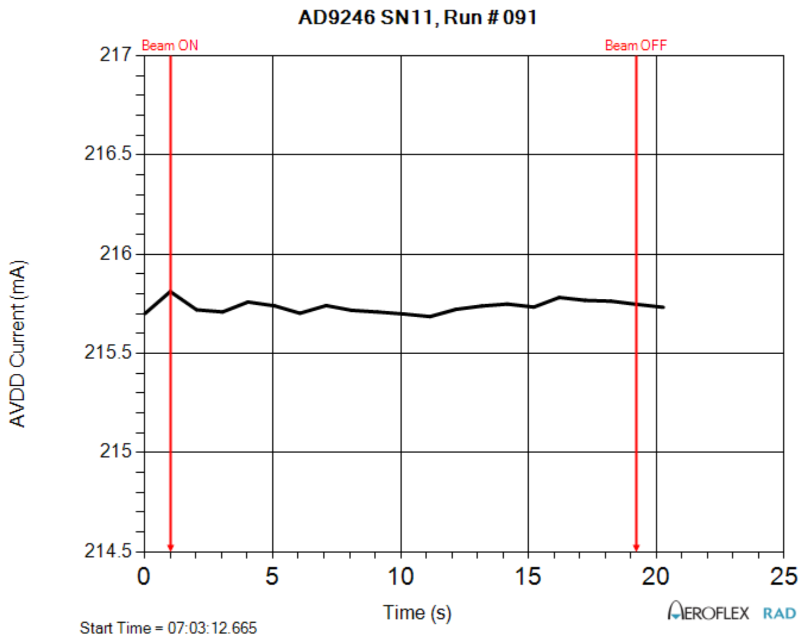

Figure F-55. AD9246 SN11, Run #91, DUT AVDD Current (mA).

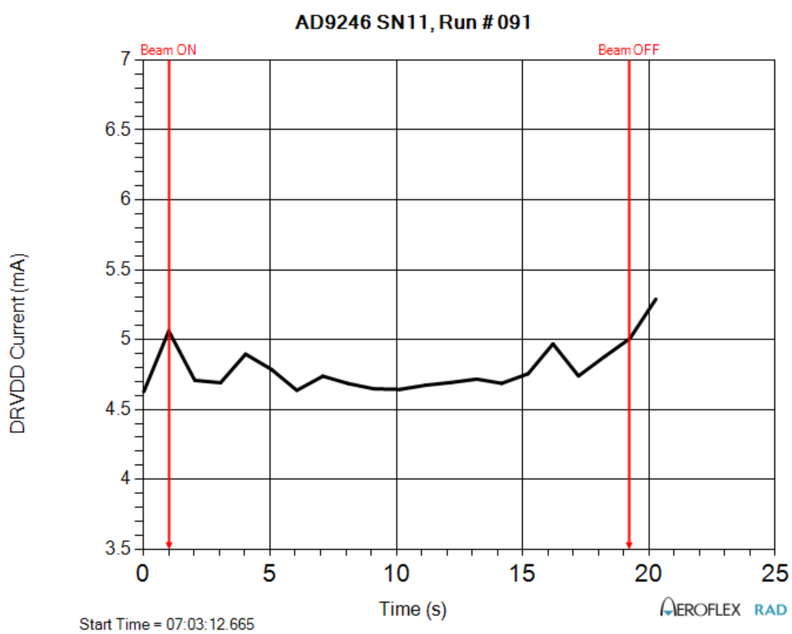

Figure F-56. AD9246 SN11, Run #91, DUT DRVDD Current (mA).

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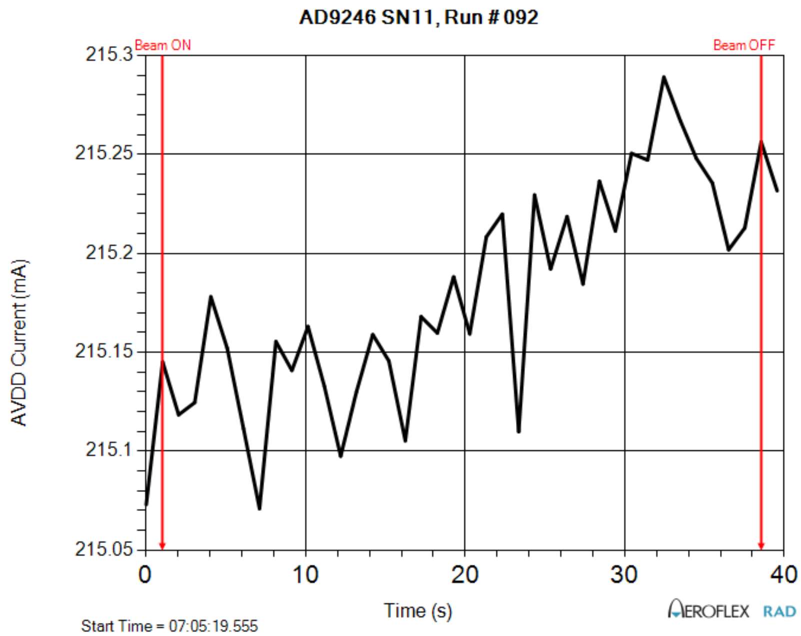

Figure F-57. AD9246 SN11, Run #92, DUT AVDD Current (mA).

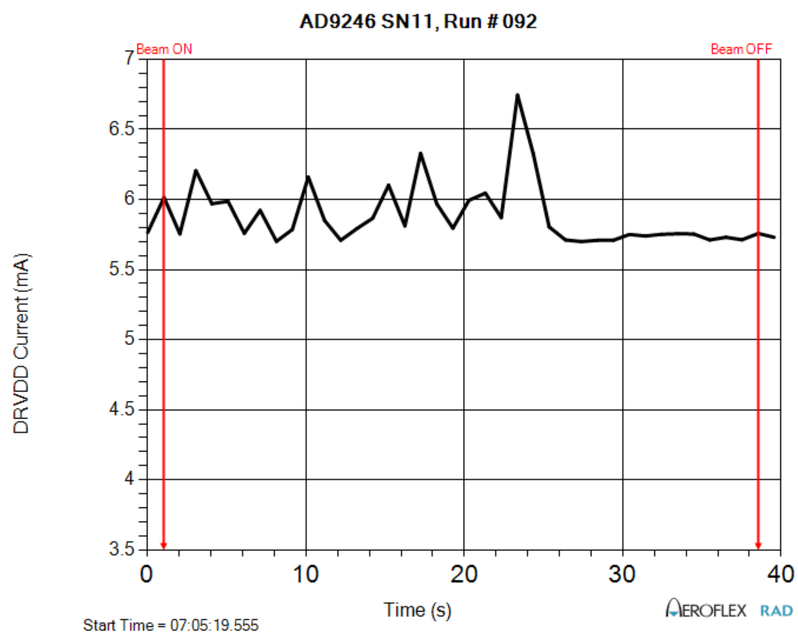

Figure F-58. AD9246 SN11, Run #92, DUT DRVDD Current (mA).

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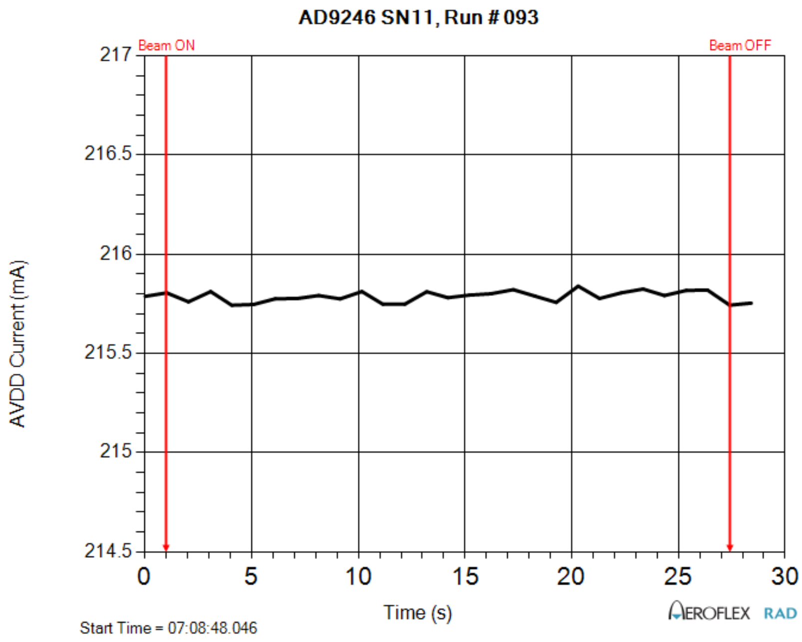

Figure F-59. AD9246 SN11, Run #93, DUT AVDD Current (mA).

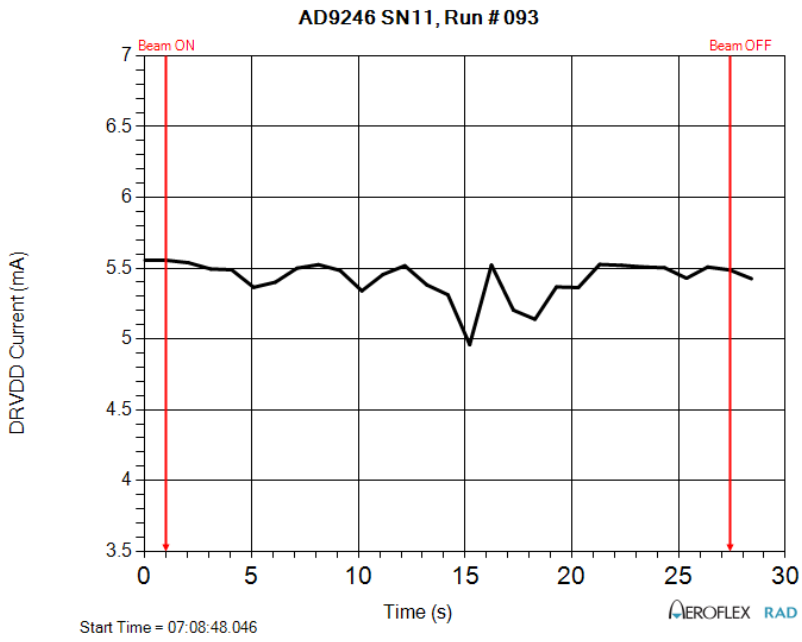

Figure F-60. AD9246 SN11, Run #93, DUT DRVDD Current (mA).

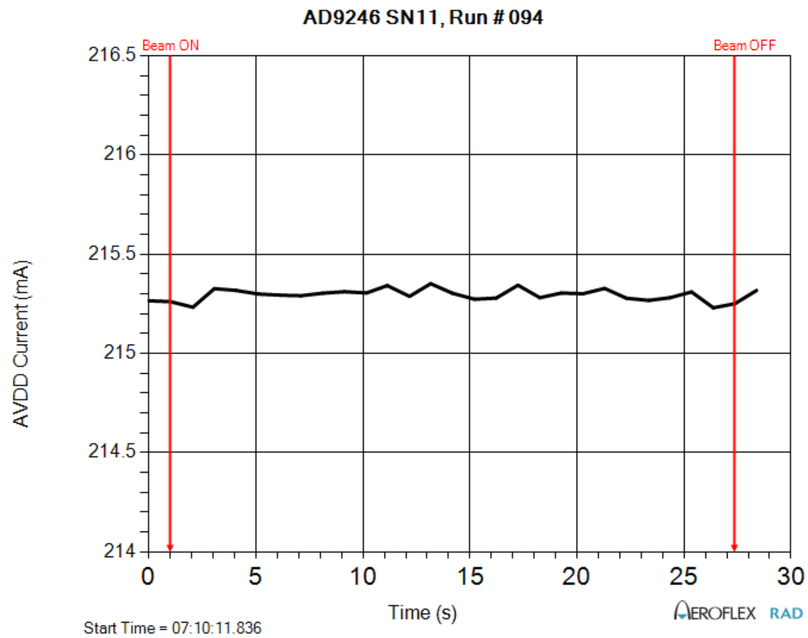

Figure F-61. AD9246 SN11, Run #94, DUT AVDD Current (mA).

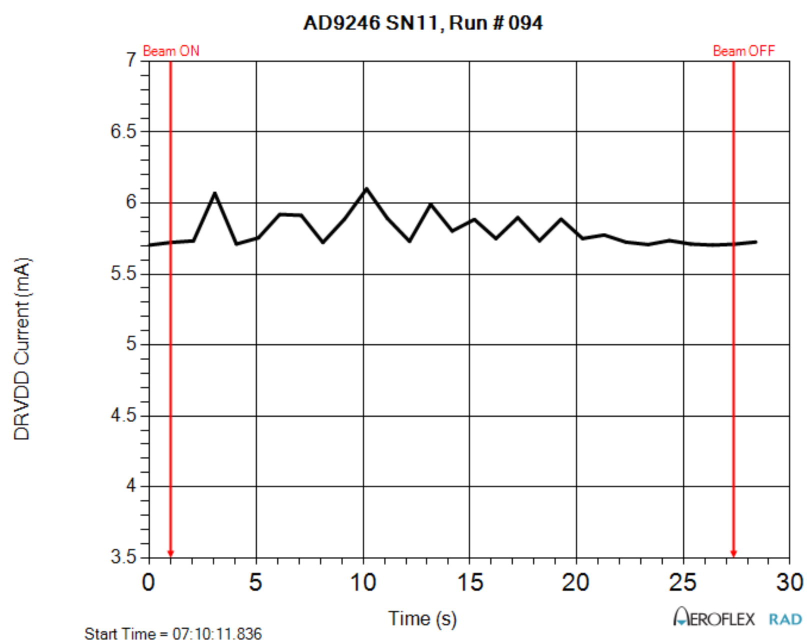

Figure F-62. AD9246 SN11, Run #94, DUT DRVDD Current (mA).

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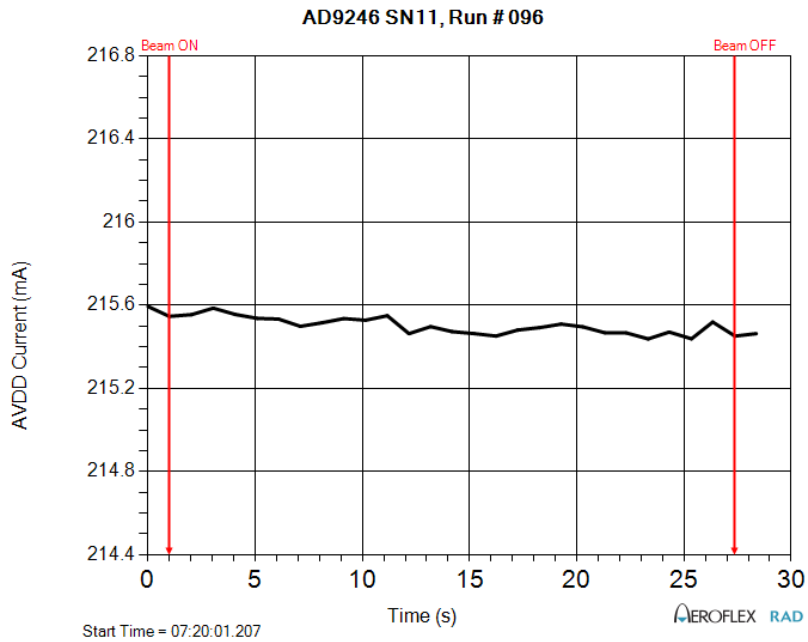

Figure F-63. AD9246 SN11, Run #95, DUT AVDD Current (mA).

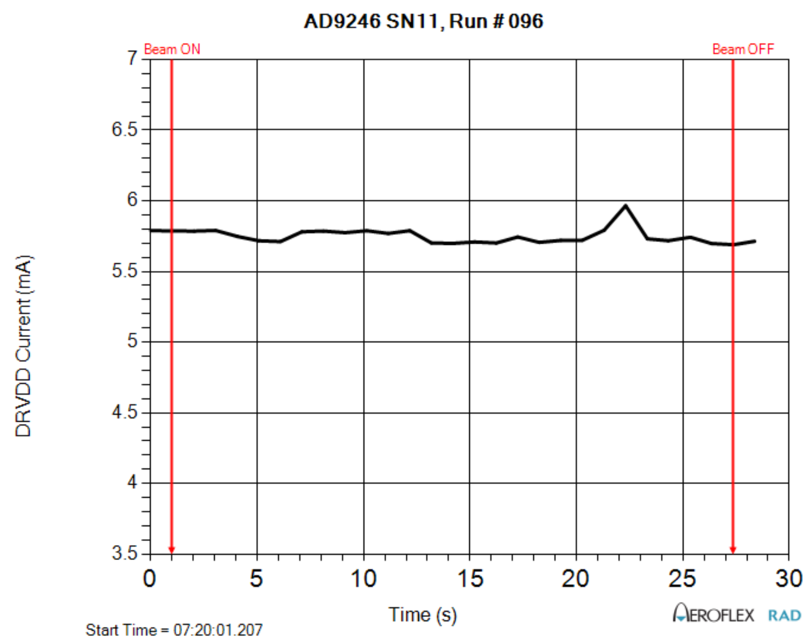

Figure F-64. AD9246 SN11, Run #95, DUT DRVDD Current (mA).

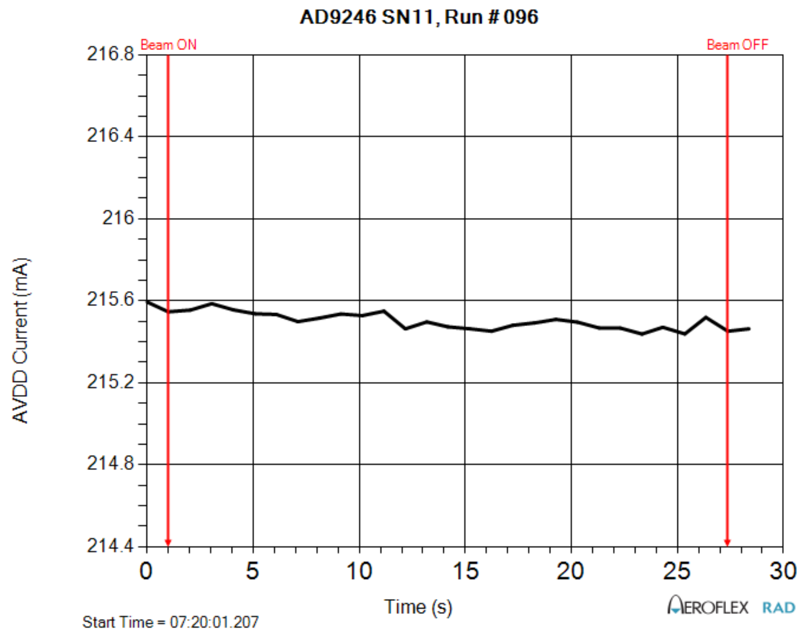

Figure F-65. AD9246 SN11, Run #96, DUT AVDD Current (mA).

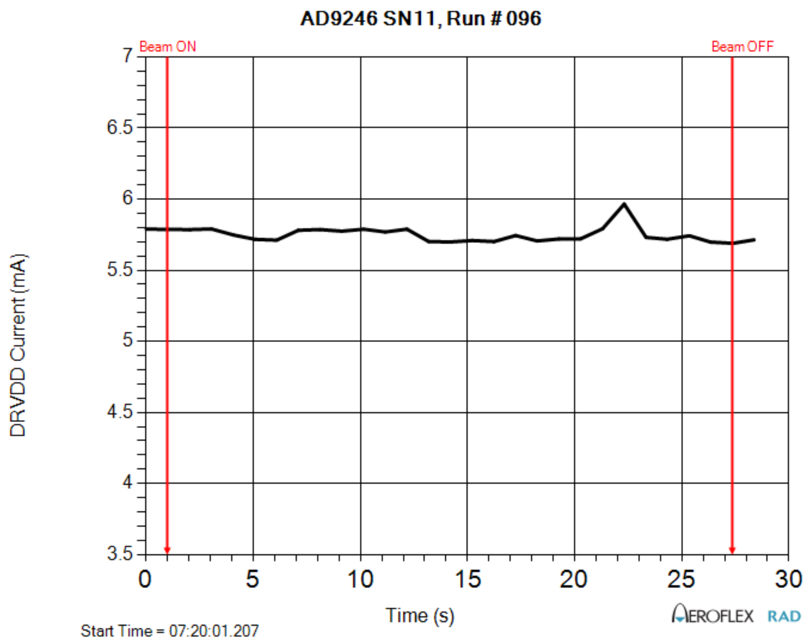

Figure F-66. AD9246 SN11, Run #96, DUT DRVDD Current (mA).

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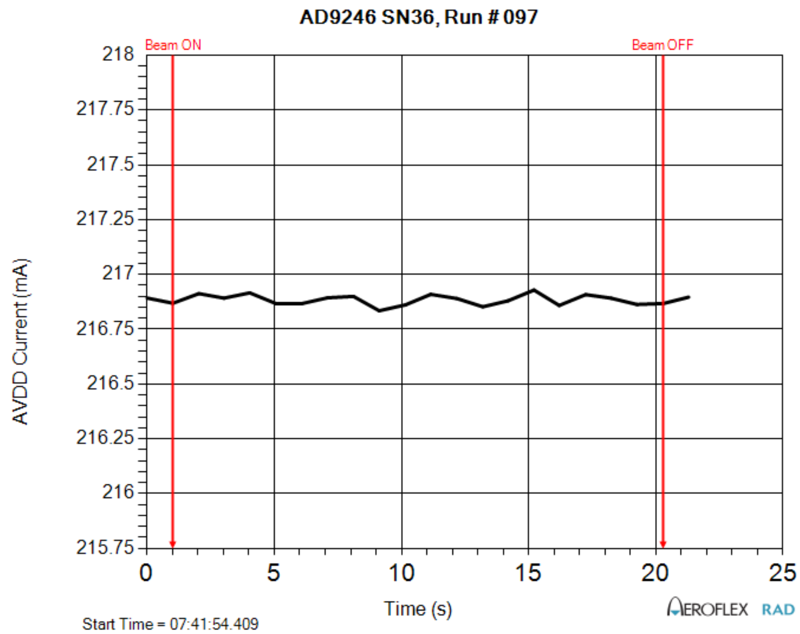

Figure F-67. AD9246 SN36, Run #97, DUT AVDD Current (mA).

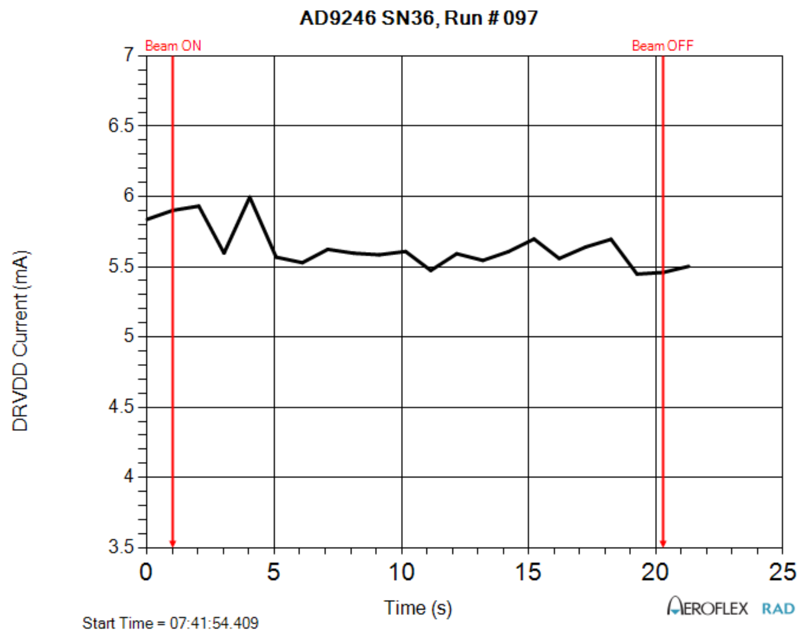

Figure F-68. AD9246 SN36, Run #97, DUT DRVDD Current (mA).

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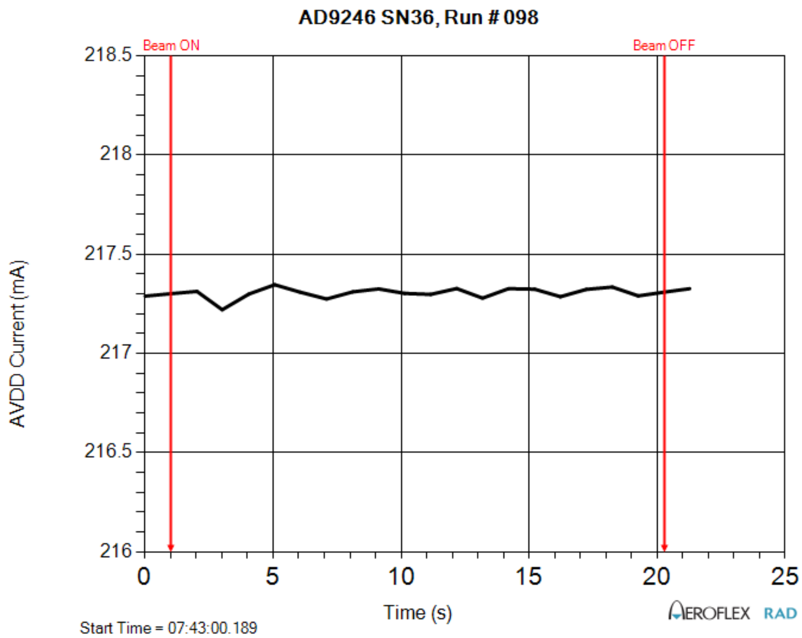

Figure F-69. AD9246 SN36, Run #98, DUT AVDD Current (mA).

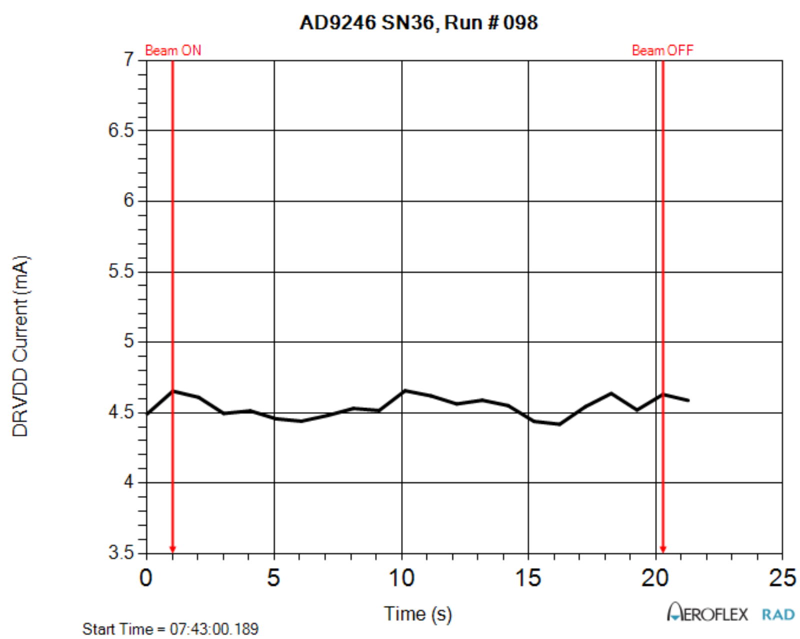

Figure F-70. AD9246 SN36, Run #98, DUT DRVDD Current (mA).

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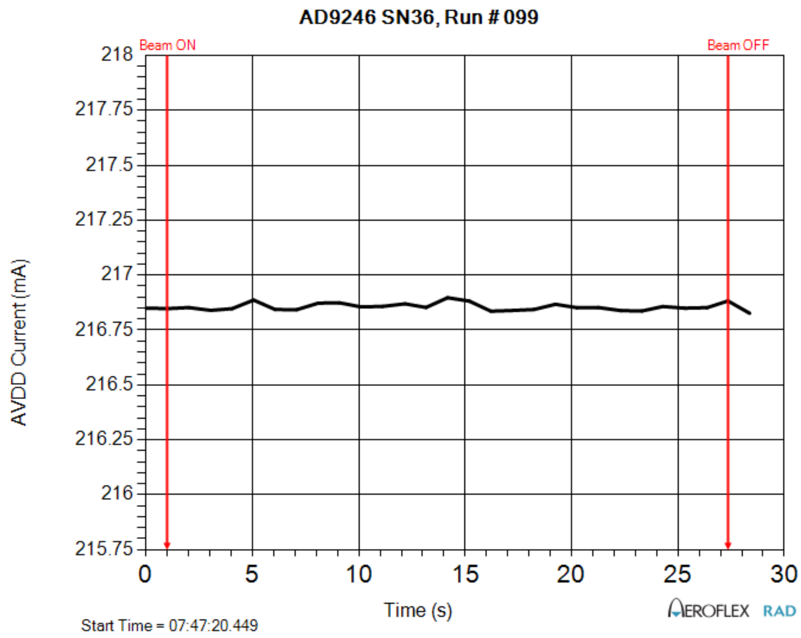

Figure F-71. AD9246 SN36, Run #99, DUT AVDD Current (mA).

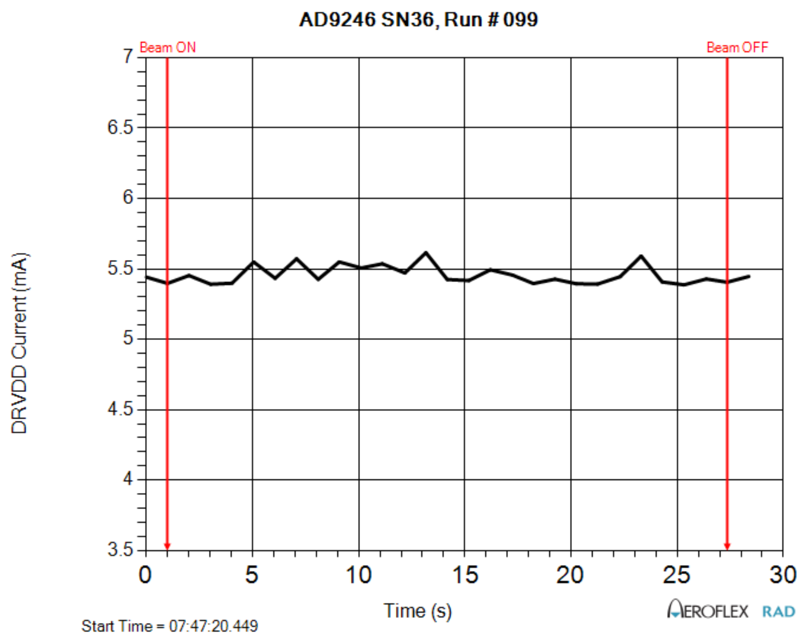

Figure F-72. AD9246 SN36, Run #99, DUT DRVDD Current (mA).

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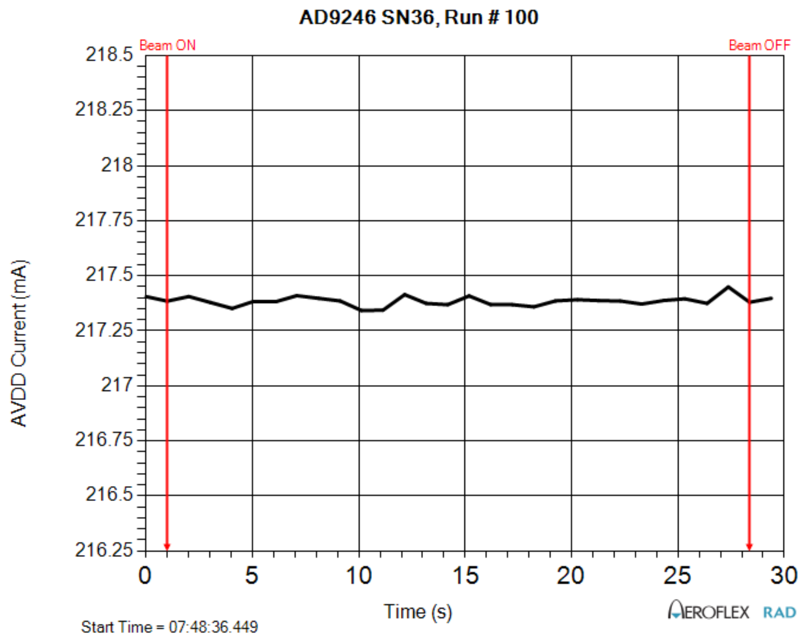

Figure F-73. AD9246 SN36, Run #100, DUT AVDD Current (mA).

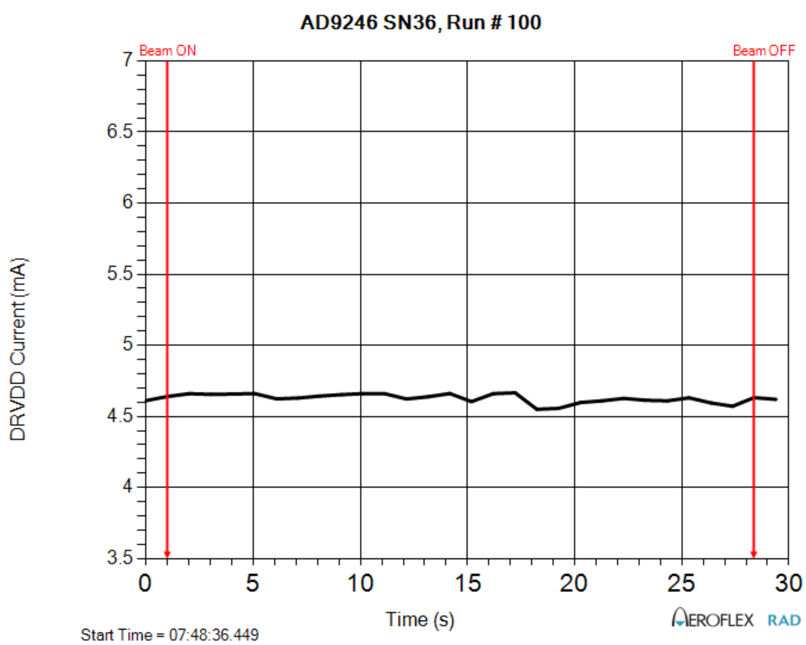

Figure F-74. AD9246 SN36, Run #100, DUT DRVDD Current (mA).

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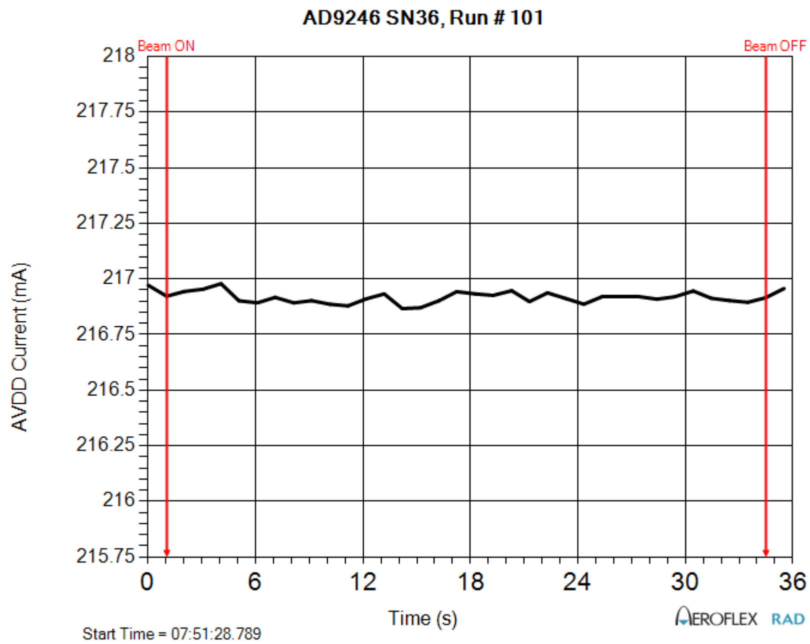

Figure F-75. AD9246 SN36, Run #101, DUT AVDD Current (mA).

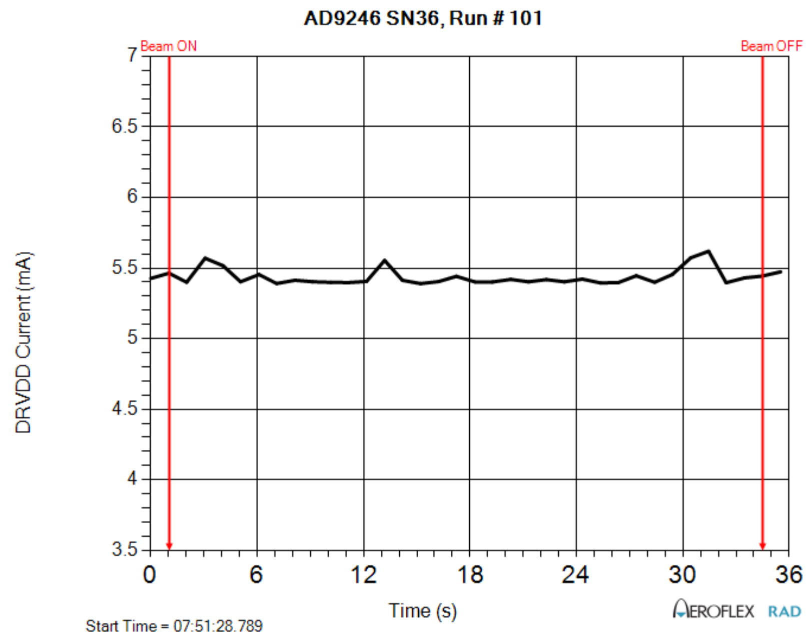

Figure F-76. AD9246 SN36, Run #101, DUT DRVDD Current (mA).

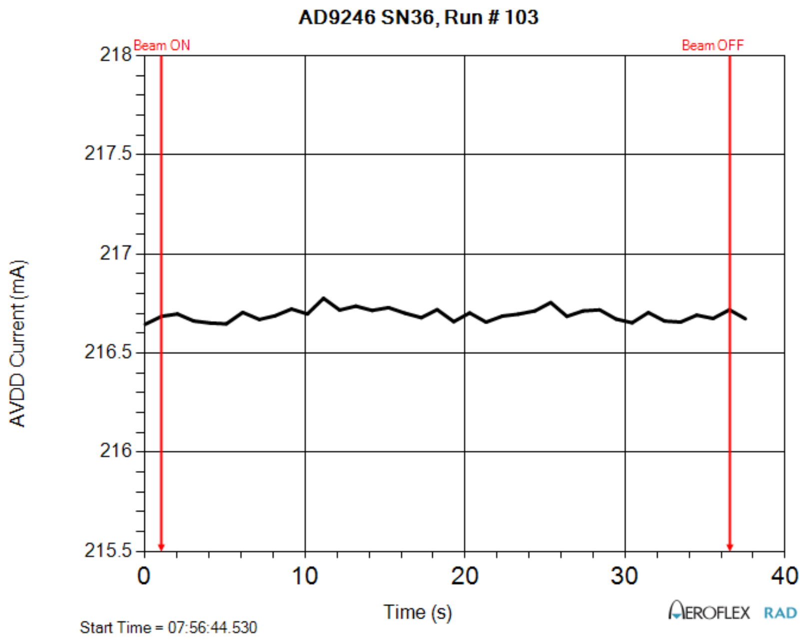

Figure F-77. AD9246 SN36, Run #102, DUT AVDD Current (mA).

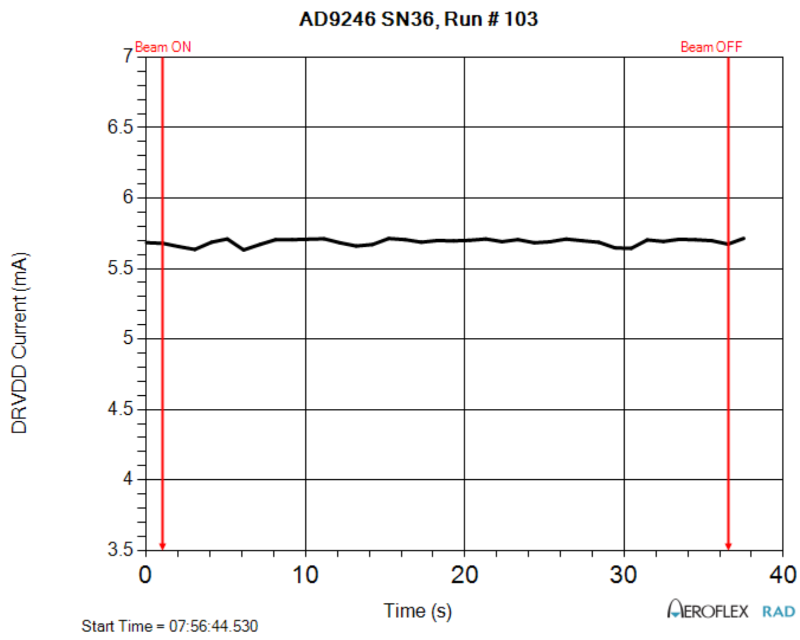

Figure F-78. AD9246 SN36, Run #102, DUT DRVDD Current (mA).

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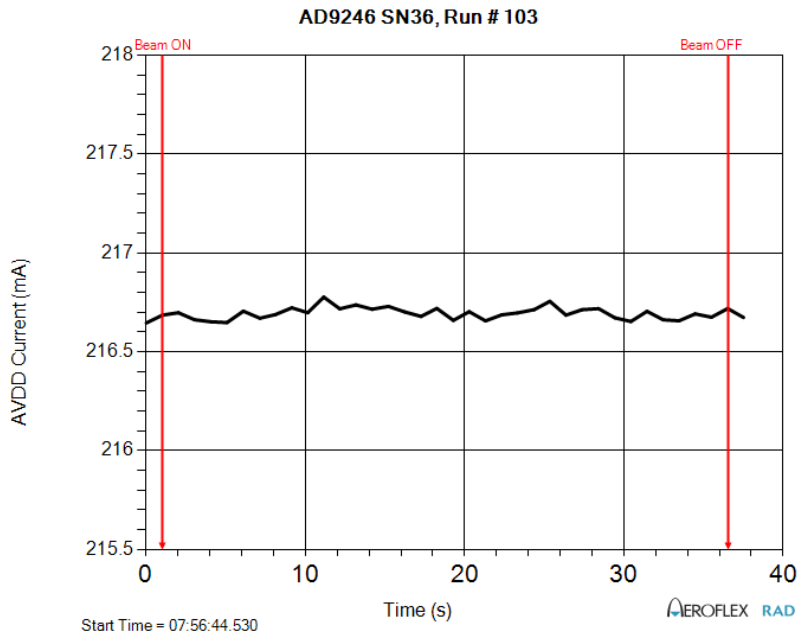

Figure F-79. AD9246 SN36, Run #103, DUT AVDD Current (mA).

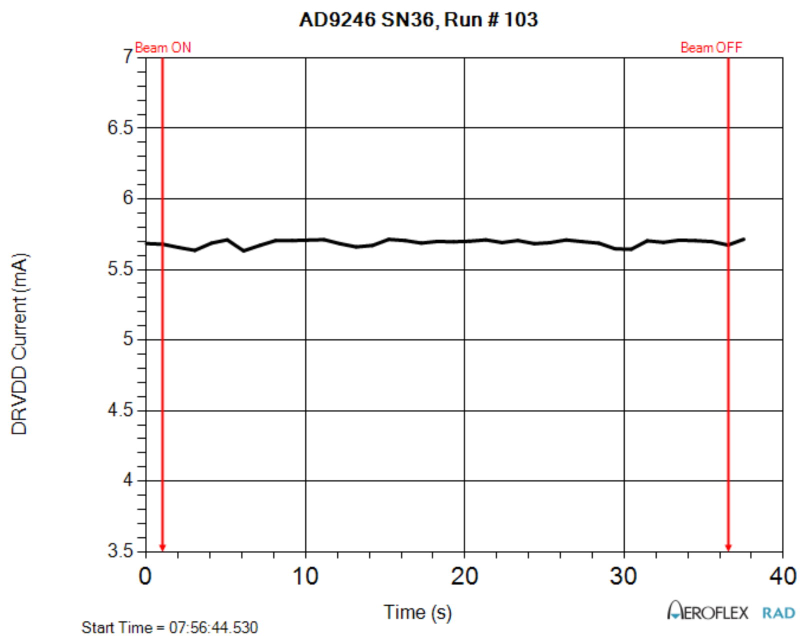

Figure F-80. AD9246 SN36, Run #103, DUT DRVDD Current (mA).

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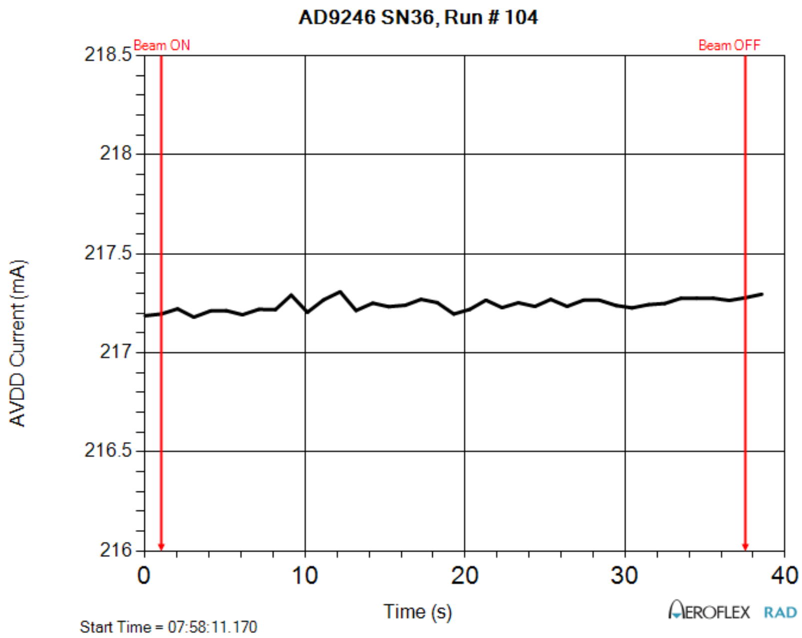


Figure F-81. AD9246 SN36, Run #104, DUT AVDD Current (mA).

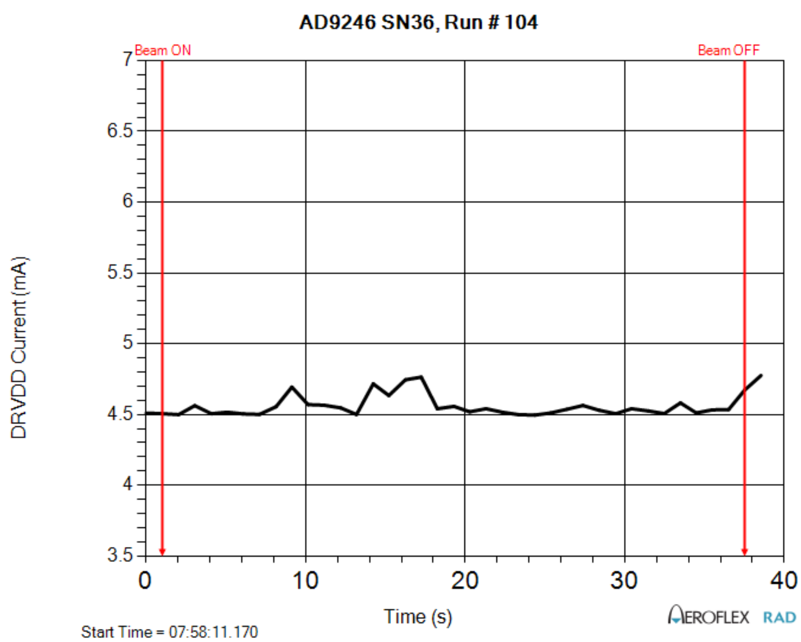
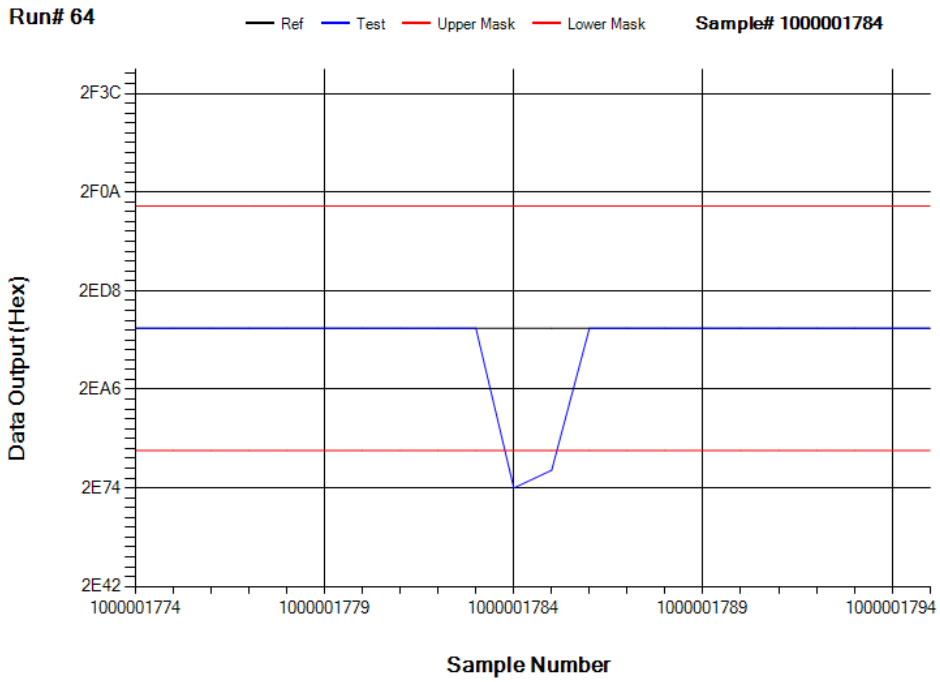
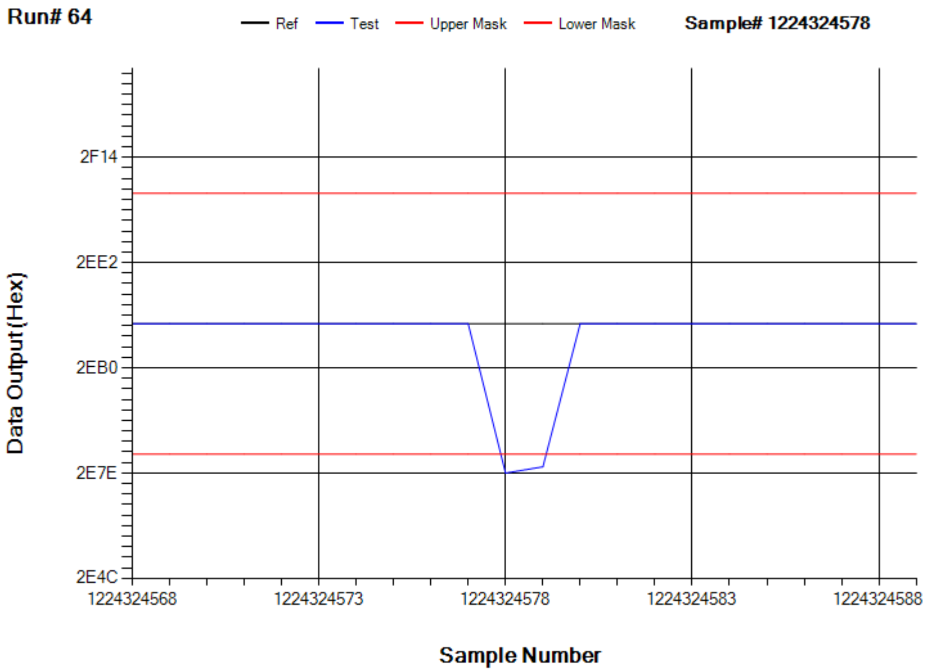


Figure F-82. AD9246 SN36, Run #104, DUT DRVDD Current (mA).

Appendix G: SET Error Plots





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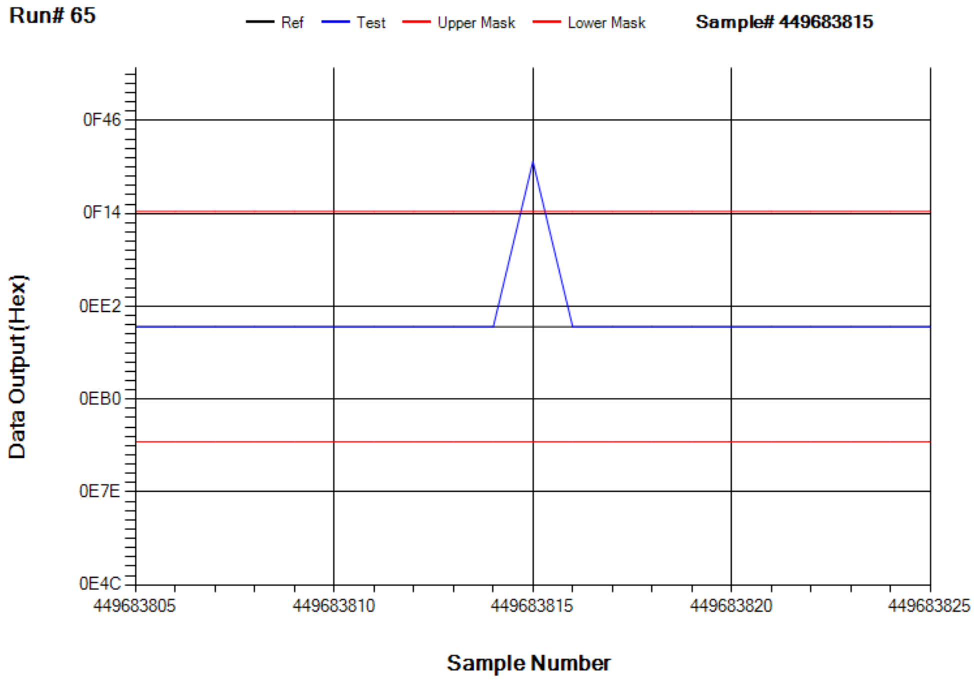

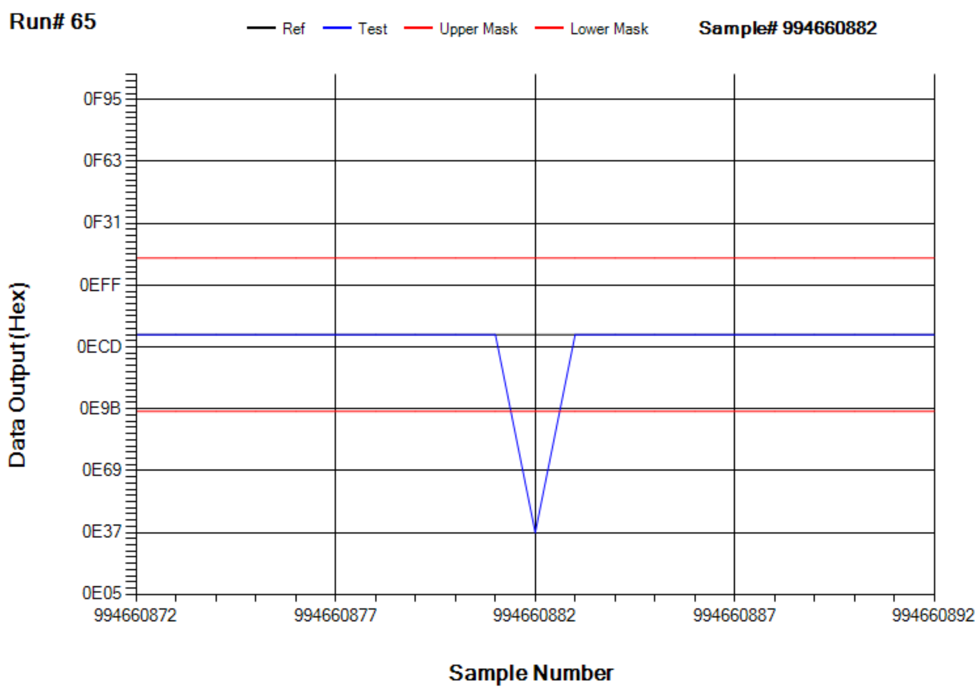

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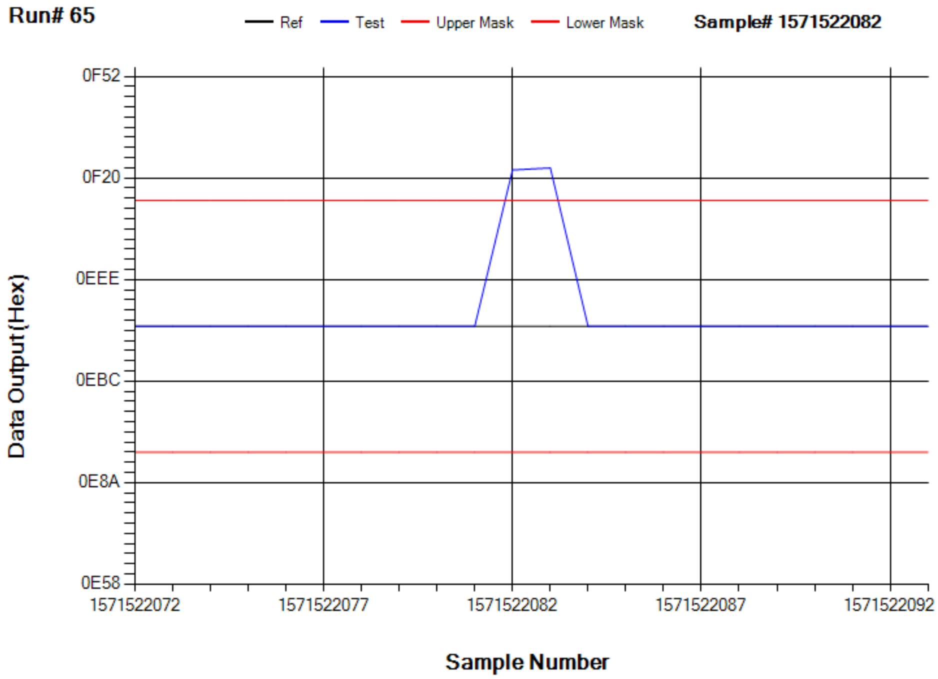

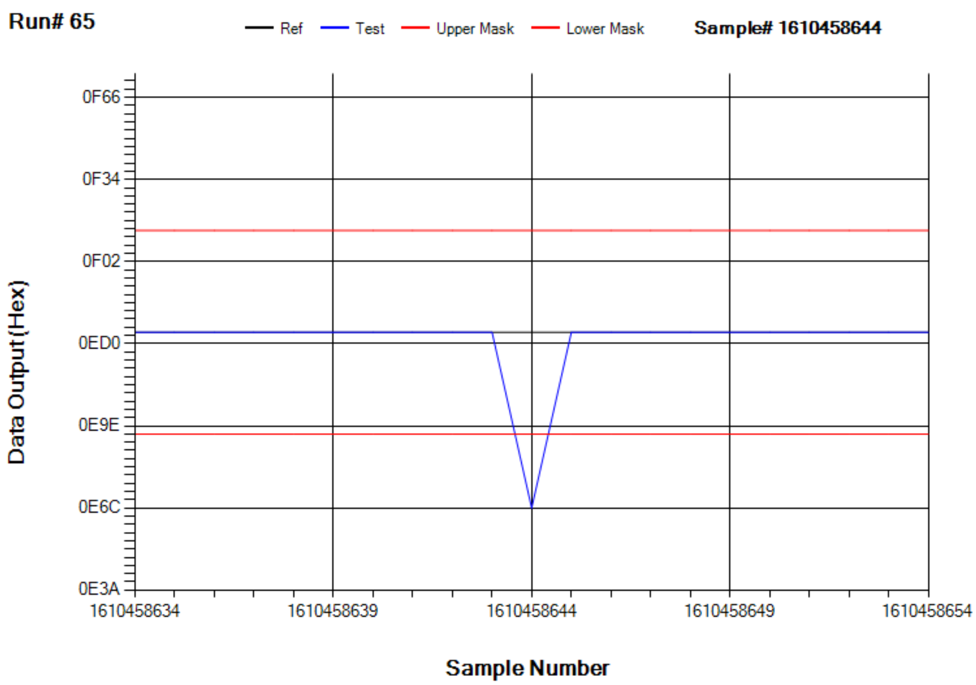

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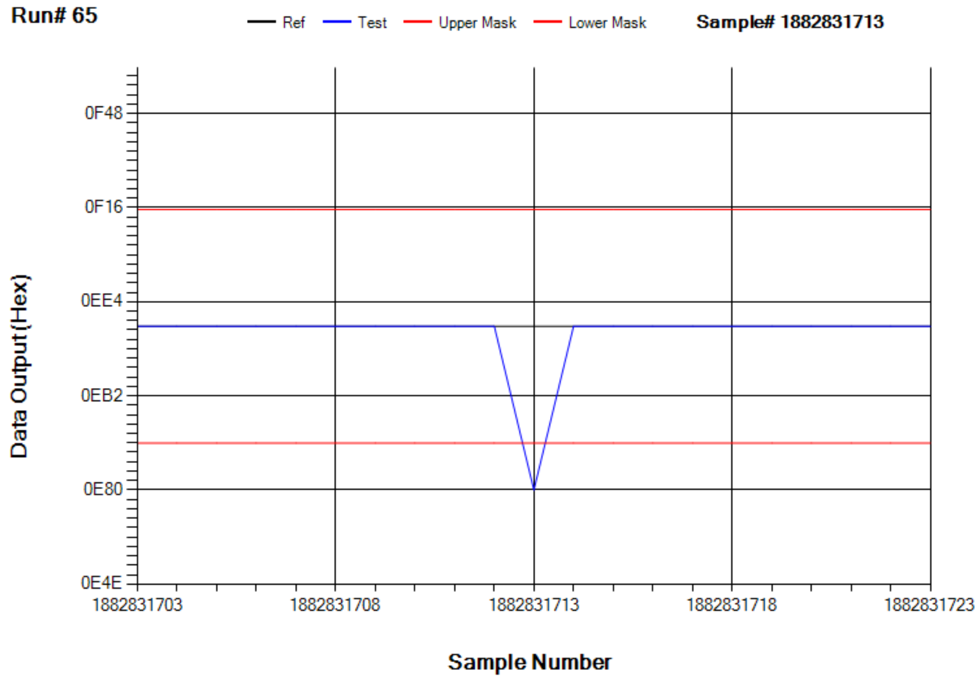

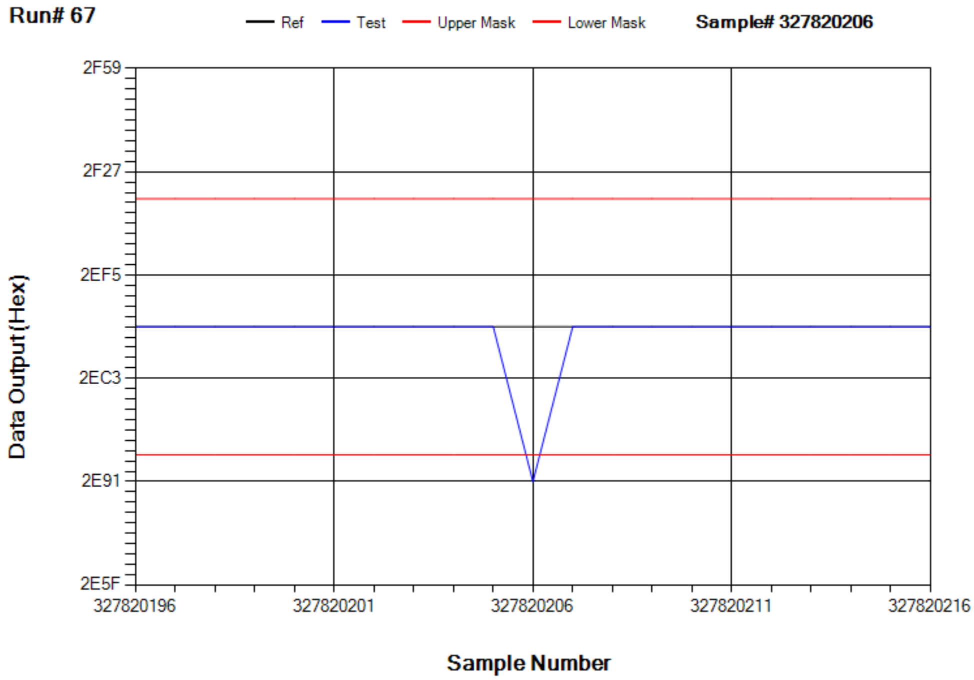

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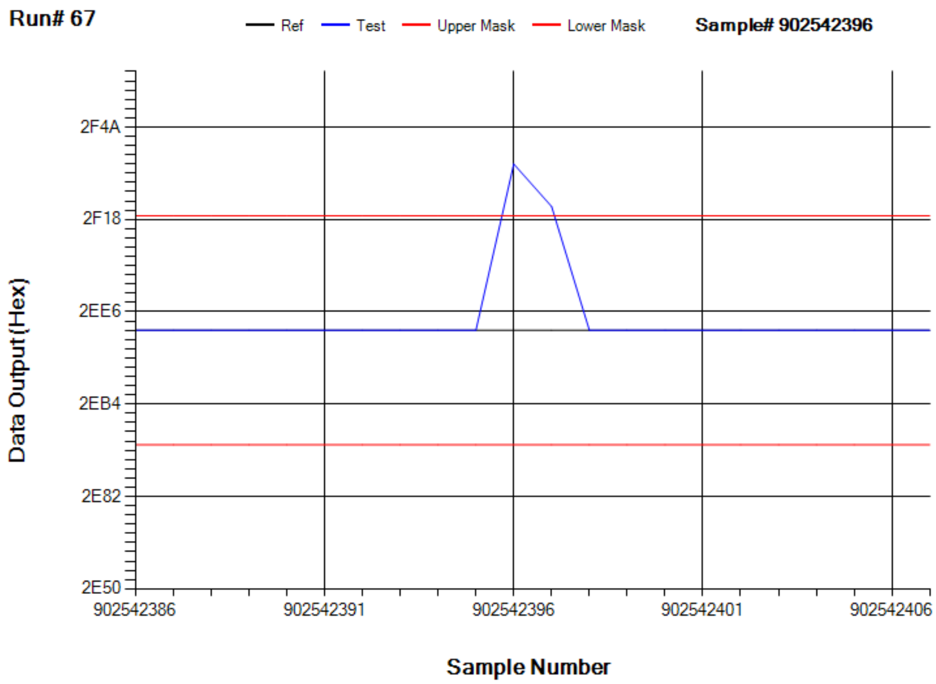

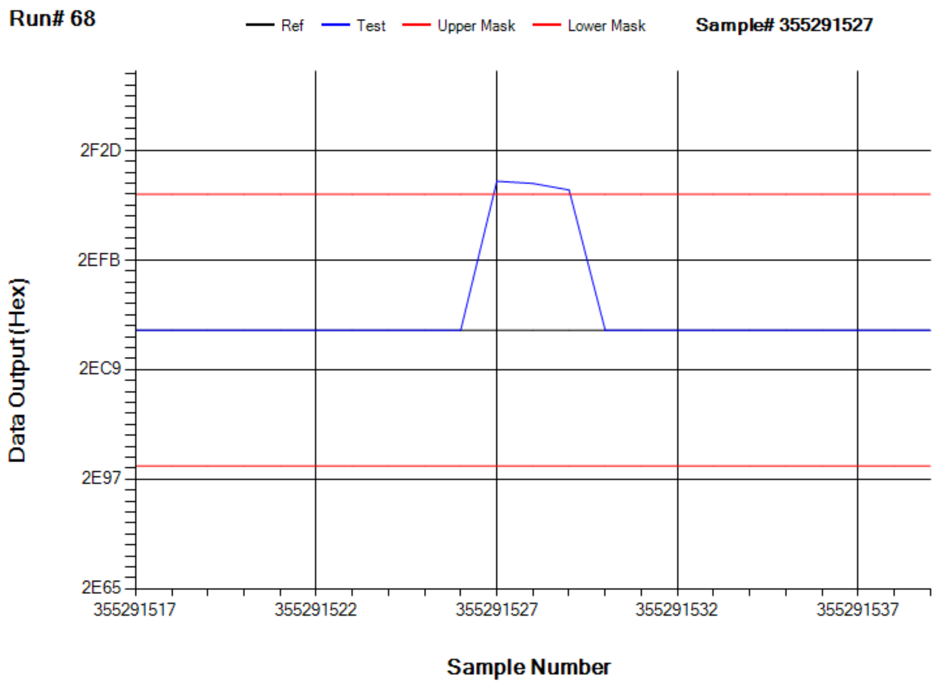

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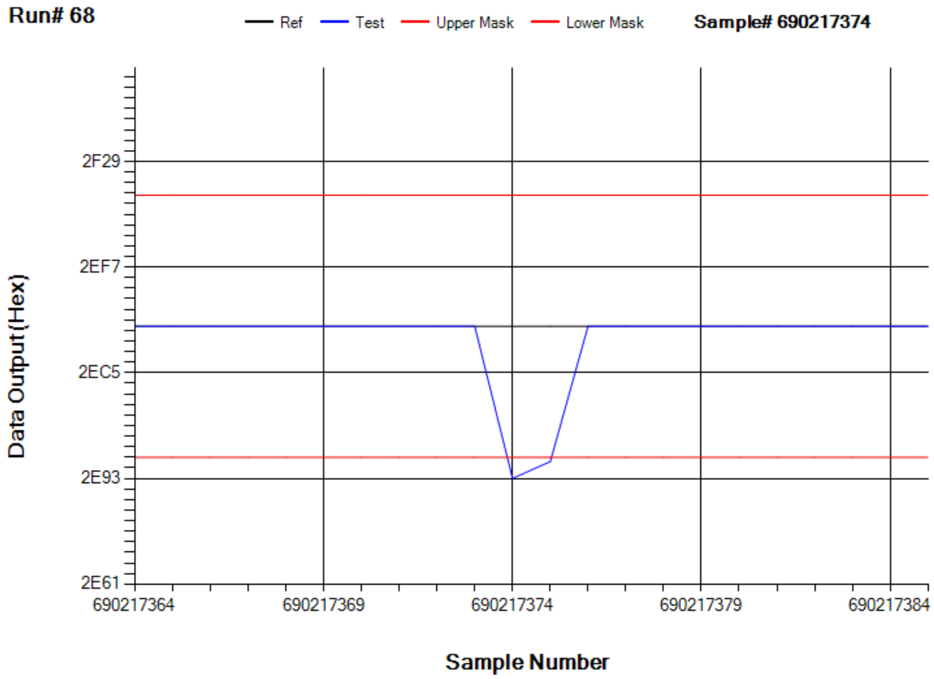

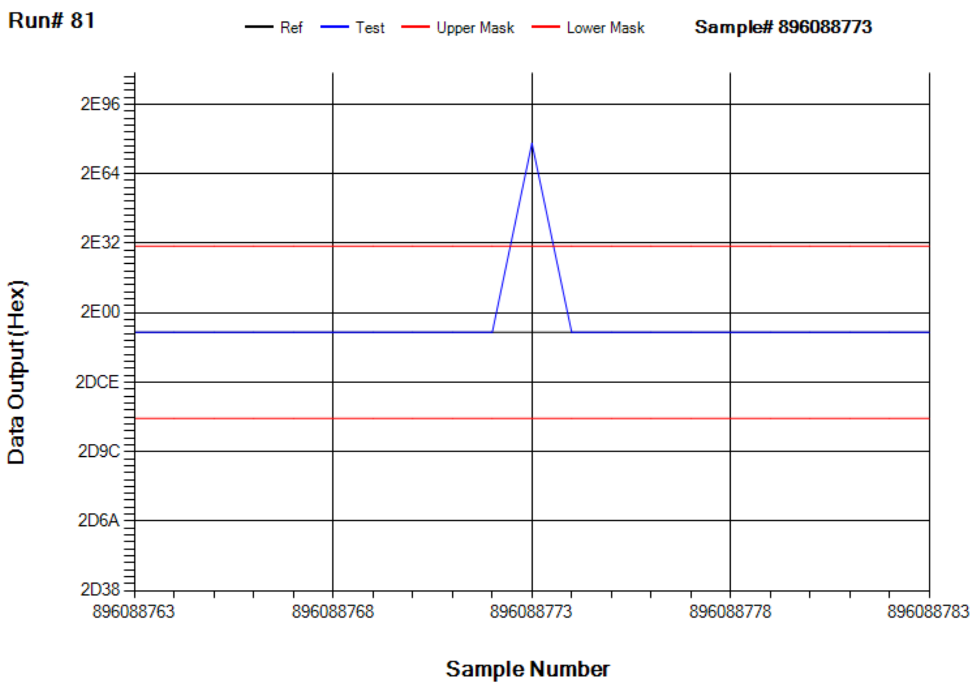

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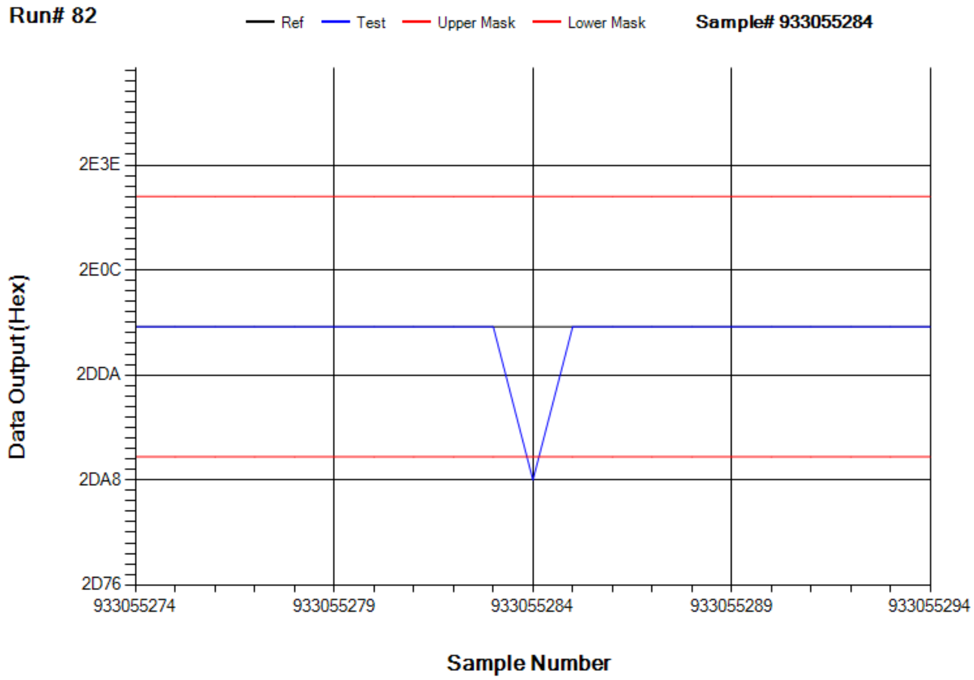

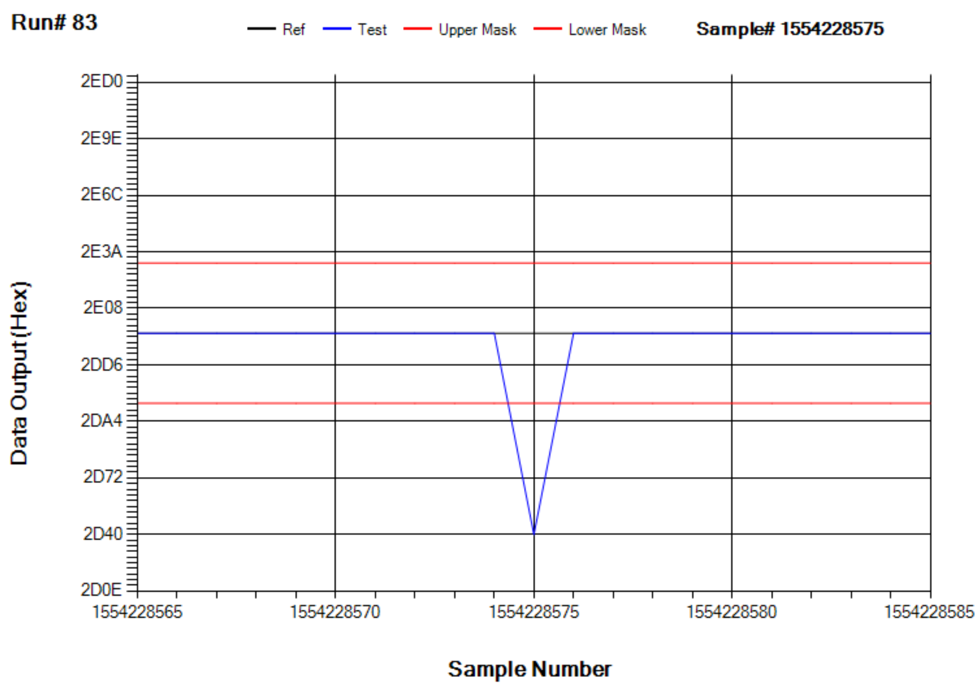

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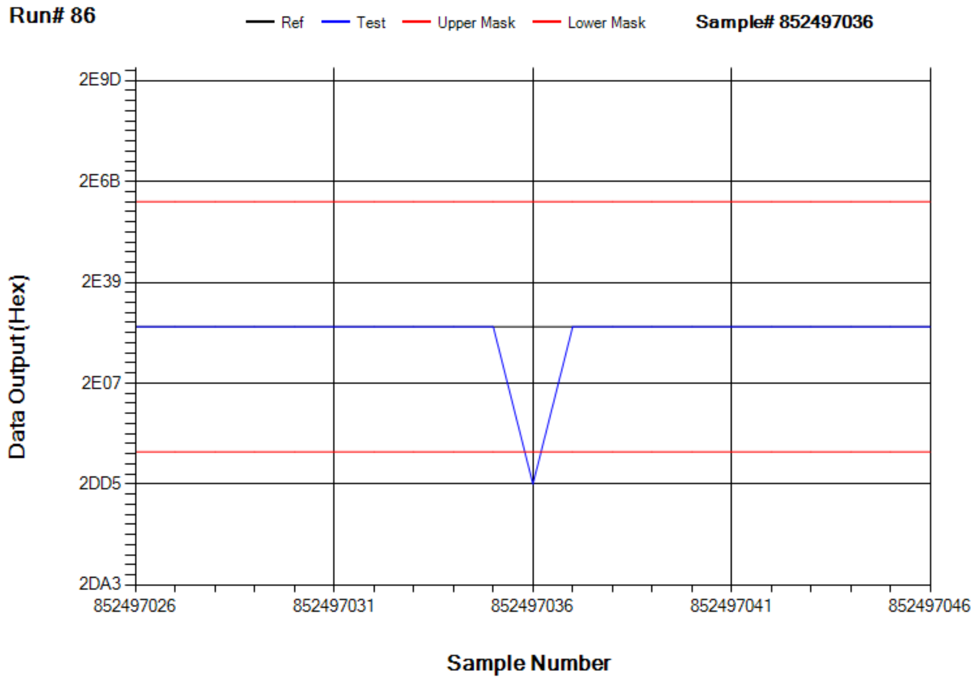

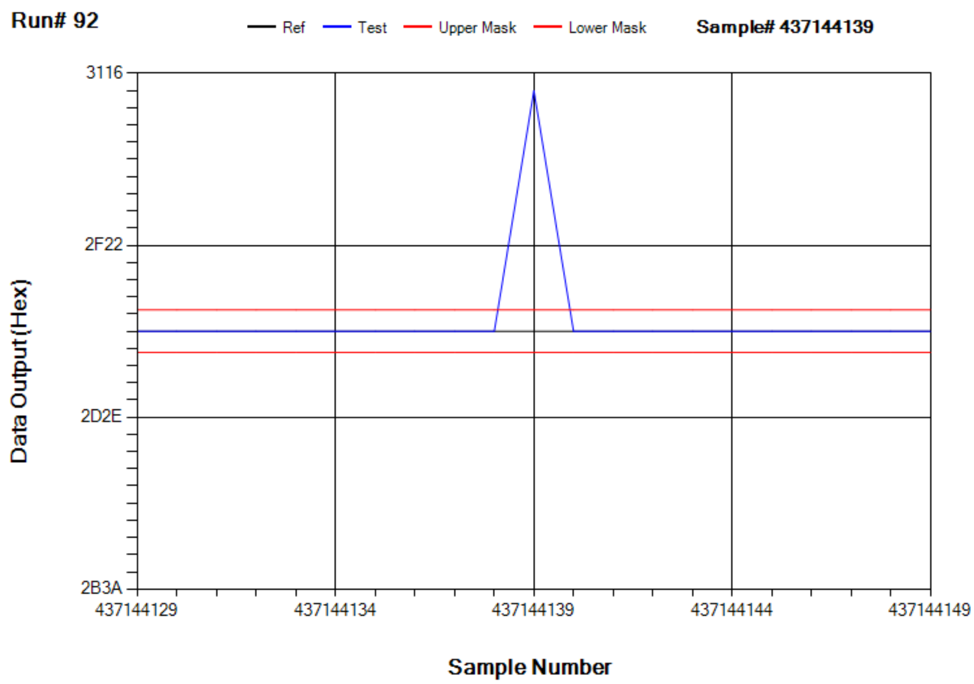

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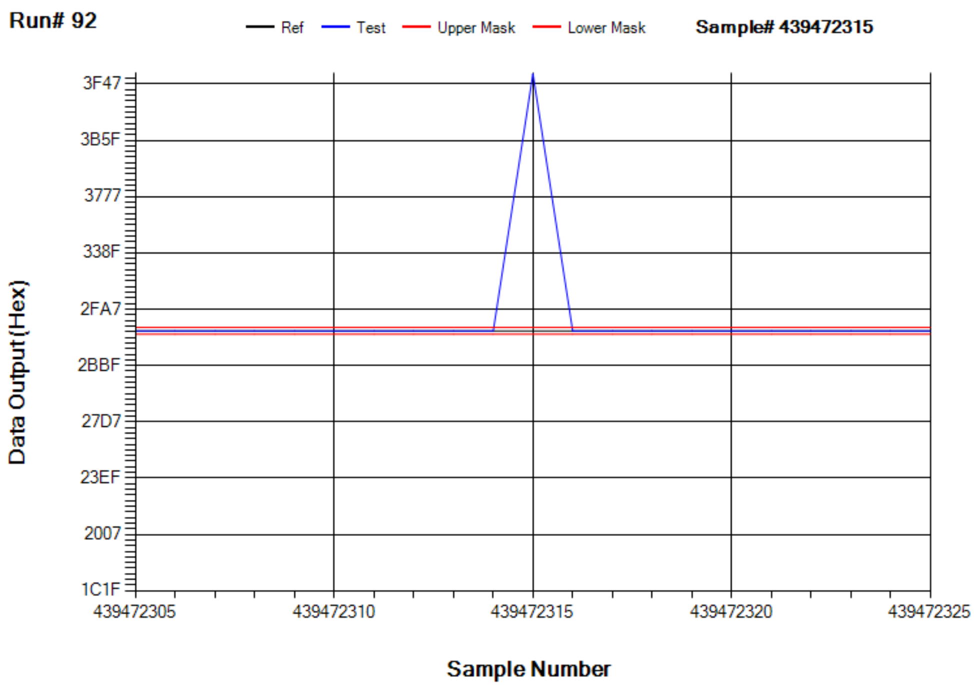

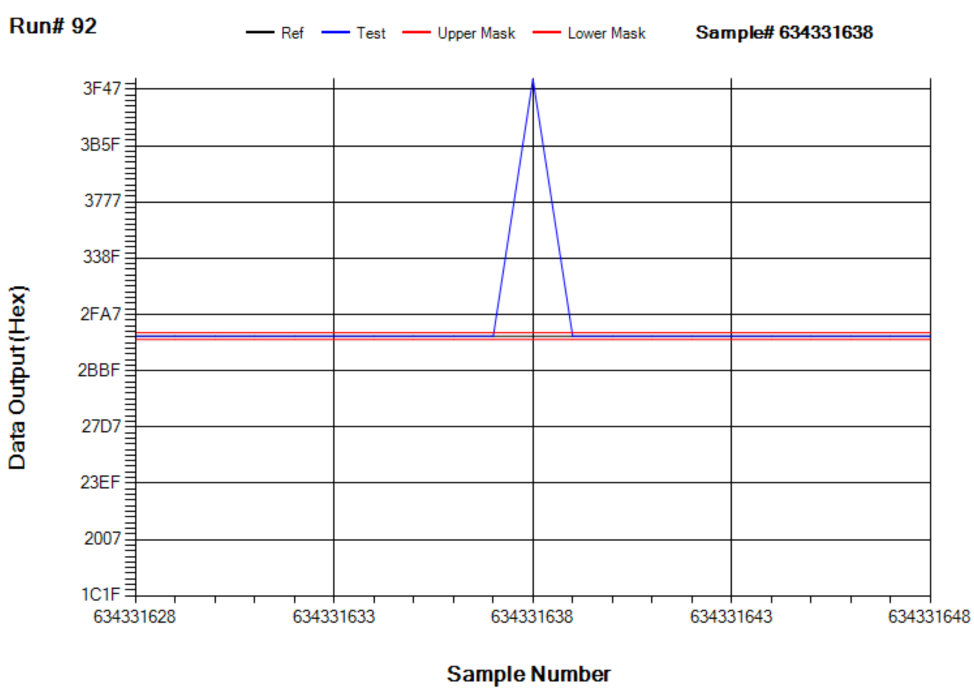

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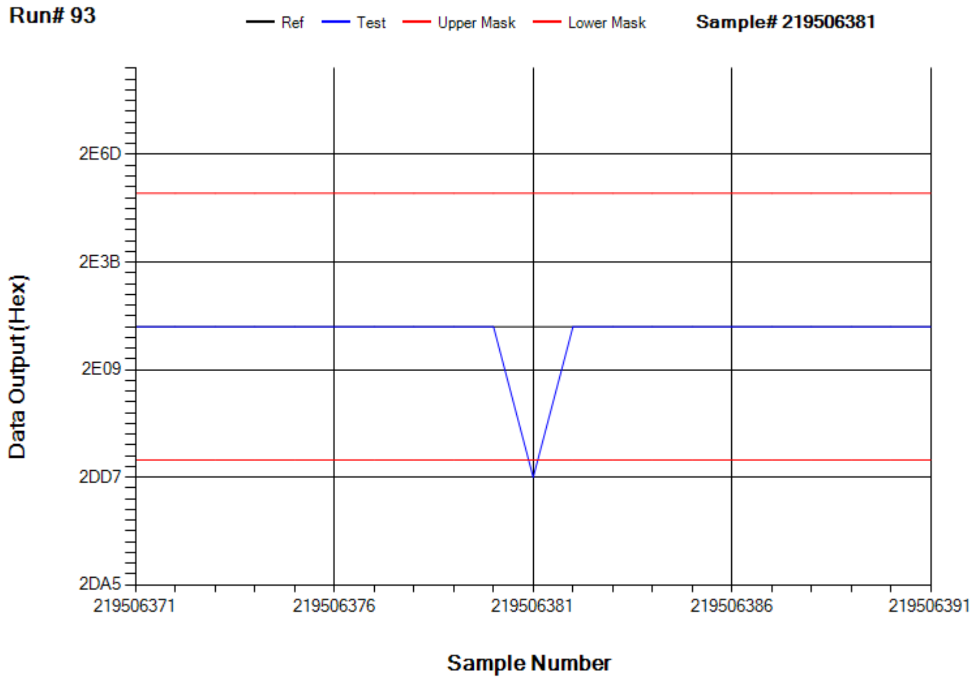

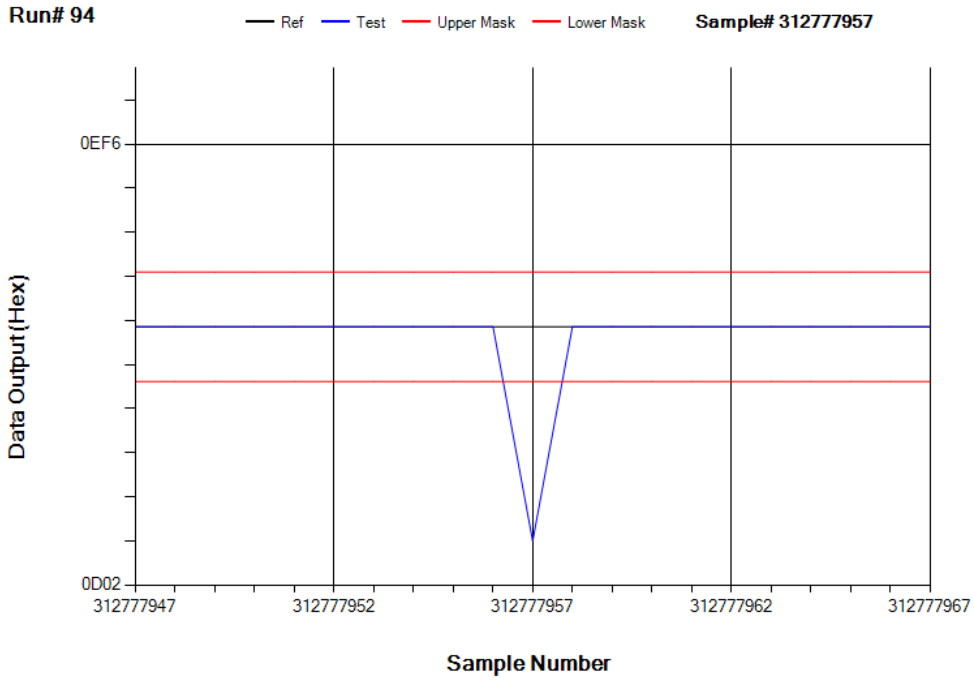

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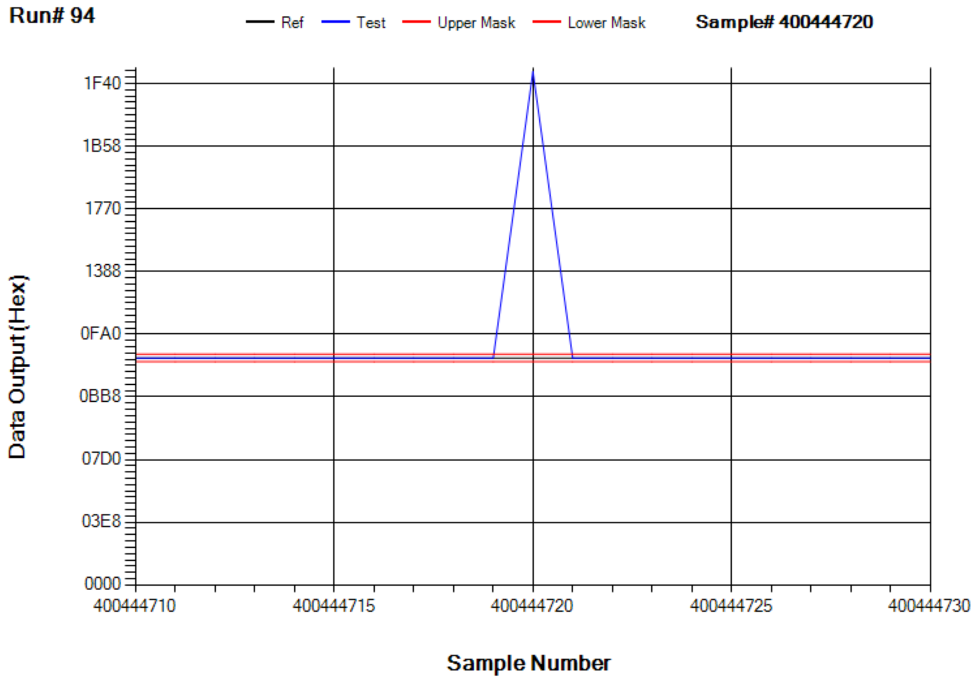

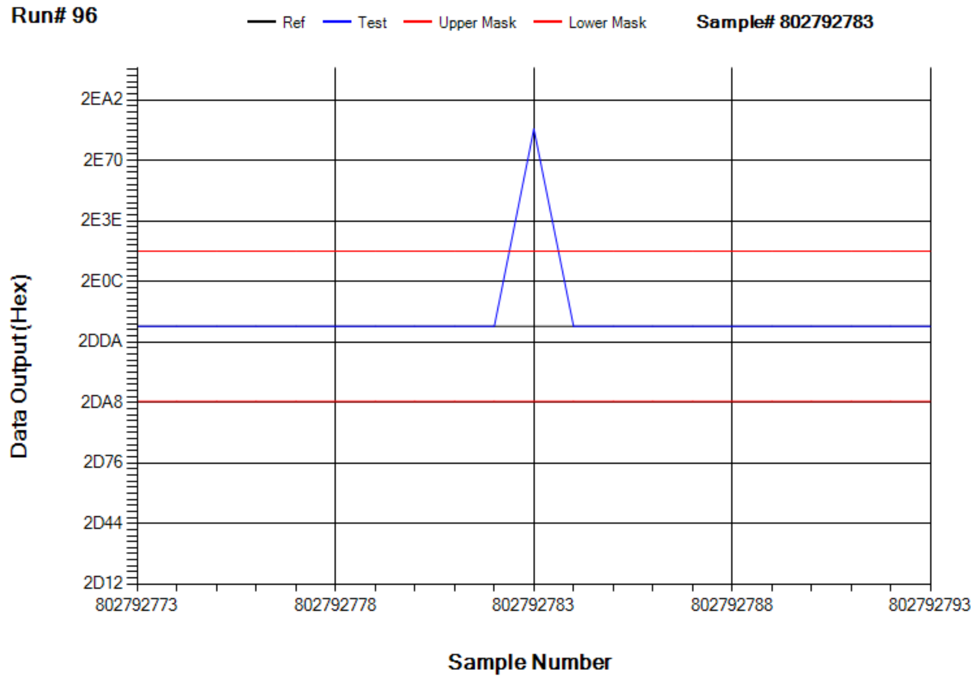

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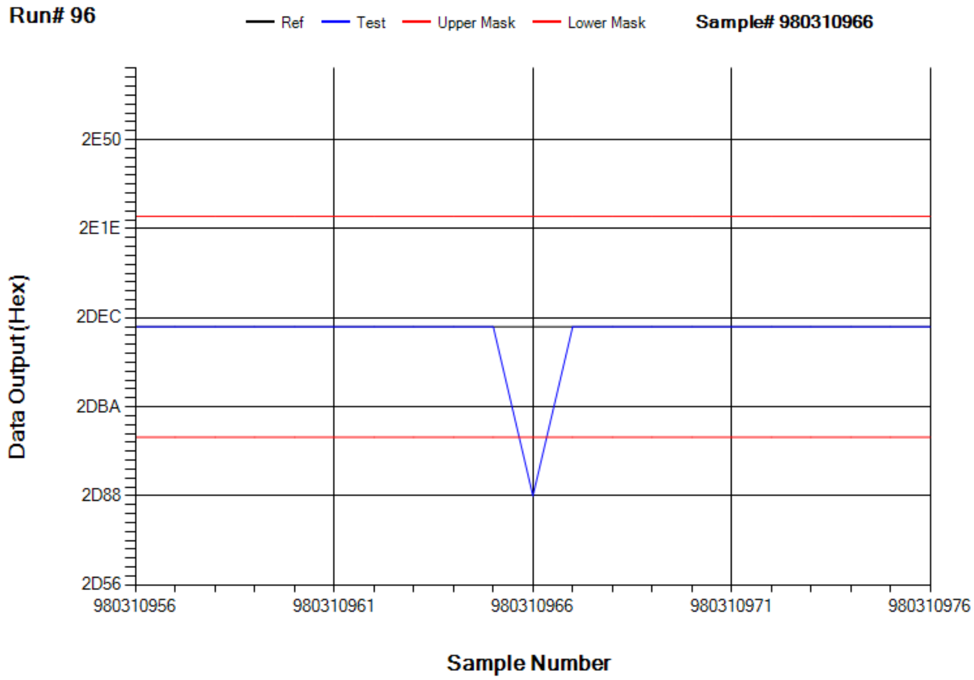

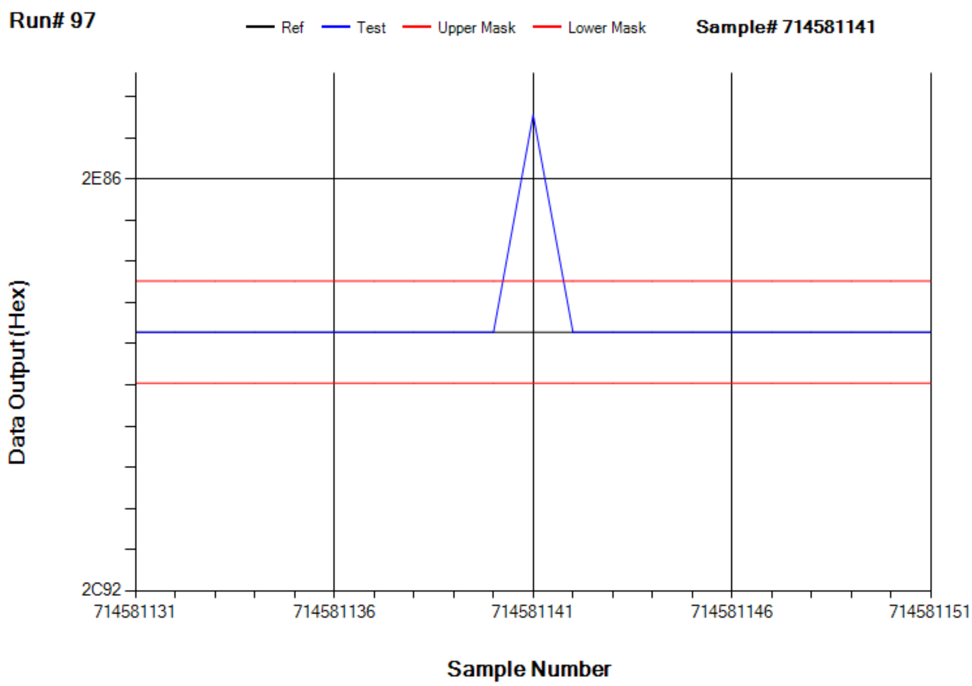

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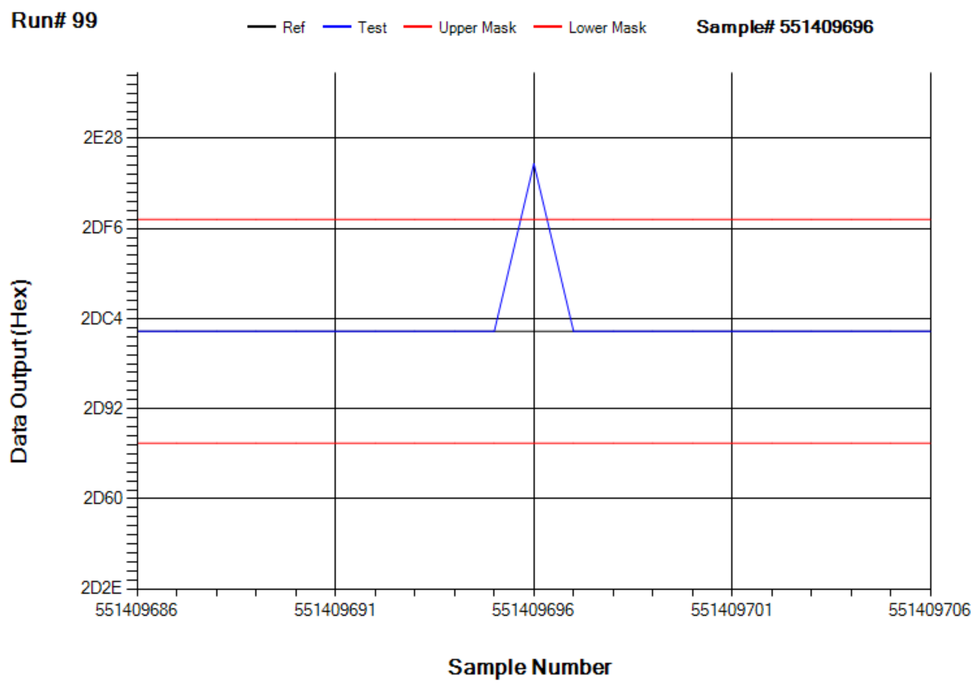

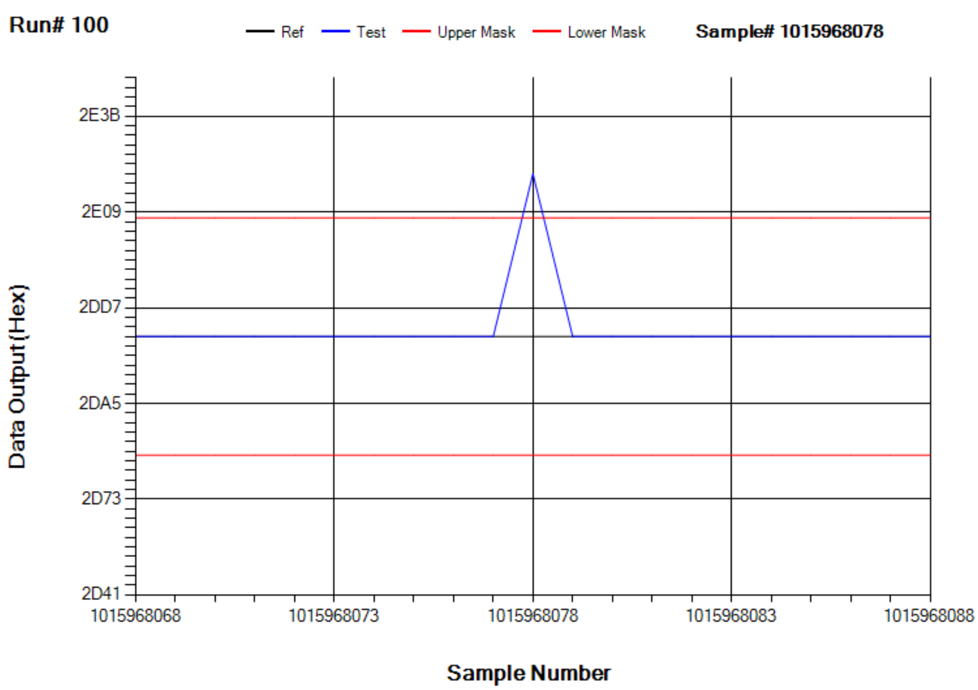

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