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Reference Circuits

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Devices Connected/Referenced

ADRF6510	30 MHz Dual Programmable Filters and Variable Gain Amplifiers
ADRF6801	750 MHz to 1150 MHz Quadrature Demodulator with Fractional-N PLL and VCO
AD9248	14-Bit, 65 MSPS Dual A/D Converter

An IQ Demodulator-Based IF-to-Baseband Receiver with IF and Baseband Variable Gain and Programmable Baseband Filtering

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

- [ADRF6510 Evaluation Board \(ADRF6510-EVALZ\)](#)
- [ADRF6801 Evaluation Board \(ADRF6801-EVALZ\)](#)
- [AD9248 Evaluation Board \(AD9248BCP-65EBZ\)](#)
- [AD8130 Evaluation Board \(AD8130-EBZ\) two required](#)
- [Data Capture Board \(HSC-ADC-EVALB-DCZ\)](#)

Design and Integration Files

- [Schematics, Layout Files, Bill of Materials](#)

CIRCUIT FUNCTION AND BENEFITS

This circuit is a flexible, frequency agile, direct conversion IF-to-baseband receiver. A fixed conversion gain of 5 dB reduces the cascaded noise figure. Variable baseband gain is used to adjust the signal level. The baseband ADC driver also includes a programmable low-pass filter that eliminates out-of-channel blockers and noise.

The bandwidth of this filter can be dynamically adjusted as the bandwidth of the input signal changes. This ensures that the available dynamic range of the ADC that this circuit drives is fully used.

The core of the circuit is an integrated IQ demodulator with fractional-N PLL and VCO. With just one (variable) reference frequency, the PLL/VCO can provide and a local oscillator (LO) between 750 MHz and 1150 MHz. Precise quadrature balance and low output dc offsets ensure that there is minimal degradation of the error vector magnitude (EVM).

The interfaces between all of the components in this circuit are fully differential. Where dc coupling is required between stages, the bias levels of the adjacent stages are compatible with each other.

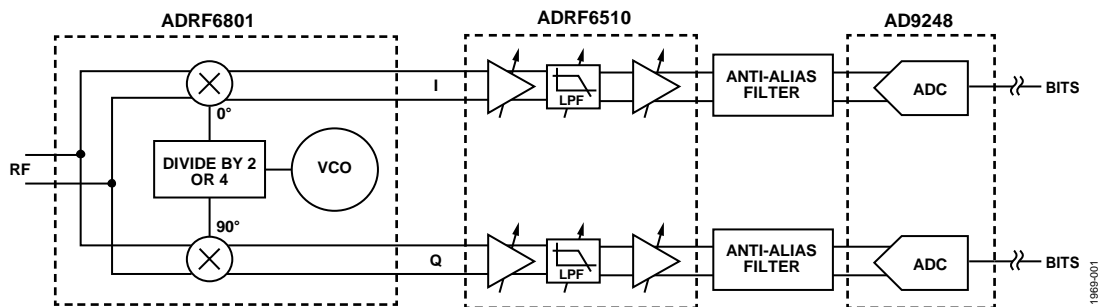


Figure 1. Direct Conversion receiver Simplified Schematic (All Connections and Decoupling Not Shown)

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CIRCUIT DESCRIPTION

Receiver Architecture

A direct conversion (also known as a homodyne or zero IF) architecture for a receiver is presented in this circuit note. Direct conversion radios perform just one frequency translation compared to a superheterodyne receiver that can perform several frequency translations. One frequency translation is advantageous because it

- Reduces receiver complexity and the number of stages needed, increasing performance and reducing power consumption
- Avoids image rejection issues and unwanted mixing products; one LPF at baseband is all that is needed
- Has high selectivity (adjacent-channel rejection ratio [ACRR])

Figure 1 shows the basic simplified schematic of the system that consists of an integrated quadrature demodulator with fractional-N PLL and VCO followed by programmable low-pass filters with variable baseband gain. The last part of the signal chain is an anti-aliasing filter and a dual A/D converter.

Ideally, the input of the first stage and the output of the last stage should set the dynamic range (signal-to-noise ratio) of the system. Practically, this may not be the case.

IQ Demodulator, Fractional-N PLL and VCO

The input signal is applied to the [ADRF6801](#) quadrature demodulator, where the frequency is translated to a zero IF. The [ADRF6801](#) has its own on-chip frequency synthesizer that provides the required LO. This frequency synthesizer consists of a fractional-N PLL and VCO, which while in the standard closed loop mode, has an LO frequency range from 750 MHz to 1150 MHz.

The [ADRF6801](#) uses two double-balanced mixers, one for the I channel and one for the Q channel. The LO provided to the mixers is generated using a divide-by-two quadrature phase splitter. This provides the 0° and 90° signals for the I and Q channels, respectively. There is about 5 dB of conversion gain provided by the [ADRF6801](#) from the RF input to the baseband I and Q outputs.

Low-Pass Filter, Baseband Variable Gain Amplifier (VGA), and ADC Driver

The low-pass filtering, baseband gain, and ADC driver functions are all achieved using the [ADRF6510](#). The signal, now in its separate I and Q paths, is applied to the [ADRF6510](#) where the signal is first amplified by the preamplifier, then low-pass filtered to suppress any unwanted out-of-band signals and/or noise, and finally amplified by the VGA.

Each channel of the [ADRF6510](#) can be broken up into three stages:

- Preamplifier
- Programmable low-pass filter
- VGA and output driver

The preamplifier has a user-selectable gain, via the GNSW pin, of either 6 dB or 12 dB. The low-pass filter can be programmed for

a corner frequency of 1 MHz to 30 MHz in 1 MHz steps via the SPI port. The VGA has a 50 dB gain range, with a 30 mV/dB gain slope. The gain of the VGA is controlled via the GAIN pin, and it can range from -5 dB to $+45$ dB when the GNSW pin is pulled low to $+1$ dB to $+51$ dB when the GNSW pin is pulled high. The output driver has the ability to drive 1.5 V p-p differential into a 1 k Ω load while maintaining an HD2 and an HD3 of better than 60 dBc.

The maximum continuous wave (CW) signal that can be applied to the low-pass filters, while still maintaining acceptable HD levels in the [ADRF6510](#), is 2 V p-p, while the gain is minimum (GNSW = 0 V and GAIN = 0 V).

From the [ADRF6510](#), the IQ signal can be applied to an analog-to-digital converter (ADC), such as the [AD9248](#), but not before some passive low-pass filtering is applied between the stages.

Anti-Aliasing Filter

The I and Q signals go through an anti-aliasing filter that helps to

- Reduce out-of-band noise
- Reduce output noise of the [ADRF6510](#) (especially at higher gains)
- Reduce charge kickback from the ADC
- Reduce out-of-band blockers (although they should have been reduced by the filtering on the [ADRF6510](#))

The anti-alias filter is a low-pass filter designed to have a corner ranging from about 30 MHz to 120 MHz. A lower corner frequency could be chosen if the spectral content of the signal is known to be something less than 30 MHz.

A total of five anti-aliasing filters were tested in the system. The first three anti-aliasing filters tested were differential RC types, shown in Figure 2. Filter 1 had $R = 33 \Omega$ and $C = 18$ pF. This created a low pass corner of approximately 134 MHz.

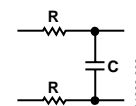


Figure 2. Anti-Alias Filter for Filters 1, 2, and 3

Filter 2 had a $R = 33 \Omega$ and $C = 39$ pF, which created a low pass corner of 62 MHz. Finally, Filter #3 had an $R = 33 \Omega$ and $C = 68$ pF, which created a corner of 35.5 MHz.

Filter 4 in Figure 3 was an LC filter with a corner frequency of 33 MHz, and Filter 5 in Figure 4 was an RLC filter also with a corner frequency of 33 MHz.

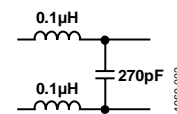


Figure 3. Anti-Aliasing Filter 4

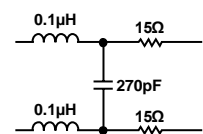


Figure 4. Anti-Aliasing Filter 5

A/D Converter

From the anti-aliasing filter the signal is applied to the ADC. The AD9248 dual 14-bit, 65 MSPS 3 V ADC features high performance sample-and-hold amplifiers and an integrated voltage reference.

Measurement Results: EVM of ADRF6510 and ADRF6510/ADRF6801 Combination

A 4-QAM, 5 MSPS modulated signal was applied to the input of the ADRF6801 quadrature demodulator and the error vector magnitude (EVM) was measured. Two AD8130-EBZ evaluation boards were used to convert the differential outputs of the ADRF6801 and the ADRF6510 to single-ended signals. For more information on the test setup, see the Circuit Evaluation and Test section.

EVM is a measure of the quality of the performance of a digital transmitter or receiver and is a measure of the deviation of the actual constellation points from their ideal locations, due to both magnitude and phase errors as shown in Figure 5.

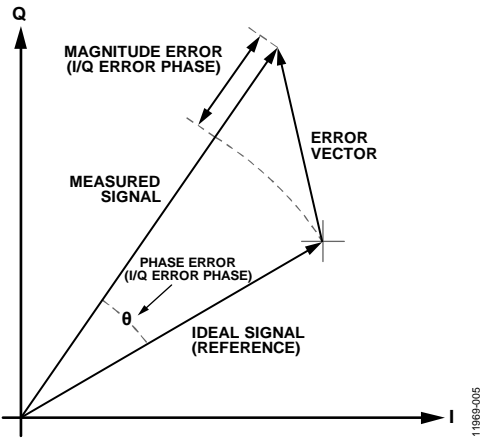


Figure 5. EVM Plot

Figure 6 shows the EVM vs. the input power to the ADRF6801 with only the ADRF6801, and the ADRF6801 followed by the ADRF6510. For the ADRF6801 and ADRF6510 curve, the gain changed on the ADRF6510 to maintain 1.5 V p-p output voltage as the input power to the ADRF6801 was swept. The preamplifier gain on the ADRF6510 is set to 6 dB.

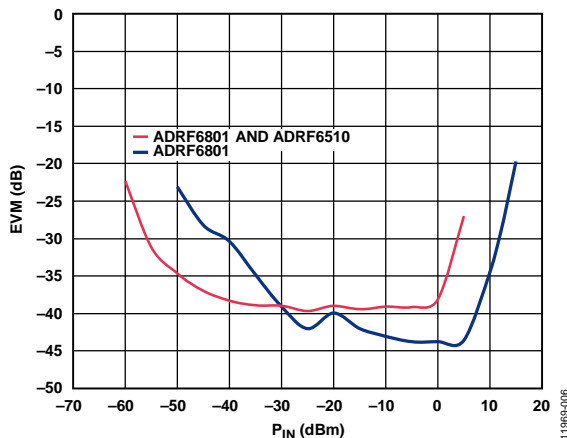


Figure 6. EVM vs. Input Power for the ADRF6801 and the ADRF6801/ADRF6510 Combination

When the ADRF6801 is tested alone, note that for high input signal levels the EVM does not degrade until about +5 dBm input power. But when the ADRF6801 is driving the ADRF6510, the EVM starts to degrade at about 0 dBm input power. This is because the low-pass filters on the ADRF6510 can only handle 2 V p-p, which is 1 V p-p at the input pins of the ADRF6510 when the preamp gain is set to 6 dB, and the analog gain is at minimum. Signal levels beyond this begin to cause distortion which degrades the EVM.

For low input signal levels, the SNR becomes smaller and starts to degrade the EVM measurement. The EVM started to degrade at about -25 dBm when the ADRF6801 was tested alone. However, when the ADRF6801 is driving the ADRF6510, the EVM does not start to degrade until -40 dBm. There is degradation of EVM when measuring both parts at low signal levels, mostly due to the noise introduced by the ADRF6510. However, the floor of the bathtub is flatter and more consistent, and the ability to discern smaller signals is much better when the ADRF6801 is driving the ADRF6510, due to the baseband variable gain.

More comprehensive EVM measurements for the ADRF6510 and the ADRF6801 can be found in each respective data sheet.

Measurement Results: Complete Signal Chain Including ADC

For Figure 7 to Figure 16, the signal chain includes the ADRF6801, ADRF6510, and the AD9248. All three parts were dc coupled to each other. The common-mode voltage between the ADRF6801 and the ADRF6510 was 2.6 V. The common-mode voltage between the ADRF6510 and the AD9248 was 2.0 V. Full-scale for the ADC was 2 V. The input power to the ADRF6801 was swept, and the gain of the ADRF6510 was varied to set the proper signal level at the ADC input, -3 dBFS. SNR, SFDR, THD, HD2 and HD3 were measured using the ADC and the Visual Analog software. The sampling rate was set to 65 MSPS from an Agilent 8665B low phase noise signal generator. Two different filter bandwidths of the ADRF6510 were used: 5 MHz and 30 MHz. Also, the preamp gain of the ADRF6510 was changed from 6 dB to 12 dB. The RF provided to the ADRF6801 was 895 MHz, and the LO was set to 900 MHz, thereby creating a 5 MHz IF tone. A 100 MHz reference was used. The reference was divided by 4 to make a PFD frequency of 25 MHz. The 100 MHz signal was generated by the Model 119-3651-00 Wenzel crystal oscillator.

The data collected in this circuit note shows that the SNR (71.6 dB) and SFDR (80.5 dBc) performance of the AD9248 ADC exceeds that of the ADRF6801 and ADRF6510 combination. The overall SNR and SFDR of the system is limited primarily by the output noise of the ADRF6510, which is specified as -130 dBV/√Hz at 20 dB of gain with a filter bandwidth of 30 MHz, measured at mid-band. (For more information of the noise vs. gain and bandwidth settings of the ADRF6510, please refer to the ADRF6510 datasheet).

ADRF6510 filters exhibit compression at high input power levels (in this case at low gains), which increases harmonic distortion. At low input power levels the ADC is essentially measuring the

output noise floor of the **ADRF6510**, and the HD2 and HD3 tones are below the noise floor. The output noise floor of the **ADRF6510** is raised due to the higher gain at lower input powers.

Figure 7 and Figure 8 show the SNR of the entire signal chain including the ADC. At low power levels, the SNR degrades almost dB-for-dB. The gain of the **ADRF6510** is at its maximum and can no longer supply -3 dBFS at lower input power levels. The signal decreases in amplitude, while the noise remains relatively constant; hence the decrease in SNR. The SNR approaches a constant level when there is enough signal and enough gain to achieve -3 dBFS. Best SNR was achieved with anti-aliasing Filter 3, although only about 1 dB was spread between all filters, except for anti-aliasing Filter 1, that caused poorer SNR than the rest of the filters.

SNR degrades sharply at the highest of input power with the **ADRF6510** filters set to 30 MHz, as shown in Figure 8. This is due to compression in the **ADRF6510** filters that causes HD2 and HD3 to degrade suddenly, and the entire noise floor rises drastically.

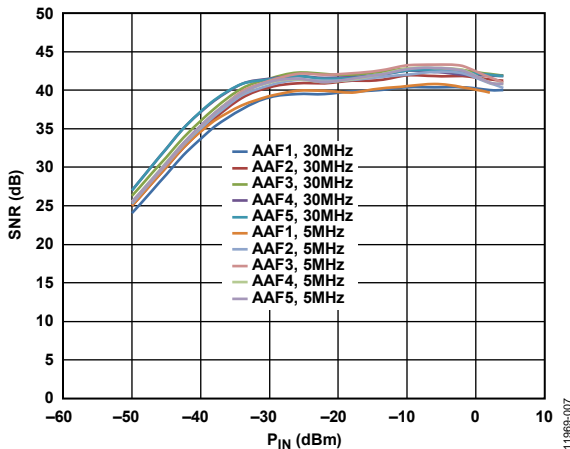


Figure 7. System SNR for Five Anti-Alias Filters, 30 MHz and 5 MHz Filter Corners for **ADRF6510**, 5 MHz IF Tone, GNSW = Low, Front-End Gain = 6 dB

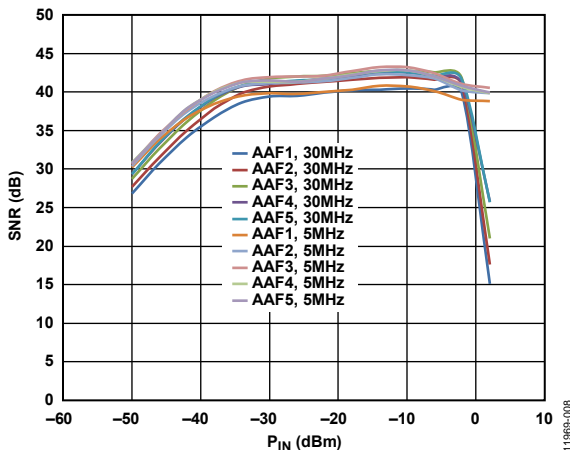


Figure 8. System SNR for Five Anti-Alias Filters, 30 MHz and 5 MHz Filter Corners for **ADRF6510**, 5 MHz IF Tone, GNSW = High, Front-End Gain = 12 dB

Figures 9 and 10 show SFDR of the entire system for the various anti-aliasing filters. Filter 4 and Filter 5 perform very poorly, with an SFDR of 40 dB across most of the input power range. This is due to the HD3 tone limiting the SFDR. For the other anti-aliasing filters, SFDR was more than 60 dB for most of the range. There is a slight degradation at the lower input powers due to the main tone not being at -3 dBFS.

At the high input power levels, the SFDR is limited by the harmonics caused by compression in the **ADRF6510** filters.

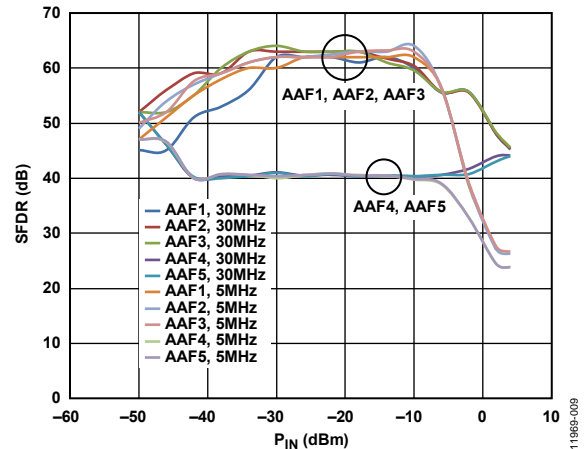


Figure 9. System SFDR for Five Anti-Alias Filters, 30 MHz and 5 MHz Filter Corners for **ADRF6510**, 5 MHz IF Tone, GNSW = Low, Front-End Gain = 6dB

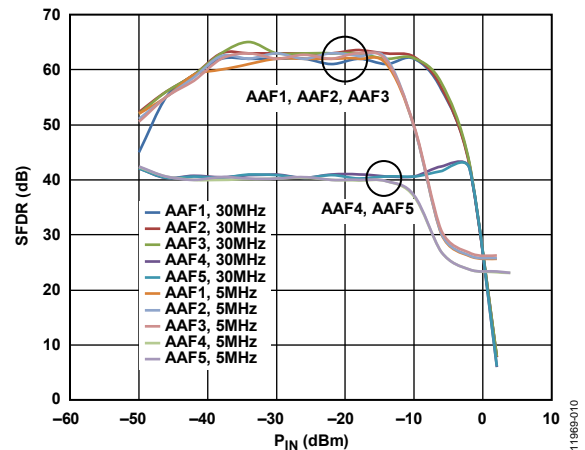


Figure 10. System SFDR for Five Anti-Alias Filters, 30 MHz and 5 MHz Filter Corners for **ADRF6510**, 5 MHz IF Tone, GNSW = High, Front-End Gain = 12 dB

Figure 11, Figure 12, Figure 13, and Figure 14 show the HD2 and HD3 of the system. Anti-aliasing filters 4 and 5 performed poorly again, achieving an HD2 performance of about -55 dBc and only -40 dBc for HD3. Filters 1, 2, and 3 performed much better, yielding results of better than -70 dBc for HD2 and HD3.

At the low end of the input power range, the HD2 and HD3 components were so small that they were less than the noise floor, and what was actually recorded was the noise. After the gain of the **ADRF6510** was lowered enough to decrease the output noise which in turn revealed the HD tones, proper measurements could be made.

At the high end of the input power range, HD2 and HD3 degraded significantly. This is due to compression in the [ADRF6510](#) filters.

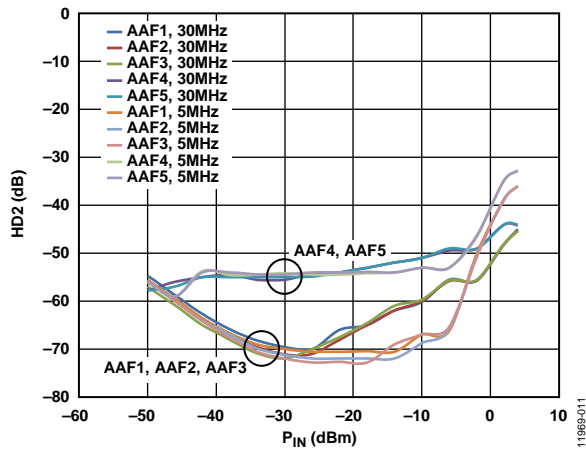


Figure 11. System HD2 for Five Anti-Alias Filters, 30 MHz and 5 MHz Filter Corners for [ADRF6510](#), 5 MHz IF Tone, GNSW = Low, Front-End Gain = 6 dB

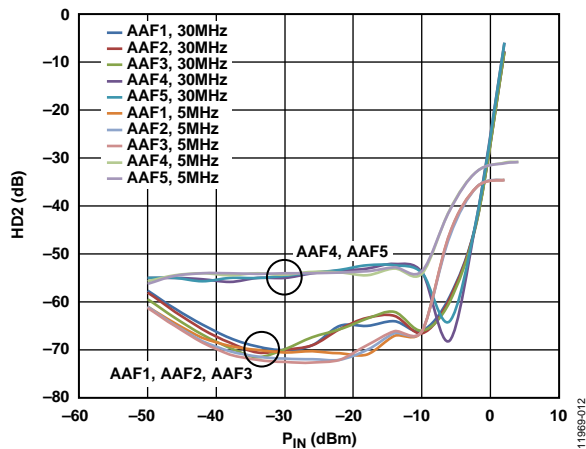


Figure 12. System HD2 for Five Anti-Alias Filters, 30 MHz and 5 MHz Filter Corners for [ADRF6510](#), 5 MHz IF Tone, GNSW = High, Front-End Gain = 12 dB

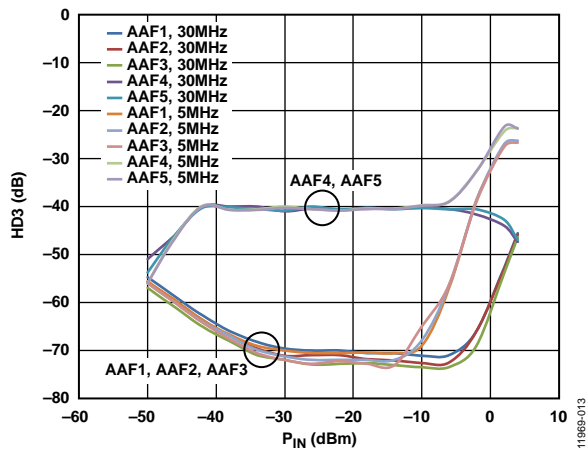


Figure 13. System HD3 for Five Anti-Alias Filters, 30 MHz and 5 MHz Filter Corners for [ADRF6510](#), 5 MHz IF Tone, GNSW = Low, Front-End Gain = 6 dB

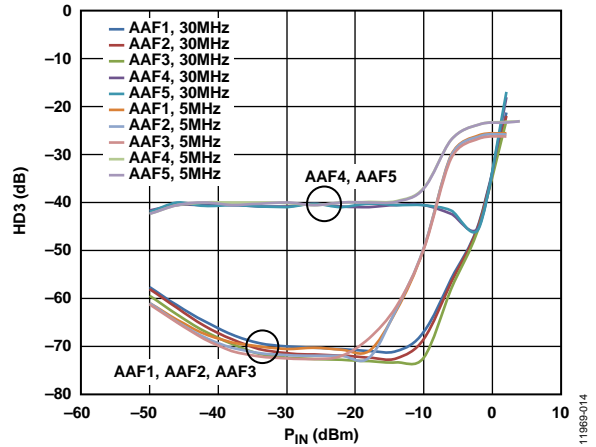


Figure 14. System HD3 for Five Anti-Alias Filters, 30 MHz and 5 MHz Filter Corners for [ADRF6510](#), 5 MHz IF Tone, GNSW = High, Front-End Gain = 12 dB

Anti-Aliasing Filter Performance Summary

Five anti-aliasing filters were tested and shown. The RC type of filter had much better harmonic distortion performance compared to the LC and RLC types. When using the [ADRF6510](#) to drive the [AD9248](#), it is recommended to use an RC filter type with a corner frequency as low as possible to achieve the best performance in the application across all the metrics.

Common-Mode Sweeps

It is possible to operate the common-mode voltage between the output of the [ADRF6510](#) and the input of the [AD9248](#) at something other than 2 V and still maintain good performance.

Figure 15 and Figure 16 show all the standard metrics over a common-mode sweep. The system maintains good performance for common-modes between 1.5 V and 3 V. The degradation for low common-mode voltage is primarily due to the [ADRF6510](#), while the degradation at high common-mode voltage is caused by a combination of the [ADRF6510](#) and the [AD9248](#). Setting the common-mode voltage at 2.25 V for the [ADRF6510](#)/[AD9248](#) is optimum.

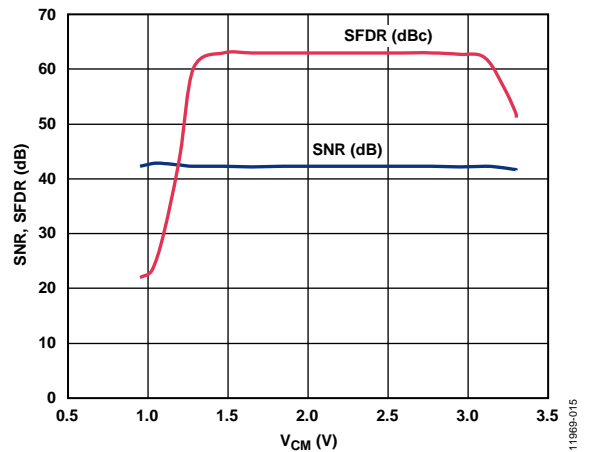


Figure 15. System SNR and SFDR vs. [ADRF6510](#) Output Common-Mode Voltage, 30 MHz [ADRF6510](#) Filter Corner, 5 MHz IF Tone, GNSW = High, Front-End Gain = 6 dB

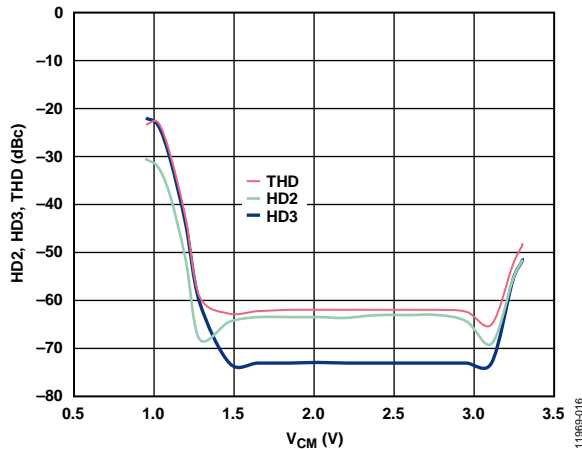


Figure 16. System HD2, HD3, and THD vs. ADRF6510 Output Common-Mode Voltage, 30 MHz ADRF6510 Filter Corner, 5 MHz IF Tone, GNSW = High, Front-End Gain = 12 dB

COMMON VARIATIONS

Different IQ Demodulators, PLLs and VCOs, ADCs

Analog Devices offers other integrated IQ demodulators such as the ADRF6806 and ADRF6807. These IQ demodulators have an RF frequency range of 50 MHz to 525 MHz, and 700 MHz to 1050 MHz, respectively. Both parts have an output common-mode of 1.65 V, making them more compatible with 3.3 V drivers and ADCs.

Analog Devices also offers solutions that separate the IQ demodulator function from the synthesizer function. IQ demodulators that operate in the same frequency range are the ADL5380, the ADL5382, and the ADL5387. Dynamic range and the quadrature system are among the differences between these IQ demodulators.

Synthesizers with integrated VCO offerings include the ADF4350, ADF4351 and the ADF4360 that operate over a wide frequency range, from 135 MHz to 4350 MHz, and have varying phase noise and output power metrics.

Adding a cascaded low noise variable gain amplifier (VGA) such as the ADL5330 before the quadrature demodulator not only adds more gain to the system, but it also helps with overall system noise performance, assuming the noise figure of the VGA is less than that of the quadrature demodulator. The noise figures of the subsequent stages are divided by the gain of the initial VGA. Another benefit of having a VGA rather than a fixed gain amplifier is that an AGC loop can be designed to maintain the incoming signal to the quadrature demodulator at a fixed level. It is important to have this ability to limit the signal levels applied to the quadrature demodulator and any subsequent stages in order to minimize distortion.

CIRCUIT EVALUATION AND TEST

Equipment Needed/Used

Signal generators include the following:

- Agilent E4438C vector signal generator
- Agilent 8665B signal generator
- Model 119-3651-00 Wenzel crystal oscillator (100 MHz)

The baseband signal capture device is the

- Agilent DSO90604A oscilloscope

The EVM computation device(s) include the following:

- Agilent 89600 VSA software
- PC running Windows XP connected to Agilent DSP90604A oscilloscope via a USB cable

The power supply includes the following:

- ± 5 V supply. All boards require +5 V with the exception of the AD8130 boards that require ± 5 V

The evaluation boards include the following:

- ADRF6801-EVALZ (one required)
- ADRF6510-EVALZ (one required)
- AD9248-BCP-65EBZ (one required)
- HSC-ADC-EVALB-DCZ (one required)
- AD8130-EBZ (two required if making EVM measurements)

Getting Started

To use the ADRF6801, ADRF6510, AD9248, and the data capture card, HSC-ADC-EVALB-DCZ, the evaluation software is needed to control various aspects of each part. This software can be found on the respective product web pages under the **Tools, Software, & Simulations Models** link. After the software is downloaded and installed, plug in the USB cables from the computer to the evaluation boards and then run the software for the part that needs to be controlled.

Functional Block Diagram

Figure 17 shows the functional block diagram of the test setup that was used for testing the receive chain. Note that the signal path is fully differential from the output of the ADRF6801 to the input of the AD9248.

Setup and Test

The first step of the setup of the receiver test is to turn on all test equipment. While the test equipment is warming up, the boards must be configured correctly for proper use in this signal chain.

On the ADRF6801 board, bypass the output baluns to obtain a fully differential, dc-coupled signal path between the ADRF6801 and the ADRF6510.

On the ADRF6510 board, do the following:

- Bypass the input and output baluns
- Replace the stock C_{OF5} capacitors with 1 μF capacitors

On the AD9248 board, the baluns were removed, and semi-rigid cables were soldered to the balun footprints. This provided a differential, dc-coupled connection between the ADRF6510 and the AD9248. The standard AD9248 evaluation board provides either single-ended ac-coupled connection (via the baluns) or a single-ended dc coupled connection (via the on-board AD8138 amplifiers). The user can use the single-ended setup and still perform all the measurements previously described except for the common-mode measurements. The full-scale voltage was set to 2 V. The anti-aliasing filters were built on the AD9248 evaluation board. There are several surface mount component pads that can be used to build the anti-aliasing filters.

Collect the evaluation boards and connect all the signal paths together, as shown in Figure 17. Connect all boards to +5 and plug in the AD9248 board and data capture board with the supplied power supplies. Ensure that the power supply current is consistent with what is expected.

Make the following connections as shown in Figure 17:

1. Connect the single-ended, 50 Ω output of the vector signal generator to RFIN of the ADRF6801 evaluation board.
2. Connect the USB cable(s) from the PC to the oscilloscope.
3. Connect the REFIN port of the ADRF6801 to a low phase noise source; in this case a Wenzel oscillator at 100 MHz.

On the Agilent E4438C vector signal generator, do the following:

1. Set the RF carrier frequency to 895 MHz.
2. Set the amplitude to -30 dBm.
3. Turn the RF port on

On the PC, start the Visual Analog Software. In the software, do the following:

1. Look for the AD9248 and open an FFT Average canvas.
2. Set the averages to 20 and set to Running Average.
3. Run the software to start collecting ADC data.

A -50 dBm to +4 dBm sweep was performed to test the receiver in this test setup. The gain on the ADRF6510 was always set to achieve a signal level of -3 dBFS at the ADC input, which was a 1.0 V p-p differential. In some cases for very small signal levels, the ADRF6510 did not have enough gain to reach the 1.0 V p-p differential level.

EVM measurements were made by connecting the I and Q differential outputs of either the ADRF6801 or the ADRF6510 to the inputs of two AD8130 evaluation boards (AD8130-EBZ) that perform the differential to single-ended signal conversion. The single-ended I and Q signals were then connected to the Agilent DSO90604A oscilloscope, and the oscilloscope connected to a Windows PC running the Agilent 89600 VSA software.

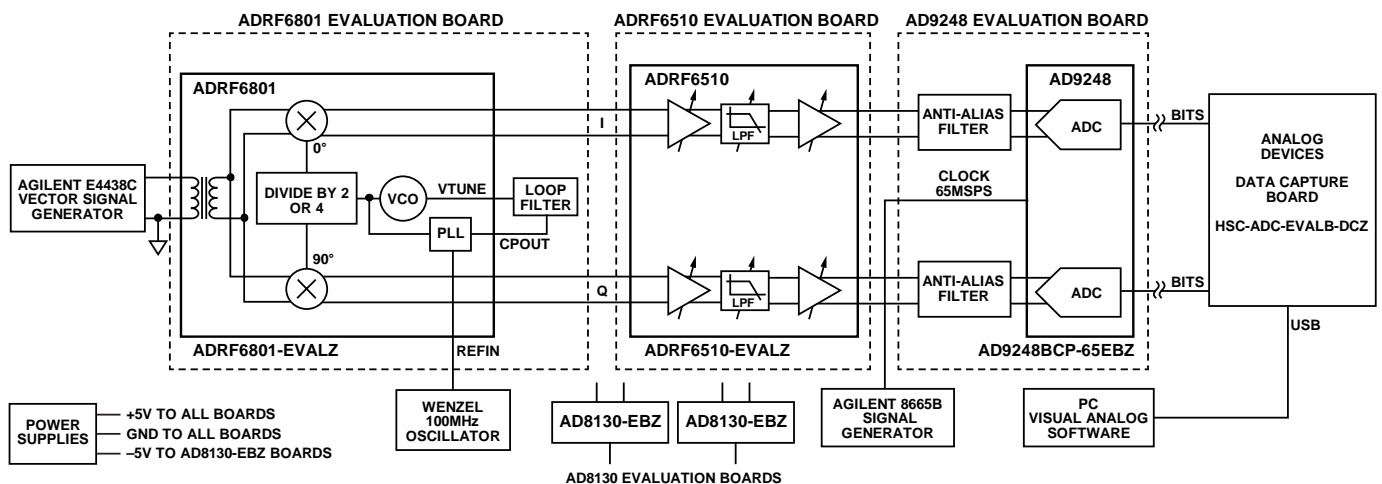


Figure 17. Functional Block Diagram for Testing Direct Conversion Receiver

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CN-0320 Design Support Package:

<http://www.analog.com/CN0320-DesignSupport>

Ardizzoni, John. *A Practical Guide to High-Speed Printed-Circuit-Board Layout*, *Analog Dialogue* 39-09, September 2005.

ADIsimPLL Design Tool

ADIsimRF Design Tool

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AN-1039 Application Note. *Correcting Imperfections in IQ Modulators to Improve RF Signal Fidelity*. Analog Devices.

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CN-0248 Circuit Note, *An IQ Demodulator-Based IF-to-Baseband Receiver with IF and Baseband Variable Gain and Programmable Baseband Filtering*, Analog Devices

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND."* Analog Devices.

MT-073 Tutorial, *High Speed Variable Gain Amplifiers (VGAs)*. Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

Data Sheets and Evaluation Boards

ADRF6801 Data Sheet and Evaluation Board

ADRF6510 Data Sheet and Evaluation Board

AD9248 Data Sheet and Evaluation Board

AD8130 Data Sheet and Evaluation Board

REVISION HISTORY

11/13—Revision 0: Initial Version

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