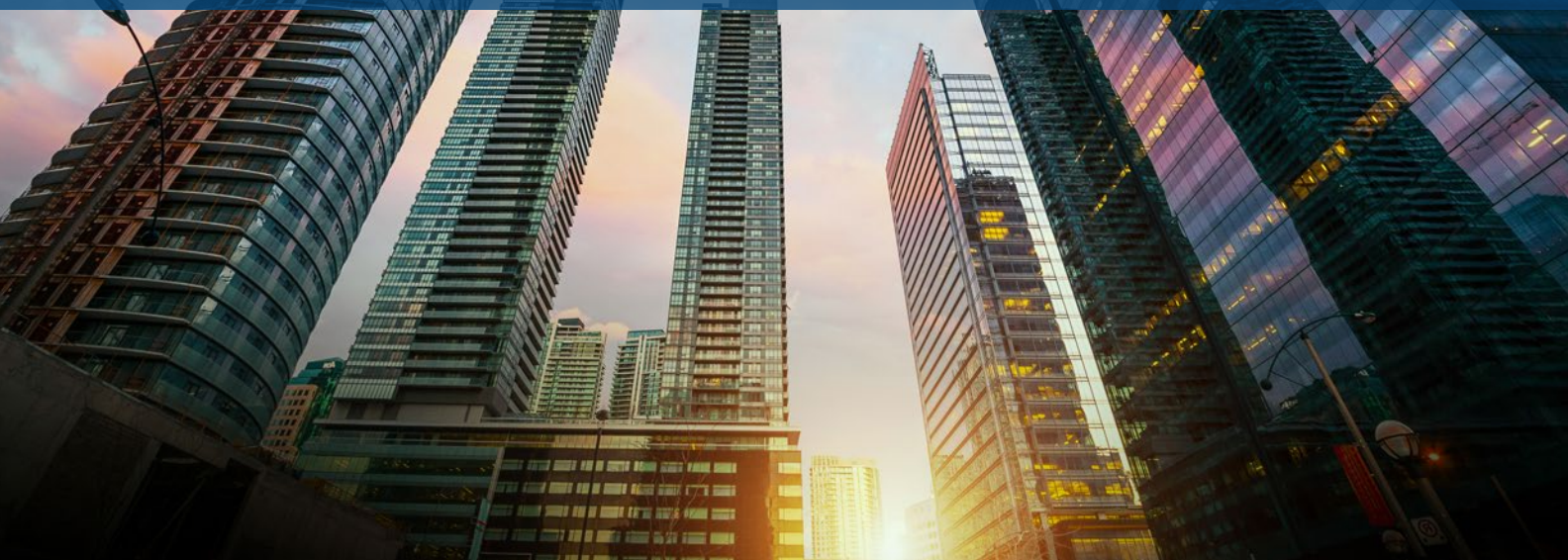


AD9375 INTEGRATED WIDEBAND RF TRANSCEIVER with Digital Predistortion (DPD) Engine

Ultralow Power DPD Solution Integrated with Award Winning AD9371 Wideband Transceiver



Ultralow Power DPD

- ▶ Solution consumes 10× less power than alternative solutions
- ▶ DPD algorithm optimized for power and area restricted 3G/4G small cell and massive MIMO applications up to 40 MHz bandwidth
- ▶ Enables use of high efficiency power amplifier (PA) to reduce system power consumption

Highly Integrated, Versatile Solution

- ▶ Smart system partition: DPD integration reduces interface bandwidths and SERDES lanes by 50%, resulting in lower system power consumption and smaller form factors
- ▶ Versatility: offers a common platform design for small cell and massive MIMO applications, covering all 3GPP frequency bands: 300 MHz to 6 GHz

Reduced FPGA Size and Cost

- ▶ Requires fewer FPGA resources and SERDES lanes, simplifying FPGA and reducing overall FPGA cost

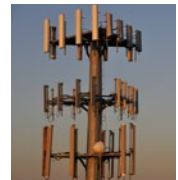
Ease of Use

- ▶ Complete development toolkit to accelerate time to market
- ▶ Library of PAs tested in collaboration with leading PA vendors
- ▶ Detailed user guides, complete application program interface (API), control GUIs
- ▶ Evaluation kit with PA daughtercard
- ▶ Complete 2 × 2 LTE, 250 mW small cell radio reference design

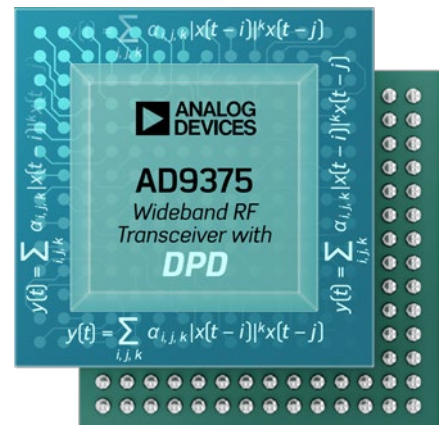
Environmentally Friendly

- ▶ Reduce base station carbon footprint with lowest power consumption DPD solution on the market

Applications



- ▶ 3G/4G small cell base stations (BTS)
- ▶ 3G/4G massive MIMO/active antenna systems



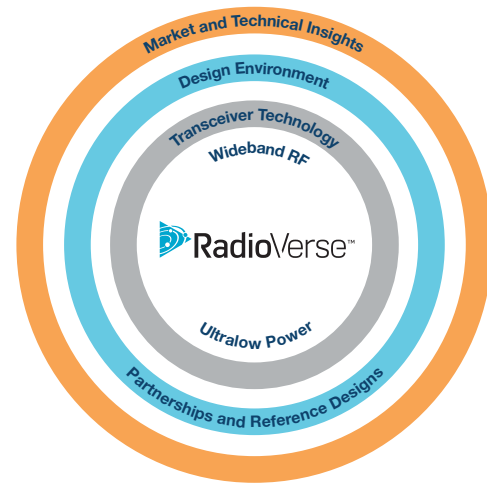
AD9375 Functionality

- ▶ Dual differential transmitters (Tx)
- ▶ Dual differential receivers (Rx)
- ▶ Observation receiver (ORx) with 2 inputs
- ▶ Sniffer receiver (SnRx) with 3 inputs
- ▶ Fully integrated ultralow power DPD actuator and adaptation engine for PA linearization
- ▶ DPD block power consumption <100 mW
- ▶ Linearization signal bandwidth (BW) to 40 MHz
- ▶ Supports 3G/4G waveforms
- ▶ Tunable range: 300 MHz to 6 kHz
- ▶ Transmitter synthesis BW to 250 MHz
- ▶ Receiver BW: 8 MHz to 100 MHz
- ▶ Supports frequency division duplex (FDD) and time division duplex (TDD) operation
- ▶ Fully integrated independent fractional-N radio frequency (RF) synthesizers for transmitters, receivers, observational receivers, and clock generation
- ▶ JESD204B digital interface
- ▶ Pin compatible with [AD9371](#)

RadioVerse™ Ecosystem and Partnerships

ADI has partnered with leading PA vendors to optimize linearization performance with high efficiency PAs and [AD9375](#) DPD. Reports for PAs with a range of different output powers and frequencies are available, enabling the system designer to quickly choose a PA suitable for their system. See the library of tested PA reports on analog.com/radioverse.

ADI has partnered with Benetel™ to develop a complete 2 × 2 LTE, 250 mW small cell radio reference design. The reference design contains all components required to implement the radio functionality from JESD204B to antenna, reducing small cell product development time and accelerating time to market.

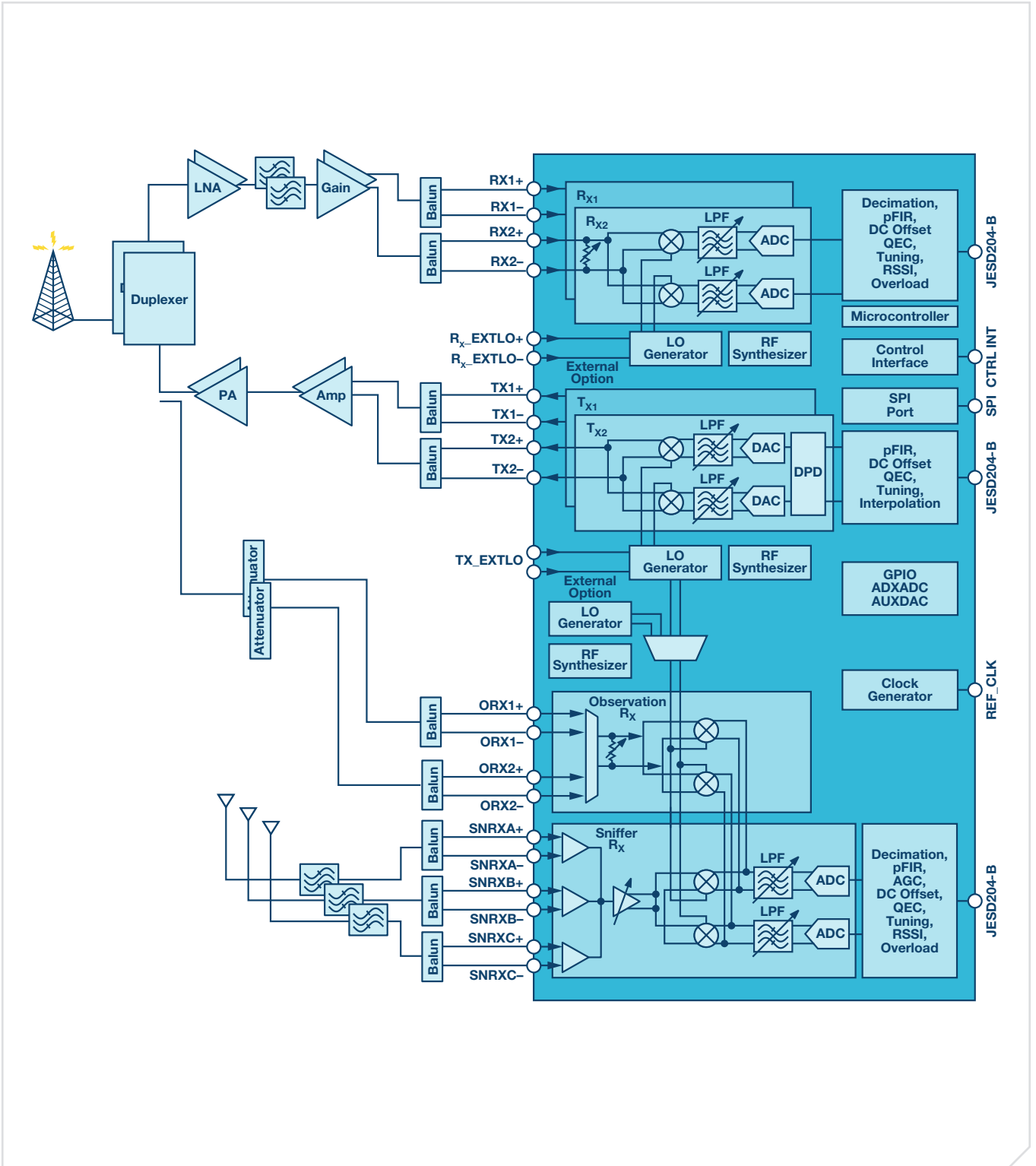


Evaluation, Prototyping, and Reference Design Options

ADI provides a full set of software and hardware tools for evaluation, prototyping, and reference design. The following table outlines the available hardware and software tools.

	FMC Mezzanine Cards	FMC Motherboards	FPGA Design	Control and Data Capture
<i>Evaluation System</i>	<ul style="list-style-type: none"> ▶ ADRV9375-N/PCBZ ▶ High efficiency power amplifier daughter card 	<ul style="list-style-type: none"> ▶ Xilinx® ZC706 	<ul style="list-style-type: none"> ▶ Binary image provided, verified with Xilinx JESD204B IP 	<ul style="list-style-type: none"> ▶ Operating system agnostic API source in ANSIC ▶ Transceiver configuration and data capture via the AD937x Windows® GUI ▶ DPD configuration via the AD9375 DPD GUI
<i>Prototyping Platform</i>	<ul style="list-style-type: none"> ▶ ADRV9375-N/PCBZ ▶ High efficiency power amplifier daughter card 	<ul style="list-style-type: none"> ▶ Variety of Xilinx development boards 	<ul style="list-style-type: none"> ▶ Publicly available HDL on GitHub, verified with Xilinx and Altera® JESD204B cores 	<ul style="list-style-type: none"> ▶ Open-source Linux driver ▶ Open-source Linux IIO device driver ▶ Steams data to GNU radio, MATLAB®, and Simulink®
<i>Small Cell Radio Reference Design</i>	<ul style="list-style-type: none"> ▶ ADRV-DPD1/PCBZ with interposer card 	<ul style="list-style-type: none"> ▶ Xilinx ZC706 	<ul style="list-style-type: none"> ▶ Binary image provided, verified with Xilinx JESD204B IP 	<ul style="list-style-type: none"> ▶ Command/control and data capture via the AD937x Windows GUI

Radio System Block Diagram with AD9375 DPD



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Circuits from the Lab Reference Designs

Circuits from the Lab® reference designs are built and tested by ADI engineers with comprehensive documentation and factory-tested evaluation hardware.

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