AN-737
APPLICATION NOTE

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How ADIsimADC Models an ADC
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CONVERTER MODELING

Converter modeling has often been overlooked, omitted, or accomplished using an ideal data converter model. With more and more systems using mixed-signal technology, the importance of system modeling is ever increasing. Coupled with shortened design cycles and pressure for first pass success, this drives the continuing importance of complete system modeling. ADIsimADC™ has been developed to answer this growing need.

Often ideal converter models are used for functional modeling, but these fail to give the required details of performance to determine if a particular device meets the desired goals of the system. This is why ADIsimADC has been developed. For the first time, ADIsimADC provides a means for users to validate performance of a particular converter in their system, using their conditions to determine the applicability of a selected device. While ADIsimADC does not emulate every characteristic of an ADC, it goes a long way towards achieving the goal of allowing users to model real converters in their system simulations.

BIT EXACT vs. BEHAVIORAL

A bit exact model is a model that, given a known stimulus, provides a known and predictable output. ADIsimADC is not a bit exact model. These types of models are often found in digital systems. In dealing with analog functions, there is never a known response for a given input because of noise, distortion, and other nonlinearities. While some portion of the response may be predictable, much of the remainder is subject to distortion, noise, and even part-to-part variation. Additionally, to provide a bit exact model requires providing circuit simulation files, such as SPICE models, that process transient response. However, these models are large, complex, very slow and, in the end, provide limited accuracy. A reduced or equivalent SPICE model reduces the complexity, but is not able to provide adequate modeling of fine details of static and dynamic performance.

A behavior model eliminates the complexity and, at the same time, allows modeling of fine performance details not possible to attain with a circuit file. ADIsimADC in conjunction with VisualAnalog™ acts as a standalone converter evaluation tool.

ADIsimADC™ can also be used with many other third party simulation tools, including ADS from Agilent Technologies, VSS from Applied Wave Research, Inc, National Instrument tools, as well as MATLAB® and C++. Usage information with these tools can be found at www.analog.com/ADIsimADC.

MODEL vs. HARDWARE

Modeling a system or an ADC should never be a substitute for building and characterizing a real system. It is one thing to model a circuit, but it is another matter to actually build it and test it.

As with any analog or mixed-signal device, proper layout and configuration is required to achieve the performance shown in simulation. Therefore, it is important that all layout rules and guidelines be followed as shown in the product data sheet (see Figure 4). An example is the importance of providing adequate power supply bypass capacitors. Because mixed-signal devices include some amount of digital circuitry, digital switching noise is often a problem, and failure to provide capacitors to moderate these switching currents can significantly reduce performance of even the best devices. Other support devices are often required around the converter, including additional capacitors, inductors, and resistors. The best way to know what is required is to consult the product data sheet and the evaluation board schematic.

WHICH SPECIFICATIONS ARE IMPORTANT TO MODEL?

ADIsimADC is targeted to provide realistic performance of real devices. Which specification is important to model depends on what kind of analysis the user is trying to perform. For example, control loops need accurate transfer function and delay information, while radio systems may require an accurate representation of noise and distortion. ADIsimADC models many of the critical specifications of data converters, including: offset, gain, sample rate, bandwidth, jitter, latency, and both ac and dc linearity. (See the AN-835 Application Note *Understanding High Speed ADC Testing and Evaluation*, for additional information on ac linearity.)

This application note describes these specifications in detail and how ADIsimADC treats them.

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GAIN, OFFSET, AND DC LINEARITY

The full-scale range of the converter is defined by the design of the converter. It can be fixed, selectable, or variable. Gain error of a converter is the deviation from the nominal value, often called the input span. Because an ADC is a voltage input device, the full-scale range is specified in volts at dc or low frequency.

Offset is defined as the deviation of the actual major carrier transition from one-half of the full-scale range of the converter. This can be measured by shorting the input(s) to one-half of the full scale. Many devices have internal connections that bias the input pins to set up the input common-mode voltage (see Figure 1). On such devices, it is not necessary to make this connection externally. The input can be floated in the case of a single-ended input, or shorted together in the case of differential inputs. Devices that do not have connections internally to the common-mode voltage must be externally connected (see Figure 2). As with input span, the common-mode voltage can be either fixed or adjustable. The device data sheet should be consulted to determine how it is configured.
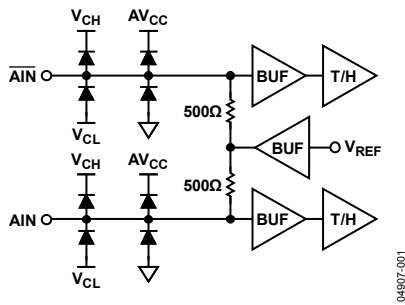

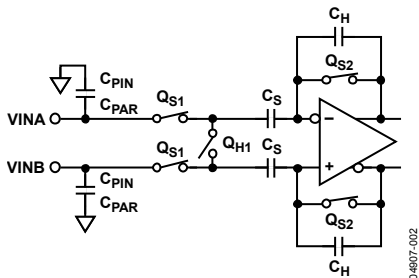Figure 1. Typical Analog Input with Internal Common-Mode Voltage

Figure 2. Typical Analog Input Without Internal Common-Mode Voltage

ADIsimADC does not allow either the input span or the common mode to be changed. Different converter models are provided for devices with multiple input spans. The common mode is fixed for all devices and cannot be changed. If it is desired to model a system that uses a different common-mode range, the difference can be subtracted by an external offset.

The dc linearity (see Figure 3) for an ADC is determined by the quantization method and the static transfer function of the converter. There are many types of converters, each of which has a unique transfer function and produces different results at dc and at high frequency. In the References section, see the Brannon (2001) and Kester (2004) references for more information about the different types of converters, and how the transfer function affects a converter performance.
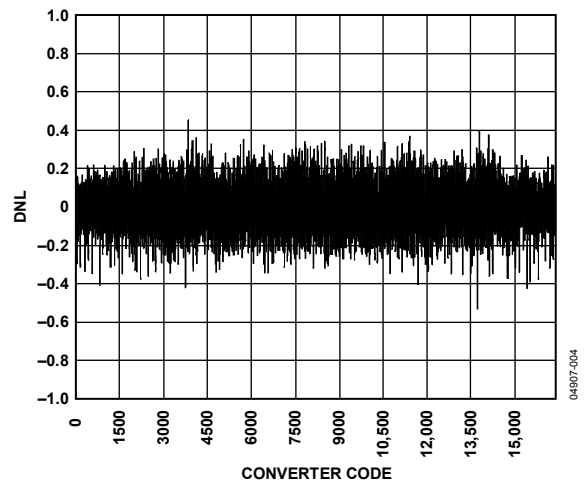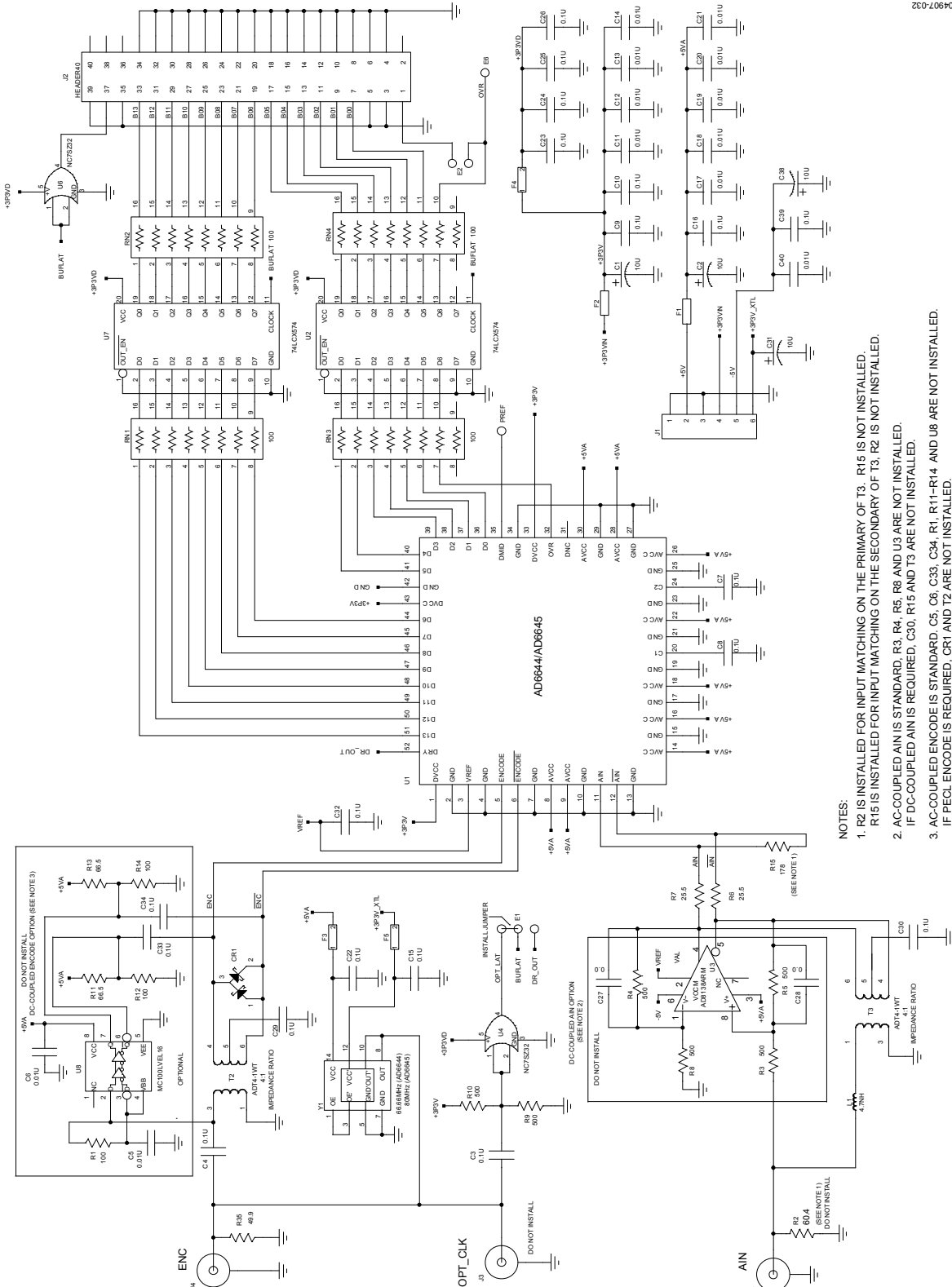

Figure 3. Typical Converter DNL, an Important Contributor to the Converter Transfer Function

Figure 4. Typical Evaluation Board Schematic: Shows Typical Support Components

SAMPLE RATE

Converter performance changes as both the sample rate and analog input frequency change. From a sample rate point of view, most good converters provide consistent performance from the minimum to the maximum specified sample rates (see Figure 5). At sample rates below the minimum, some converters fail to operate properly. This may be due to charges stored on on-chip capacitors that are discharging or drooping, causing incorrect data conversion. Therefore, the converter data sheet should be consulted to determine the minimum usable sample rate. Above the maximum sample rate, one of two problems may occur. The device may not be able to pass on-chip digital signals from one stage to the next. This is the result of running out of setup or hold time on chip. The other problem is failure of a critical analog signal to stabilize during the time allocated to the process. One such example is acquisition time for a hold capacitor. As before, the data sheet should be consulted to determine the maximum sample rate. ADIsimADC uses the specified sample rate to determine how the converter should perform. However, outside the specified range of the device, the model produces all zero results.

BANDWIDTH

As the analog input frequency is increased, attenuation in the amplitude response effectively increases the apparent full-scale range of the converter, causing a roll-off in the response of the converter. The frequency where the response has diminished by 3 dB is called the 3 dB bandwidth of the converter.
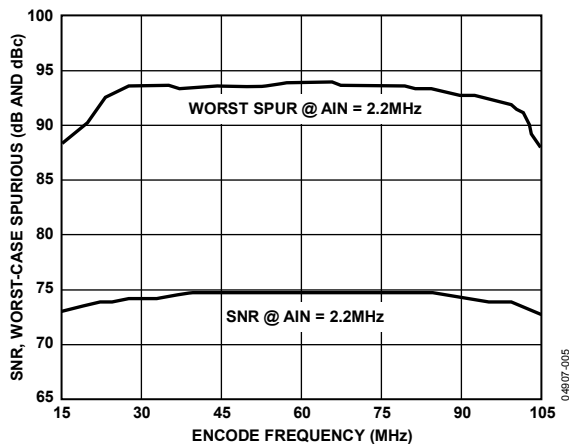

Figure 5. Typical Converter Performance vs. Sample Rate Bandwidth

A converter's performance rolls off according to its frequency response as the analog input frequency increases (see Figure 6). This is modeled in ADIsimADC and results in a reduced response within the model. To counter this loss, the input signal amplitude must increase above the span specified as the default for the model, resulting in an input that appears to be above the full-scale range of the converter. In reality, this signal is attenuated by package and device parasitics, as well as the filter formed by the hold capacitor of the sample-and-hold amplifier (SHA), and, therefore, the signal is actually within the specified span.
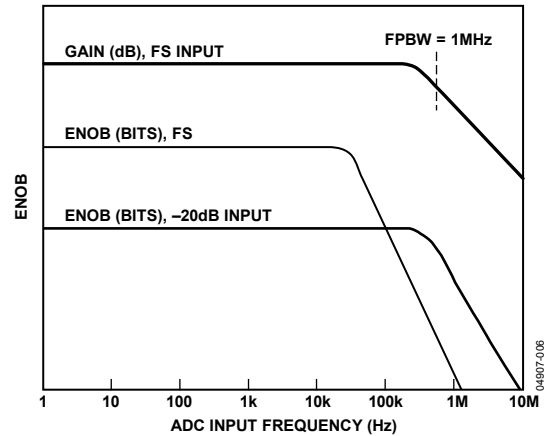

Figure 6. Typical Converter Analog Bandwidth

DISTORTION: DYNAMIC AND STATIC

Due to an ADC's finite bandwidth, there is also a fundamental slew rate limitation, or dynamic limitation. This slew rate limitation is one source of distortion within an ADC. As the input frequency of a data converter is swept from dc to some upper frequency, the SFDR performance and the harmonic performance of the converter decline (see Figure 7).
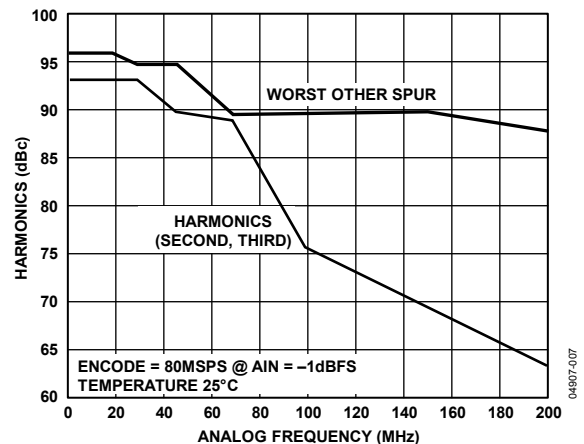

Figure 7. Typical Converter Performance vs. Analog Input Frequency

Because distortion limitations are due at least in part to slew rate issues, the amplitude of the signal input can be reduced while keeping the analog frequency constant, resulting in a reduced slew rate and improved harmonics and distortion relative to the full scale of the converter. While these spurs do not always follow the classic trend of nth-order products, this trend can often be weakly observed. As the signal levels are reduced, dynamic effects diminish, but static effects rapidly replace them as the dominant contributor to distortion.

Static distortion is distortion due to the transfer function of the converter (see Figure 8). This distortion often has some very unpredictable results. This may include spurs that change rapidly as a function of input level, and can exhibit both positive and negative slope characteristics. Largely, these spurs are due to the architecture characteristics of the converter. Different converters have different static transfer functions, resulting in very different distortion responses. Additionally, because these

are analog components, each part within the same design exhibit different responses to an input signal. Therefore, on a part-to-part basis, some variation exists.
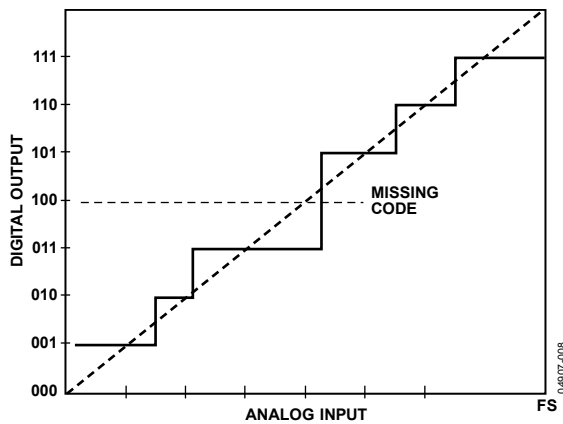

Figure 8. Typical Data Conversion Transfer Function

ADIsimADC attempts to model the nominal performance of the data converter. While it does an excellent job, some part-to-part variation is normal. Consult the converter data sheet to determine what performance variation can be expected.

JITTER

In addition to the analog input slew rate limitations of the converter, one of the most difficult aspects of sampling high frequency analog signals is jitter. Jitter is the sample-to-sample variation in the sampling process at the front end of every data converter. At low analog input frequencies, the jitter is negligible. However, at high analog input frequencies, errors made in the analog sampling process due to jitter can cause significant degradation (see Figure 9). While the sampling time errors can be on the order of femtoseconds, the resulting limitations in SNR can be significant (see the AN-501 Application Note, *Aperture Uncertainty and ADC System Performance*, available at www.analog.com). Although there are multiple contributors to overall noise, at high frequencies, jitter is clearly the dominant factor, especially for high resolution converters, as shown in Equation 1.
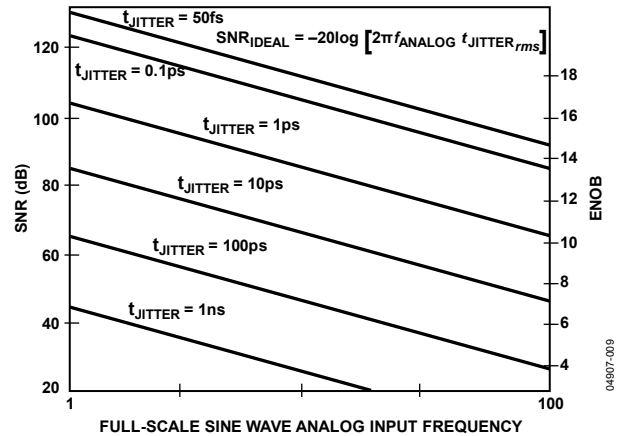

Figure 9. Typical Converter Performance vs. Jitter

There are two sources of jitter. The first is the native or internal jitter to the device. Because most contemporary converter designers seek to minimize the internal jitter by various techniques, internal jitter is usually the smaller (but not negligible) of the two types. The second and major source of jitter is the external clock jitter. When the model is computing the noise due to jitter, these two jitter sources are combined prior to the noise being computed.

ADIsimADC estimates the instantaneous slew rate of the input signal and multiplies this by a Gaussian modeled jitter noise source with a sigma equal to the combined rms values of the internal and external jitter. The result is a jitter contribution to the noise that accurately models the effects of jitter as a function of both the analog input frequency and amplitude level. The default for external jitter is that of the setup used during characterization of the device. However, the user can set this to any value.

$$SNR = -20\log\left[\sqrt{\left(2\pi f_{ana\log} t_{jitter_{rms}}\right)^2 + \left(\frac{2}{3}\right)\left(\frac{1+\varepsilon}{2^N}\right)^2 + \left(\frac{2V_{Noise_{rms}}\sqrt{2}}{2^N}\right)^2}\right] \qquad (1)$$

LATENCY

Many types of converters include a delay between the sample time and when valid data appears on the digital outputs. SAR and flash converters generally provide output data immediately after the sample period. Multistage converters, such as pipelined and Σ-Δ converters, do not offer an output for many clock cycles. This is a concern for control systems and other systems where latency is important. ADIsimADC models latency in terms of whole values of the clock period. This has the effect of producing invalid data at the beginning of a conversion period while the pipeline fills, as well as producing valid data after the end of the conversion period while the pipeline flushes. Care must be taken when using the model to properly account for the pipeline delay either by flushing the buffer or by other means.

CONCLUSION

ADIsimADC is a useful tool for simulating ADC performance under specific operating conditions. The software emulates real world conditions, enabling more complete system modeling. While it is not a replacement for hardware, it is a good first step to understanding how an ADC works in a system design.

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ANALOG
DEVICES

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