ANALOG DEVICES

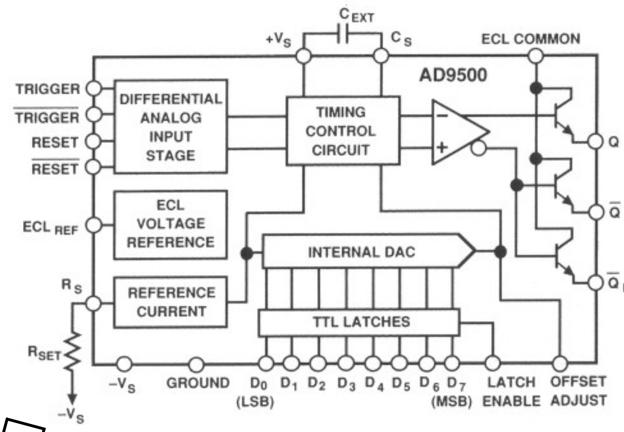
Digitally Programmable Delay Generator

AD9500

FEATURES
10ps Delay Resolution
2.5ns to 10μs Full-Scale Range
Fully Differential Inputs
Separate Trigger and Reset Inputs
Low Power Dissipation – 310mW

APPLICATIONS
ATE
Pulse Deskewing
Arbitrary Waveform Generators
High-Stability Timing Source
Multiple Phase Clock Generators

AD9500 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

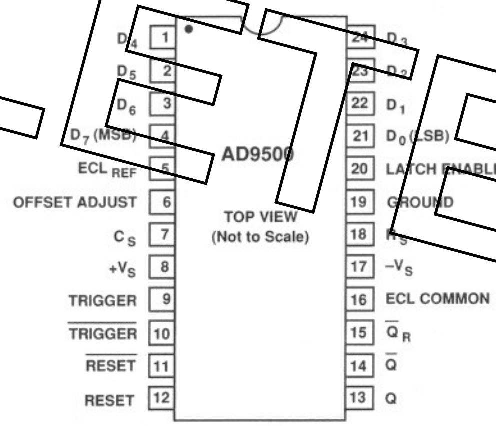
The AD9500 is a digitally programmable delay generator, which provides programmed delays, selected through an 8-bit digital code, in resolutions as small as 10ps. The AD9500 is constructed in a high-performance bipolar process, designed to provide high-speed operation for both digital and analog circuits.

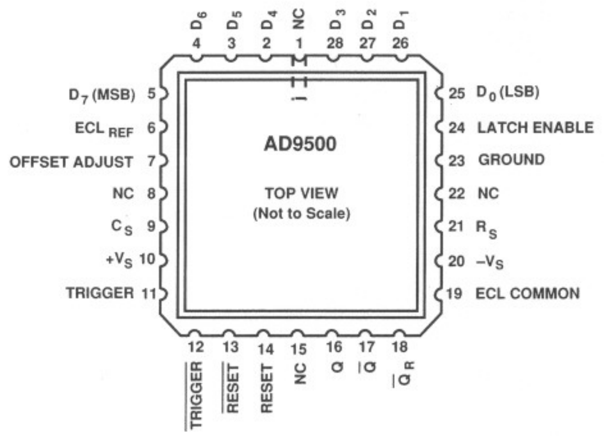
The AD9500 employs differential TRIGGER and RESET inputs which are designed primarily for ECL signal levels but function with analog and TTL input levels. An on-board ECL reference midpoint allows both of the inputs to be driven by either single ended or differential ECL circuits. The AD9500 output is a complementary ECL stage, which also provides a parallel $\overline{Q_R}$ output circuit to facilitate reset timing implementations.

The digital control data is passed to the AD9500 through a transparent latch controlled by the LATCH ENABLE signal. In the transparent mode, the internal DAC of the AD9500 will attempt to follow changes at the inputs. The LATCH ENABLE is otherwise used to strobe the digital data into the AD9500 latches.

The AD9500 is available as an industrial temperature range device, −25°C to +85°C, and as an extended temperature range device, −55°C to +125°C. Both grades are packaged in a 24-pin ceramic "Skinny" DIP (0.3″ package width), as well as 28-pin surface mount packages. Extended temperature devices are fully qualified to MIL-STD-883, Class B.

PIN CONFIGURATIONS





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AD9500—SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage ($+V_S$) . . . . +7V
Negative Supply Voltage ($-V_S$) . . . . −7V
ECL COMMON to Ground Differential . . −2.0V to +5.0V
Digital Input Voltage Range . . . . −3.5V to +5.0V
Trigger/Reset Input Voltage Range . . . . ±5.0V
Trigger/Reset Differential Voltage 5.0V
Minimum R_{SET} 220Ω
Digital Output Current (Q and $\overline{Q}$) 30mA
Digital Output Current ($\overline{Q_R}$) 2mA
Offset Adjust Current (Sinking) 4mA
Operating Temperature Range
AD9500BP/BQ . . . . −25°C to +85°C
AD9500TE/TQ/883B . . . . −55°C to +125°C
Storage Temperature Range . . . . −65°C to +150°C
Junction Temperature . . . . +175°C
Lead Soldering Temperature (10sec) . . . . +300°C

ELECTRICAL CHARACTERISTICS (Supply Voltages $+V_S = +5.0V$, $-V_S = -5.2V$; $C_{EXT} = 0pF$; $R_{SET} = 500\Omega$, unless otherwise stated)

Parameter	Test Level	Mil[3] Sub Group	Temp	Industrial −25°C to +85°C AD9500BP/BQ Min	Typ	Max	Military −55°C to +125°C AD9500TE/TQ/883B Min	Typ	Max	Units
RESOLUTION				8			8			Bits
ACCURACY[4]										
Differential Linearity	I	7	+25°C			0.5			0.5	LSB
Integral Linearity	I	7	+25°C			1.0			1.0	LSB
Monotonicity	I	7	+25°C		Guaranteed			Guaranteed		
DIGITAL INPUT										
Logic "1" Voltage	VI	7, 8	Full	2.0			2.0			V
Logic "0" Voltage	VI	7, 8	Full			0.8			0.8	V
Logic "1" Current	VI	1, 2, 3	Full			5			5	µA
Logic "0" Current	VI	1, 2, 3	Full			5			5	µA
Digital Input Capacitance	VI		+25°C			5.5			5.5	pF
Data Setup Time[5]	V		+25°C		0.4	0.75		0.4	0.75	ns
Data Hold Time[6]	V		+25°C		0.4	0.75		0.4	0.75	ns
Latch Pulse Width (t_{LPW})	V		+25°C	3.0			3.0			ns
RESET/TRIGGER INPUTS[7]										
TRIGGER Input Voltage Range	IV		Full		−2.5; 4.5			−2.5; 4.5		V
RESET Input Voltage Range	IV		Full		−2.5; 2.0			−2.5; 2.0		V
Differential Switching Voltage	IV	7, 8	Full		40	300		40	300	mV
Input Bias Current	I	1	+25°C		40	50		40	50	µA
	VI	2, 3	Full			75			75	µA
Input Resistance	IV		+25°C		4			4		kΩ
Input Capacitance	IV		+25°C		6.5	7.25		6.5	7.25	pF
Minimum Input Pulse Width t_{TPW}, t_{RPW}	V		+25°C		2.0			2.0		ns
DYNAMIC PERFORMANCE[8]										
Maximum Trigger Rate	IV		+25°C		60			60		MHz
Minimum Propagation Delay (t_{PD})[9]	I	4	+25°C	5.4	6.4	7.4	5.4	6.4	7.4	ns
Minimum Propagation Delay TC	V		Full		7.5			7.5		ps/°C
Full-Scale Range TC[10]	V		Full		0.5			0.5		ps/°C
Delay Uncertainty (Jitter)	V		+25°C		10			10		ps
Reset Propagation Delay (t_{RD})[11]	I	4	+25°C	5.4	6.4	7.4	5.4	6.4	7.4	ns
Reset-to-Trigger Holdoff (t_{THO})[12]	IV		+25°C	0.2	0		0.2	0		ns
Trigger-to-Reset Holdoff (t_{RHO})[13]	IV		+25°C	2.0	1.5		2.0	1.5		ns
Minimum Output Pulse Width	V		+25°C		3.3			3.3		ns
Output Rise Time[8]	I	9	+25°C			2.0			2.0	ns
Output Fall Time[8]	I	9	+25°C			2.0			2.0	ns
Delay Coefficient Settling Time (t_{DAC})[14]	V		+25°C		29			29		ns
Linear Ramp Settling Time (t_{LRS})	V		+25°C		22			22		ns

Parameter	Test Level	Mil[3] Sub Group	Temp	Industrial −25°C to +85°C AD9500BP/BQ Min	Typ	Max	Military −55°C to +125°C AD9500TE/TQ/883B Min	Typ	Max	Units
SUPPORT FUNCTIONS										
ECL_{REF}	IV	1	+25°C	−1.4	−1.3	−1.2	−1.4	−1.3	−1.2	V
ECL_{REF} Voltage Drift[15]	V		Full		1.1			1.1		mV/°C
Offset Adjust Range	V		Full		−2			−2		mA
DIGITAL OUTPUTS[8]										
Logic "1" Voltage	VI	1, 2, 3	Full	−1.1			−1.1			V
Logic "0" Voltage	VI	1, 2, 3	Full			−1.5			−1.5	V
POWER SUPPLY[16]										
Positive Supply Current (+5.0V)	I	1	+25°C		24	28		24	28	mA
	VI	2, 3	Full			30			30	mA
Negative Supply Current (−5.2V)	I	1	+25°C		37	42		37	42	mA
	VI	2, 3	Full			44			44	mA
Nominal Power Dissipation	V		+25°C		312			312		mW
Power Supply Rejection Ratio[17]										
Full-Scale Range Sensitivity	I	7	+25°C		70	300		70	300	ps/V
Minimum Propagation Delay Sensitivity	I	7	+25°C		150	500		150	500	ps/V

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Typical thermal impedance

24-Pin Ceramic	$\theta_{JA} = 56°C/W$; $\theta_{JC} = 16°C/W$
28-Pin PLCC (Plastic)	$\theta_{JA} = 60°C/W$; $\theta_{JC} = 22°C/W$
28-Pin Ceramic LCC	$\theta_{JA} = 69°C/W$; $\theta_{JC} = 25°C/W$

[3]Military subgroups apply to military qualified devices only.

[4]$R_{SET} = 10k\Omega$ (Full-scale delay = 100ns).

[5]The digital data inputs must remain stable for the specified time prior to the LATCH ENABLE signal.

[6]The digital data inputs must remain stable for the specified time after the LATCH ENABLE signal.

[7]The TRIGGER and RESET inputs are differential and must be driven relative to one another. Both of these inputs are ECL compatible, but can also be used with TTL logic families in a limited fashion.

[8]Outputs terminated through 50Ω resistors to −2.0V.

[9]Program Delay = 0.0ps (Digital Data = 00_H). In Operation, any programmed delays are in addition to the Minimum Propagation Delay.

[10]Change in total delay through AD9500, exclusive of changes in minimum-propagation delay t_{PD}.

[11]Measured from the 50% transition point of the reset signal input, to the 50% transition point of the resetting output.

[12]Minimum time from falling edge of RESET to triggering input, to insure a valid output event.

[13]Minimum time from triggering event to rising edge of RESET, to insure a valid output event.

[14]Measured from the LATCH ENABLE input to the point when the AD9500 becomes 8-bit accurate again, after a full-scale change in the programmed delay.

[15]Standard 10K and 10KH ECL families operate with a 1.1mV/°C drift by design.

[16]Supply voltages should remain stable within ±5% for normal operation.

[17]Measured at ±5% of $-V_S$ and $+V_S$.

Specifications subject to change without notice.

EXPLANATION OF GROUP A MILITARY SUBGROUPS

Subgroup 1 – Static tests at +25°C.
Subgroup 2 – Static tests at max rated operating temp.
Subgroup 3 – Static tests at min rated operating temp.
Subgroup 4 – Dynamic tests at +25°C.
Subgroup 5 – Dynamic tests at max rated operating temp.
Subgroup 6 – Dynamic tests at min rated operating temp.
Subgroup 7 – Functional tests at +25°C.
Subgroup 8 – Functional tests at max and min rated operating temp.
Subgroup 9 – Switching tests at +25°C.
Subgroup 10 – Switching tests at max rated operating temp.
Subgroup 11 – Switching tests at min rated operating temp.
Subgroup 12 – Periodically sample tested.

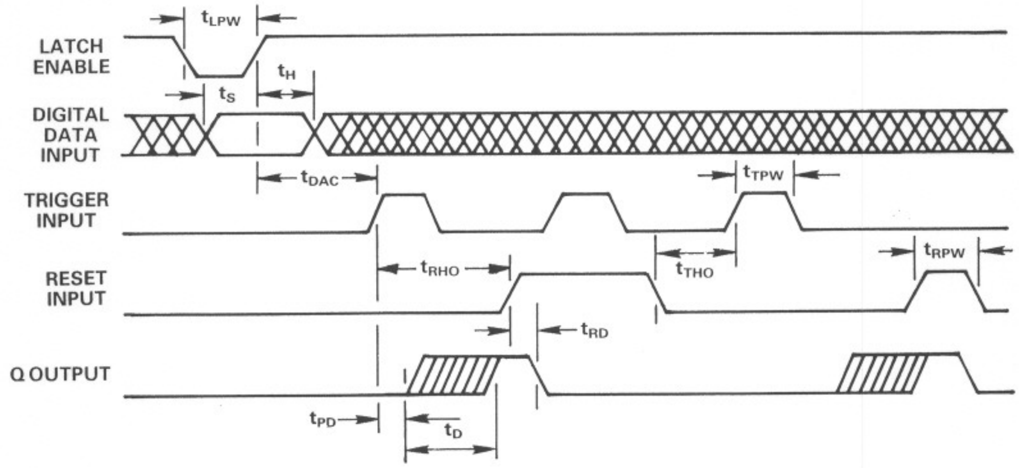
EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures.
III – Periodically sample tested.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

FUNCTIONAL DESCRIPTION

PIN NAME	DESCRIPTION
D_4–D_6	– One of eight digital inputs used to set the programmed delay.
D_7 (MSB)	– One of eight digital inputs used to set the programmed delay. D_7 (MSB) is the most significant bit of the digital input word.
ECL_{REF}	– ECL midpoint reference, nominally −1.3V. Use of the ECL_{REF}, allows either of the TRIGGER or the RESET inputs to be configured for single-ended ECL inputs.
OFFSET ADJUST	– The OFFSET ADJUST is used to adjust the minimum propagation delay (t_{PD}), by pulling or pushing a small current out of or into the pin.
C_S	– C_S allows the full-scale range to be extended by using an external timing capacitor. The value of C_{EXT}, connected between C_S and $+V_S$, may range from no external capacitance to 0.1μF+. See R_S ($C_{INTERNAL}$ = 10pF).
$+V_S$	– Positive supply terminal, nominally +5.0V.
TRIGGER	– Noninverted input of the edge-sensitive differential trigger input stage. The output at Q will be delayed by the programmed delay, after the triggering event. The programmed delay is set by the digital input word. The TRIGGER input must be driven in conjunction with the $\overline{\text{TRIGGER}}$ input.
$\overline{\text{TRIGGER}}$	– Inverted input of the edge-sensitive differential trigger input stage. The output at Q will be delayed by the programmed delay, after the triggering event. The programmed delay is set by the digital input word. The $\overline{\text{TRIGGER}}$ input must be driven in conjunction with the TRIGGER input.
$\overline{\text{RESET}}$	– Inverted input of the level-sensitive differential reset input stage. The output at Q will be reset after a signal is received at the reset inputs. In the "minimum configuration," the minimum output pulse width will be equal to the "reset propagation delay," t_{RD}. The RESET input must be driven in conjunction with the $\overline{\text{RESET}}$ input.
RESET	– Noninverted input of the level-sensitive differential reset input stage. The output at Q will be reset after a signal is received at the reset inputs. In the "minimum configuration," the minimum output pulse width will be equal to the "reset propagation delay," t_{RD}. The $\overline{\text{RESET}}$ input must be driven in conjunction with the RESET input.
Q	– One of two complementary ECL outputs. A "triggering" event at the inputs will produce a logic HIGH on the Q output. A "resetting" event at the inputs will produce a logic LOW on the Q output
$\overline{Q}$	– One of two complementary ECL outputs. A "triggering" event at the inputs will produce a logic LOW on the $\overline{Q}$ output. A "resetting" event at the inputs will produce a logic HIGH on the $\overline{Q}$ output.
$\overline{Q_R}$	– $\overline{Q_R}$ output is parallel to the $\overline{Q}$ output. The $\overline{Q_R}$ output is typically used to drive delaying circuits for extending output pulse widths. A "triggering" event at the inputs will produce a logic LOW on the $\overline{Q_R}$ output. A "resetting" event at the inputs will produce a logic HIGH on the $\overline{Q_R}$ output.
ECL COMMON	– The collector common for the ECL output stage. The collector common may be tied to +5.0V, but normally it is tied to the circuit ground for standard ECL outputs.
$-V_S$	– Negative supply terminal, nominally −5.2V.
R_S	– R_S is the reference current setting terminal. An external setting resistor, R_{SET}, connected between R_S and $-V_S$ determines the internal reference current. See C_S ($250\Omega \leq R_{SET} \leq 50k\Omega$).
GROUND	– The ground return for the TTL and analog inputs.
LATCH ENABLE	– Transparent TTL latch control line. A logic HIGH on the LATCH ENABLE freezes the digital code at the logic inputs. A logic LOW on the LATCH ENABLE allows the internal current levels to be continuously updated through the logic inputs D_0 thru D_7.
D_0 (LSB)	– One of eight digital inputs used to set the programmed delay. D_0 (LSB) is the least significant bit of the digital input word.
D_3–D_1	– One of eight digital inputs used to set the programmed delay.

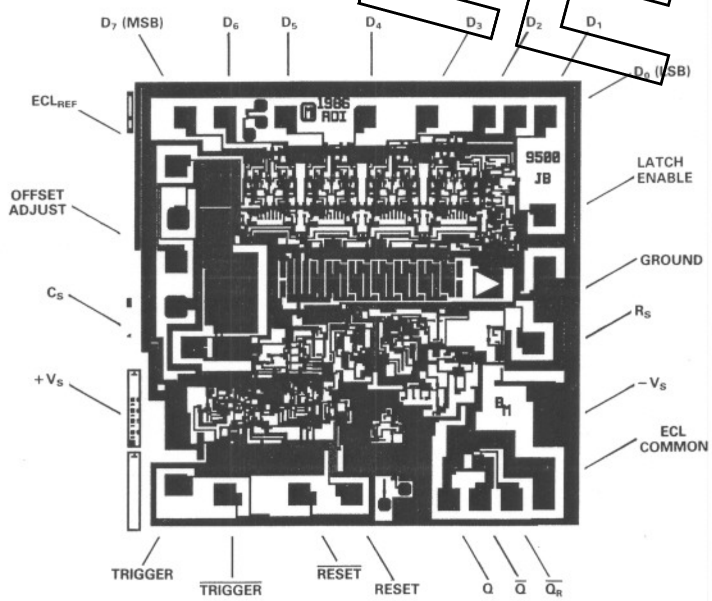


t_S – DIGITAL DATA SETUP TIME
t_H – DIGITAL DATA HOLD TIME
t_{LPW} – LATCH ENABLE PULSE WIDTH
t_{DAC} – INTERNAL DAC SETTLING TIME
t_{PD} – MINIMUM PROPAGATION DELAY
t_{RD} – RESET PROPAGATION DELAY
t_D – PROGRAMMED DELAY
t_{TPW} – TRIGGER PULSE WIDTH
t_{RPW} – RESET PULSE WIDTH
t_{THO} – RESET-TO-TRIGGER HOLDOFF
t_{RHO} – TRIGGER-TO-RESET HOLDOFF

NOTE
A TRIGGERING EVENT MAY OCCUR AT ANY TIME WHILE THE INTERNAL DAC (PROGRAMMED DELAY) IS BEING CHANGED. TRIGGERING EVENTS DURING THE INTERNAL DAC SETTLING TIME MAY NOT GENERATE AN ACCURATE PULSE DELAY.

System Timing Diagram

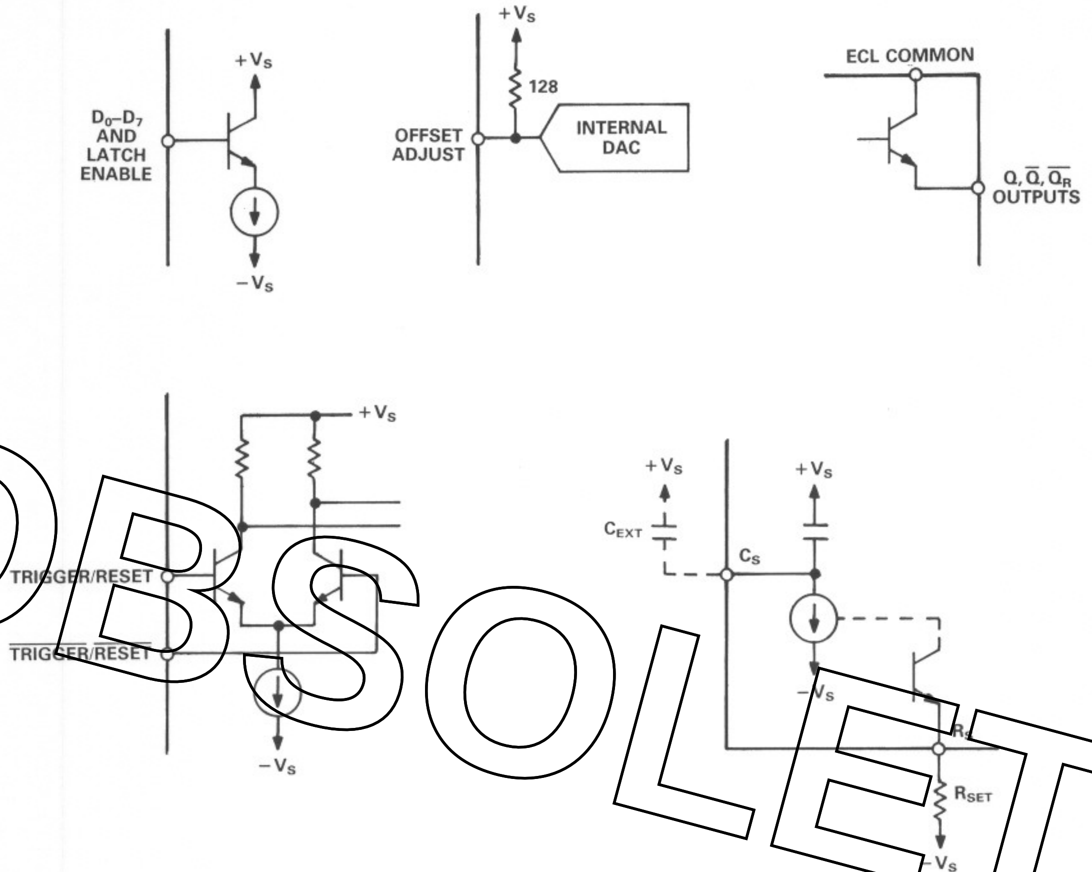
DIE LAYOUT



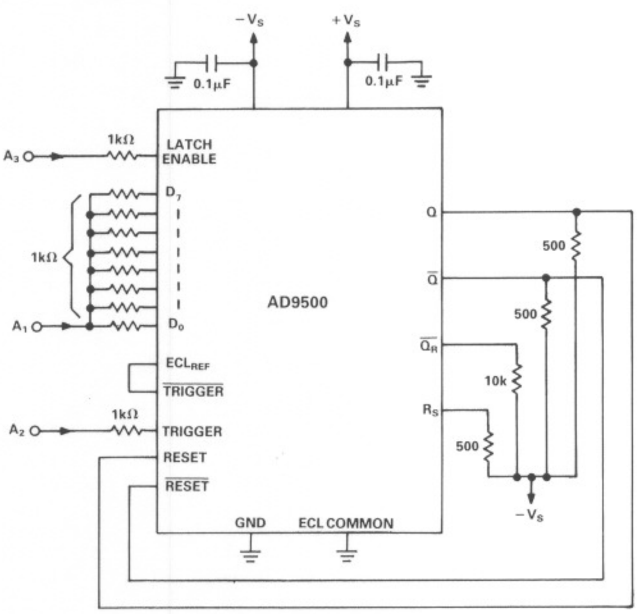
MECHANICAL INFORMATION

Die Dimensions	104 × 103 × 18 (max) mils
Pad Dimensions	4 × 4 (min)mils
Metalization	Aluminum
Backing	None
Substrate Potential	$-V_S$
Passivation	Oxynitride
Die Attach	Gold Eutectic
Bond Wire	1.25 mil, Aluminum; Ultrasonic Bonding or 1mil, Gold; Gold Ball Bonding

Input/Output Circuits



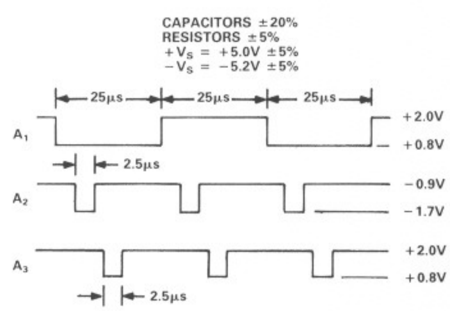
Burn-In Circuit



MIL-STD-883 COMPLIANCE INFORMATION

The AD9500 is classified within Microcircuits Group 49, Technology Group D (bipolar delay generators) and is constructed in accordance with MIL-STD-883. It is electrostatic sensitive and falls within electrostatic sensitivity classification Class 1. Percent Defective Allowance (PDA) is computed based on Subgroup 1 of the specified Group A test list. Quality Assurance (QA) screening is in accordance with Alternate Method A of Method 5005.

The following apply: Burn-In per 1015; Life Test per 1005; Electrical Testing per 5004. (Note: Group A electrical testing assumes $T_A = T_C = T_J$.) MIL-STD-883-compliant devices are marked with "C" to indicate compliance.



INSIDE THE AD9500

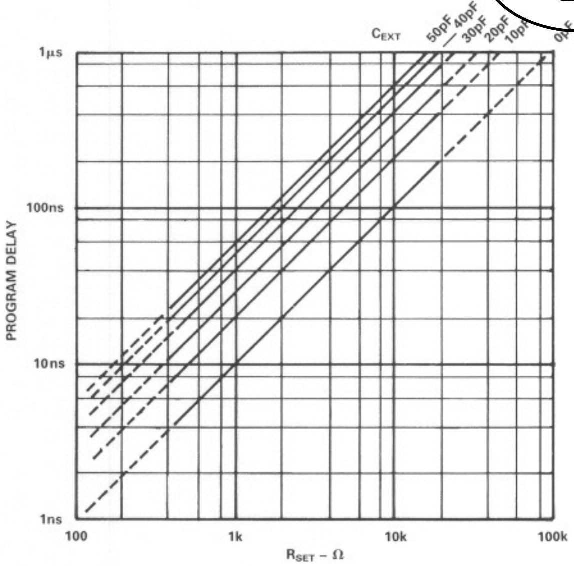
The heart of the AD9500 is the linear ramp generator. A triggering event at the input of the AD9500 initiates the ramp cycle. As the ramp voltage falls, it will eventualy go below the threshold set up by the internal DAC (digital-to-analog converter). A comparator monitors both the linear ramp voltage and the DAC threshold level. The output of the comparator serves as the output for the AD9500, and the interval from the trigger until the output switches is the total delay time of the AD9500.

The total delay through the AD9500 is made up of two components. The first is the full-scale programmed delay, $t_{D\,(max)}$, determined by R_{SET} and C_{EXT}. The second component of the total delay is the minimum propagation delay through the AD9500 (t_{PD}). The full-scale delay is variable from 2.5ns to greater than 1ms. The internal DAC is capable of generating 256 separate programmed delays within the full-scale range (this gives 10ps increments for a 2.5ns full-scale setting).

The actual programmed delay is directly related to both the digital control data (digital data to the internal DAC) and the RC time constant established by R_{SET} and C_{EXT}. The specific relationship is as follows:

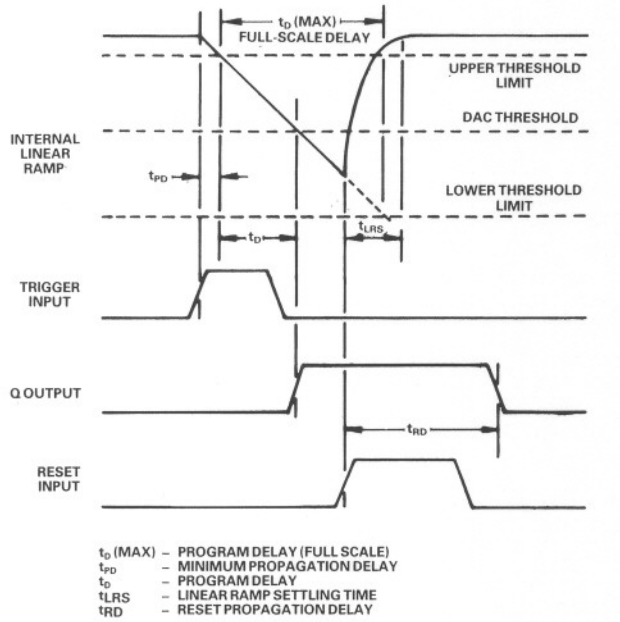
Total Delay = Minimum Propagation Delay + Programmed Delay

$$= t_{PD} + (\text{digital value}/256)\, R_{SET}\, (C_{EXT} + 10pF)$$



Typical Programmed Delay Ranges

The internal DAC determines the programmed delay by way of the threshold level at its output. The LATCH ENABLE control for the on-board latch is active (latches) logic "HIGH". In the logic "LOW" state, the latch is transparent, and the internal DAC will attempt to follow changes at the digital data inputs. Both the LATCH ENABLE control and the data inputs are TTL compatible. The internal DAC may be updated at any time, but full timing accuracy may not be attained unless triggering events are held off until after the DAC settling time (t_{DAC}).



Internal Timing Diagram

On resetting, the ramp voltage held in the timing capacitor (C_{EXT} + 10pF) is discharged. The AD9500 discharges the bulk of the ramp voltage very quickly, but to maintain *absolute* accuracy, subsequent triggering events should be held off until after the linear ramp settling time (t_{LRS}). Applications which employ high frequency triggering at a constant rate will not be affected by the slight settling errors since they will be constant for fixed reset-to-trigger cycles.

The RESET and TRIGGER inputs of the AD9500 are differential and must be driven relative to one another. Accordingly, the TRIGGER and RESET inputs are ideally suited for analog or complementary input signals. Single-ended ECL input signals can be accommodated by using the ECL midpoint reference (ECL_{REF}) to drive one side of the differential inputs.

The output of the AD9500 consists of both Q and $\overline{Q}$ driver stages, as well as the $\overline{Q_R}$ output which is used primarily for extending the output pulse width. In the most direct reset configuration, either the Q or the $\overline{Q}$ output is tied to the respective RESET input. This generates a delayed output pulse with a duration equal to the reset delay time (t_{RD}) of approximately 6ns. Note that the reset delay time (t_{RD}) becomes extended for very small programmed delay settings. The duration of the output pulse can be extended by driving the reset inputs with the $\overline{Q_R}$ output through an RC network (see "Extended Output Pulse Width" application). Using the $\overline{Q_R}$ output to drive the reset circuit avoids loading the Q or $\overline{Q}$ outputs.

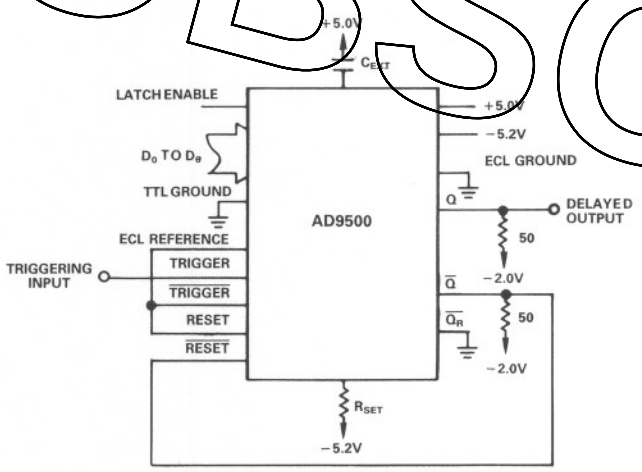
Values in the specification table are based on 5ns FSR test conditions. Nearly all dynamic specifications degrade for longer full-scales. For details of performance change, request the application note "Using Digitally Programmable Delay Generators."

APPLICATIONS

The AD9500 is a very versatile device, but at the same time, it is not difficult to use. Essentially there are only a few basic configurations which can be extended into a number of applications. The TRIGGER and RESET inputs of the AD9500 can be treated as single ended, or as differential, which allows the AD9500 to operate with a wide range of signal sources. The output pulse from the AD9500 can be reset in one of two ways, either immediately by driving the RESET inputs with the output itself, or in a delayed mode.

MINIMUM CONFIGURATION

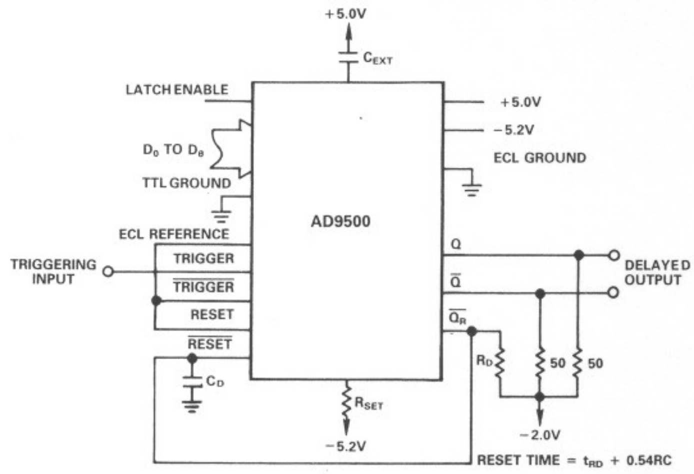
The minimum configuration uses only one of the TRIGGER inputs. The other is connected to the ECL reference midpoint, ECL_{REF}. This allows the AD9500 to be triggered with standard 10K or 10KH ECL signals. Once a triggering event occurs, the Q output will go into the logic HIGH state, and the $\overline{Q}$ output will go into the logic LOW state after the programmed delay. The Q output is then used to drive the RESET input, causing the AD9500 to reset itself. The result is a delayed output pulse which is only as wide as the reset propagation delay (t_{RD}).



Single Input – Minimum Timing Configuration

EXTENDED OUTPUT PULSE WIDTHS

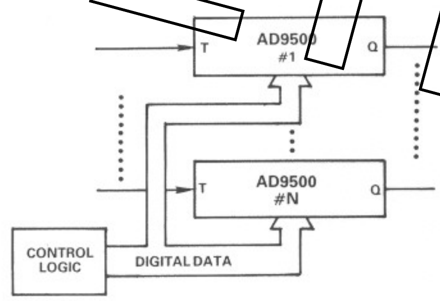
The extended pulse configuration is similar to the minimum configuration. The difference here is that the output pulse width has been extended. Operation is identical in terms of triggering the AD9500; the functional difference is in the resetting circuit. In this case the $\overline{Q_R}$ output is used to drive the $\overline{RESET}$ input through a resistor/capacitor charging network. The charging network will cause the signal at the $\overline{RESET}$ input to fall more slowly, which will extend the output pulse width. An added benefit of the extended pulse width configurations is that both the Q and the $\overline{Q}$ outputs are completely free for other uses. $\overline{Q}$ has limited current drive; the minimum resistance for R_D should be 4kΩ.



Extended Output Pulse Width Configuration

MULTICHANNEL DESKEWING

Perhaps the most appropriate use of the AD9500 is in multiple delay matching applications. Slight differences in impedance and cable length can create large timing skews within a high-speed system. Much of this skew can be eliminated by running each signal through an AD9500. With one line used as a standard, the programmed delays of the other AD9500s are adjusted to eliminate the timing skews. With the very fine timing adjustments possible from the AD9500 (as small as 10ps), nearly any high-speed system should be able to automatically adjust itself to extremely tight tolerances.

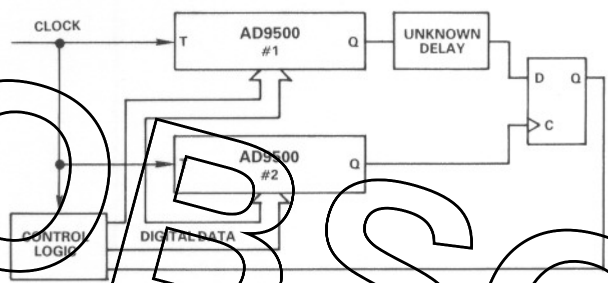


Multiple Delay Matching

MEASURING UNKNOWN DELAYS

Two AD9500s can be combined to measure delays with a high degree of precision. One AD9500 is set with little or no programmed delay, and its output is used to drive the unknown delay circuit, which in turn drives the input of a "D" type flipflop. The second AD9500 is triggered along with the first, and its output provides a clocking signal for the flipflop. The programmed delay of the second AD9500 is then varied to detect the output edge from the unknown delay circuit.

Detecting the output edge is relatively straightforward. If the programmed delay through the second AD9500 is too long, the flipflop output will be at logic HIGH. If, on the other hand, the programmed delay through the second AD9500 is too short, the flipflop output will be at logic LOW. When the programmed delay is properly adjusted, the flipflop will likely bounce between logic HIGH and logic LOW. The digital code value used to create the second programmed delay is a direct indication of the delay through the unknown circuit. The most accurate results can only be attained by calibrating the system without the unknown delay circuit in place.

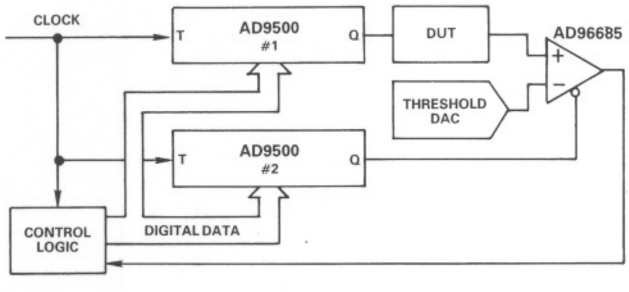


Measuring Unknown Delays

MEASURING HIGH-SPEED AC WAVEFORMS

The same circuitry used to measure unknown delays can be extended to measure the time response of high-speed ac waveforms. With the addition of a digital-to-analog converter and an analog comparator, the circuit functions very much like the previous application. The DAC sets a threshold level which drives one of the differential comparator inputs. The other comparator input is driven by the device under test (DUT). The output of the first AD9500 causes the DUT to produce an output. The second AD9500, which is also triggered along with the first AD9500, strobes the comparator latch enable.

If the DUT output is greater than the DAC threshold when the comparator is latched, the comparator output will be at logic HIGH. If the output is below the DAC threshold, the comparator will be at logic LOW. The programmed delay setting of the second AD9500 is adjusted to the point where the DUT output equals the DAC threshold. By varying the DAC threshold level and adjusting the second AD9500 programmed delay, a point by point reconstruction of the ac waveform can be created.

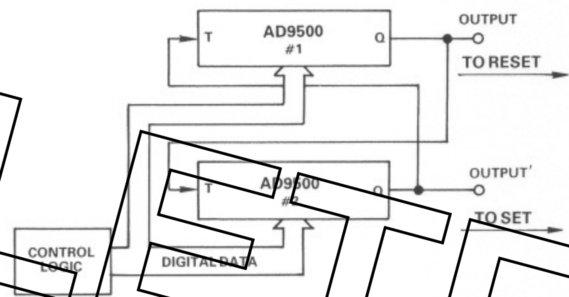


Measuring AC Waveforms

PROGRAMMABLE OSCILLATOR

Another interesting use of the AD9500 is in a digitally programmable oscillator. The highly accurate delays generated by the AD9500 can be exploited to create a ring oscillator with variable duty cycle. The delayed output of the first AD9500 is used to drive the TRIGGER input of the second AD9500. The output of the second AD9500, in turn, is used to drive the TRIGGER input of the first AD9500. Together the two devices will alternately trigger each other creating two pulse chains on the outputs.

The total delay through both AD9500s combined, determines the period of the oscillation frequency. The duty cycle can be controlled by using the outputs to drive the SET and RESET inputs of a flipflop. The total delay through the first AD9500 will control the flipflop logic LOW output pulse width, and the second AD9500 will control the flipflop logic HIGH output pulse width.



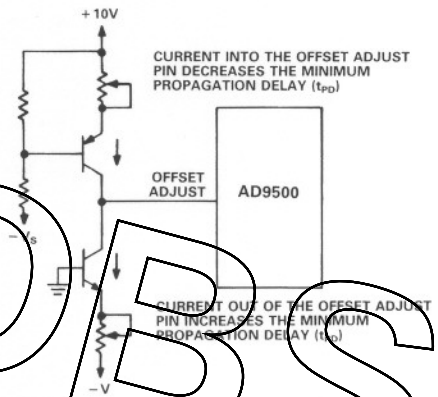
Ring Oscillator

LAYOUT CONSIDERATIONS

The AD9500 is a precision timing device, and as such high-frequency design techniques must be employed to achieve the best performance. The use of a low impedance ground plane is particularly important. Ideally the ground plane should be on the component side of the layout and extend under the AD9500, to shield it from system timing signals. Sockets pose a special problem for a circuit like the AD9500 because of the additional inter-lead capacitance they create. If sockets must be used, pin sockets are generally preferred. Power supply decoupling is also critical to a high-speed design; a 0.1µF ceramic capacitor and a 0.01µF mica capacitor for both power supplies should be very effective. DAC threshold stability can be improved by decoupling the OFFSET ADJUST pin to +5.0V (note that this will lengthen the DAC settling time, t_{DAC}).

DELAY OFFSET ADJUSTMENTS

As the full-scale delay is increased, a component of the minimum propagation delay also increases. This is caused by the additional time required by the ramp (now with a much "flatter" slope) to fall below the DAC threshold corresponding to the minimum propagation delay (t_{PD}). One means of decreasing the minimum propagation delay (when the full-scale delay, set by R_{SET} and C_{EXT} is large) is to offset the internal DAC threshold toward the initial ramp levels, thus reducing the time for the internal ramp to cross the threshold once the AD9500 is triggered.



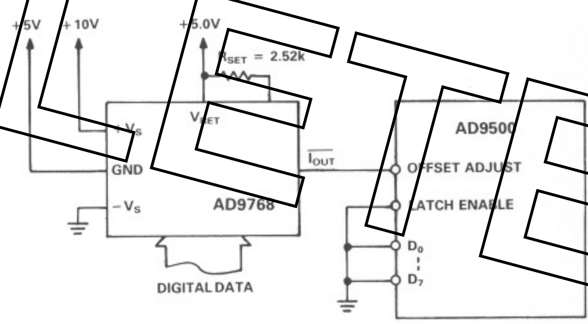
The Offset Adjust Pin Can Be Used to Match Several AD9500s

The DAC levels are offset toward the initial ramp level by injecting a small current into the offset adjust pin. Note, however, that the ramp start-up region is less linear than the later portions of the ramp, which is the primary reason for the built-in offset. If the minimum propagation delay is kept above 5ns (the linear portion of the ramp), no significant degradation in linearity should result. This concept can be extended to match the actual propagation delays of several AD9500s, by injecting or sinking a small current (<2mA) into or out of each of the OFFSET ADJUST pins.

GENERAL PERFORMANCE ENCHANCEMENTS

High-speed operation is generally more consistent if C_{EXT} is kept small (i.e., no external capacitor) to maintain small discharge time constants. Integral linearity, however, benefits from larger values of C_{EXT} by buffering small system spikes and surges. Another means of improving integral linearity is to draw a small current ($\approx$200μA) out of the OFFSET ADJUST pin with a 47kΩ pull-down resistor. This has the effect of moving the internal DAC reference levels into a relatively more linear region of the ramp. This technique is generally only useful for small full-scale delay configurations. Its use with larger full-scale delays will extend the minimum propagation delay (t_{PD}). A pull-up resistor to +5.0V creates the opposite effect by reducing the minimum propagation delay (t_{PD}) at the expense of increased reset propagation delay (t_{RD}) and degraded linearity (see OFFSET matching circuit).

An external DAC can be used with the AD9500 for increased resolution and higher update rates. For the most part, a standard ECL DAC, operating between +5.0V and ground, should work with the AD9500. The output of the external DAC must be connected to the OFFSET ADJUST pin of the AD9500 with the internal DAC turned off (D_0 thru D_7 at logic LOW). For normal operation, the external DAC output should range from 0mA to −2mA (sinking).



Operation with External DAC

ORDERING INFORMATION

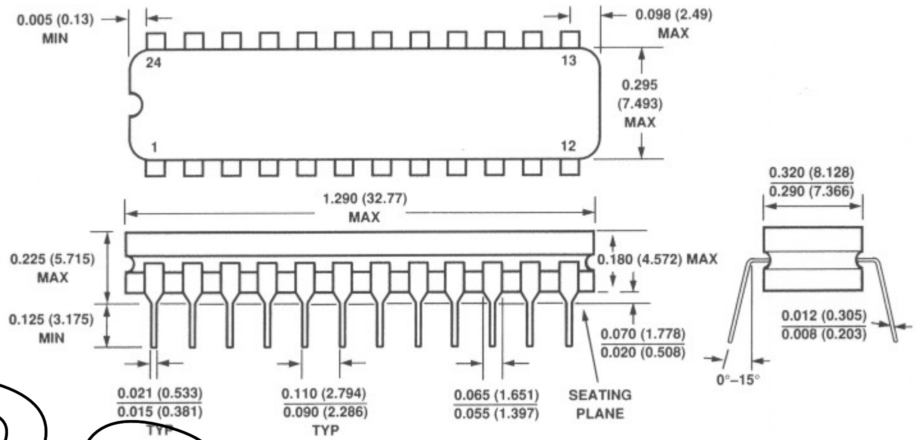
Device	Temperature Range	Description	Package Options*
AD9500BP	−25°C to +85°C	28-Pin PLCC (Plastic), Industrial Temperature	P-28A
AD9500BQ	−25°C to +85°C	24-Pin "Skinny" DIP, Industrial Temperature	Q-28
AD9500TE/883B	−55°C to +125°C	28-Pin LCC, Extended Temperature	E-28A
AD9500TQ/883B	−55°C to +125°C	24-Pin "Skinny" DIP, Extended Temperature	Q-28

*E = Leadless Ceramic Chip Carrier; P = Plastic Leaded Chip Carrier; Q = Cerdip.

OUTLINE DIMENSIONS

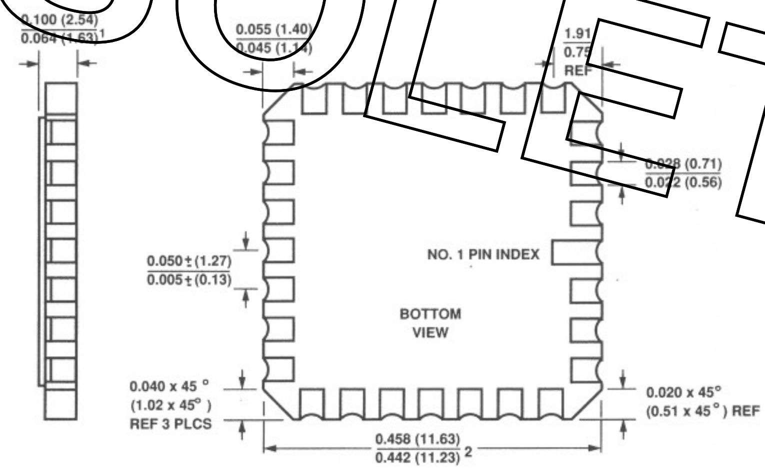
Dimensions shown in inches and (mm).

24-Pin Ceramic "Skinny" DIP



NOTE
CERDIP LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-385 10 REQUIREMENTS.

28-Pin LCC



NOTES
1. THIS DIMENSION CONTROLS THE OVERALL PACKAGE THICKNESS.
2. APPLIES TO ALL FOUR SIDES.
3. ALL TERMINALS ARE GOLD PLATED.

28-Pin PLCC