ANALOG DEVICES

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APPLICATION NOTE

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Programmable-Delay ICs Control System Timing

by Craven Hilton and Jeff Barrow

Low cost, low power, and small package size extend the application of digital-to-time converters in system timing applications. By exploiting the programmability features of these devices, you can both simplify timing-system design and gain greater control of timing parameters than you can by using analog time-delaying methods.

Accurate control of pulse timing is extremely important in digital electronic systems in those applications where system requirements dictate digital control of delays. Until now, you've had to use an analog method, employing a high-speed comparator to detect the incremental delays on a linear ramp, and a D/A converter to set the threshold level of the comparator. This design uses as much as one watt of power; now, however, monolithic digital-to-time converters (DTCs), such as the AD9500, accomplish the same function while only dissipating 300 mW. You can use the AD9500 to control time delays having intervals as small as 10 psec in a full-scale span of 2.5 nsec min.

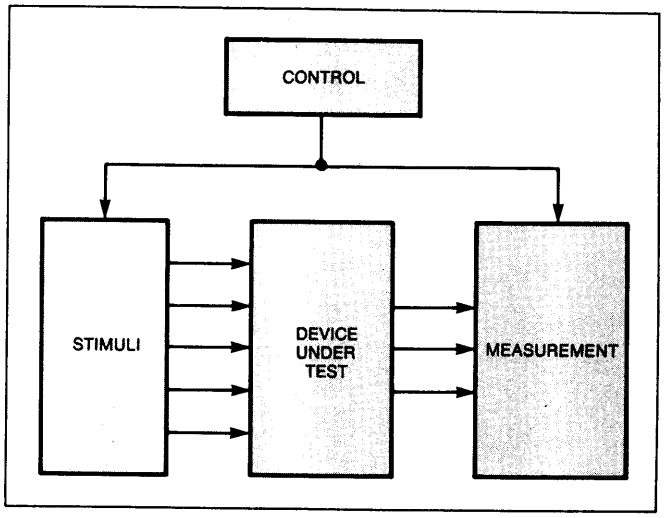

Fig 1—This test configuration, typical of virtually all electronic measurement systems, *comprises four blocks: stimuli, control, measurement, and the device under test.*

Some circuit examples illustrate the benefits of using a monolithic DTC in such applications as LSI and VLSI automatic test systems, which present significant challenges in pulse generation and distribution. For instance, although you can achieve repeatable delays of less than 100 psec by using an analog technique with an RC time reference, this method will not provide you with *variable* delays having such short intervals. The key to the flexibility of the monolithic DTC is the device's programmability.

Fig 1 is a generic block diagram of virtually all

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electronic measuring systems. Such a system can evaluate any device (the device under test, or DUT) for virtually any performance criteria if you apply the proper stimuli and use the appropriate measurement circuits. This electronic measuring system will serve as a model for the timing circuits throughout the remainder of the text.

One way to exploit the programmability of the DTC is to use two DTCs triggered from the same clock to program both the leading and trailing edges of an output pulse. This application is illustrated in **Fig 2a.** The first DTC (IC_1), which produces the leading edge of the output pulse, drives the clock input of IC_3, a D-type flip-flop whose D input is tied to a logic one. After IC_1

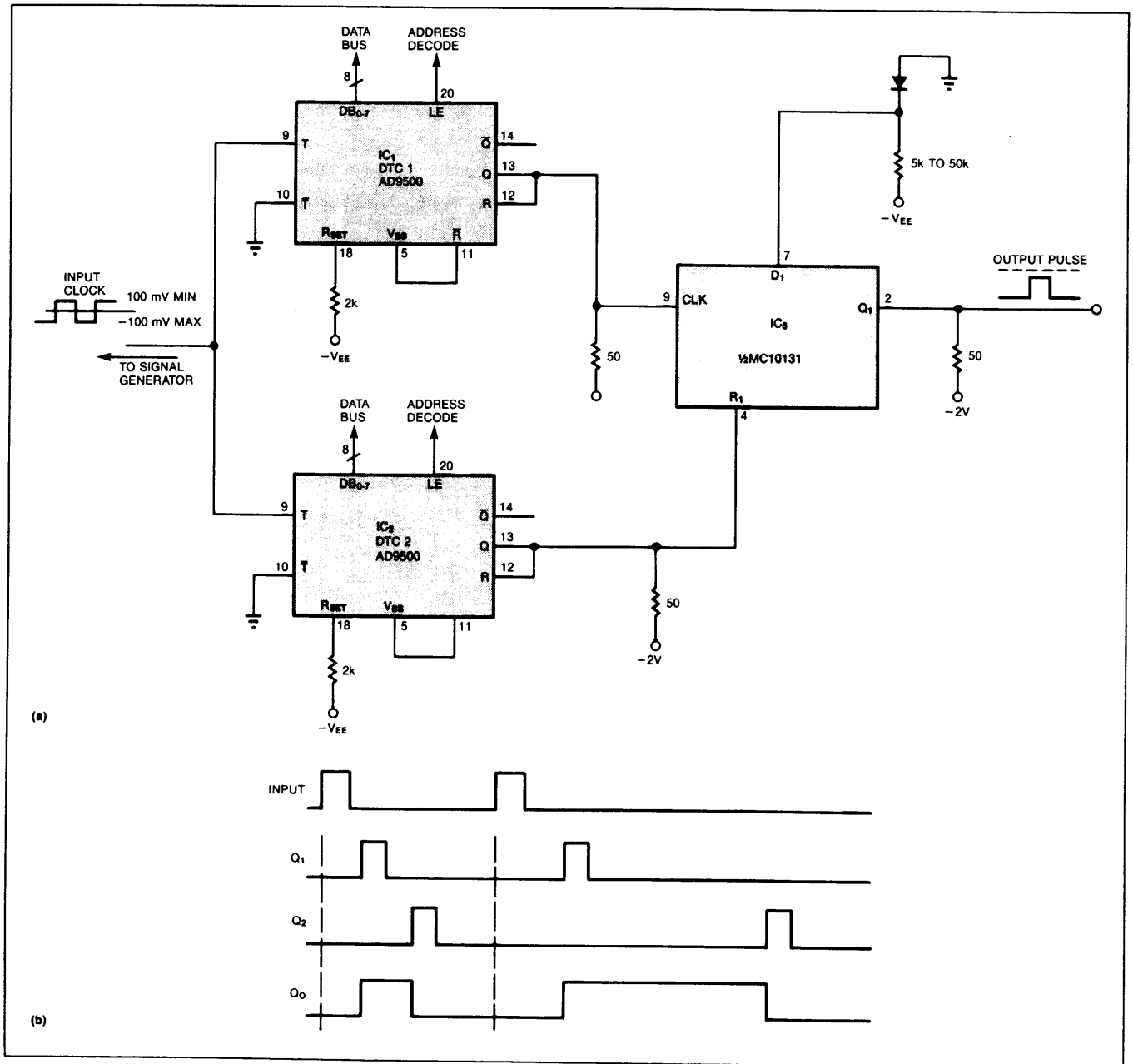

Fig 2—Two DTCs control the output's leading and trailing edges *in this digitally controlled pulse generator. The timing diagram in* ***b*** *brings out the fact that the leading edge of the output pulse, Q_o, occurs after an interval equal to the propagation delay plus the programmed delay.*

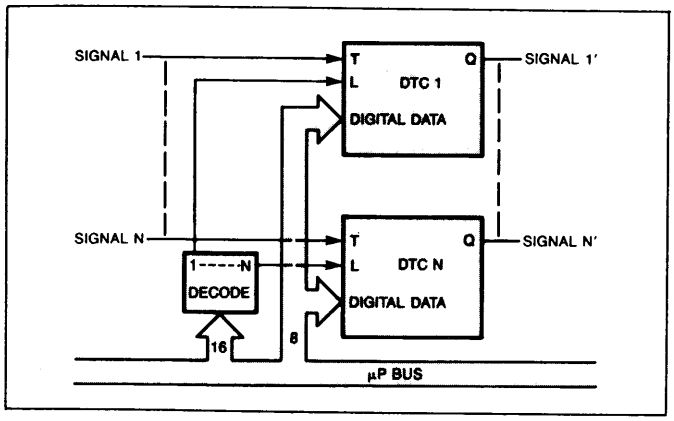

Fig 3—Providing precise delay matching in critical applications, *this circuit uses multiple DTCs to compensate for differences in the delays inherent in different signal paths. The closed-loop circuit provides a deskewing function.*

clocks the one through the flip-flop, the second DTC (IC_2) resets the flip-flop, thereby producing the falling edge.

At a time equal to the propagation delay plus the programmed delay of the first DTC (**Fig 2b**), the flip-flop produces the leading edge of the output pulse. Because the propagation delays of the two DTCs cancel each other, the width of the output pulse is exactly the difference between the programmed delays of the two DTCs. You can determine the programmed delay of each DTC from

$$t_D = t_{PD} + \frac{XX_{16}}{FF_{16}} (R_{SET}\ C_{SET}).$$

The circuit of **Fig 3** provides precise delay matching for those applications in which you need to distribute a

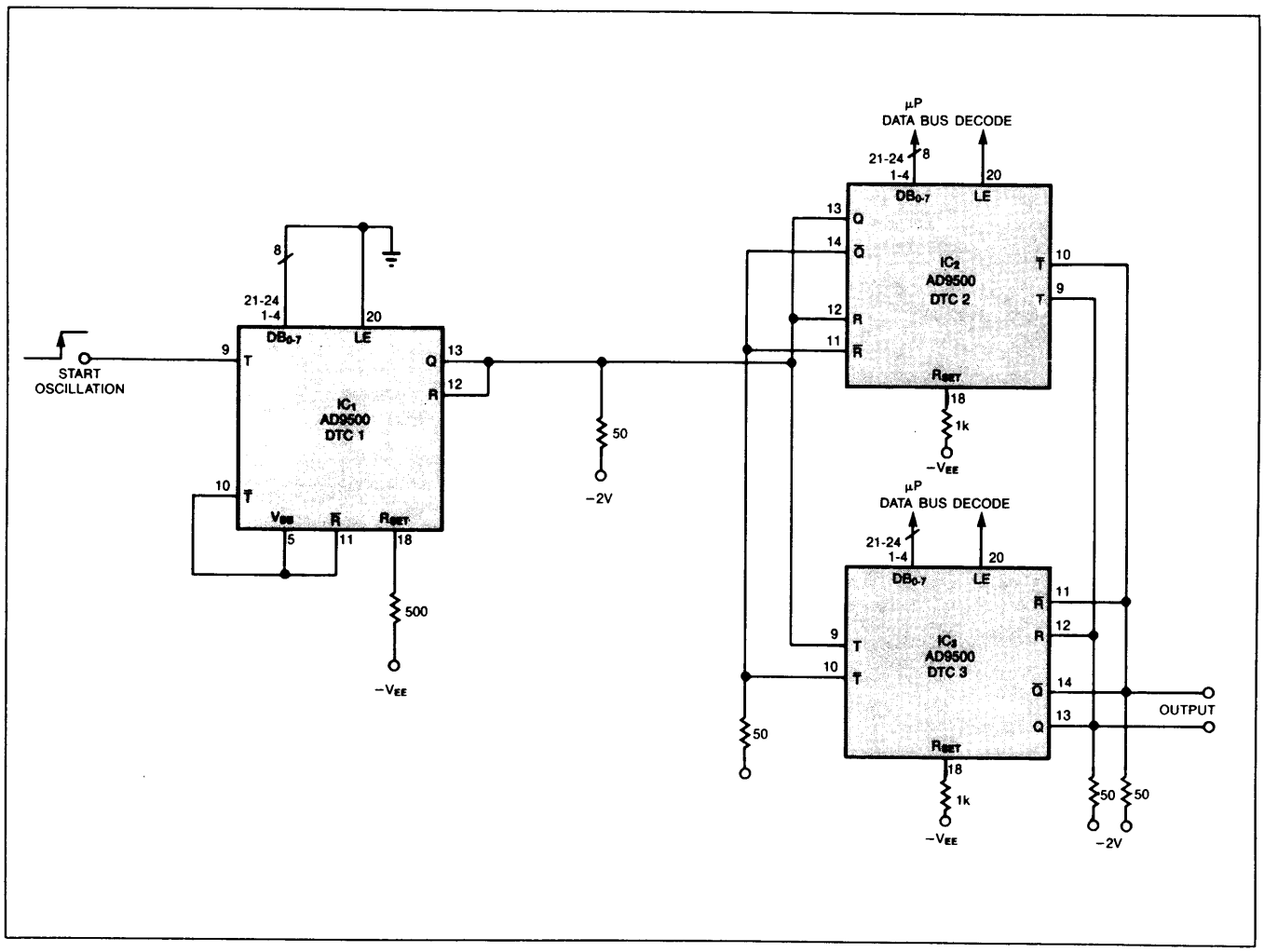

Fig 4—Using DTCs configured to start and stop the oscillation, *this digitally programmable oscillator gives you complete control over the start-up, shutdown, and frequency of oscillation.*

number of pulses and maintain good coherence between those pulses. Because individual test circuits may have extraneous delays in the signal paths to the DUTs, close matching in the initial tester delays will not be sufficient to guarantee close matching between the delivered pulses. The combination of programmable deskewing circuitry and the closed-loop calibration scheme of **Fig 3** allows you to compensate for the timing variations in the circuit paths during your test-system setup cycle.

During the setup cycle, the closed-loop system measures the delay to each input pin of the DUT. It then modifies the delay values stored in each of the DTCs until the input pulses arrive at the DUT's pins simultaneously. This method allows you to match the delays to the DUT to a resolution of 20 psec for a full-scale delay period of 5 nsec.

Programmable oscillator

Fig 4 shows that you can also create a digitally programmable oscillator by using three DTCs. IC_1 acts as a start-up pulser to trigger the other two DTCs, which are configured as astable oscillators interconnected in a wired-OR configuration. You can generate the start-oscillation pulse locally, or you can use the system power-up-reset signal to generate the start-oscillation pulse. Because the DTC is edge triggered and the oscillator is stable in either the oscillating or

DTC uses analog, digital internal circuitry

Fig A displays the AD9500 along with the external circuitry required to configure it as a DTC. An 8-bit word sets the output voltage of the IC's internal D/A converter. The DAC's output voltage in turn establishes a threshold for the high-speed voltage comparator. You can latch the input word to the AD9500 by applying a one to the latch-enable input of the device. Alternatively, if you want to change the value of the input on the fly, hold the latch-enable input at logic zero and the latches will remain transparent.

Because the DTC controls precision delays for high-speed signals, its delay-path inputs and outputs are designed to be ECL compatible. The IC's differential-I/O structure affords maximum timing-noise immunity when you interface the chip to either 10K or 100K logic. For less demanding applications that use 10K ECL circuitry, you can use the on-chip ECL reference and operate the chip in a single-ended mode.

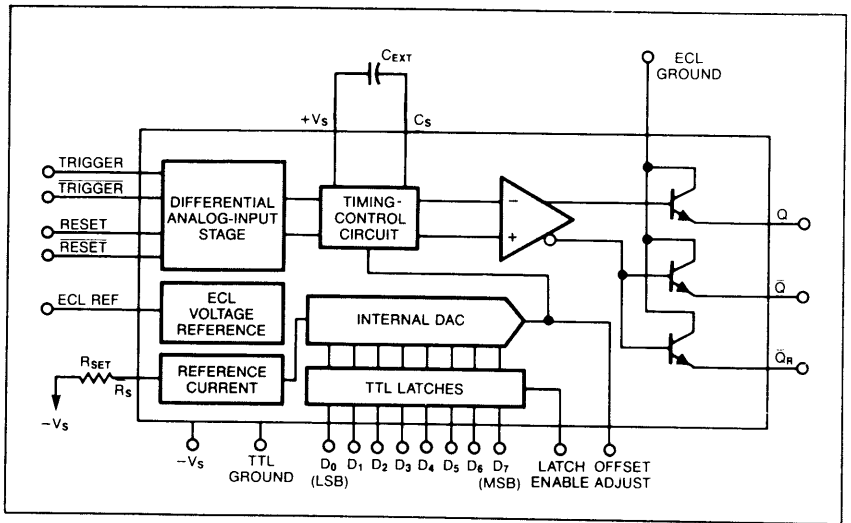

Fig A—Using both analog and digital internal circuitry, *the AD9500 requires only a resistor and a capacitor as external components in programmable-delay applications. R_{SET} and C_{SET} (C_{EXT}+C_{INT}) provide a reference for the internal timing-control circuit. The ramp generated by the R_{SET}/C_{SET} time reference remains linear despite the effects of time, temperature, and supply-voltage variations.*

The DTC's time reference is RC based; it serves as the ramp generator and as a timebase for the on-chip DAC. Because the DAC's gain is proportional to the time reference, any change in the ramp's slope is compensated by the DAC's gain. This compensation reduces the effects of environmental changes on full-scale time and timing linearity.

You determine the full-scale delay of the device through your selection of external, passive components. Although the recommended range of full-scale delays is from 2.5 nsec to 100 μsec, you can extend delays beyond 100 μsec if you can tolerate a degradation of the linearity and

nonoscillating mode, a single pulse from IC_1 will start the oscillation. By grounding the trigger input on either IC_2 or IC_3, you can stop the oscillation.

As **Fig 4** shows, each DTC resets itself as it triggers the alternate DTC. The programmed delay of each device is determined by the equation given earlier. This delay, in turn, determines the output frequency of the oscillator, which is simply the reciprocal of the sum of the two propagation delays plus the two programmed delays.

When you need to measure a time delay, you can use two DTCs in conjunction with two comparators, a D-type flip-flop, and a successive-approximation register (SAR) as illustrated in **Fig 5a.** Flip-flop IC_3 serves as a coincidence detector. The first DTC (IC_1) varies the delay of the pulse applied to the D input of the flip-flop. The coincidence detector serves as a time comparator, whose function is analogous to that of a voltage comparator in a successive-approximation A/D converter.

The clock input to the flip-flop is delayed by a period equal to the unknown ECL delay. The circuit compares the first cycle of the 1-MHz clock with the unknown delay and checks to see if the delay is greater than half-scale. Then it checks for one-quarter or three-quarters scale, one-eighth or seven-eighths scale, and so on. At the end of the test process, then, the output of the SAR provides an 8-bit representation of the delay through the DUT. To measure TTL-circuit delays, you

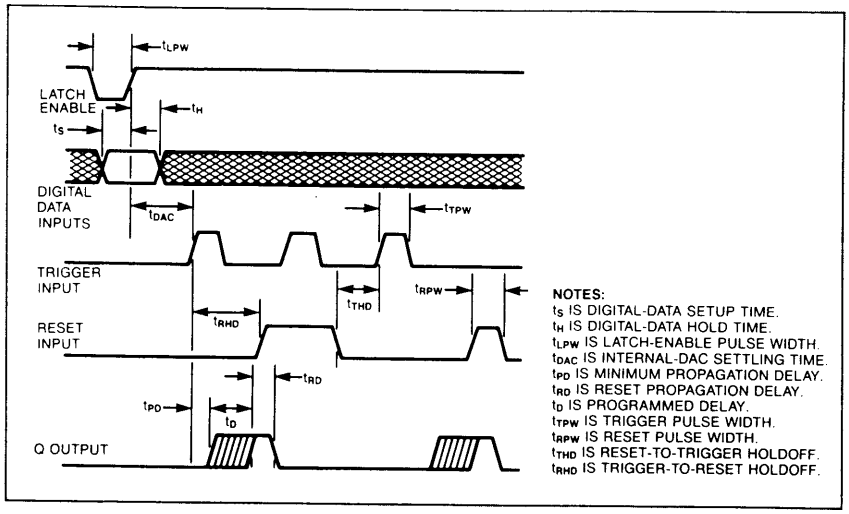

***Fig B—Timing characteristics for the digital-to-time converter** are shown in this timing diagram. The illustration shows the relationship between the digital delay-coefficient data and the latch-enable strobe. The text delineates the limits you should observe for the various inputs, in order to obtain proper operation of the DTC.*

Fig B. Lines 1 and 2 show the timing relationship between digital-delay coefficient data and the latch-enable strobe. The minimum latch-enable pulse width is 2 nsec. The data setup time for the input latch is a maximum of 2.5 nsec, and the hold time is a minimum of 4.5 nsec. You must allow at least 25 nsec from the rising edge of the latch-enable pulse before you trigger an event, otherwise the internal DAC might not have time to settle.

Lines 3, 4, and 5 of **Fig B** show the relationship of the output to the reset and trigger events. The total delay through the DTC is the sum of the propagation delay and the programmed delay. The propagation delay equals the delay through the differential input stage, the comparator, and the delay attributable to ignoring the first, nonlinear portion of the ramp. The last of these components increases with full-scale delay.

repeatability of the delay. At the other end of the spectrum, if you choose a full-scale range of 2.5 nsec, then the smallest incremental delay available to you is 10 psec.

The maximum delay trigger rate is 100 MHz, but an offset adjustment in the device allows you to operate two DTCs in a ping-pong fashion to double the trigger rate. The IC's maximum differential nonlinearity is ±½ LSB at 25°C and ±1 LSB over the operating-temperature range. Maximum integral nonlinearity for the device is ±1.25 LSB for full-scale delays of 100 nsec or more over the operating-temperature range.

The timing characteristics of the AD9500 are illustrated in

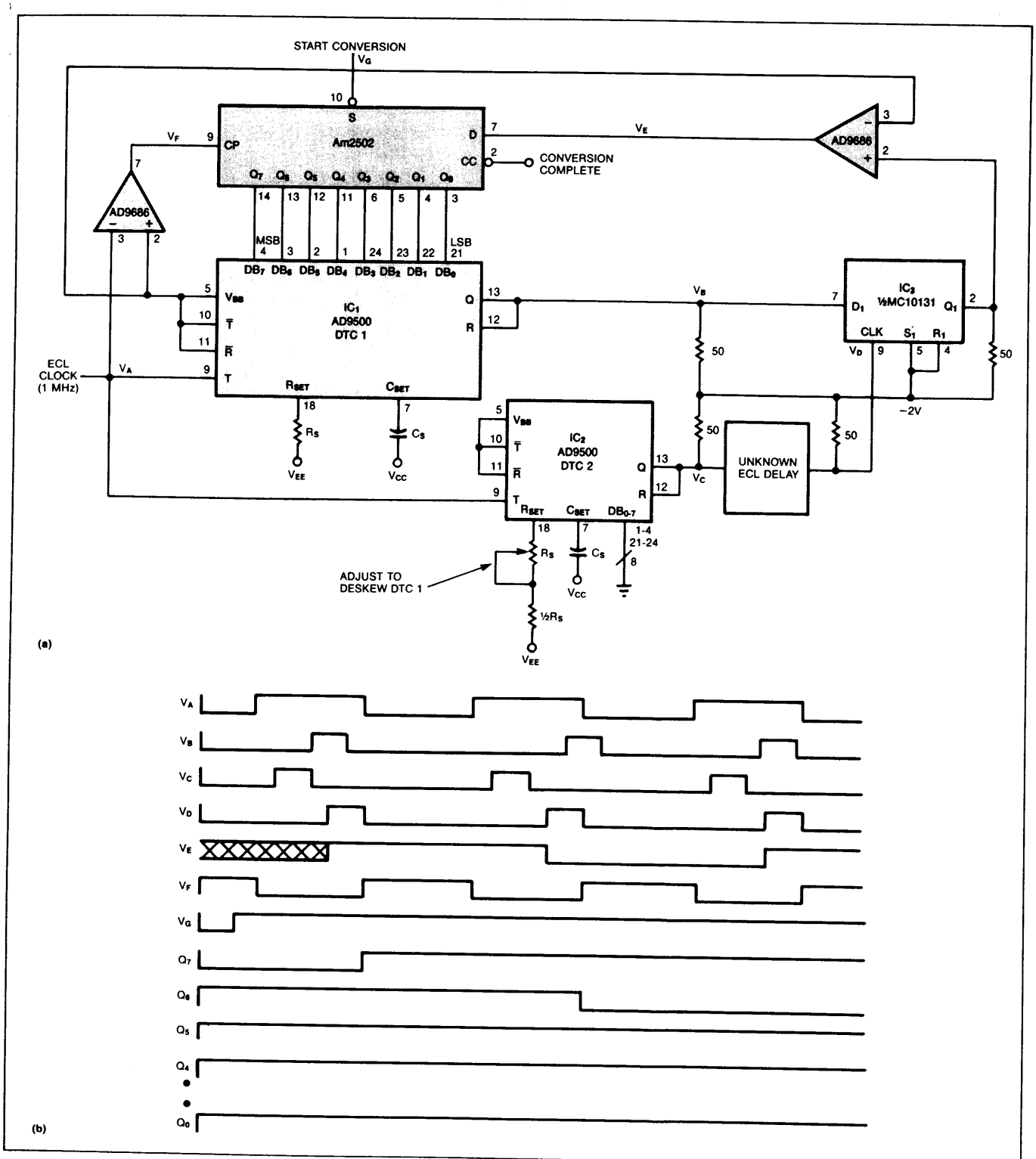

Fig 5—Operating in similar fashion to a successive-approximation A/D converter, *this circuit allows you to make precise delay measurements. The circuit in* ***a*** *handles ultrafast ECL circuitry; you can easily modify it to accommodate TTL circuits. The timing diagram in* ***b*** *illustrates the timing characteristics at various points in the circuit.*

add an AD9686 comparator between the Q output of the second DTC (IC_2) and the input to the unknown-delay circuit, and an AD96685 comparator between the output of the unknown-delay circuit and the flip-flop.

To calibrate the circuit of **Fig 5b,** you insert a shorting strap in place of the unknown-delay circuit to eliminate extraneous circuit delays and the flip-flop's setup time. To null the circuit, apply a digital code of 00_{16} to IC_2 and adjust potentiometer R_S. This adjustment varies the propagation delay through IC_2. The calibration is complete when the output of the SAR is also 00_{16}. You must apply start-conversion pulses during the calibration. This calibration procedure is equally valid for the modified, TTL-delay configuration. **Fig 5b** shows the timing for a typical conversion cycle.

You can use the circuit of **Fig 6a** to measure the settling time of analog signals—for example, the output of a D/A converter. The operation of this circuit is similar to the operation of the digital delay detector, but it uses a voltage-input window comparator in place

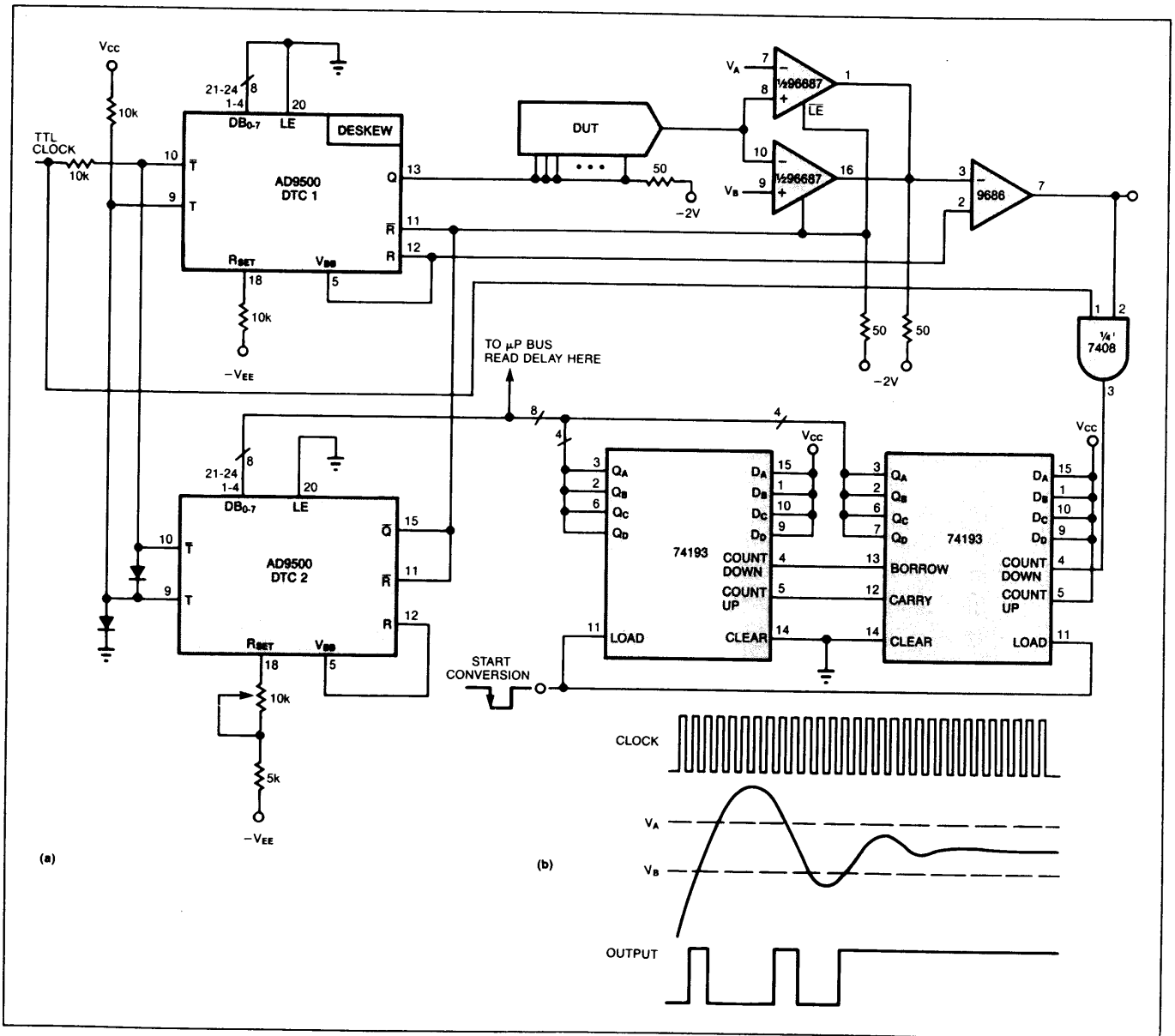

Fig 6—You can measure the settling time of analog signals *by using the circuit in* ***a****. The operation of this circuit is similar to that of the digital delay detector in* ***Fig 5a****. A typical analog voltage-settling waveform is illustrated in* ***b****.*

of the coincidence detector, and down counters in place of the SAR.

Fig 6b shows a typical analog voltage-settling waveform, as well as the output of a window comparator that uses a constant high-frequency strobe. This continuous-clock method produces ambiguous results because the signal comes into the error-band window during three clock periods. The circuit of **Fig 6a,** however, produces a single strobe per cycle of the analog signal and homes in on the correct measurement in the following manner.

The first DTC (IC_1) controls the timing of the DUT switching. The second DTC (IC_2) delays the latch-enable strobe to the high-speed window comparators. The start-conversion pulse initiates the down counters to a full-scale setting. On each cycle of the clock, the counter decrements and the strobe to the window comparator moves back closer to the time when the DUT is switched. Because the circuit starts at full-scale time, the first strobe occurs well after the DUT has settled. As successive clocks arrive, the circuit causes the strobe to back up until the DUT signal falls out of the range of the window comparator. As a result, the window comparator stops the down counter, whose output represents the settling time of the DUT.

To compensate for extraneous circuit delays, you can adjust the R_{SET} potentiometer. Insert a shorting strap in place of the DUT and change the window reference voltages V_A and V_B to $-1.28V$ and $-1.32V$, respectively. Then adjust R_{SET} until you receive a zero output from the down counters. When you reset the voltages for the window around the DUT's output and the conversion takes place, the output of the down counter will represent the propagation delay plus the settling time of the DUT.