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Register Map Reference Manual for the AD9546

INTRODUCTION

This reference manual is supplemental to the AD9546 data sheet and contains the complete register map of the AD9546 with detailed bit descriptions. This reference manual has two main sections. The Register Address Map section includes Table 2, which provides a general overview of the entire register map and shows register address groups relating to the various functional features of the AD9546. The Register Bit Details section contains details associated with an individual register or a group of registers having consecutive addresses (see Table 3 to Table 111).

Table 3 to Table 111 in the Register Bit Details section include a reset column. The reset column shows the default value of a register bit (or group of bits). The value appears as hexadecimal notation with a 0x prefix or decimal notation (decimal notation only applies for a single bit or for a group of up to three bits). The last three columns in Table 3 to Table 111 (R/W, IO Update, and Autoclear) indicate the following access attributes of a bit or group of bits:

- Read/write capability
- Input/output (IO) update dependence
- Autoclear functionality

Table 1 lists these bit access attributes. For the IO update attribute, f_S is the frequency at the output of the VCO of the system clock PLL (~2.33 GHz), and the significance of serial port clock vs. core clock is how the device transfers data to the affected register. Registers or bits with access designated as serial port clock update via the serial port clock (SCLK or SCL) in conjunction with the assertion of an IO update. Thus, the register and bit contents update virtually coincident with the serial clock edge that makes Register 0x000F, Bit 0 = 1. Registers and bits with access designated as core clock update via the core clock (f_S/96). As such, unless the system PLL is locked, these registers/bits do not update. Thus, for an IO update asserted while the system clock PLL is unlocked, data read from (or written to) registers or bits with IO update = core clock access may not be valid.

Table 1. Bit Access Attributes

Attribute	Description
Read/Write	
R	Read only
W	Write only
R/W	Both read and write
IO Update	
Live	IO update not required
Serial Port Clock	IO update qualified by the serial port clock
Core Clock	IO update qualified by the core clock (f_S/96) and requires that the system clock PLL be locked
Autoclear	
No	Not autoclearing
Yes	Autoclearing

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REVISION HISTORY

5/2021—Revision 0: Initial Version

CLOCK OUTPUT NOMENCLATURE

This reference manual makes use of specific nomenclature regarding the clock outputs of the AD9546, which constitute five 2-pin pairs. Each output pin has a dedicated output driver and the drivers can receive clock signals from one or two distribution dividers, depending on the output configuration (see Figure 1). The output pin pairs can be configured as follows:

- One differential output associated with a single distribution divider (single divider, differential drivers)
- Two single-ended outputs associated with a single distribution divider (single divider, single-ended drivers)
- Two single-ended outputs associated with independent distribution dividers (dual divider, single-ended drivers)

The clock output pin names follow the naming convention of OUTxyP and OUTxyN, where

- x is 0 or 1 (corresponding to PLL Channel 0 or PLL Channel 1)
- y is the output number (0, 1, or 2 for PLL Channel 0; and 0 or 1 for PLL Channel 1)
- P denotes the positive (normal) pin of the output pin pair
- N denotes the negative (complementary) pin of the output pin pair

For the single-divider configurations, the distribution dividers follow the naming convention of Qxy, with x and y being the same as for the pin names, where x is 0 or 1 and y is the output number. The dual-divider configuration requires two distribution dividers, one for each pin. In this case, the OUTxyP pin associates with Distribution Divider Qxy, whereas the OUTxyN pin associates with Distribution Divider Qxyy. For example, given the Output 0A pin pair (OUT0A) with dual divider configuration, Pin OUT0AP associates with Distribution Divider Q0A and Pin OUT0AN associates with Distribution Divider Q0AA.

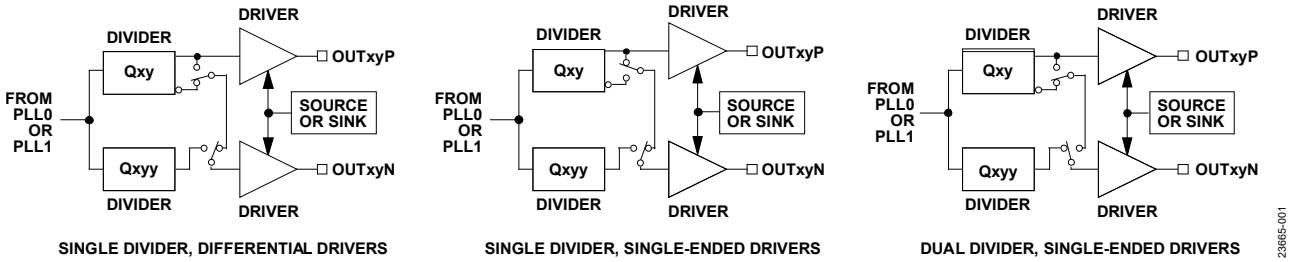

Figure 1. Clock Output Configurations

REGISTER ADDRESS MAP

Table 2. Register Map

Register Address	Register Description
Configuration and Setup	See Table 3
Register 0x0000 to Register 0x0001	Serial port configuration
Register 0x0002 to Register 0x0002	Not applicable
Register 0x0003 to Register 0x0006	Device ID
Register 0x0007 to Register 0x000A	Not applicable
Register 0x000B to Register 0x000B	SPI version
Register 0x000C to Register 0x000D	Vendor ID
Register 0x000E to Register 0x000E	Not applicable
Register 0x000F to Register 0x000F	Address looping and IO update
Register 0x0010 to Register 0x0010	Address loop length
Register 0x0020 to Register 0x0023	Scratch pad
Register 0x0024 to Register 0x00FF	Not applicable
Mx Pin	
Register 0x0100 to Register 0x0101	Mx pin mode (see Table 4)
Register 0x0102 to Register 0x0108	Mx pin status or control select (see Table 5)
Register 0x0109	Serial port and Mx pin output drive current (see Table 6)
Watchdog Timer	
Register 0x010A to Register 0x010B	Watchdog timer (see Table 7)
IRQ Enable	
Register 0x010C to Register 0x011F	IRQ enable (see Table 8)
Register 0x0120 to Register 0x0181	Not applicable
M0 to CSB/M6 Pin Function	
Register 0x0182	M0 pin function (see Table 9)
Register 0x0183	M1 pin function (see Table 10)
Register 0x0184	M2 pin function (see Table 10)
Register 0x0185	M3 pin function (see Table 10)
Register 0x0186	M4 pin function (see Table 10)
Register 0x0187	SDO/M5 pin function (see Table 10)
Register 0x0188	CSB/M6 pin function (see Table 10)
Register 0x0189 to Register 0x01FF	Not applicable
System Clock PLL	
Register 0x0200 to Register 0x0209	System clock PLL (see Table 11)
Register 0x0210 to Register 0x027F	Not applicable
System Clock Compensation	
Register 0x0280 to Register 0x029C	System clock compensation (see Table 12)
Register 0x029D to Register 0x02FF	Not applicable
Reference Input Configuration and Parameters	
Register 0x0300 to Register 0x030F	Reference input configuration (see Table 13)
Register 0x0310 to Register 0x03FF	Not applicable
Register 0x0400 to Register 0x0414	Reference input parameters: REFA (see Table 14)
Register 0x0415 to Register 0x041F	Not applicable
Register 0x0420 to Register 0x0434	Reference input parameters: REFAA (see Table 15)
Register 0x0435 to Register 0x043F	Not applicable
Register 0x0440 to Register 0x0454	Reference input parameters: REFB (see Table 16)
Register 0x0455 to Register 0x045F	Not applicable
Register 0x0460 to Register 0x0474	Reference input parameters: REFBB (see Table 17)
Register 0x0475 to Register 0x047F	Not applicable
Register 0x0480 to Register 0x0494	Reference input parameters: Auxiliary REF0 (see Table 18)
Register 0x0495 to Register 0x049F	Not applicable
Register 0x04A0 to Register 0x04B4	Reference input parameters: Auxiliary REF1 (see Table 19)

Register Address	Register Description
Register 0x04B5 to Register 0x04BF	Not applicable
Register 0x04C0 to Register 0x04D4	Reference input parameters: Auxiliary REF2 (see Table 20)
Register 0x04D5 to Register 0x04DF	Not applicable
Register 0x04E0 to Register 0x04F4	Reference input parameters: Auxiliary REF3 (see Table 21)
Register 0x04F5 to Register 0x07FF	Not applicable
Source Profiles	
Register 0x0800 to Register 0x0811	Source profile: REFA (see Table 22)
Register 0x0812 to Register 0x081F	Not applicable
Register 0x0820 to Register 0x0831	Source profile: REFAA (see Table 23)
Register 0x0832 to Register 0x083F	Not applicable
Register 0x0840 to Register 0x0851	Source profile: REFB (see Table 24)
Register 0x0852 to Register 0x085F	Not applicable
Register 0x0860 to Register 0x0871	Source profile: REFBB (see Table 25)
Register 0x0872 to Register 0x087F	Not applicable
Register 0x0880 to Register 0x0891	Source profile: Auxiliary NCO 0 (see Table 26)
Register 0x0892 to Register 0x089F	Not applicable
Register 0x08A0 to Register 0x08B1	Source profile: Auxiliary NCO 1 (see Table 27)
Register 0x08B2 to Register 0x08BF	Not applicable
Register 0x08C0 to Register 0x08D1	Source profile: DPLL0 (see Table 28)
Register 0x08D2 to Register 0x08DF	Not applicable
Register 0x08E0 to Register 0x08F1	Source profile: DPLL1 (see Table 29)
Register 0x08F2 to Register 0x08FF	Not applicable
Register 0x0900 to Register 0x0911	Source profile: IUTS 0 (see Table 30)
Register 0x0912 to Register 0x091F	Not applicable
Register 0x0920 to Register 0x0931	Source profile: IUTS 1 (see Table 31)
Register 0x0932 to Register 0x093F	Not applicable
Register 0x0940 to Register 0x0951	Source profile: Auxiliary REF0 (see Table 32)
Register 0x0952 to Register 0x095F	Not applicable
Register 0x0960 to Register 0x0971	Source profile: Auxiliary REF1 (see Table 33)
Register 0x0972 to Register 0x097F	Not applicable
Register 0x0980 to Register 0x0991	Source profile: Auxiliary REF2 (see Table 34)
Register 0x0992 to Register 0x099F	Not applicable
Register 0x09A0 to Register 0x09B1	Source profile: Auxiliary REF3 (see Table 35)
Register 0x09B2 to Register 0x0BBF	Not applicable
DPLL Loop Filter Coefficients	
Register 0x0C00 to Register 0x0C0B	Loop Filter 0 (LF0) Coefficient (see Table 36)
Register 0x0C0C to Register 0x0C17	Loop Filter 1 (LF1) Coefficient (see Table 37)
Register 0x0C18 to Register 0x0CFF	Not applicable
Common Clock DPLL Lock Detector Parameters	
Register 0x0D00 to Register 0x0D05	Common clock DPLL lock detector parameters (see Table 38)
Register 0x0D06 to Register 0x0D0F	Not applicable
Common Clock DPLL/Synchronizer	
Register 0x0D10 to Register 0x0D1D	Common clock DPLL/Synchronizer Source 0, primary reference, CCR0 (see Table 39)
Register 0x0D1E to Register 0x0D1F	Not applicable
Register 0x0D20 to Register 0x0D2D	Common clock DPLL/Synchronizer Source 1, secondary reference, CCR1 (see Table 40)
Register 0x0D2E to Register 0x0D2F	Not applicable
Common Clock Synchronizer (CCS) Parameters	
Register 0x0D30 to Register 0x0D3C	Common clock synchronizer parameters (see Table 41)
Register 0x0D3D to Register 0x0D3F	Not applicable

Register Address	Register Description
Digitized Clocking Status	
Register 0x0D40	Digitized clocking status (see Table 42)
User Time Stamper Control	
Register 0x0E00 to Register 0x0E04	User Time Stamper 0 (UTS 0) control (see Table 43)
Register 0x0E05 to Register 0x0E09	User Time Stamper 1 (UTS 1) control (see Table 44)
Register 0x0E0A to Register 0x0E0E	User Time Stamper 2 (UTS 2) control (see Table 45)
Register 0x0E0F to Register 0x0E13	User Time Stamper 3 (UTS 3) control (see Table 46)
Register 0x0E14 to Register 0x0E18	User Time Stamper 4 (UTS 4) control (see Table 47)
Register 0x0E19 to Register 0x0E1D	User Time Stamper 5 (UTS 5) control (see Table 48)
Register 0x0E1E to Register 0x0E22	User Time Stamper 6 (UTS 6) control (see Table 49)
Register 0x0E23 to Register 0x0E27	User Time Stamper 7 (UTS 7) control (see Table 50)
Register 0x0E28 to Register 0x0E2C	User Time Stamper 8 (UTS 8) control (see Table 51)
Register 0x0E2D to Register 0x0E3A	User time stamper FIFO (see Table 52)
Register 0x0E3B to Register 0x0EFF	Not applicable
Inverse User Time Stamper (IUTS) Parameters	
Register 0x0F00 to Register 0x0F03	Inverse User Time Stamper 0 (IUTS 0) parameters (see Table 53)
Register 0x0F04 to Register 0x0F07	Inverse user time stamper 1 (IUTS 1) parameters (see Table 54)
Register 0x0F08 to Register 0x0F15	Inverse user time stamper: IUTS control (see Table 55)
Register 0x0F16 to Register 0x0FFF	Not applicable
Digital Phase-Locked Loop 0 (DPLL0) Parameters	
Register 0x1000 to Register 0x102A	DPLL0 parameters (see Table 56)
Register 0x102B to Register 0x107F	Not applicable
Analog Phase-Locked Loop 0 (APLL0) Parameters	
Register 0x1080 to Register 0x1083	APLL0 parameters (see Table 57)
Register 0x1084 to Register 0x10BF	Not applicable
Distribution Control and Parameters	
Register 0x10C0 to Register 0x10DC	Distribution control: PLL Channel 0 (see Table 58)
Register 0x10DD to Register 0x10FF	Not applicable
Register 0x1100 to Register 0x1108	Distribution parameters: Q0A (see Table 59)
Register 0x1109 to Register 0x1111	Distribution parameters: Q0AA (see Table 60)
Register 0x1112 to Register 0x111A	Distribution parameters: Q0B (see Table 61)
Register 0x111B to Register 0x1123	Distribution parameters: Q0BB (see Table 62)
Register 0x1124 to Register 0x112C	Distribution parameters: Q0C (see Table 63)
Register 0x112D to Register 0x1135	Distribution parameters: Q0CC (see Table 64)
Register 0x1136 to Register 0x11FF	Not applicable
Translation Profile 0.0 to Translation Profile 0.5	
Register 0x1200 to Register 0x1217	Translation Profile 0.0 (see Table 65)
Register 0x1218 to Register 0x121F	Not applicable
Register 0x1220 to Register 0x1237	Translation Profile 0.1 (see Table 66)
Register 0x1238 to Register 0x123F	Not applicable
Register 0x1240 to Register 0x1257	Translation Profile 0.2 (see Table 67)
Register 0x1258 to Register 0x125F	Not applicable
Register 0x1260 to Register 0x1277	Translation Profile 0.3 (see Table 68)
Register 0x1278 to Register 0x127F	Not applicable
Register 0x1280 to Register 0x1297	Translation Profile 0.4 (see Table 69)
Register 0x1298 to Register 0x129F	Not applicable
Register 0x12A0 to Register 0x12B7	Translation Profile 0.5 (see Table 70)
Register 0x12B8 to Register 0x13FF	Not applicable
Digital Phase-Locked Loop 1 (DPLL1) Parameters	
Register 0x1400 to Register 0x142A	DPLL1 parameters (see Table 71)
Register 0x142B to Register 0x147F	Not applicable

Register Address	Register Description
Analog Phase-Locked Loop 1 (APLL1) Parameters	
Register 0x1480 to Register 0x1483	APLL1 parameters (see Table 72)
Register 0x1484 to Register 0x14BF	Not applicable
Distribution Control and Parameters	
Register 0x14C0 to Register 0x14DC	Distribution control: PLL Channel 1 (see Table 73)
Register 0x14DD to Register 0x14FF	Not applicable
Register 0x1500 to Register 0x1508	Distribution parameters: Q1A (see Table 74)
Register 0x1509 to Register 0x1511	Distribution parameters: Q1AA (see Table 75)
Register 0x1512 to Register 0x151A	Distribution parameters: Q1B (see Table 76)
Register 0x151B to Register 0x1523	Distribution parameters: Q1BB (see Table 77)
Register 0x1524 to Register 0x15FF	Not applicable
Translation Profile 1.0 to Translation Profile 1.5	
Register 0x1600 to Register 0x1617	Translation Profile 1.0 (see Table 78)
Register 0x1618 to Register 0x161F	Not applicable
Register 0x1620 to Register 0x1637	Translation Profile 1.1 (see Table 79)
Register 0x1638 to Register 0x163F	Not applicable
Register 0x1640 to Register 0x1657	Translation Profile 1.2 (see Table 80)
Register 0x1658 to Register 0x165F	Not applicable
Register 0x1660 to Register 0x1677	Translation Profile 1.3 (see Table 81)
Register 0x1678 to Register 0x167F	Not applicable
Register 0x1680 to Register 0x1697	Translation Profile 1.4 (see Table 82)
Register 0x1698 to Register 0x169F	Not applicable
Register 0x16A0 to Register 0x16B7	Translation Profile 1.5 (see Table 83)
Register 0x16B8 to Register 0x1FFF	Not applicable
Operational Control: General	
Register 0x2000 to Register 0x2004	Operational control: general (see Table 84)
IRQ Clear	Exception: Register 0x2005, Bit 7, reset watchdog timer
Register 0x2005 to Register 0x2019	IRQ clear (see Table 85)
Register 0x201A to Register 0x20FF	Not applicable
Operational Control	
Register 0x2100 to Register 0x2107	Operational control: PLL Channel 0 (see Table 86)
Register 0x2108 to Register 0x21FF	Not applicable
Register 0x2200 to Register 0x2207	Operational control: PLL Channel 1 (see Table 87)
Register 0x2208 to Register 0x27FF	Not applicable
Auxiliary NCO x Parameters	
Register 0x2800 to Register 0x281E	Auxiliary NCO 0 parameters (see Table 88)
Register 0x281F to Register 0x283F	Not applicable
Register 0x2840 to Register 0x285E	Auxiliary NCO 1 parameters (see Table 89)
Register 0x285F to Register 0x28FF	Not applicable
Temperature Sensor	
Register 0x2900 to Register 0x2906	Temperature sensor (see Table 90)
Register 0x2907 to Register 0x2A11	Not applicable
User Time Stamp Processor (UTSP) Controls	
Register 0x2A12 to Register 0x2A13	UTSP controls (see Table 91)
Skew Measurement Processor Controls	
Register 0x2A14 to Register 0x2A16	Skew measurement processor controls (see Table 92)
Register 0x2A17 to Register 0x2D01	Not applicable
Analog Loopback	
Register 0x2D02	Analog loopback (see Table 93)
Register 0x2D03 to Register 0x2DFF	Not applicable

Register Address	Register Description
EEPROM Controls	
Register 0x2E00 to Register 0x2E03	EEPROM controls (see Table 94)
Register 0x2E04 to Register 0x2E0F	Not applicable
Register 0x2E10 to Register 0x2E1E	EEPROM upload instruction space (see Table 95)
Register 0x2E1F to Register 0x2FFF	Not applicable
Status	
Register 0x3000	EEPROM status (see Table 96)
Register 0x3001	PLL (system clock PLL, PLL0 and PLL1) status (see Table 97)
Register 0x3002	Miscellaneous status (see Table 98)
Register 0x3003	Temperature sensor output (see Table 99)
Register 0x3005 to Register 0x3008	REFx status (see Table 100)
Register 0x3009 to Register 0x300A	DPLL profile status (see Table 101)
Register 0x300B to Register 0x301E	IRQ status (see Table 102)
Register 0x301F to Register 0x3022	Auxiliary REFx status (see Table 103)
Register 0x3023	IUTS status (see Table 104)
Register 0x3024 to Register 0x30FF	Not applicable
Register 0x3100 to Register 0x310E	PLL Channel 0 status (see Table 105)
Register 0x310F to Register 0x31FF	Not applicable
Register 0x3200 to Register 0x320E	PLL Channel 1 status (see Table 106)
Register 0x320F to Register 0x39FF	Not applicable
Auxiliary NCO x Time Scale	
Register 0x3A00 to Register 0x3A09	Auxiliary NCO 0 time scale (see Table 107)
Register 0x3A0A to Register 0x3A13	Auxiliary NCO 1 time scale (see Table 108)
Processor Outputs	
Register 0x3A14 to Register 0x3A1F	User time stamp processor output: UTSP0 (see Table 109)
Register 0x3A20 to Register 0x3A2B	User time stamp processor output: UTSP1 (see Table 110)
Register 0x3A2C to Register 0x3A3B	Skew measurement processor output (see Table 111)
Register 0x3A3C to Register 0xFFFF	Not applicable

REGISTER BIT DETAILS

SERIAL PORT—REGISTER 0x0000 TO REGISTER 0x0023

Table 3. Serial Port Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0000	7	Soft reset		Soft Reset. This bit must be set identical to Bit 0 (see Bit 0 for details).	0	R/W	Live	No
	6	LSB first (SPI only)		SPI LSB First. This bit must be set identical to Bit 1 (see Bit 1 for details).	0	R/W	Live	No
	5	Address ascension (SPI only)		SPI Address Ascension. This bit must be set identical to Bit 2 (see Bit 2 for details).	0	R/W	Live	No
	4	SDO active (SPI only)		Enable SPI 4-wire Mode. This bit must be set identical to Bit 3 (see Bit 3 for details).	0	R/W	Live	No
	3	SDO active (SPI only)		This bit selects whether the SPI SDO pin is an active output pin (4-wire SPI mode) or tristate (3-wire SPI mode). This bit has no effect in I²C mode.	0	R/W	Live	No
			0	SDO pin tristate (SDIO pin bidirectional), 3-wire SPI mode.				
			1	SDO pin active output (SDIO pin input only), 4-wire SPI mode.				
	2	Address ascension (SPI only)		SPI Address Ascension. This bit controls the direction (decrement or increment) that register addressing occurs during multibyte transfers. This bit has no effect in I²C mode.	0	R/W	Live	No
			0	Decrement.				
			1	Increment.				
	1	LSB first (SPI only)		SPI LSB First. Bit order for SPI port. This bit has no effect in I²C mode.	0	R/W	Live	No
			0	Most Significant Bit (MSB) First.				
			1	Least Significant Bit (LSB) First.				
	0	Soft reset		Soft Reset. Logic 1 invokes a device reset. Also, if the Mx pins are configured for an automatic EEPROM download, an EEPROM download initiates.	0	R/W	Live	No
0x0001	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	Read buffer register		Read Buffer Register. For buffered registers, this bit controls whether the value read from the serial port is buffered data or active data (active being data transferred to active registers via assertion of an IO update).	0	R/W	Live	No
			0	Reads the register values that are currently active (default).				
			1	Reads buffered values that take effect on next I/O update.				
	[4:3]	Reserved		Reserved.	0x0	R	Live	No
	2	Reset sans registers		Reset Sans Register Map. Writing Logic 1 resets the device while maintaining the current settings.	0	R/W	Live	No
	[1:0]	Reserved		Reserved.	0x0	R	Live	No
0x0003	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	[3:0]	Chip type		Chip Type. This register is a part of the Analog Devices unified SPI protocol, and is used to identify this chip as a clock IC.	0x5	R	Live	No
			0x5	clock chip.				
0x0004	[7:0]	Device Code[7:0]		Device Code. This read only register contains device identification details.	0x21	R	Live	No
0x0005	[7:0]	Device Code[15:8]		Continuation of the device code bit field. See the Device Code[7:0] description.	0x01	R	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0006	[7:0]	Device Code[23:16]		Continuation of the device code bit field. See the Device Code[7:0] description.	0x04	R	Live	No
0x000B	[7:0]	SPI version		Version of Analog Devices Unified SPI Protocol.	0x00	R	Live	No
0x000C	[7:0]	Vendor ID[7:0]		Analog Devices Unified SPI Vendor ID.	0x56	R	Live	No
0x000D	[7:0]	Vendor ID[15:8]		Continuation of the vendor ID bit field. See the Vendor ID[7:0] description.	0x04	R	Live	No
0x000F	[7:2]	Reserved		Reserved.	0x00	R	Live	No
	1	Address loop IO update		Address Loop IO Update. An IO update is automatically issued each time the address field loops. This is useful when polling a range of registers and an I/O update needs to be issued after each cycle.	0	R/W	Live	No
	0	IO update		IO Update. Setting this autoclearing bit transfers values from the buffered to active register space.	0	W	Live	Yes
0x0010	[7:0]	Address loop length		Address Loop Length. The number of consecutive addresses that are written or read in each cycle in an address loop.	0x00	R/W	Live	No
0x0020	[7:0]	User Scratchpad[7:0]		User Scratchpad. This register has no effect on device operation. It is available for device debugging or register setting revision control.	0x00	R/W	Live	No
0x0021	[7:0]	User Scratchpad[15:8]		Continuation of the user scratchpad bit field. See the User Scratchpad[7:0] description.	0x00	R/W	Live	No
0x0022	[7:0]	User Scratchpad[23:16]		Continuation of the user scratchpad bit field. See the User Scratchpad[7:0] description.	0x00	R/W	Live	No
0x0023	[7:0]	User Scratchpad[31:24]		Continuation of the user scratchpad bit field. See the User Scratchpad[7:0] description.	0x00	R/W	Live	No

Mx PIN MODE—REGISTER 0x0100 TO REGISTER 0x0101

Driver details apply when the corresponding Mx pin is configured as a status pin. Receiver details apply when the corresponding Mx pin is configured as a control pin. To configure an Mx pin for status or control see the Mx Pin Status or Control Select—Register 0x0102 to Register 0x0108 section.

Table 4. Mx Pin Mode Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0100	[7:6]	M3 driver		M3 Pin Status Mode (Output). When M3 is configured as a status pin, the user can choose the output polarity (normal (default) or inverted) and output driver type (complementary (default) or open drain). Polarity: relates to how the output pin responds to the true or false state of the selected M3 status function (for example, REFA faulted). With normal polarity, when the selected status function state is true or false, the output pin state is Logic 1 or Logic 0, respectively. With inverted polarity, when the selected status function state is true or false, the output pin state is Logic 0 or Logic 1, respectively. Driver type: complementary uses a CMOS output circuit. Open drain uses an NMOS or PMOS output circuit (polarity dependent). Normal polarity uses a PMOS device, which actively drives Logic 1, but is high impedance for Logic 0 (requires an external pull-down resistor). Inverted polarity uses an NMOS device, which actively drives Logic 0, but is high impedance for Logic 1 (requires an external pull-up resistor). The open-drain configuration allows a wire-OR'ed connection to other Mx status pins having an open-drain driver with like polarity.	0x0	R/W	Serial port clock	No
			0	Complementary normal (default).				
			1	Complementary inverted.				
			2	Open drain normal.				
			3	Open drain inverted.				
	[7:6]	M3 receiver		M3 Pin Control Mode (Input). When M3 is configured as a control pin, the user can choose the input polarity (normal (default) or inverted) and logical type (AND (default) or OR). Polarity: normal polarity makes no change to the input pin signal. Inverted polarity inverts the input pin signal. Logical type: the logical type is only meaningful when the Mx pins other than M3 share a common control function (for example, IO update). In this case, the control function responds to all Mx control pins having the same control function as follows. The OR inputs combine in a logical OR sense to yield a single OR result. The AND inputs, along with the OR result, combine in a logical AND sense to yield a single AND result, which applies to the common control function (for example, IO update).	0x0	R/W	Serial port clock	No
			0	AND normal (default).				
			1	AND inverted.				
			2	OR normal.				
			3	OR inverted.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[5:4]	M2 driver		M2 Pin Status Mode (Output). When M2 is configured as a status pin, the user can choose the output polarity (normal (default) or inverted) and output driver type (complementary (default) or open drain). Polarity: relates to how the output pin responds to the true or false state of the selected M2 status function (for example, REFA faulted). With normal polarity, when the selected status function state is true or false, the output pin state is Logic 1 or Logic 0, respectively. With inverted polarity, when the selected status function state is true or false, the output pin state is Logic 0 or Logic 1, respectively.	0x0	R/W	Serial port clock	No
				Driver type: complementary uses a CMOS output circuit. Open drain uses an NMOS or PMOS output circuit (polarity dependent). Normal polarity uses a PMOS device, which actively drives Logic 1, but is high impedance for Logic 0 (requires an external pull-down resistor). Inverted polarity uses an NMOS device, which actively drives Logic 0, but is high impedance for Logic 1 (requires an external pull-up resistor). The open-drain configuration allows a wire-OR'ed connection to other Mx status pins having an open-drain driver with like polarity.				
			0	Complementary normal (default).				
			1	Complementary inverted.				
			2	Open drain normal.				
			3	Open drain inverted.				
	[5:4]	M2 receiver		M2 Pin Control Mode (Input). When M2 is configured as a control pin, the user can choose the input polarity (normal (default) or inverted) and logical type (AND (default) or OR). Polarity: normal polarity makes no change to the input pin signal. Inverted polarity inverts the input pin signal. Logical type: the logical type is only meaningful when the Mx pins other than M2 share a common control function (for example, IO update). In this case, the control function responds to all Mx control pins having the same control function as follows. The OR inputs combine in a logical OR sense to yield a single OR result. The AND inputs, along with the OR result, combine in a logical AND sense to yield a single AND result, which applies to the common control function (for example, IO update).	0x0	R/W	Serial port clock	No
			0	AND normal (default).				
			1	AND inverted.				
			2	OR normal.				
			3	OR inverted.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[3:2]	M1 driver		M1 Pin Status Mode (Output). When M1 is configured as a status pin, the user can choose the output polarity (normal (default) or inverted) and output driver type (complementary (default) or open drain). Polarity: relates to how the output pin responds to the true or false state of the selected M1 status function (for example, REFA faulted). With normal polarity, when the selected status function state is true or false, the output pin state is Logic 1 or Logic 0, respectively. With inverted polarity, when the selected status function state is true or false, the output pin state is Logic 0 or Logic 1, respectively. Driver type: complementary uses a CMOS output circuit. Open drain uses an NMOS or PMOS output circuit (polarity dependent). Normal polarity uses a PMOS device, which actively drives Logic 1, but is high impedance for Logic 0 (requires an external pull-down resistor). Inverted polarity uses an NMOS device, which actively drives Logic 0, but is high impedance for Logic 1 (requires an external pull-up resistor). The open-drain configuration allows a wire-OR'ed connection to other Mx status pins having an open-drain driver with like polarity.	0x0	R/W	Serial port clock	No
			0	Complementary normal (default).				
			1	Complementary inverted.				
			2	Open drain normal.				
			3	Open drain inverted.				
	[3:2]	M1 receiver		M1 Pin Control Mode (Input). When M1 is configured as a control pin, the user can choose the input polarity (normal (default) or inverted) and logical type (AND (default) or OR). Polarity: normal polarity makes no change to the input pin signal. Inverted polarity inverts the input pin signal. Logical type: the logical type is only meaningful when the Mx pins other than M1 share a common control function (for example, IO update). In this case, the control function responds to all Mx control pins having the same control function as follows. The OR inputs combine in a logical OR sense to yield a single OR result. The AND inputs, along with the OR result, combine in a logical AND sense to yield a single AND result, which applies to the common control function (for example, IO update).	0x0	R/W	Serial port clock	No
			0	AND normal (default).				
			1	AND inverted.				
			2	OR normal.				
			3	OR inverted.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[1:0]	M0 driver		M0 Pin Status Mode (Output). When M0 is configured as a status pin, the user can choose the output polarity (normal (default) or inverted) and output driver type (complementary (default) or open drain). Polarity: relates to how the output pin responds to the true or false state of the selected M0 status function (for example, REFA faulted). With normal polarity, when the selected status function state is true or false, the output pin state is Logic 1 or Logic 0, respectively. With inverted polarity, when the selected status function state is true or false, the output pin state is Logic 0 or Logic 1, respectively. Driver type: complementary uses a CMOS output circuit. Open drain uses an NMOS or PMOS output circuit (polarity dependent). Normal polarity uses a PMOS device, which actively drives Logic 1, but is high impedance for Logic 0 (requires an external pull-down resistor). Inverted polarity uses an NMOS device, which actively drives Logic 0, but is high impedance for Logic 1 (requires an external pull-up resistor). The open-drain configuration allows a wire-OR'ed connection to other Mx status pins having an open-drain driver with like polarity.	0x0	R/W	Serial port clock	No
			0	Complementary normal (default).				
			1	Complementary inverted.				
			2	Open drain normal.				
			3	Open drain inverted.				
	[1:0]	M0 receiver		M0 Pin Control Mode (Input). When M0 is configured as a control pin, the user can choose the input polarity (normal (default) or inverted) and logical type (AND (default) or OR). Polarity: normal polarity makes no change to the input pin signal. Inverted polarity inverts the input pin signal. Logical type: the logical type is only meaningful when the Mx pins other than M0 share a common control function (for example, IO update). In this case, the control function responds to all Mx control pins having the same control function as follows. The OR inputs combine in a logical OR sense to yield a single OR result. The AND inputs, along with the OR result, combine in a logical AND sense to yield a single AND result, which applies to the common control function (for example, IO update).	0x0	R/W	Serial port clock	No
			0	AND normal (default).				
			1	AND inverted.				
			2	OR normal.				
			3	OR inverted.				
0x0101	[7:6]	Reserved		Reserved.	0x0	R	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[5:4]	M6 driver		CSB/M6 Pin Status Mode (Output). When CSB/M6 is configured as a status pin, the user can choose the output polarity (normal (default) or inverted) and output driver type (complementary (default) or open drain). Polarity: relates to how the output pin responds to the true or false state of the selected M6 status function (for example, REFA faulted). With normal polarity, when the selected status function state is true or false, the output pin state is Logic 1 or Logic 0, respectively. With inverted polarity, when the selected status function state is true or false, the output pin state is Logic 0 or Logic 1, respectively. Driver type: complementary uses a CMOS output circuit. Open drain uses an NMOS or PMOS output circuit (polarity dependent). Normal polarity uses a PMOS device, which actively drives Logic 1, but is high impedance for Logic 0 (requires an external pull-down resistor). Inverted polarity uses an NMOS device, which actively drives Logic 0, but is high impedance for Logic 1 (requires an external pull-up resistor). The open-drain configuration allows a wire-OR'ed connection to other Mx status pins having an open-drain driver with like polarity.	0x0	R/W	Serial port clock	No
			0	Complementary normal (default).				
			1	Complementary inverted.				
			2	Open drain normal.				
			3	Open drain inverted.				
	[5:4]	M6 receiver		CSB/M6 Pin Control Mode (Input). When CSB/M6 is configured as a control pin, the user can choose the input polarity (normal (default) or inverted) and logical type (AND (default) or OR). Polarity: normal polarity makes no change to the input pin signal. Inverted polarity inverts the input pin signal. Logical type: the logical type is only meaningful when the Mx pins other than CSB/M6 share a common control function (for example, IO update). In this case, the control function responds to all Mx control pins having the same control function as follows. The OR inputs combine in a logical OR sense to yield a single OR result. The AND inputs, along with the OR result, combine in a logical AND sense to yield a single AND result, which applies to the common control function (for example, IO update).	0x0	R/W	Serial port clock	No
			0	AND normal (default).				
			1	AND inverted.				
			2	OR normal.				
			3	OR inverted.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[3:2]	M5 driver		SDO/M5 Pin Status Mode (Output). When SDO/M5 is configured as a status pin, the user can choose the output polarity (normal (default) or inverted) and output driver type (complementary (default) or open drain). Polarity: relates to how the output pin responds to the true or false state of the selected M5 status function (for example, REFA faulted). With normal polarity, when the selected status function state is true or false, the output pin state is Logic 1 or Logic 0, respectively. With inverted polarity, when the selected status function state is true or false, the output pin state is Logic 0 or Logic 1, respectively.	0x0	R/W	Serial port clock	No
				Driver type: complementary uses a CMOS output circuit. Open drain uses an NMOS or PMOS output circuit (polarity dependent). Normal polarity uses a PMOS device, which actively drives Logic 1, but is high impedance for Logic 0 (requires an external pull-down resistor). Inverted polarity uses an NMOS device, which actively drives Logic 0, but is high impedance for Logic 1 (requires an external pull-up resistor). The open-drain configuration allows a wire-OR'ed connection to other Mx status pins having an open-drain driver with like polarity.				
			0	Complementary normal (default).				
			1	Complementary inverted.				
			2	Open drain normal.				
			3	Open drain inverted.				
	[3:2]	M5 receiver		SDO/M5 Pin Control Mode (Input). When SDO/M5 is configured as a control pin, the user can choose the input polarity (normal (default) or inverted) and logical type (AND (default) or OR). Polarity: normal polarity makes no change to the input pin signal. Inverted polarity inverts the input pin signal. Logical type: the logical type is only meaningful when the Mx pins other than SDO/M5 share a common control function (for example, IO update). In this case, the control function responds to all Mx control pins having the same control function as follows. The OR inputs combine in a logical OR sense to yield a single OR result. The AND inputs, along with the OR result, combine in a logical AND sense to yield a single AND result, which applies to the common control function (for example, IO update).	0x0	R/W	Serial port clock	No
			0	AND normal (default).				
			1	AND inverted.				
			2	OR normal.				
			3	OR inverted.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[1:0]	M4 driver		M4 Pin Status Mode (Output). When M4 is configured as a status pin, the user can choose the output polarity (normal (default) or inverted) and output driver type (complementary (default) or open drain). Polarity: relates to how the output pin responds to the true or false state of the selected M4 status function (for example, REFA faulted). With normal polarity, when the selected status function state is true or false, the output pin state is Logic 1 or Logic 0, respectively. With inverted polarity, when the selected status function state is true or false, the output pin state is Logic 0 or Logic 1, respectively. Driver type: complementary uses a CMOS output circuit. Open drain uses an NMOS or PMOS output circuit (polarity dependent). Normal polarity uses a PMOS device, which actively drives Logic 1, but is high impedance for Logic 0 (requires an external pull-down resistor). Inverted polarity uses an NMOS device, which actively drives Logic 0, but is high impedance for Logic 1 (requires an external pull-up resistor). The open-drain configuration allows a wire-OR'ed connection to other Mx status pins having an open-drain driver with like polarity.	0x0	R/W	Serial port clock	No
			0	Complementary normal (default).				
			1	Complementary inverted.				
			2	Open drain normal.				
			3	Open drain inverted.				
	[1:0]	M4 receiver		M4 Pin Control Mode (Input). When M4 is configured as a control pin, the user can choose the input polarity (normal (default) or inverted) and logical type (AND (default) or OR). Polarity: normal polarity makes no change to the input pin signal. Inverted polarity inverts the input pin signal. Logical type: the logical type is only meaningful when the Mx pins other than M4 share a common control function (for example, IO update). In this case, the control function responds to all Mx control pins having the same control function as follows. The OR inputs combine in a logical OR sense to yield a single OR result. The AND inputs, along with the OR result, combine in a logical AND sense to yield a single AND result, which applies to the common control function (for example, IO update).	0x0	R/W	Serial port clock	No
			0	AND normal (default).				
			1	AND inverted.				
			2	OR normal.				
			3	OR inverted.				

Mx PIN STATUS OR CONTROL SELECT—REGISTER 0x0102 TO REGISTER 0x0108

Table 5. Mx Pin Status or Control Select Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0102	7	M0 OE		M0 Control/Status Select. This bit configures the M0 pin as a control input pin (default) or a status output pin. See special instructions for Bits[6:0].	0	R/W	Serial port clock	No
			0	Control input (default).				
			1	Status output.				
	[6:0]	Reserved		When writing to Bit 7 of this register, make Bits[6:0] the same values as Register 0x0182, Bits[6:0].	0x00	R/W	Serial port clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0103	7	M1 OE		M1 Control/Status Select. This bit configures the M1 pin as a control input pin (default) or a status output pin. See special instructions for Bits[6:0].	0	R/W	Serial port clock	No
			0	Control input (default).				
			1	Status output.				
	[6:0]	Reserved		When writing to Bit 7 of this register, make Bits[6:0] the same values as Register 0x0183, Bits[6:0].	0x00	R/W	Serial port clock	No
0x0104	7	M2 OE		M2 Control/Status Select. This bit configures the M2 pin as a control input pin (default) or a status output pin. See special instructions for Bits[6:0].	0	R/W	Serial port clock	No
			0	Control input (default).				
			1	Status output.				
	[6:0]	Reserved		When writing to Bit 7 of this register, make Bits[6:0] the same values as Register 0x0184, Bits[6:0].	0x00	R/W	Serial port clock	No
0x0105	7	M3 OE		M3 Control/Status Select. This bit configures the M3 pin as a control input pin (default) or a status output pin. See special instructions for Bits[6:0].	0	R/W	Serial port clock	No
			0	Control input (default).				
			1	Status output.				
	[6:0]	Reserved		When writing to Bit 7 of this register, make Bits[6:0] the same values as Register 0x0185, Bits[6:0].	0x00	R/W	Serial port clock	No
0x0106	7	M4 OE		M4 Control/Status Select. This bit configures the M4 pin as a control input pin (default) or a status output pin. See special instructions for Bits[6:0].	0	R/W	Serial port clock	No
			0	Control input (default).				
			1	Status output.				
	[6:0]	Reserved		When writing to Bit 7 of this register, make Bits[6:0] the same values as Register 0x0186, Bits[6:0].	0x00	R/W	Serial port clock	No
0x0107	7	M5 OE		M5 Control/Status Select. This bit configures the SDO/M5 pin as a control input pin (default) or a status output pin. See special instructions for Bits[6:0].	0	R/W	Serial port clock	No
			0	Control input (default).				
			1	Status output.				
	[6:0]	Reserved		When writing to Bit 7 of this register, make Bits[6:0] the same values as Register 0x0187, Bits[6:0].	0x00	R/W	Serial port clock	No
0x0108	7	M6 OE		M6 Control/Status Select. This bit configures the CSB/M6 pin as a control input pin (default) or a status output pin. See special instructions for Bits[6:0].	0	R/W	Serial port clock	No
			0	Control input (default).				
			1	Status output.				
	[6:0]	Reserved		When writing to Bit 7 of this register, make Bits[6:0] the same values as Register 0x0188, Bits[6:0].	0x00	R/W	Serial port clock	No

SERIAL PORT AND Mx PIN OUTPUT DRIVE CURRENT—REGISTER 0x0109

Bits[6:0] only have meaning when an Mx pin is configured as a status pin. To configure an Mx pin for status or control, see the Mx Pin Status or Control Select—Register 0x0102 to Register 0x0108 section.

Table 6. Serial Port and Mx Pin Output Drive Current Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0109	7	SPI configuration		SPI Output Drive Strength. This bit selects the nominal output drive strength of the SPI port pins.	0	R/W	Live	No
			0	6 mA nominal drive strength (default).				
			1	3 mA nominal drive strength.				
	6	M6 configuration		CSB/M6 Output Drive Strength. This bit selects the output drive current of the CSB/M6 pin, which is only meaningful when CSB/M6 is configured as a status (output) pin.	0	R/W	Live	No
			0	6 mA nominal drive strength (default).				
			1	3 mA nominal drive strength.				
	5	M5 configuration		SDO/M5 Output Drive Strength. This bit selects the output drive current of the SDO/M5 pin, which is only meaningful when SDO/M5 is configured as a status (output) pin.	0	R/W	Live	No
			0	6 mA nominal drive strength (default).				
			1	3 mA nominal drive strength.				
	4	M4 configuration		M4 Output Drive Strength. This bit selects the output drive current of the M4 pin, which is only meaningful when M4 is configured as a status (output) pin.	0	R/W	Live	No
			0	6 mA nominal drive strength (default).				
			1	3 mA nominal drive strength.				
	3	M3 configuration		M3 Output Drive Strength. This bit selects the output drive current of the M3 pin, which is only meaningful when M3 is configured as a status (output) pin.	0	R/W	Live	No
			0	6 mA nominal drive strength (default).				
			1	3 mA nominal drive strength.				
	2	M2 configuration		M2 Output Drive Strength. This bit selects the output drive current of the M2 pin, which is only meaningful when M2 is configured as a status (output) pin.	0	R/W	Live	No
			0	6 mA nominal drive strength (default).				
			1	3 mA nominal drive strength.				
	1	M1 configuration		M1 Output Drive Strength. This bit selects the output drive current of the M1 pin, which is only meaningful when M1 is configured as a status (output) pin.	0	R/W	Live	No
			0	6 mA nominal drive strength (default).				
			1	3 mA nominal drive strength.				
	0	M0 configuration		M0 Output Drive Strength. This bit selects the output drive current of the M0 pin, which is only meaningful when M0 is configured as a status (output) pin.	0	R/W	Live	No
			0	6 mA nominal drive strength (default).				
			1	3 mA nominal drive strength.				

WATCHDOG TIMER—REGISTER 0x010A TO REGISTER 0x010B

Table 7. Watchdog Timer Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x010A	[7:0]	Watchdog Timer[7:0]		Watchdog Timer Period. This 16-bit unsigned watchdog timer value in units of milliseconds (default = 0), sets the period of the watchdog timer. Programming the watchdog timer value = 0 disables the watchdog timer. The watchdog timer resets upon a write to this register and starts running upon subsequent assertion of IO update.	0x00	R/W	Core clock	No
0x010B	[7:0]	Watchdog Timer[15:8]		Continuation of the watchdog timer bit field. See the Watchdog Timer[7:0] description.	0x00	R/W	Core clock	No

IRQ ENABLE—REGISTER 0x010C TO REGISTER 0x011F

Table 8. IRQ Enable Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x010C	7	SYSCLK unlock IRQ enable		System Clock (SYSCLK) PLL Unlocked IRQ Enable (Common Group). Program Logic 1 to allow a system clock PLL has phase unlocked event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Serial port clock	No
	6	SYSCLK stable IRQ enable		System Clock PLL Stable IRQ Enable (Common Group). Program Logic 1 to allow a system clock PLL is phase locked and the stability period has been met event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	5	SYSCLK lock IRQ enable		System Clock PLL Locked IRQ Enable (Common Group). Program Logic 1 to allow a system clock PLL has phase locked event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Serial port clock	No
	4	SYSCLK calibration end IRQ enable		System Clock PLL Calibration Ended IRQ Enable (Common Group). Program Logic 1 to allow a calibration of the system clock PLL has ended event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Serial port clock	No
	3	SYSCLK calibration start IRQ enable		System Clock PLL Calibration Started IRQ Enable (Common Group). Program Logic 1 to allow a calibration of the system clock PLL has started event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Serial port clock	No
	2	Watchdog timeout IRQ enable		Watchdog Timeout IRQ Enable (Common Group). Program Logic 1 to allow a watchdog timer expired event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	1	EEPROM fault IRQ enable		EEPROM Upload Fault IRQ Enable (Common Group). Program Logic 1 to allow an EEPROM upload fault event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Serial port clock	No
	0	EEPROM complete IRQ enable		EEPROM Action Complete IRQ Enable (Common Group). Program Logic 1 to allow the EEPROM controller completed an invoked action (for example, an upload sequence) to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Serial port clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x010D	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	Skew limit exceeded IRQ enable		Skew Limit Exceeded IRQ Enable (Common Group). Program Logic 1 to allow the time skew measurement processor reported drift beyond its 1/16th UI drift limit event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	4	Temperature warning IRQ enable		Temperature Range Warning IRQ Enable (Common Group). Program Logic 1 to allow a temperature sensor output violated the user programmed threshold limits event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	3	Auxiliary DPLL unfault IRQ enable		Auxiliary DPLL Unfaulted IRQ Enable (Common Group). Program Logic 1 to allow the auxiliary DPLL reference monitor unfaulted event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W -	Core clock	No
	2	Auxiliary DPLL fault IRQ enable		Auxiliary DPLL Faulted IRQ Enable (Common Group). Program Logic 1 to allow the auxiliary DPLL reference monitor faulted event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	1	Auxiliary DPLL unlock IRQ enable		Auxiliary DPLL Unlocked IRQ Enable (Common Group). Program Logic 1 to allow the auxiliary DPLL phase unlocked event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	0	Auxiliary DPLL lock IRQ enable		Auxiliary DPLL Locked IRQ Enable (Common Group). Program Logic 1 to allow the auxiliary DPLL phase locked event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
0x010E	7	REFAA R divider resynchronization IRQ enable		REFAA Divider Resynchronization IRQ Enable (Common Group). Program Logic 1 to allow a REFAA reference divider was resynchronized event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	6	REFAA valid IRQ enable		REFAA Validated IRQ Enable (Common Group). Program Logic 1 to allow a REFAA reference monitor validated event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	5	REFAA unfault IRQ enable		REFAA Unfaulted IRQ Enable (Common Group). Program Logic 1 to allow a REFAA reference monitor unfaulted event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	4	REFAA fault IRQ enable		REFAA Faulted IRQ Enable (Common Group). Program Logic 1 to allow a REFAA reference monitor faulted event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	3	REFA R divider resynchronization IRQ enable		REFA Divider Resynchronization IRQ Enable (Common Group). Program Logic 1 to allow a REFA reference divider was resynchronized event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	2	REFA valid IRQ enable		REFA Validated IRQ Enable (Common Group). Program Logic 1 to allow a REFA reference monitor validated event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	1	REFA unfault IRQ enable		REFA Unfaulted IRQ Enable (Common Group). Program Logic 1 to allow a REFA reference monitor unfaulted event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	0	REFA fault IRQ enable		REFA Faulted IRQ Enable (Common Group). Program Logic 1 to allow a REFA reference monitor faulted event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
0x010F	7	REFBB R divider resynchronization IRQ enable		REFBB Divider Resynchronization IRQ Enable (Common Group). Program Logic 1 to allow a REFBB reference divider was resynchronized event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	6	REFBB valid IRQ enable		REFBB Validated IRQ Enable (Common Group). Program Logic 1 to allow a REFBB reference monitor validated event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	5	REFBB unfault IRQ enable		REFBB Unfaulted IRQ Enable (Common Group). Program Logic 1 to allow a REFBB reference monitor unfaulted event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	4	REFBB fault IRQ enable		REFBB Faulted IRQ Enable (Common Group). Program Logic 1 to allow a REFBB reference monitor faulted event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	3	REFB R divider resynchronization IRQ enable		REFB Divider Resynchronization IRQ Enable (Common Group). Program Logic 1 to allow a REFB reference divider was resynchronized event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	2	REFB valid IRQ enable		REFB Validated IRQ Enable (Common Group). Program Logic 1 to allow a REFB reference monitor validated event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	1	REFB unfault IRQ enable		REFB Unfaulted IRQ Enable (Common Group). Program Logic 1 to allow a REFB reference monitor unfaulted event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	0	REFB fault IRQ enable		REFB Faulted IRQ Enable (Common Group). Program Logic 1 to allow a REFB reference monitor faulted event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
0x0110	[7:5]	Reserved		Reserved.	0x0	R/W	Core clock	No
	4	Skew measurement updated IRQ enable		Skew Measurement Updated IRQ Enable (Common Group). Program Logic 1 to allow the time skew measurement processor completed a time skew measurement event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	3	UTSP1 update IRQ enable		UTSP1 Update IRQ Enable (Common Group). Program Logic 1 to allow a User Time Stamp Processor 1 completed a time stamp conversion event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	2	UTSP0 update IRQ enable		UTSP0 Update IRQ Enable (Common Group). Program Logic 1 to allow a User Time Stamp Processor 0 completed a time stamp conversion event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	1	Auxiliary NCO 1 event IRQ enable		Auxiliary NCO 1 Event IRQ Enable (Common Group). Program Logic 1 to allow an Auxiliary NCO 1 accumulator rollover occurred event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	0	Auxiliary NCO 0 event IRQ enable		Auxiliary NCO 0 Event IRQ Enable (Common Group). Program Logic 1 to allow an Auxiliary NCO 0 accumulator rollover occurred event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
0x0111	7	DPLL0 frequency unclamped IRQ enable		DPLL0 Frequency Unclamped IRQ Enable (PLL0 Group). Program Logic 1 to allow a DPLL0 frequency clamp became unclamped event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	6	DPLL0 frequency clamped IRQ enable		DPLL0 Frequency Clamped IRQ Enable (PLL0 Group). Program Logic 1 to allow a DPLL0 frequency clamp started actively clamping event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	5	DPLL0 phase slew limiter inactive IRQ enable		DPLL0 Phase Slew Limiter Inactive IRQ Enable (PLL0 Group). Program Logic 1 to allow a DPLL0 phase slew limiter became inactive event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	4	DPLL0 phase slew limiter active IRQ enable		DPLL0 Phase Slew Limiter Active IRQ Enable (PLL0 Group). Program Logic 1 to allow a DPLL0 phase slew limiter became active event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	3	DPLL0 frequency unlocked IRQ enable		DPLL0 Frequency Unlocked IRQ Enable (PLL0 Group). Program Logic 1 to allow a DPLL0 frequency lock to unlock transition event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	2	DPLL0 frequency locked IRQ enable		DPLL0 Frequency Locked IRQ Enable (PLL0 Group). Program Logic 1 to allow a DPLL0 frequency unlock to lock transition event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	1	DPLL0 phase unlocked IRQ enable		DPLL0 Phase Unlocked IRQ Enable (PLL0 Group). Program Logic 1 to allow a DPLL0 phase lock to unlock transition event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	0	DPLL0 phase locked IRQ enable		DPLL0 Phase-Locked IRQ Enable (PLL0 Group). Program Logic 1 to allow a DPLL0 phase unlock to lock transition event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0112	7	DPLL0 reference switch IRQ enable		DPLL0 Reference Switch IRQ Enable (PLL0 Group). Program Logic 1 to allow a DPLL0 initiated a reference switchover event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	6	DPLL0 entered freerun mode IRQ enable		DPLL0 Entered Freerun Mode IRQ Enable (PLL0 Group). Program Logic 1 to allow a DPLL0 entered freerun mode event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	5	DPLL0 entered holdover mode IRQ enable		DPLL0 Entered Holdover Mode IRQ Enable (PLL0 Group). Program Logic 1 to allow a DPLL0 entered holdover mode event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	4	DPLL0 hitless mode entered IRQ enable		DPLL0 Hitless Mode Entered IRQ Enable (PLL0 Group). Program Logic 1 to allow a DPLL0 entered hitless mode event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	3	DPLL0 hitless mode exited IRQ enable		DPLL0 Hitless Mode Exited IRQ Enable (PLL0 Group). Program Logic 1 to allow a DPLL0 exited hitless mode event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	2	DPLL0 holdover FTW history updated IRQ enable		DPLL0 Holdover Frequency Tuning Word (FTW) History Updated IRQ Enable (PLL0 Group). Program Logic 1 to allow a DPLL0 holdover frequency tuning word history updated event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	1	Reserved		Reserved.	0	R/W	Core clock	No
	0	DPLL0 phase step detected IRQ enable		DPLL0 Phase Step Detected IRQ Enable (PLL0 Group). Program Logic 1 to allow a DPLL0 reference input phase step detected event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
0x0113	[7:5]	Reserved		Reserved.	0x0	R/W	Core clock	No
	4	DPLL0 N divider resynchronized IRQ enable		DPLL0 N Divider Resynchronized IRQ Enable (PLL0 Group). Program Logic 1 to allow a DPLL0 feedback divider resynchronized event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	3	DPLL0 fast acquisition completed IRQ enable		DPLL0 Fast Acquisition Completed IRQ Enable (PLL0 Group). Program Logic 1 to allow a DPLL0 completed a fast acquisition sequence event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	2	DPLL0 fast acquisition started IRQ enable		DPLL0 Fast Acquisition Started IRQ Enable (PLL0 Group). Program Logic 1 to allow a DPLL0 started a fast acquisition sequence event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	[1:0]	Reserved		Reserved.	0x0	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0114	[7:6]	Reserved		Reserved.	0x0	R/W	Core clock	No
	5	DPLL0 Translation Profile 0.5 activated FTW IRQ enable		DPLL0 Translation Profile 0.5 Activated IRQ Enable (PLL0 Group). Program Logic 1 to allow a DPLL0 Translation Profile 0.5 activated event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	4	DPLL0 Translation Profile 0.4 activated IRQ enable		DPLL0 Translation Profile 0.4 Activated IRQ Enable (PLL0 Group). Program Logic 1 to allow a DPLL0 Translation Profile 0.4 activated event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	3	DPLL0 Translation Profile 0.3 activated IRQ enable		DPLL0 Translation Profile 0.3 Activated IRQ Enable (PLL0 Group). Program Logic 1 to allow a DPLL0 Translation Profile 0.3 activated event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	2	DPLL0 Translation Profile 0.2 activated IRQ enable		DPLL0 Translation Profile 0.2 Activated IRQ Enable (PLL0 Group). Program Logic 1 to allow a DPLL0 Translation Profile 0.2 activated event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	1	DPLL0 Translation Profile 0.1 activated IRQ enable		DPLL0 Translation Profile 0.1 Activated IRQ Enable (PLL0 Group). Program Logic 1 to allow a DPLL0 Translation Profile 0.1 activated event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	0	DPLL0 Translation Profile 0.0 activated IRQ enable		DPLL0 Translation Profile 0.0 Activated IRQ Enable (PLL0 Group). Program Logic 1 to allow a DPLL0 Translation Profile 0.0 activated event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
0x0115	[7:5]	Reserved		Reserved.	0x0	R/W	Core clock	No
	4	PLL0 clock outputs synchronized IRQ enable		PLL0 Clock Outputs Synchronized IRQ Enable (PLL0 Group). Program Logic 1 to allow a PLL0 clock distribution outputs synchronized event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	3	APLL0 phase unlocked IRQ enable		APLL0 Phase Unlocked IRQ Enable (PLL0 Group). Program Logic 1 to allow an APLL0 phase lock to unlock transition event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	2	APLL0 phase locked IRQ enable		APLL0 Phase-Locked IRQ Enable (PLL0 Group). Program Logic 1 to allow an APLL0 phase unlock to lock transition event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	1	APLL0 calibration completed IRQ enable		APLL0 Calibration Completed IRQ Enable (PLL0 Group). Program Logic 1 to allow an APLL0 calibration completed event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	0	APLL0 calibration started IRQ enable		APLL0 Calibration Started IRQ Enable (PLL0 Group). Program Logic 1 to allow an APLL0 calibration started event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0116	7	DPLL1 frequency unclamped IRQ enable		DPLL1 Frequency Unclamped IRQ Enable (PLL1 Group). Program Logic 1 to allow a DPLL1 frequency clamp became unclamped event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	6	DPLL1 frequency clamped IRQ enable		DPLL1 Frequency Clamped IRQ Enable (PLL1 Group). Program Logic 1 to allow a DPLL1 frequency clamp started actively clamping event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	5	DPLL1 phase slew limiter inactive IRQ enable		DPLL1 Phase Slew Limiter Inactive IRQ Enable (PLL1 Group). Program Logic 1 to allow a DPLL1 phase slew limiter became inactive event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	4	DPLL1 phase slew limiter active IRQ enable		DPLL1 Phase Slew Limiter Active IRQ Enable (PLL1 Group). Program Logic 1 to allow a DPLL1 phase slew limiter became active event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	3	DPLL1 frequency unlocked IRQ enable		DPLL1 Frequency Unlocked IRQ Enable (PLL1 Group). Program Logic 1 to allow a DPLL1 frequency lock to unlock transition event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	2	DPLL1 frequency locked IRQ enable		DPLL1 Frequency Locked IRQ Enable (PLL1 Group). Program Logic 1 to allow a DPLL1 frequency unlock to lock transition event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	1	DPLL1 phase unlocked IRQ enable		DPLL1 Phase Unlocked IRQ Enable (PLL1 Group). Program Logic 1 to allow a DPLL1 phase lock to unlock transition event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	0	DPLL1 phase-locked IRQ enable		DPLL1 Phase-Locked IRQ Enable (PLL1 Group). Program Logic 1 to allow a DPLL1 phase unlock to lock transition event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
0x0117	7	DPLL1 reference switch IRQ enable		DPLL1 Reference Switch IRQ Enable (PLL1 Group). Program Logic 1 to allow a DPLL1 initiated a reference switchover event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	6	DPLL1 entered freerun mode IRQ enable		DPLL1 Entered Freerun Mode IRQ Enable (PLL1 Group). Program Logic 1 to allow a DPLL1 entered freerun mode event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	5	DPLL1 entered holdover mode IRQ enable		DPLL1 Entered Holdover Mode IRQ Enable (PLL1 Group). Program Logic 1 to allow a DPLL1 entered holdover mode event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	4	DPLL1 hitless mode entered IRQ enable		DPLL1 Hitless Mode Entered IRQ Enable (PLL1 Group). Program Logic 1 to allow a DPLL1 entered hitless mode event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	3	DPLL1 hitless mode exited IRQ enable		DPLL1 Hitless Mode Exited IRQ Enable (PLL1 Group). Program Logic 1 to allow a DPLL1 exited hitless mode event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	2	DPLL1 holdover FTW history updated IRQ enable		DPLL1 Holdover FTW History Updated IRQ Enable (PLL1 Group). Program Logic 1 to allow a DPLL1 holdover frequency tuning word history updated event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	1	Reserved		Reserved.	0	R/W	Core clock	No
	0	DPLL1 phase step detected IRQ enable		DPLL1 Phase Step Detected IRQ Enable (PLL1 Group). Program Logic 1 to allow a DPLL1 reference input phase step detected event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
0x0118	[7:5]	Reserved		Reserved.	0x0	R/W	Core clock	No
	4	DPLL1 N divider resynchronized IRQ enable		DPLL1 N Divider Resynchronized IRQ Enable (PLL1 Group). Program Logic 1 to allow a DPLL1 feedback divider resynchronized event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	3	DPLL1 fast acquisition completed IRQ enable		DPLL1 Fast Acquisition Completed IRQ Enable (PLL1 Group). Program Logic 1 to allow a DPLL1 completed a fast acquisition sequence event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	2	DPLL1 fast acquisition started IRQ enable		DPLL1 Fast Acquisition Started IRQ Enable (PLL1 Group). Program Logic 1 to allow a DPLL1 started a fast acquisition sequence event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	[1:0]	Reserved		Reserved.	0x0	R/W	Core clock	No
0x0119	[7:6]	Reserved		Reserved.	0x0	R/W	Core clock	No
	5	DPLL1 Translation Profile 1.5 activated IRQ enable		DPLL1 Translation Profile 1.5 Activated IRQ Enable (PLL1 Group). Program Logic 1 to allow a DPLL1 Translation Profile 1.5 activated event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	4	DPLL1 Translation Profile 1.4 activated IRQ enable		DPLL1 Translation Profile 1.4 Activated IRQ Enable (PLL1 Group). Program Logic 1 to allow a DPLL1 Translation Profile 1.4 activated event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	3	DPLL1 Translation Profile 1.3 activated IRQ enable		DPLL1 Translation Profile 1.3 Activated IRQ Enable (PLL1 Group). Program Logic 1 to allow a DPLL1 Translation Profile 1.3 activated event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	2	DPLL1 Translation Profile 1.2 activated IRQ enable		DPLL1 Translation Profile 1.2 Activated IRQ Enable (PLL1 Group). Program Logic 1 to allow a DPLL1 Translation Profile 1.2 activated event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	1	DPLL1 Translation Profile 1.1 activated IRQ enable		DPLL1 Translation Profile 1.1 Activated IRQ Enable (PLL1 Group). Program Logic 1 to allow a DPLL1 Translation Profile 1.1 activated event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	0	DPLL1 Translation Profile 1.0 activated IRQ enable		DPLL1 Translation Profile 1.0 Activated IRQ Enable (PLL1 Group). Program Logic 1 to allow a DPLL1 Translation Profile 1.0 activated event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
0x011A	[7:5]	Reserved		Reserved.	0x0	R/W	Core clock	No
	4	PLL1 clock outputs synchronized IRQ enable		PLL1 Clock Outputs Synchronized IRQ Enable (PLL1 Group). Program Logic 1 to allow a PLL1 clock distribution outputs synchronized event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	3	APLL1 phase unlocked IRQ enable		APLL1 Phase Unlocked IRQ Enable (PLL1 Group). Program Logic 1 to allow an APLL1 phase lock to unlock transition event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	2	APLL1 phase-locked IRQ enable		APLL1 Phase-Locked IRQ Enable (PLL1 Group). Program Logic 1 to allow an APLL1 phase unlock to lock transition event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	1	APLL1 calibration completed IRQ enable		APLL1 Calibration Completed IRQ Enable (PLL1 Group). Program Logic 1 to allow an APLL1 calibration completed event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	0	APLL1 calibration started IRQ enable		APLL1 Calibration Started IRQ Enable (PLL1 Group). Program Logic 1 to allow an APLL1 calibration started event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
0x011B	7	Auxiliary REF1 R divider resynchronization IRQ enable		Auxiliary REF1 Divider Resynchronization IRQ Enable (Common Group). Program Logic 1 to allow an auxiliary REF1 reference divider was resynchronized event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	6	Auxiliary REF1 valid IRQ enable		Auxiliary REF1 Validated IRQ Enable (Common Group). Program Logic 1 to allow an Auxiliary REF1 reference monitor validated event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	5	Auxiliary REF1 unfault IRQ enable		Auxiliary REF1 Unfaulted IRQ Enable (Common Group). Program Logic 1 to allow an auxiliary REF1 reference monitor unfaulted event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	4	Auxiliary REF1 fault IRQ enable		Auxiliary REF1 Faulted IRQ Enable (Common Group). Program Logic 1 to allow an auxiliary REF1 reference monitor faulted event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	3	Auxiliary REF0 R divider resynchronization IRQ enable		Auxiliary REF0 Divider Resynchronization IRQ Enable (Common Group). Program Logic 1 to allow an auxiliary REF0 reference divider was resynchronized event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	2	Auxiliary REF0 valid IRQ enable		Auxiliary REF0 Validated IRQ Enable (Common Group). Program Logic 1 to allow an Auxiliary REF0 reference monitor validated event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	1	Auxiliary REF0 unfault IRQ enable		Auxiliary REF0 Unfaulted IRQ Enable (Common Group). Program Logic 1 to allow an Auxiliary REF0 reference monitor unfaulted event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	0	Auxiliary REF0 fault IRQ enable		Auxiliary REF0 Faulted IRQ Enable (Common Group). Program Logic 1 to allow an Auxiliary REF0 reference monitor faulted event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
0x011C	7	Auxiliary REF3 R divider resynchronization IRQ enable		Auxiliary REF3 Divider Resynchronization IRQ Enable (Common Group). Program Logic 1 to allow an Auxiliary REF3 reference divider was resynchronized event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	6	Auxiliary REF3 valid IRQ enable		Auxiliary REF3 Validated IRQ Enable (Common Group). Program Logic 1 to allow an Auxiliary REF3 reference monitor validated event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	5	Auxiliary REF3 unfault IRQ enable		Auxiliary REF3 Unfaulted IRQ Enable (Common Group). Program Logic 1 to allow an Auxiliary REF3 reference monitor unfaulted event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	4	Auxiliary REF3 fault IRQ enable		Auxiliary REF3 Faulted IRQ Enable (Common Group). Program Logic 1 to allow an Auxiliary REF3 reference monitor faulted event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	3	Auxiliary REF2 R divider resynchronization IRQ enable		Auxiliary REF2 Divider Resynchronization IRQ Enable (Common Group). Program Logic 1 to allow an Auxiliary REF2 reference divider was resynchronized event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	2	Auxiliary REF2 valid IRQ enable		Auxiliary REF2 Validated IRQ Enable (Common Group). Program Logic 1 to allow an Auxiliary REF2 reference monitor validated event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	1	Auxiliary REF2 unfault IRQ enable		Auxiliary REF2 Unfaulted IRQ Enable (Common Group). Program Logic 1 to allow an Auxiliary REF2 reference monitor unfaulted event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	0	Auxiliary REF2 fault IRQ enable		Auxiliary REF2 Faulted IRQ Enable (Common Group). Program Logic 1 to allow an Auxiliary REF2 reference monitor faulted event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x011D	7	UTS FIFO overflowed IRQ enable		UTS FIFO Overflowed IRQ Enable (Common Group). Program Logic 1 to allow a user time stamper FIFO overflowed (data lost) event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	6	UTS FIFO new sample arrived IRQ enable		UTS FIFO New Sample Arrived IRQ Enable (Common Group). Program Logic 1 to allow a user time stamper FIFO received a sample from a UTS event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	5	UTS FIFO became not empty IRQ enable		UTS FIFO Became Not empty IRQ Enable (Common Group). Program Logic 1 to allow a User Time Stamper FIFO transitioned from empty to not empty event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	4	Common clock DPLL switched to holdover IRQ enable		Common Clock DPLL (CCPDLL) Switched to Holdover IRQ Enable (Common Group). Program Logic 1 to allow the common clock DPLL switched to holdover (no reference available) event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	3	Common clock DPLL selected secondary reference IRQ enable		Common Clock DPLL Selected Secondary Reference IRQ Enable (Common Group). Program Logic 1 to allow the common clock DPLL selected CCR1 event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	2	Common clock DPLL selected primary reference IRQ enable		Common Clock DPLL Selected Primary Reference IRQ Enable (Common Group). Program Logic 1 to allow the common clock DPLL selected CCR0 event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	1	Common clock DPLL unlock IRQ enable		Common Clock DPLL Unlocked IRQ Enable (Common Group). Program Logic 1 to allow the common clock DPLL phase unlocked event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	0	Common clock DPLL lock IRQ enable		Common Clock DPLL Locked IRQ Enable (Common Group). Program Logic 1 to allow the common clock DPLL phase locked event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
0x011E	7	Common clock DPLL secondary reference invalid IRQ enable		Common Clock DPLL Secondary Reference Invalidated IRQ Enable (Common Group). Program Logic 1 to allow a common clock DPLL CCR1 reference monitor invalidated event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	6	Common clock DPLL secondary reference valid IRQ enable		Common Clock DPLL Secondary Reference Validated IRQ Enable (Common Group). Program Logic 1 to allow a common clock DPLL CCR1 reference monitor validated event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	5	Common clock DPLL primary reference invalid IRQ enable		Common Clock DPLL Primary Reference Invalidated IRQ Enable (Common Group). Program Logic 1 to allow a common clock DPLL CCR0 reference monitor invalidated event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	4	Common clock DPLL primary reference valid IRQ enable		Common Clock DPLL Primary Reference Validated IRQ Enable (Common Group). Program Logic 1 to allow a common clock DPLL CCR0 reference monitor validated event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	3	CCS slew limiter stopped slewing IRQ enable		Common Clock Synchronizer Slew Limiter Stopped Slewing IRQ Enable (Common Group). Program Logic 1 to allow a CCS slew limiter stopped slewing event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	2	CCS slew limiter started slewing IRQ enable		Common Clock Synchronizer Slew Limiter Started Slewing IRQ Enable (Common Group). Program Logic 1 to allow a CCS slew limiter started slewing event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	1	CCS synchronization guard activated IRQ enable		Common Clock Synchronizer Synchronization Guard Activated IRQ Enable (Common Group). Program Logic 1 to allow a CCS synchronization guard was activated event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	0	CCS ready IRQ enable		Common Clock Synchronizer Ready IRQ Enable (Common Group). Program Logic 1 to allow a CCS is ready to support digitized clocking resources event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
0x011F	[7:4]	Reserved		Reserved.	0x0	R/W	Core clock	No
	3	IUTS 1 Invalid IRQ Enable		IUTS 1 Became Invalid IRQ Enable (Common Group). Program Logic 1 to allow an IUTS 1 became invalid event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	2	IUTS 1 Valid IRQ Enable		IUTS 1 Became Valid IRQ Enable (Common Group). Program Logic 1 to allow an IUTS 1 became valid event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	1	IUTS 0 Invalid IRQ Enable		IUTS 0 Became Invalid IRQ Enable (Common Group). Program Logic 1 to allow an IUTS 0 became invalid event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No
	0	IUTS 0 Valid IRQ Enable		IUTS 0 Became Valid IRQ Enable (Common Group). Program Logic 1 to allow an IUTS 0 became valid event to appear as an IRQ. Logic 0 (default) prevents this event from appearing as an IRQ.	0	R/W	Core clock	No

M0 PIN FUNCTION—REGISTER 0x0182

The control (status) function details apply when the M0 pin is configured as a control (status) pin. To configure the M0 pin for control or status, see the Mx Pin Status or Control Select—Register 0x0102 to Register 0x0108 section. The M0 pin default condition is as a control input with a function value of 0x00 (no function = high impedance input).

Table 9. M0 Pin Function Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0182	[7:0]	M0 control function		M0 Pin Function Input. These bits determine the control function of the M0 pin. The M0 pin default condition is as a control input with a function value of 0x00 (no function = high impedance input).	0x00	R/W	Serial port clock	No
			0x0	No function.				
			0x1	IO update. Control bit proxy: Register 0x000F, Bit 0.				
			0x2	Full power-down. Control bit proxy: Register 0x2000, Bit 0.				
			0x3	Clear watchdog timer. Control bit proxy: Register 0x2005, Bit 7.				
			0x4	Synchronize all distribution dividers. Control bit proxy: Register 0x2000, Bit 3.				
			0x10	IRQ: clear all. Control bit proxy: Register 0x2005, Bit 0.				
			0x11	IRQ: clear common group. Control bit proxy: Register 0x2005, Bit 1.				
			0x12	IRQ: clear PLL0 group. Control bit proxy: Register 0x2005, Bit 2.				
			0x13	IRQ: clear PLL1 group. Control bit proxy: Register 0x2005, Bit 3.				
			0x20	REFA: force invalid. Control bit proxy: Register 0x2003, Bit 0.				
			0x21	REFAA: force invalid. Control bit proxy: Register 0x2003, Bit 1.				
			0x22	REFB: force invalid. Control bit proxy: Register 0x2003, Bit 2.				
			0x23	REFBB: force invalid. Control bit proxy: Register 0x2003, Bit 3.				
			0x24	Auxiliary REF0: force invalid. Control bit proxy: Register 0x2003, Bit 4.				
			0x25	Auxiliary REF1: force invalid. Control bit proxy: Register 0x2003, Bit 5.				
			0x26	Auxiliary REF2: force invalid. Control bit proxy: Register 0x2003, Bit 6.				
			0x27	Auxiliary REF3: force invalid. Control bit proxy: Register 0x2003, Bit 7.				
			0x28	REFA: force validation timeout. Control bit proxy: Register 0x2002, Bit 0.				
			0x29	REFAA: force validation timeout. Control bit proxy: Register 0x2002, Bit 1.				
			0x2A	REFB: force validation timeout. Control bit proxy: Register 0x2002, Bit 2.				
			0x2B	REFBB: force validation timeout. Control bit proxy: Register 0x2002, Bit 3.				
			0x2C	Auxiliary REF0: force validation timeout. Control bit proxy: Register 0x2002, Bit 4.				
			0x2D	Auxiliary REF1: force validation timeout. Control bit proxy: Register 0x2002, Bit 5.				
			0x2E	Auxiliary REF2: force validation timeout. Control bit proxy: Register 0x2002, Bit 6.				
			0x2F	Auxiliary REF3: force validation timeout. Control bit proxy: Register 0x2002, Bit 7.				
			0x30	M0 connects to the input of Auxiliary REF0.				
			0x31	M0 connects to the input of Auxiliary REF1.				
			0x33	M0 connects to the input of Auxiliary REF2.				
			0x34	M0 connects to the input of Auxiliary REF3.				
			0x40	Channel 0: power-down. Control bit proxy: Register 0x2100, Bit 0.				
			0x41	DPLL0: force freerun mode. Control bit proxy: Register 0x2105, Bit 0.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
			0x42	DPLL0: force holdover mode. Control bit proxy: Register 0x2105, Bit 1.				
			0x43	DPLL0: clear tuning word history. Control bit proxy: Register 0x2107, Bit 1.				
			0x44	Channel 0: synchronize distribution dividers. Control bit proxy: Register 0x2101, Bit 3.				
			0x45	DPLL0: translation profile select (Bit 0 of Bits[2:0]). Control bit proxy: Register 0x2105, Bit 4.				
			0x46	DPLL0: translation profile select (Bit 1 of Bits[2:0]). Control bit proxy: Register 0x2105, Bit 5.				
			0x47	DPLL0: translation profile select (Bit 2 of Bits[2:0]). Control bit proxy: Register 0x2105, Bit 6.				
			0x50	OUT0AP: mute. Control bit proxy: Register 0x2102, Bit 2.				
			0x51	OUT0AN: mute. Control bit proxy: Register 0x2102, Bit 3.				
			0x52	OUT0AP/OUT0AN: reset. Control bit proxy: Register 0x2102, Bit 5.				
			0x53	OUT0BP: mute. Control bit proxy: Register 0x2103, Bit 2.				
			0x54	OUT0BN: mute. Control bit proxy: Register 0x2103, Bit 3.				
			0x55	OUT0BP/OUT0BN: reset. Control bit proxy: Register 0x2103, Bit 5.				
			0x56	OUT0CP: mute. Control bit proxy: Register 0x2104, Bit 2.				
			0x57	OUT0CN: mute. Control bit proxy: Register 0x2104, Bit 3.				
			0x58	OUT0CP/OUT0CN: reset. Control bit proxy: Register 0x2104, Bit 5.				
			0x59	Channel 0: mute all drivers. Control bit proxy: Register 0x2101, Bit 1.				
			0x5A	Channel 0: reset all drivers. Control bit proxy: Register 0x2101, Bit 2.				
			0x5B	Channel 0: JESD204B N shot request. Control bit proxy: Register 0x2101, Bit 0.				
			0x60	Channel 1: power-down. Control bit proxy: Register 0x2200, Bit 0.				
			0x61	DPLL1: force freerun mode. Control bit proxy: Register 0x2205, Bit 0.				
			0x62	DPLL1: force holdover mode. Control bit proxy: Register 0x2205, Bit 1.				
			0x63	DPLL1: clear tuning word history. Control bit proxy: Register 0x2207, Bit 1.				
			0x64	Channel 1: synchronize distribution dividers. Control bit proxy: Register 0x2201, Bit 3.				
			0x65	DPLL1: translation profile select (Bit 0 of Bits[2:0]). Control bit proxy: Register 0x2205, Bit 4.				
			0x66	DPLL1: translation profile select (Bit 1 of Bits[2:0]). Control bit proxy: Register 0x2205, Bit 5.				
			0x67	DPLL1: translation profile select (Bit 2 of Bits[2:0]). Control bit proxy: Register 0x2205, Bit 6.				
			0x70	OUT1AP: mute. Control bit proxy: Register 0x2202, Bit 2.				
			0x71	OUT1AN: mute. Control bit proxy: Register 0x2202, Bit 3.				
			0x72	OUT1APN: reset. Control bit proxy: Register 0x2202, Bit 5.				
			0x73	OUT1BP: mute. Control bit proxy: Register 0x2203, Bit 2.				
			0x74	OUT1BN: mute. Control bit proxy: Register 0x2203, Bit 3.				
			0x75	OUT1BPN: reset. Control bit proxy: Register 0x2203, Bit 5.				
			0x79	Channel 1: mute all drivers. Control bit proxy: Register 0x2201, Bit 1.				
			0x7A	Channel 1: reset all drivers. Control bit proxy: Register 0x2201, Bit 2.				
			0x78	Channel 1: JESD204B N shot request. Control bit proxy: Register 0x2201, Bit 0				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[7:0]	M0 status function		M0 Pin Status Output. These bits determine the status function of the M0 pin. The M0 pin default condition is as a control input with a function value of 0x00 (no function = high impedance input).	0x00	R/W	Serial port clock	No
			0x0	Static Logic 0.				
			0x1	Static Logic 1.				
			0x2	Core clock (system clock PLL VCO frequency divided by 96).				
			0x3	Watchdog timer output. A strobe pulse of approximately 40 ns duration when the watchdog timer expires.				
			0x4	System clock PLL calibration in progress. Status bit proxy: Register 0x3001, Bit 2.				
			0x5	System clock PLL lock detect. Status bit proxy: Register 0x3001, Bit 0.				
			0x6	System clock PLL stable. Status bit proxy: Register 0x3001, Bit 1.				
			0x7	All PLLs locked. Status bit proxy: Logical AND of Register 0x3001, Bits[5:4] and Bit 1.				
			0x8	Channel 0 PLLs locked. Status bit proxy: Register 0x3001, Bit 4.				
			0x9	Channel 1 PLLs locked. Status bit proxy: Register 0x3001, Bit 5.				
			0xA	EEPROM upload (write to EEPROM) in progress. Status bit proxy: Register 0x3000, Bit 0.				
			0xB	EEPROM download (read from EEPROM) in progress. Status bit proxy: Register 0x3000, Bit 1.				
			0xC	EEPROM general fault detected. Status bit proxy: Register 0x3000, Bit 2.				
			0xD	Temperature sensor limit alarm. Status bit proxy: Register 0x3002, Bit 0.				
			0x10	IRQ: any. Logical OR of IRQs associated with IRQ status bits in Register 0x300B to Register 301E.				
			0x11	IRQ: common group. Logical OR of IRQs associated with IRQ status bits in Register 0x300B to Register 0x300F and Register 0x301A to Register 0x301E.				
			0x12	IRQ: PLL0 group. Logical OR of IRQs associated with IRQ status bits in Register 0x3010 to Register 0x3014.				
			0x13	IRQ: PLL1 group. Logical OR of IRQs associated with IRQ status bits in Register 0x3015 to Register 0x3019.				
			0x14	REFA: demodulated clock.				
			0x16	REFAA: demodulated clock.				
			0x18	REFB: demodulated clock.				
			0x1A	REFBB: demodulated clock.				
			0x1C	REFA: resynchronization event occurred (associated with IRQ status bit Register 0x300D, Bit 3).				
			0x1D	REFAA: resynchronization event occurred (associated with IRQ status bit Register 0x300D, Bit 7).				
			0x1E	REFB: resynchronization event occurred (associated with IRQ status bit Register 0x300E, Bit 3).				
			0x1F	REFBB: resynchronization event occurred (associated with IRQ status bit Register 0x300E, Bit 7).				
			0x20	REFA: faulted. Status bit proxy: Register 0x3005, Bit 3.				
			0x21	REFAA: faulted. Status bit proxy: Register 0x3006, Bit 3.				
			0x22	REFB: faulted. Status bit proxy: Register 0x3007, Bit 3.				
			0x23	REFBB: faulted. Status bit proxy: Register 0x3008, Bit 3.				
			0x24	REFA: valid. Status bit proxy: Register 0x3005, Bit 4.				
			0x25	REFAA: valid. Status bit proxy: Register 0x3006, Bit 4.				
			0x26	REFB: valid. Status bit proxy: Register 0x3007, Bit 4.				
			0x27	REFBB: valid. Status bit proxy: Register 0x3008, Bit 4.				
			0x28	REFA: active. REFA is the input source to a DPLL per an active translation profile.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
			0x29	REFAA: active. REFAA is the input source to a DPLL per an active translation profile.				
			0x2A	REFB: active. REFB is the input source to a DPLL per an active translation profile.				
			0x2B	REFBB: active. REFBB is the input source to a DPLL per an active translation profile.				
			0x2C	Auxiliary NCO 0: active. Auxiliary NCO 0 is the input source to a DPLL per an active translation profile.				
			0x2D	Auxiliary NCO 1: active. Auxiliary NCO 1 is the input source to a DPLL per an active translation profile.				
			0x2E	DPLL0: feedback time to digital converter (TDC) active. Indicates that the feedback TDC for DPLL0 is in use as a time stamp source to DPLL1 when operating in cascaded DPLL mode.				
			0x2F	DPLL1: feedback TDC active. Indicates that the feedback TDC for DPLL1 is in use as a time stamp source to DPLL0 when operating in cascaded DPLL mode.				
			0x30	DPLL0: phase locked. Status bit proxy: Register 0x3100, Bit 1.				
			0x31	DPLL0: frequency locked. Status bit proxy: Register 0x3100, Bit 2.				
			0x32	APLL0: locked. Status bit proxy: Register 0x3100, Bit 3.				
			0x33	APLL0: calibration in progress. Status bit proxy: Register 0x3100, Bit 4.				
			0x34	DPLL0: actively tracking a reference input. Status bit proxy: Register 0x3101, Bit 3.				
			0x35	DPLL0: freerun mode active. Status bit proxy: Register 0x3101, Bit 0.				
			0x36	DPLL0: holdover mode active. Status bit proxy: Register 0x3101, Bit 1.				
			0x37	DPLL0: switching reference inputs. Status bit proxy: Register 0x3101, Bit 2.				
			0x38	DPLL0: frequency tuning word history available. Status bit proxy: Register 0x3102, Bit 0.				
			0x39	DPLL0: frequency tuning word history updated. (associated with IRQ status bit Register 0x3011, Bit 2).				
			0x3A	DPLL0: frequency clamp is active. Status bit proxy: Register 0x3102, Bit 1.				
			0x3B	DPLL0: phase slew limiter is active. Status bit proxy: Register 0x3102, Bit 2.				
			0x3C	Channel 0: output distribution synchronization event (associated with IRQ status bit Register 0x3014, Bit 4).				
			0x3E	DPLL0: phase step detected. (associated with IRQ status bit Register 0x3011, Bit 0).				
			0x3F	DPLL0: fast acquisition active. Status bit proxy: Register 0x3102, Bit 4.				
			0x40	DPLL0: fast acquisition complete. Status bit proxy: Register 0x3102, Bit 5.				
			0x41	DPLL0: N divider resynchronization (associated with IRQ status bit, Register 0x3012, Bit 4)				
			0x42	Channel 0: distribution phase slew active. Status bit proxy: Logical OR of Register 0x310D, Bits[5:0].				
			0x43	Channel 0: distribution invalid phase offset value. Status bit proxy: Logical OR of Register 0x310E, Bits[5:0].				
			0x50	DPLL1: phase locked. Status bit proxy: Register 0x3200, Bit 1.				
			0x51	DPLL1: frequency locked. Status bit proxy: Register 0x3200, Bit 2.				
			0x52	APLL1: locked. Status bit proxy: Register 0x3200, Bit 3.				
			0x53	APLL1: calibration in progress. Status bit proxy: Register 0x3200, Bit 4.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
			0x54	DPLL1: actively tracking a reference input. Status bit proxy: Register 0x3201, Bit 3.				
			0x55	DPLL1: freerun mode active. Status bit proxy: Register 0x3201, Bit 0.				
			0x56	DPLL1: holdover mode active. Status bit proxy: Register 0x3201, Bit 1.				
			0x57	DPLL1: Switching reference inputs. Status bit proxy: Register 0x3201, Bit 2.				
			0x58	DPLL1: frequency tuning word history available. Status bit proxy: Register 0x3202, Bit 0.				
			0x59	DPLL1: frequency tuning word history updated (associated with IRQ status bit Register 0x3016, Bit 2).				
			0x5A	DPLL1: frequency clamp is active. Status bit proxy: Register 0x3202, Bit 1.				
			0x5B	DPLL1: phase slew limiter is active. Status bit proxy: Register 0x3202, Bit 2.				
			0x5C	Channel 1: output distribution synchronization event (associated with IRQ status bit Register 0x3019, Bit 4).				
			0x5E	DPLL1: phase step detected (associated with IRQ status bit Register 0x3016, Bit 0).				
			0x5F	DPLL: fast acquisition active. Status bit proxy: Register 0x3202, Bit 4.				
			0x60	DPLL1: fast acquisition complete. Status bit proxy: Register 0x3202, Bit 5.				
			0x61	DPLL1: N divider resynchronization (associated with IRQ status bit Register 0x3017, Bit 4).				
			0x62	Channel 1: distribution phase slew active. Status bit proxy: Logical OR of Register 0x320D, Bits[3:0].				
			0x63	Channel 1: distribution invalid phase offset value. Status bit proxy: Logical OR of Register 0x320E, Bits[3:0].				
			0x70	Auxiliary NCO 0: untagged output. Periodic pulses occurring at the user programmed frequency of Auxiliary NCO 0 (coincident with the accumulator rollover).				
			0x71	Auxiliary NCO 0: tagged output. Periodic pulses occurring at the user programmed tagged frequency of Auxiliary NCO 0 (coincident with the accumulator rollover).				
			0x72	Auxiliary NCO 1: untagged output. Periodic pulses occurring at the user programmed frequency of Auxiliary NCO 1 (coincident with the accumulator rollover).				
			0x73	Auxiliary NCO 1: tagged output. Periodic pulses occurring at the user programmed tagged frequency of Auxiliary NCO 1 (coincident with the accumulator rollover).				
			0x74	Auxiliary DPLL: locked. Status bit proxy: Register 0x3002, Bit 1.				
			0x75	Auxiliary DPLL: reference fault. Status bit proxy: Register 0x3002, Bit 2.				
			0x78	UTSP0: User Time Stamp Processor 0 time code available (associated with IRQ status bit, Register 0x300F, Bit 2).				
			0x79	UTSP1: User Time Stamp Processor 1 time code available (associated with IRQ status bit, Register 0x300F, Bit 3).				
			0x7A	Time skew measurement processor: Skew measurement updated (associated with IRQ status bit, Register 0x300F, Bit 4).				
			0x80	Auxiliary DPLL: reference source fault. Alternatively indicates a primary reference (CCR0) source fault for the common clock DPLL. Status bit proxy: Register 0x3002, Bit 2.				
			0x81	Common clock DPLL: secondary reference (CCR1) source fault. Status bit proxy: Logical NOT of Register 0x3002, Bit 2.				
			0x82	Common clock DPLL: primary reference (CCR0) source valid. Status bit proxy: Register 0x0D40, Bit 4.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
			0x83	Common clock DPLL: primary reference (CCR1) source valid. Status bit proxy: Register 0x0D40, Bit 5.				
			0x84	Common clock DPLL: actively tracking a reference input. Status bit proxy: Register 0x0D40, Bit 0.				
			0x85	Common clock DPLL: Currently selected source. M0 = 0 indicates the common clock digital phase-locked loop (CCDPLL) is using CCR0 as its reference source. M0 = 1 indicates the CCDPLL is using CCR1 as its reference source.				
			0x86	Common clock synchronizer: ready for use. The CCS received an initial valid synchronization event. Status bit proxy: Register 0x0D40, Bit 2.				
			0x94	Auxiliary REF0: demodulated clock.				
			0x96	Auxiliary REF1: demodulated clock.				
			0x98	Auxiliary REF2: demodulated clock.				
			0x9A	Auxiliary REF3: demodulated clock.				
			0x9C	Auxiliary REF0: resynchronization event occurred (associated with IRQ status bit, Register 0x301A, Bit 3).				
			0x9D	Auxiliary REF1: Resynchronization event occurred (associated with IRQ status bit, Register 0x301A, Bit 7).				
			0x9E	Auxiliary REF2: resynchronization event occurred (associated with IRQ status bit, Register 0x301B, Bit 3).				
			0x9F	Auxiliary REF3: resynchronization event occurred (associated with IRQ status bit, Register 0x301B, Bit 7).				
			0xA0	Auxiliary REF0: faulted. Status bit proxy: Register 0x301F, Bit 3.				
			0xA1	Auxiliary REF1: faulted. Status bit proxy: Register 0x3020, Bit 3.				
			0xA2	Auxiliary REF2: faulted. Status bit proxy: Register 0x3021, Bit 3.				
			0xA3	Auxiliary REF3: faulted. Status bit proxy: Register 0x3022, Bit 3.				
			0xA4	Auxiliary REF0: valid. Status bit proxy: Register 0x301F, Bit 4.				
			0xA5	Auxiliary REF1: valid. Status bit proxy: Register 0x3020, Bit 4.				
			0xA6	Auxiliary REF2: valid. Status bit proxy: Register 0x3021, Bit 4.				
			0xA7	Auxiliary REF3: valid. Status bit proxy: Register 0x3022, Bit 4.				
			0xA8	Auxiliary REF0: active. Auxiliary REF0 is the input source to a DPLL per an active translation profile.				
			0xA9	Auxiliary REF1: Active. Auxiliary REF1 is the input source to a DPLL per an active translation profile.				
			0xAA	Auxiliary REF2: Active. Auxiliary REF2 is the input source to a DPLL per an active translation profile.				
			0xAB	Auxiliary REF3: active. Auxiliary REF3 is the input source to a DPLL per an active translation profile.				
			0xAC	IUTS 0: active. IUTS 0 is the input source to a DPLL per an active translation profile.				
			0xAD	IUTS 1: active. IUTS 1 is the input source to a DPLL per an active translation profile.				
			0xB0	CCS: slewing status. Status bit proxy: Register 0x0D40, Bit 6.				
			0xB1	CCS: synchronization error. Status bit proxy: Register 0x0D40, Bit 7.				
			0xB8	IUTS 0: valid. The absence of these conditions: user declared invalidation; CCDPLL unlocked (assuming bypass lock option inactive); input time code with a restart; input time code while the IUTS is busy; and IUTS period monitor detected a period discontinuity. Status bit proxy: Register 0x3023, Bit 0.				
			0xB9	IUTS 1: valid. The absence of these conditions: user declared invalidation; CCDPLL unlocked (assuming bypass lock option inactive); input time code with a restart; input time code while the IUTS is busy; IUTS period monitor detected a period discontinuity. Status bit proxy: Register 0x3023, Bit 1.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
			0xC0	UTS FIFO: overfill status. Status bit proxy: Register 0x0E2D, Bit 7.				
			0xC1	UTS FIFO: not empty status. Logic 1 when Register 0x0E2D, Bits[6:0] > 0.				
			0xC2	UTS FIFO: update. A pulse generated when the UTS FIFO receives a new time stamp sample from one of the UTSs.				

M1 TO CSB/M6 PIN FUNCTIONS—REGISTER 0x0183 TO REGISTER 0x0188

To configure an Mx pin for control or status, see the Mx Pin Status or Control Select—Register 0x0102 to Register 0x0108 section. The default condition for an Mx pin is as a control input with a function value of 0x00 (no function = high impedance input).

Table 10. M1 Pin to CSB/M6 Pin Function Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0183	[7:0]	M1 control function		The control and status functions of the M1 pin are identical to the control and status functions of the M0 pin.	0x00	R/W	Serial port clock	No
0x0184	[7:0]	M2 control function		The control and status functions of the M2 pin are identical to the control and status functions of the M0 pin.	0x00	R/W	Serial port clock	No
0x0185	[7:0]	M3 control function		The control and status functions of the M3 pin are identical to the control and status functions of the M0 pin.	0x00	R/W	Serial port clock	No
0x0186	[7:0]	M4 control function		The control and status functions of the M4 pin are identical to the control and status functions of the M0 pin.	0x00	R/W	Serial port clock	No
0x0187	[7:0]	M5 control function		The control and status functions of the SDO/M5 pin are identical to the control and status functions of the M0 pin.	0x00	R/W	Serial port clock	No
0x0188	[7:0]	M6 control function		The control and status functions of the CSB/M6 pin are identical to the control and status functions of the M0 pin.	0x00	R/W	Serial port clock	No

SYSTEM CLOCK PLL—REGISTER 0x0200 TO REGISTER 0x0209

Table 11. System Clock PLL Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0200	[7:0]	Feedback divide ratio		PLL Multiplication Ratio. This 8-bit unsigned value, K (default = 0), is the value of the system clock PLL feedback divide ratio. For example, K = 100 equates to divide by 100. The valid range of K is 4 to 255. Because the default is K = 0, the user must program a valid K value.	0x00	R/W	Serial port clock	No
0x0201	[7:4]	Reserved		Reserved.	0x0	R/W	Serial port clock	No
	3	SYSCLK input path select		System Clock PLL Input Path Select. This bit selects between the direct (default) and the crystal resonator input paths to the system clock PLL.	0	R/W	Serial port clock	No
			0	Direct path (default). The XOA and XOB pins are inputs to a differential receiver.				
			1	Crystal resonator path. The XOA and XOB pins are the input and output, respectively, of a maintaining amplifier for use with a crystal resonator.				
	[2:1]	SYSCLK input divide ratio		System Clock Prescaler Ratio. This 2-bit value (default = 0) selects a prescale divide of the system clock input frequency (that is, prior to the input of the system clock PLL).	0x0	R/W	Serial port clock	No
			0	Divide by 1 (default).				
			1	Divide by 2.				
			2	Divide by 4.				
			3	Divide by 8.				
	0	Enable SYSCLK doubler		Frequency Doubler Enable. Use only in conjunction with a crystal resonator as the system clock source.	0	R/W	Serial port clock	No
			0	Disabled (default).				
			1	Enabled.				
0x0202	[7:0]	SYSCLK Reference Frequency[7:0]		System Clock Reference Frequency. This 40-bit unsigned integer, FSYS, in units of millihertz (default = 0), is the declaration by the user of the system clock frequency, f_{OSC}, applied to the XOA and XOB pins. FSYS relates to f_{OSC} as follows: $FSYS = f_{OSC} \times 10^3$ For example, given f_{OSC} = 52 MHz, then FSYS = 52,000,000,000 (0x0C 1B71 0800).	0x00	R/W	Serial port clock	No
0x0203	[7:0]	SYSCLK Reference Frequency[15:8]		Continuation of the SYSCLK reference frequency bit field. See the SYSCLK Reference Frequency[7:0] description.	0x00	R/W	Serial port clock	No
0x0204	[7:0]	SYSCLK Reference Frequency[23:16]		Continuation of the SYSCLK reference frequency bit field. See the SYSCLK Reference Frequency[7:0] description.	0x00	R/W	Serial port clock	No
0x0205	[7:0]	SYSCLK Reference Frequency[31:24]		Continuation of the SYSCLK reference frequency bit field. See the SYSCLK Reference Frequency[7:0] description.	0x00	R/W	Serial port clock	No
0x0206	[7:0]	SYSCLK Reference Frequency[39:32]		Continuation of the SYSCLK reference frequency bit field. See the SYSCLK Reference Frequency[7:0] description.	0x00	R/W	Serial port clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0207	[7:0]	System Clock Stability Period[7:0]		System Clock Stability Period. This 20-bit unsigned value, ST, in units of milliseconds (default = 0), is a user defined amount of stability timer time, t_{ST}, that the system clock PLL must remain continuously phase locked before indication of system clock stable status (Register 0x3001, Bit 1 = 1). ST relates to t_{ST} as follows: $ST = t_{ST} \times 10^3$ sec For example, given t_{ST} = 0.05 sec (50 ms), ST = 50 (0x32). ST = 0 is a debug setting, because it forces a system clock unstable status (Register 0x3001, Bit 1 = 0) even when the system clock is stable. ST = 1,048,575 (0xF FFFF) is an invalid entry and causes Register 0x3001, Bit 1 to be indeterminate when the system clock PLL is unlocked.	0x00	R/W	Core clock	No
0x0208	[7:0]	System Clock Stability Period[15:8]		Continuation of the system clock stability period bit field. See the System Clock Stability Period[7:0] description.	0x00	R/W	Core clock	No
0x0209	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	[3:0]	System Clock Stability Period[19:16]		Continuation of the system clock stability period bit field. See the System Clock Stability Period[7:0] description.	0x0	R/W	Core clock	No

SYSTEM CLOCK COMPENSATION—REGISTER 0x0280 TO REGISTER 0x029C

The user can apply a combination of Method 1, Method 2, and Method 3 to a given system clock compensation target. For example, programming Register 0x0280, Bits[2:0] = 5 applies Method 1 and Method 3 system clock compensation to the TDCs.

Table 12. System Clock Compensation Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0280	[7:6]	Reserved		Reserved.	0x0	R/W	Core clock	No
	5	Method 2 target auxiliary DPLL		Method 2 target: auxiliary DPLL. Setting this bit invokes Method 2 system clock compensation targeting the auxiliary DPLL or Common Clock DPLL.	0	R/W	Core clock	No
	4	Method 1 target auxiliary DPLL		Method 1 target: auxiliary DPLL. Setting this bit invokes Method 1 system clock compensation targeting the auxiliary DPLL or Common Clock DPLL.	0	R/W	Core clock	No
	3	Reserved		Reserved.	0	R	Live	No
	2	Method 3 target TDCs		Method 3 target: TDCs. Setting this bit invokes Method 3 system clock compensation targeting the REFx and Auxiliary REFx TDCs.	0	R/W	Core clock	No
	1	Method 2 target TDCs		Method 2 target: TDCs. Setting this bit invokes Method 2 system clock compensation targeting the REFx and Auxiliary REFx TDCs.	0	R/W	Core clock	No
	0	Method 1 target TDCs		Method 1 target: TDCs. Setting this bit invokes Method 1 system clock compensation targeting the REFx and Auxiliary REFx TDCs.	0	R/W	Core clock	No
0x0281	7	Reserved		Reserved.	0	R	Live	No
	6	Method 3 target Auxiliary NCO 1		Method 3 target: Auxiliary NCO 1. Setting this bit invokes Method 3 system clock compensation targeting Auxiliary NCO 1.	0	R/W	Core clock	No
	5	Method 2 target Auxiliary NCO 1		Method 2 target: Auxiliary NCO 1. Setting this bit invokes Method 2 system clock compensation targeting Auxiliary NCO 1.	0	R/W	Core clock	No
	4	Method 1 target Auxiliary NCO 1		Method 1 target: Auxiliary NCO 1. Setting this bit invokes Method 1 system clock compensation targeting Auxiliary NCO 1.	0	R/W	Core clock	No
	3	Reserved		Reserved.	0	R	Live	No
	2	Method 3 target Auxiliary NCO 0		Method 3 target: Auxiliary NCO 0. Setting this bit invokes Method 3 system clock compensation targeting Auxiliary NCO 0.	0	R/W	Core clock	No
	1	Method 2 target Auxiliary NCO 0		Method 2 target: Auxiliary NCO 0. Setting this bit invokes Method 2 system clock compensation targeting Auxiliary NCO 0.	0	R/W	Core clock	No
	0	Method 1 target Auxiliary NCO 0		Method 1 target: Auxiliary NCO 0. Setting this bit invokes Method 1 system clock compensation targeting Auxiliary NCO 0.	0	R/W	Core clock	No
0x0282	7	Reserved		Reserved.	0	R	Live	No
	6	Method 3 target DPLL1		Method 3 target: DPLL1. Setting this bit invokes Method 3 system clock compensation targeting DPLL1.	0	R/W	Core clock	No
	5	Method 2 target DPLL1		Method 2 target: DPLL1. Setting this bit invokes Method 2 system clock compensation targeting DPLL1. Requires Register 0x0287, Bit 0 = 0.	0	R/W	Core clock	No
	4	Method 1 target DPLL1		Method 1 target: DPLL1. Setting this bit invokes Method 1 system clock compensation targeting DPLL1.	0	R/W	Core clock	No
	3	Reserved		Reserved.	0	R	Live	No
	2	Method 3 target DPLL0		Method 3 target: DPLL0. Setting this bit invokes Method 3 system clock compensation targeting DPLL0.	0	R/W	Core clock	No
	1	Method 2 target DPLL0		Method 2 target: DPLL0. Setting this bit invokes Method 2 system clock compensation targeting DPLL0. Requires Register 0x0287, Bit 0 = 1.	0	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	0	Method 1 target DPLL0		Method 1 target: DPLL0. Setting this bit invokes Method 1 system clock compensation targeting DPLL0.	0	R/W	Core clock	No
0x0283	[7:3]	Reserved		Reserved.	0x00	R	Live	No
	[2:0]	SYSCLK compensation slew rate limit		System Clock Compensation Slew Rate Limit Control. The system clock compensation system employs a combiner that mixes the compensation coefficients generated by the three compensation methods. The output of the combiner employs a slew rate limiting function that effectively prevents the rate of change of frequency originating with compensation sources from exceeding a preset limit as determined by these three bits.	0x0	R/W	Core clock	No
			0	None (default).				
			1	0.715 ppm/sec.				
			2	1.430 ppm/sec.				
			3	2.860 ppm/sec.				
			4	5.720 ppm/sec.				
			5	11.44 ppm/sec.				
			6	22.88 ppm/sec.				
			7	45.76 ppm/sec.				
0x0284	[7:5]	Reserved		Reserved.	0x0	R/W	Live	No
	[4:0]	Auxiliary DPLL source		Auxiliary DPLL Input Source. System clock compensation Method 3 makes use of the auxiliary DPLL. These five bits select an input time stamp source to the auxiliary DPLL.	0x00	R/W	Core clock	No
			0	REFA.				
			1	REFAA.				
			2	REFB.				
			3	REFBB.				
			6	Auxiliary REF0.				
			7	Auxiliary REF1.				
			11	Auxiliary REF2.				
			12	Auxiliary REF3.				
0x0285	[7:0]	Auxiliary DPLL Loop Filter Bandwidth[7:0]		Auxiliary DPLL Loop Filter Bandwidth. This 16-bit unsigned value, BW in units of 0.1 Hz (default = 0), sets the open-loop bandwidth (BW_{COMP} in Hz) of the auxiliary DPLL loop filter. BW (rounded to the nearest integer) relates to BW_{COMP} as follows: $BW = 10 \times BW_{COMP}$ For example, given BW_{COMP} = 247.6 Hz, then BW = 2476 (0x09AC).	0x00	R/W	Core clock	No
0x0286	[7:0]	Auxiliary DPLL Loop Filter Bandwidth[15:8]		Continuation of the auxiliary DPLL loop filter bandwidth bit field. See the Auxiliary DPLL Loop Filter Bandwidth[7:0] description.	0x00	R/W	Core clock	No
0x0287	[7:1]	Reserved		Reserved.	0x00	R	Live	No
	0	Method 2 DPLL select		Method 2 DPLL Select. This bit selects a DPLL channel for Method 2 system clock compensation.	0	R/W	Core clock	No
			0	DPLL0.				
			1	DPLL1.				
0x0288	[7:3]	Reserved		Reserved.	0x00	R	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[2:0]	Method 1 filter cutoff		Method 1 Filter Cutoff. Method 1 system clock compensation employs a digital low-pass filter at the output of the polynomial coefficient calculator. This 3-bit unsigned value selects the 3 dB cutoff frequency of the filter.	0x0	R/W	Core clock	No
			000	156 Hz (default).				
			001	78 Hz.				
			010	39 Hz.				
			011	20 Hz.				
			100	10 Hz.				
			101	5 Hz.				
			110	2 Hz.				
			111	1 Hz.				
0x0289	[7:0]	Method 1 C_0[7:0]		Method 1 Coefficient 0. This 40-bit signed coefficient value, CV, is a unitless quantity constituting the 0^{th}-order coefficient, C_0, for Method 1 system clock compensation. The value, CV (rounded to the nearest integer), relates to C_0 as follows: $CV = 2^{45}C_0$ For example, given $C_0 = 1.0046936 \times 10^{-3}$, then CV = 35,349,513,305 (0x08 3AFE C459).	0x00	R/W	Core clock	No
0x028A	[7:0]	Method 1 C_0[15:8]		Continuation of the Method 1 C_0 bit field. See the Method 1 C_0[7:0] description.	0x00	R/W	Core clock	No
0x028B	[7:0]	Method 1 C_0[23:16]		Continuation of the Method 1 C_0 bit field. See the Method 1 C_0[7:0] description.	0x00	R/W	Core clock	No
0x028C	[7:0]	Method 1 C_0[31:24]		Continuation of the Method 1 C_0 bit field. See the Method 1 C_0[7:0] description.	0x00	R/W	Core clock	No
0x028D	[7:0]	Method 1 C_0[39:32]		Continuation of the Method 1 C_0 bit field. See the Method 1 C_0[7:0] description.	0x00	R/W	Core clock	No
0x028E	[7:0]	Method 1 C_1 Significand[7:0]		Method 1 Coefficient 1 Significand. Synopsis: Method 1 system clock compensation generates a temperature (T) dependent time correction factor (CF_1) based on a fifth-order polynomial such that $CF_1 = \Sigma(C_x \times T^x)$ (x = 1 to 5). T originates either from the on-board temperature sensor or from Register 0x2901 to Register 0x2900, Bits[15:0]. Each coefficient, C_x, takes the following form: $C_x = C_{x\_S} \times 2^{C_{x\_E}}$ where: C_{x_S} denotes the significand associated with C_x. C_{x_E} denotes the power of 2 exponent associated with C_x. When $C_x = 0$ or $\lvert C_x \rvert < 2^{-128}$, then $C_{x\_E} = 0$ and $C_{x\_S} = 0$. Detail: this 16-bit signed value, C_{1_S} (default = 0), constitutes the significand associated with C_1. C_{1_S} relates to C_1 as follows: $C_{1\_S} = \text{round}(C_1 \times 2^{15 - C_{1\_E}})$ where round(x) means round x to the nearest integer. Example: given $C_1 = -2.8927765 \times 10^{-6}$, then $C_{1\_E} = -18$ (see Register 0x0290), and thus $C_{1\_S} = -24{,}849$ (0x9EEF).	0x00	R/W	Core clock	No
0x028F	[7:0]	Method 1 C_1 Significand[15:8]		Continuation of the Method 1 C_1 significand bit field. See the Method 1 C_1 Significand[7:0] description.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0290	[7:0]	Method 1 C_1 exponent		Method 1 Coefficient 1 Exponent. Synopsis: see Register 0x028E. Detail: this 8-bit signed value, C_{1_E} (default = 0), constitutes the power of 2 exponent associated with C_1. C_{1_E} relates to C_1 as follows: $C_{1\_E} = \text{floor}(\log(\lvert C_1 \rvert)/\log(2)) + 1$ where floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction. Example: given $C_1 = -2.8927765 \times 10^{-6}$, then $C_{1\_E} = -18$ (0xEE).	0x00	R/W	Core clock	No
0x0291	[7:0]	Method 1 C_2 Significand[7:0]		Method 1 Coefficient 2 Significand. This 16-bit signed value, C_{2_S} (default = 0), constitutes the significand associated with C_2. C_{2_S} relates to C_2 as follows: $C_{2\_S} = \text{round}(C_2 \times 2^{15 - C_{2\_E}})$ See Register 0x028E for guidance.	0x00	R/W	Core clock	No
0x0292	[7:0]	Method 1 C_2 Significand[15:8]		Continuation of the Method 1 C_2 significand bit field. See the Method 1 C_2 Significand[7:0] description.	0x00	R/W	Core clock	No
0x0293	[7:0]	Method 1 C_2 exponent		Method 1 Coefficient 2 Exponent. This 8-bit signed value, C_{2_E} (default = 0), constitutes the power of 2 exponent associated with C_2. C_{2_E} relates to C_2 as follows: $C_{2\_E} = \text{floor}(\log(\lvert C_2 \rvert)/\log(2)) + 1$ See Register 0x0290 for guidance.	0x00	R/W	Core clock	No
0x0294	[7:0]	Method 1 C_3 Significand[7:0]		Method 1 Coefficient 3 Significand. This 16-bit signed value, C_{3_S} (default = 0), constitutes the significand associated with C_3. C_{3_S} relates to C_3 as follows: $C_{3\_S} = \text{round}(C_3 \times 2^{15 - C_{3\_E}})$ See Register 0x028E for guidance.	0x00	R/W	Core clock	No
0x0295	[7:0]	Method 1 C_3 Significand[15:8]		Continuation of the Method 1 C_3 significand bit field. See the Method 1 C_3 Significand[7:0] description.	0x00	R/W	Core clock	No
0x0296	[7:0]	Method 1 C_3 exponent		Method 1 Coefficient 3 Exponent. This 8-bit signed value, C_{3_E} (default = 0), constitutes the power of 2 exponent associated with C_3. C_{3_E} relates to C_3 as follows: $C_{3\_E} = \text{floor}(\log(\lvert C_3 \rvert)/\log(2)) + 1$ See Register 0x0290 for guidance.	0x00	R/W	Core clock	No
0x0297	[7:0]	Method 1 C_4 Significand[7:0]		Method 1 Coefficient 4 Significand. This 16-bit signed value, C_{4_S} (default = 0), constitutes the significand associated with C_4. C_{4_S} relates to C_4 as follows: $C_{4\_S} = \text{round}(C_4 \times 2^{15 - C_{4\_E}})$ See Register 0x028E for guidance.	0x00	R/W	Core clock	No
0x0298	[7:0]	Method 1 C_4 Significand[15:8]		Continuation of the Method 1 C_4 significand bit field. See the Method 1 C_4 Significand[7:0] description.	0x00	R/W	Core clock	No
0x0299	[7:0]	Method 1 C_4 exponent		Method 1 Coefficient 4 Exponent. This 8-bit signed value, C_{4_E} (default = 0), constitutes the power of 2 exponent associated with C_4. C_{4_E} relates to C_4 as follows: $C_{4\_E} = \text{floor}(\log(\lvert C_4 \rvert)/\log(2)) + 1$ See Register 0x0290 for guidance.	0x00	R/W	Core clock	No
0x029A	[7:0]	Method 1 C_5 Significand[7:0]		Method 1 Coefficient 5 Significand. This 16-bit signed value, C_{5_S} (default = 0), constitutes the significand associated with C_5. C_{5_S} relates to C_5 as follows: $C_{5\_S} = \text{round}(C_5 \times 2^{15 - C_{5\_E}})$ See Register 0x028E for guidance.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x029B	[7:0]	Method 1 C_5 Significand[15:8]		Continuation of the Method 1 C_5 significand bit field. See the Method 1 C_5 Significand[7:0] description.	0x00	R/W	Core clock	No
0x029C	[7:0]	Method 1 C_5 exponent		Method 1 Coefficient 5 Exponent. This 8-bit signed value, C_{5_E} (default = 0), constitutes the power of 2 exponent associated with C_5. C_{5_E} relates to C_5 as follows: $C_{5\_E} = \text{floor}(\log(\lvert C_5 \rvert)/\log(2)) + 1$ See Register 0x0290 for guidance.	0x00	R/W	Core clock	No

REFERENCE INPUT CONFIGURATION—REGISTER 0x0300 TO REGISTER 0x030F

Table 13. Reference Input Configuration Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0300	[7:6]	REFAA single-ended mode		REFAA Single-Ended Input Options. This 2-bit unsigned value (default = 0) selects from a group of single-ended input configurations.	0x0	R/W	Live	No
			0	AC-Coupled 1.2 V (default). Use this mode for ac coupling a single-ended reference input. The input impedance is approximately 23.5 kΩ with dc bias voltage of approximately 0.6 V.				
			1	DC-Coupled 1.2 V CMOS. Use this mode for single-ended, dc-coupled 1.2 V CMOS.				
			2	DC-Coupled 1.8 V CMOS. Use this mode for single-ended, dc-coupled 1.8 V CMOS.				
			3	Internal Pull-Up Termination. This 1.2 V CMOS single-ended mode uses a pull-up resistor (approximately 46 kΩ) to 1.2 V. This arrangement prevents chatter when the input pin is unconnected.				
	[5:4]	REFA single-ended mode		REFA Single-Ended Input Options. This 2-bit unsigned value (default = 0) selects from a group of single-ended input configurations.	0x0	R/W	Live	No
			0	AC-Coupled 1.2 V (default). Use this mode for ac coupling a single-ended reference input. The input impedance is approximately 23.5 kΩ with an internal bias voltage of approximately 0.6 V.				
			1	DC-Coupled 1.2 V CMOS. Use this mode for single-ended, dc-coupled 1.2 V CMOS.				
			2	DC-Coupled 1.8 V CMOS. Use this mode for single-ended, dc-coupled 1.8 V CMOS.				
			3	Internal Pull-Up Termination. This 1.2 V CMOS single-ended mode uses a pull-up resistor (approximately 46 kΩ) to 1.2 V. This arrangement prevents chatter when the input pin is unconnected.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[3:2]	REFA differential mode		REFA Differential Input Options. This 2-bit unsigned value (default = 0) selects from a group of differential input configurations.	0x0	R/W	Live	No
			0	Self Biased AC-Coupled (default). Use this mode for ac-coupled differential clocks. The input provides a differential resistive termination (~16 kΩ) with a common-mode bias voltage (~0.6 V). The external decoupling capacitors in conjunction with the internal termination resistors form a high-pass network that imposes a lower bound on the input operating frequency.				
			1	DC-Coupled Differential Mode. Use this mode for dc-coupled differential clocks whose common-mode voltage is approximately 0.6 V. There is no internally generated dc bias voltage in this mode (see the AD9546 data sheet for the actual specifications limits).				
			2	DC-Coupled LVDS Mode. Use this mode for dc-coupled LVDS clocks <10 MHz. The input receiver expects a common-mode dc level of approximately 1.2 V (see the AD9546 data sheet for the actual specifications limits).				
	1	Reserved		Reserved.	0	R/W	Live	No
	0	REFA input mode		REFA Input Mode. This bit selects between single-ended (default) and differential input modes.	0	R/W	Live	No
			0	Single-ended (default). The REFA and REFAA pins are independent single-ended inputs.				
			1	Differential. The REFA and REFAA pins form a differential input pair. When configured as a differential input, reference demodulation uses only the REFA reference demodulator.				
0x0301	[7:1]	Reserved		Reserved.	0x00	R	Live	No
	0	REFA/REFAA demodulator bandwidth select		REFA/REFAA Demodulator Bandwidth. This bit selects the carrier frequency operating bandwidth of the reference demodulator for REFA, REFAA, Auxiliary REF0, and Auxiliary REF1. See the AD9546 data sheet for bandwidth limits.	1	R/W	Live	No
			0	Band 0: narrow band.				
			1	Band 1: wide band (default).				
0x0302	7	Enable REFA demodulator polarity		REFA Demodulator Automatic Polarity Detect Enable. This bit selects between manual (default) and automatic polarity detection. Manual detection relies on Register 0x0302, Bit 2.	0	R/W	Live	No
			0	Manual (default).				
			1	Automatic.				
	6	Enable REFA demodulator persist		REFA Demodulator Persistence Enable. This bit (default = 0) selects if the demodulated clock output persists after received modulation events cease.	1	R/W	Live	No
			0	Disabled (default). The demodulated clock output triggers with each demodulated modulation event, which means the TDC associated with REFA generates demodulation tags strictly on detection of modulation events.				
			1	Enabled. The demodulator learns the rate of input modulation events and generates a demodulated clock output at the learned rate. At least five consecutive, periodic, on grid modulation events are necessary for the demodulator to learn the rate. The demodulated clock output causes the TDC associated with REFA to generate demodulation tags at the learned rate, even when modulation events cease (or intermittently occur off grid).				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[5:4]	REFA demodulator sync edge		REFA Demodulator Synchronization Edge Select. This 2-bit unsigned value, SYNC_EDGE (default = 0), allows the user to delay the demodulated clock output edge by an integer number of carrier periods. The first rising carrier edge following the second pulse of a modulation event constitutes the base edge. The demodulated clock output edge occurs SYNC_EDGE + 1 carrier periods after the base edge. The default value is invalid. Thus, the user must program SYNC_EDGE > 0.	0x0	R/W	Live	No
			0	SYNC_EDGE = 0 (invalid) (default).				
			1	SYNC_EDGE = 1.				
			2	SYNC_EDGE = 2.				
			3	SYNC_EDGE = 3.				
	3	Enable REFA demodulator		REFA Demodulator Enable.	0	R/W	Live	No
			0	Disabled (default).				
			1	Enabled.				
	2	REFA demodulator event polarity		REFA Demodulator Polarity. This bit declares the expected polarity of a received modulation event. This bit is only meaningful when Register 0x0302, Bit 7 = 0.	0	R/W	Live	No
			0	The first pulse of a modulation event is narrow (<50% duty cycle), and the second pulse is wide (>50% duty cycle).				
			1	The first pulse of a modulation event is wide (>50% duty cycle), and the second pulse is narrow (<50% duty cycle).				
	[1:0]	REFA demodulator sensitivity		REFA Demodulator Sensitivity. This 2-bit unsigned value (default = 0, maximum sensitivity) sets the sensitivity of the demodulator. Modulation events having a small pulse width variation require greater relative sensitivity.	0x0	R/W	Live	No
			0	Level 0 sensitivity (maximum) (default).				
			1	Level 1 sensitivity.				
			2	Level 2 sensitivity.				
			3	Level 3 sensitivity (minimum).				
0x0303	7	Enable REFAA demodulator polarity		REFAA Demodulator Automatic Polarity Detect Enable. This bit selects between manual (default) and automatic polarity detection. Manual detection relies on Register 0x0303, Bit 2.	0	R/W	Live	No
			0	Manual (default).				
			1	Automatic.				
	6	Enable REFAA demodulator persist		REFAA Demodulator Persistence Enable. This bit (default = 0) selects if the demodulated clock output persists after received modulation events cease.	1	R/W	Live	No
			0	Disabled (default). The demodulated clock output triggers with each demodulated modulation event, which means the TDC associated with REFAA generates demodulation tags strictly on detection of modulation events.				
			1	Enabled. The demodulator learns the rate of input modulation events and generates a demodulated clock output at the learned rate. At least five consecutive, periodic, on grid modulation events are necessary for the demodulator to learn the rate. The demodulated clock output causes the TDC associated with REFAA to generate demodulation tags at the learned rate, even when modulation events cease (or intermittently occur off grid).				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[5:4]	REFAA demodulator sync edge		REFAA Demodulator Synchronization Edge Select. This 2-bit unsigned value, SYNC_EDGE (default = 0), allows the user to delay the demodulated clock output edge by an integer number of carrier periods. The first rising carrier edge following the second pulse of a modulation event constitutes the base edge. The demodulated clock output edge occurs SYNC_EDGE + 1 carrier periods after the base edge. The default value is invalid. Thus, the user must program SYNC_EDGE > 0.	0x0	R/W	Live	No
			0	SYNC_EDGE = 0 (invalid) (default).				
			1	SYNC_EDGE = 1.				
			2	SYNC_EDGE = 2.				
			3	SYNC_EDGE = 3.				
	3	Enable REFAA demodulator		REFAA Demodulator Enable.	0	R/W	Live	No
			0	Disabled (default).				
			1	Enabled.				
	2	REFAA demodulator event polarity		REFAA Demodulator Polarity. This bit declares the expected polarity of a received modulation event. This bit is only meaningful when Register 0x0303, Bit 7 = 0.	0	R/W	Live	No
			0	The first pulse of a modulation event is narrow (<50% duty cycle), and the second pulse is wide (>50% duty cycle).				
			1	The first pulse of a modulation event is wide (>50% duty cycle), and the second pulse is narrow (<50% duty cycle).				
	[1:0]	REFAA demodulator sensitivity		REFAA Demodulator Sensitivity. This 2-bit unsigned value (default = 0, maximum sensitivity) sets the sensitivity of the demodulator. Modulation events having a small pulse width variation require greater relative sensitivity.	0x0	R/W	Live	No
			0	Level 0 sensitivity (maximum) (default).				
			1	Level 1 sensitivity.				
			2	Level 2 sensitivity.				
			3	Level 3 sensitivity (minimum).				
0x0304	[7:6]	REFBB single-ended mode		REFBB Single-Ended Input Options. This 2-bit unsigned value (default = 0) selects from a group of single-ended input configurations.	0x0	R/W	Live	No
			0	AC-Coupled 1.2 V (default). Use this mode for ac coupling a single-ended reference input. The input impedance is approximately 23.5 kΩ with dc bias voltage of approximately 0.6 V.				
			1	DC-Coupled 1.2 V CMOS. Use this mode for single-ended, dc-coupled 1.2 V CMOS.				
			2	DC-Coupled 1.8 V CMOS. Use this mode for single-ended, dc-coupled 1.8 V CMOS.				
			3	Internal Pull-Up Termination. This 1.2 V CMOS single-ended mode uses a pull-up resistor (approximately 46 kΩ) to 1.2 V. This arrangement prevents chatter when the input pin is unconnected.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[5:4]	REFB single-ended mode		REFB Single-Ended Input Options. This 2-bit unsigned value (default = 0) selects from a group of single-ended input configurations.	0x0	R/W	Live	No
			0	AC-Coupled 1.2 V (default). Use this mode for ac coupling a single-ended reference input. The input impedance is approximately 23.5 kΩ with an internal bias voltage of approximately 0.6 V.				
			1	DC-Coupled 1.2 V CMOS. Use this mode for single-ended, dc-coupled 1.2 V CMOS.				
			2	DC-Coupled 1.8 V CMOS. Use this mode for single-ended, dc-coupled 1.8 V CMOS.				
			3	Internal Pull-Up Termination. This 1.2 V CMOS single-ended mode uses a pull-up resistor (approximately 46 kΩ) to 1.2 V. This arrangement prevents chatter when the input pin is unconnected.				
	[3:2]	REFB differential mode		REFB Differential Input Options. This 2-bit unsigned value (default = 0) selects from a group of differential input configurations.	0x0	R/W	Live	No
			0	Self Biased AC-Coupled (default). Use this mode for ac-coupled differential clocks. The input provides a differential resistive termination (~16 kΩ) with a common-mode bias voltage (~0.6 V). The external decoupling capacitors in conjunction with the internal termination resistors form a high-pass network that imposes a lower bound on the input operating frequency.				
			1	DC-Coupled Differential Mode. Use this mode for dc-coupled differential clocks whose common-mode voltage is approximately 0.6 V. There is no internally generated dc bias voltage in this mode (see the AD9546 data sheet for the actual specifications limits).				
			2	DC-Coupled LVDS Mode. Use this mode for dc-coupled LVDS clocks <10 MHz. The input receiver expects a common-mode dc level of approximately 1.2 V (see the AD9546 data sheet for the actual specifications limits).				
	1	Reserved		Reserved.	0	R/W	Live	No
	0	REFB input mode		REFB Input Mode. This bit selects between single-ended (default) and differential input modes.	0	R/W	Live	No
			0	Single-ended (default). The REFB and REFBB pins are independent single-ended inputs.				
			1	Differential. The REFB and REFBB pins form a differential input pair. When configured as a differential input, reference demodulation uses only the REFB reference demodulator.				
0x0305	[7:1]	Reserved		Reserved.	0x00	R/W	Live	No
	0	REFB/REFBB demodulator bandwidth select		REFB/REFBB Demodulator Bandwidth. This bit selects the carrier frequency operating bandwidth of the reference demodulator for REFB, REFBB, Auxiliary REF2, and Auxiliary REF3. See the AD9546 data sheet for bandwidth limits.	1	R/W	Live	No
			0	Band 0: narrow band.				
			1	Band 1: wide band (default).				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0306	7	Enable REFB demodulator polarity		REFB Demodulator Automatic Polarity Detect Enable. This bit selects between manual (default) and automatic polarity detection. Manual detection relies on Register 0x0306, Bit 2.	0	R/W	Live	No
			0	Manual (default).				
			1	Automatic.				
	6	Enable REFB demodulator persist		REFB Demodulator Persistence Enable. This bit (default = 0) selects if the demodulated clock output persists after received modulation events cease.	1	R/W	Live	No
			0	Disabled (default). The demodulated clock output triggers with each demodulated modulation event, which means the TDC associated with REFB generates demodulation tags strictly on detection of modulation events.				
			1	Enabled. The demodulator learns the rate of input modulation events and generates a demodulated clock output at the learned rate. At least five consecutive, periodic, on grid modulation events are necessary for the demodulator to learn the rate. The demodulated clock output causes the TDC associated with REFB to generate demodulation tags at the learned rate, even when modulation events cease (or intermittently occur off grid).				
	[5:4]	REFB demodulator sync edge		REFB Demodulator Synchronization Edge Select. This 2-bit unsigned value, SYNC_EDGE (default = 0), allows the user to delay the demodulated clock output edge by an integer number of carrier periods. The first rising carrier edge following the second pulse of a modulation event constitutes the base edge. The demodulated clock output edge occurs SYNC_EDGE +1 carrier periods after the base edge. The default value is invalid. Thus, the user must program SYNC_EDGE > 0.	0x0	R/W	Live	No
			0	SYNC_EDGE = 0 (invalid) (default).				
			1	SYNC_EDGE = 1.				
			2	SYNC_EDGE = 2.				
			3	SYNC_EDGE = 3.				
	3	Enable REFB demodulator		REFB Demodulator Enable.	0	R/W	Live	No
			0	Disabled (default).				
			1	Enabled.				
	2	REFB demodulator event polarity		REFB Demodulator Polarity. This bit declares the expected polarity of a received modulation event. This bit is only meaningful when Register 0x0306, Bit 7 = 0.	0	R/W	Live	No
			0	The first pulse of a modulation event is narrow (<50% duty cycle), and the second pulse is wide (>50% duty cycle).				
			1	The first pulse of a modulation event is wide (>50% duty cycle), and the second pulse is narrow (<50% duty cycle).				
	[1:0]	REFB demodulator sensitivity		REFB Demodulator Sensitivity. This 2-bit unsigned value (default = 0, maximum sensitivity) sets the sensitivity of the demodulator. Modulation events having a small pulse width variation require greater relative sensitivity.	0x0	R/W	Live	No
			0	Level 0 sensitivity (maximum) (default).				
			1	Level 1 sensitivity.				
			2	Level 2 sensitivity.				
			3	Level 3 sensitivity (minimum).				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0307	7	Enable REFBB demodulator polarity		REFBB Demodulator Automatic Polarity Detect Enable. This bit selects between manual (default) and automatic polarity detection. Manual detection relies on Register 0x0307, Bit 2.	0	R/W	Live	No
			0	Manual (default).				
			1	Automatic.				
	6	Enable REFBB demodulator persist		REFBB Demodulator Persistence Enable. This bit (default = 0) selects if the demodulated clock output persists after received modulation events cease.	1	R/W	Live	No
			0	Disabled (default). The demodulated clock output triggers with each demodulated modulation event, which means the TDC associated with REFBB generates demodulation tags strictly on detection of modulation events.				
			1	Enabled. The demodulator learns the rate of input modulation events and generates a demodulated clock output at the learned rate. At least five consecutive, periodic, on grid modulation events are necessary for the demodulator to learn the rate. The demodulated clock output causes the TDC associated with REFBB to generate demodulation tags at the learned rate, even when modulation events cease (or intermittently occur off grid).				
	[5:4]	REFBB demodulator sync edge		REFBB Demodulator Synchronization Edge Select. This 2-bit unsigned value, SYNC_EDGE (default = 0), allows the user to delay the demodulated clock output edge by an integer number of carrier periods. The first rising carrier edge following the second pulse of a modulation event constitutes the base edge. The demodulated clock output edge occurs SYNC_EDGE + 1 carrier periods after the base edge. The default value is invalid, so the user must program SYNC_EDGE > 0.	0x0	R/W	Live	No
			0	SYNC_EDGE = 0 (invalid) (default).				
			1	SYNC_EDGE = 1.				
			2	SYNC_EDGE = 2.				
			3	SYNC_EDGE = 3.				
	3	Enable REFBB demodulator		REFBB Demodulator Enable.	0	R/W	Live	No
			0	Disabled (default).				
			1	Enabled.				
	2	REFBB demodulator event polarity		REFBB Demodulator Polarity. This bit declares the expected polarity of a received modulation event. This bit is only meaningful when Register 0x0307, Bit 7 = 0.	0	R/W	Live	No
			0	The first pulse of a modulation event is narrow (<50% duty cycle), and the second pulse is wide (>50% duty cycle).				
			1	The first pulse of a modulation event is wide (>50% duty cycle), and the second pulse is narrow (<50% duty cycle).				
	[1:0]	REFBB demodulator sensitivity		REFBB Demodulator Sensitivity. This 2-bit unsigned value (default = 0, maximum sensitivity) sets the sensitivity of the demodulator. Modulation events having a small pulse width variation require greater relative sensitivity.	0x0	R/W	Live	No
			0	Level 0 sensitivity (maximum) (default).				
			1	Level 1 sensitivity.				
			2	Level 2 sensitivity.				
			3	Level 3 sensitivity (minimum).				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x030A	7	Enable Auxiliary REF0 demodulator polarity		Auxiliary REF0 Demodulator Automatic Polarity Detect Enable. This bit selects between manual (default) and automatic polarity detection. Manual detection relies on Register 0x030A, Bit 2.	0	R/W	Live	No
			0	Manual (default).				
			1	Automatic.				
	6	Enable Auxiliary REF0 demodulator persist		Auxiliary REF0 Demodulator Persistence Enable. This bit (default = 0) selects if the demodulated clock output persists after received modulation events cease.	1	R/W	Live	No
			0	Disabled (default). The demodulated clock output triggers with each demodulated modulation event, which means the TDC associated with Auxiliary REF0 generates demodulation tags strictly on detection of modulation events.				
			1	Enabled. The demodulator learns the rate of input modulation events and generates a demodulated clock output at the learned rate. At least five consecutive, periodic, on grid modulation events are necessary for the demodulator to learn the rate. The demodulated clock output causes the TDC associated with Auxiliary REF0 to generate demodulation tags at the learned rate, even when modulation events cease (or intermittently occur off grid).				
	[5:4]	Auxiliary REF0 demodulator sync edge		Auxiliary REF0 Demodulator Synchronization Edge Select. This 2-bit unsigned value, SYNC_EDGE (default = 0), allows the user to delay the demodulated clock output edge by an integer number of carrier periods. The first rising carrier edge following the second pulse of a modulation event constitutes the base edge. The demodulated clock output edge SYNC_EDGE + 1 carrier periods after the base edge. The default value is invalid. Thus, the user must program SYNC_EDGE > 0.	0x0	R/W	Live	No
			0	SYNC_EDGE = 0 (invalid) (default).				
			1	SYNC_EDGE = 1.				
			2	SYNC_EDGE = 2.				
			3	SYNC_EDGE = 3.				
	3	Enable Auxiliary REF0 demodulator		Auxiliary REF0 Demodulator Enable.	0	R/W	Live	No
			0	Disabled (default).				
			1	Enabled.				
	2	Auxiliary REF0 demodulator event polarity		Auxiliary REF0 Demodulator Polarity. This bit declares the expected polarity of a received modulation event. This bit is only meaningful when Register 0x030A, Bit 7 = 0.	0	R/W	Live	No
			0	The first pulse of a modulation event is narrow (<50% duty cycle), and the second pulse is wide (>50% duty cycle).				
			1	The first pulse of a modulation event is wide (>50% duty cycle), and the second pulse is narrow (<50% duty cycle).				
	[1:0]	Auxiliary REF0 demodulator sensitivity		Auxiliary REF0 Demodulator Sensitivity. This 2-bit unsigned value (default = 0, maximum sensitivity) sets the sensitivity of the demodulator. Modulation events having a small pulse width variation require greater relative sensitivity.	0x0	R/W	Live	No
			0	Level 0 sensitivity (maximum) (default).				
			1	Level 1 sensitivity.				
			2	Level 2 sensitivity.				
			3	Level 3 sensitivity (minimum).				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x030B	7	Enable Auxiliary REF1 demodulator polarity		Auxiliary REF1 Demodulator Automatic Polarity Detect Enable. This bit selects between manual (default) and automatic polarity detection. Manual detection relies on Register 0x030B, Bit 2.	0	R/W	Live	No
			0	Manual (default).				
			1	Automatic.				
	6	Enable Auxiliary REF1 demodulator persist		Auxiliary REF1 Demodulator Persistence Enable. This bit (default = 0) selects if the demodulated clock output persists after received modulation events cease.	1	R/W	Live	No
			0	Disabled (default). The demodulated clock output triggers with each demodulated modulation event, which means the TDC associated with Auxiliary REF1 generates demodulation tags strictly on detection of modulation events.				
			1	Enabled. The demodulator learns the rate of input modulation events and generates a demodulated clock output at the learned rate. At least five consecutive, periodic, on grid modulation events are necessary for the demodulator to learn the rate. The demodulated clock output causes the TDC associated with Auxiliary REF1 to generate demodulation tags at the learned rate, even when modulation events cease (or intermittently occur off grid).				
	[5:4]	Auxiliary REF1 demodulator sync edge		Auxiliary REF1 Demodulator Synchronization Edge Select. This 2-bit unsigned value, SYNC_EDGE (default = 0), allows the user to delay the demodulated clock output edge by an integer number of carrier periods. The first rising carrier edge following the second pulse of a modulation event constitutes the base edge. The demodulated clock output edge occurs SYNC_EDGE + 1 carrier periods after the base edge. The default value is invalid. Thus, the user must program SYNC_EDGE > 0.	0x0	R/W	Live	No
			0	SYNC_EDGE = 0 (invalid) (default).				
			1	SYNC_EDGE = 1.				
			2	SYNC_EDGE = 2.				
			3	SYNC_EDGE = 3.				
	3	Enable Auxiliary REF1 demodulator		Auxiliary REF1 Demodulator Enable.	0	R/W	Live	No
			0	Disabled (default).				
			1	Enabled.				
	2	Auxiliary REF1 demodulator event polarity		Auxiliary REF1 Demodulator Polarity. This bit declares the expected polarity of a received modulation event. This bit is only meaningful when Register 0x030B, Bit 7 = 0.	0	R/W	Live	No
			0	The first pulse of a modulation event is narrow (<50% duty cycle), and the second pulse is wide (>50% duty cycle).				
			1	The first pulse of a modulation event is wide (>50% duty cycle), and the second pulse is narrow (<50% duty cycle).				
	[1:0]	Auxiliary REF1 demodulator sensitivity		Auxiliary REF1 Demodulator Sensitivity. This 2-bit unsigned value (default = 0, maximum sensitivity) sets the sensitivity of the demodulator. Modulation events having a small pulse width variation require greater relative sensitivity.	0x0	R/W	Live	No
			0	Level 0 sensitivity (maximum) (default).				
			1	Level 1 sensitivity.				
			2	Level 2 sensitivity.				
			3	Level 3 sensitivity (minimum).				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x030E	7	Enable Auxiliary REF2 demodulator polarity		Auxiliary REF2 Demodulator Automatic Polarity Detect Enable. This bit selects between manual (default) and automatic polarity detection. Manual detection relies on Register 0x030E, Bit 2.	0	R/W	Live	No
			0	Manual (default).				
			1	Automatic.				
	6	Enable Auxiliary REF2 demodulator persist		Auxiliary REF2 Demodulator Persistence Enable. This bit (default = 0) selects if the demodulated clock output persists after received modulation events cease.	1	R/W	Live	No
			0	Disabled (default). The demodulated clock output triggers with each demodulated modulation event, which means the TDC associated with Auxiliary REF2 generates demodulation tags strictly on detection of modulation events.				
			1	Enabled. The demodulator learns the rate of input modulation events and generates a demodulated clock output at the learned rate. At least five consecutive, periodic, on grid modulation events are necessary for the demodulator to learn the rate. The demodulated clock output causes the TDC associated with Auxiliary REF2 to generate demodulation tags at the learned rate, even when modulation events cease (or intermittently occur off grid).				
	[5:4]	Auxiliary REF2 demodulator sync edge		Auxiliary REF2 Demodulator Synchronization Edge Select. This 2-bit unsigned value, SYNC_EDGE (default = 0), allows the user to delay the demodulated clock output edge by an integer number of carrier periods. The first rising carrier edge following the second pulse of a modulation event constitutes the base edge. The demodulated clock output edge occurs SYNC_EDGE + 1 carrier periods after the base edge. The default value is invalid. Thus, the user must program SYNC_EDGE > 0.	0x0	R/W	Live	No
			0	SYNC_EDGE = 0 (invalid) (default).				
			1	SYNC_EDGE = 1.				
			2	SYNC_EDGE = 2.				
			3	SYNC_EDGE = 3.				
	3	Enable Auxiliary REF2 demodulator		Auxiliary REF2 Demodulator Enable.	0	R/W	Live	No
			0	Disabled (default).				
			1	Enabled.				
	2	Auxiliary REF2 demodulator event polarity		Auxiliary REF2 Demodulator Polarity. This bit declares the expected polarity of a received modulation event. This bit is only meaningful when Register 0x030E, Bit 7 = 0.	0	R/W	Live	No
			0	The first pulse of a modulation event is narrow (<50% duty cycle), and the second pulse is wide (>50% duty cycle).				
			1	The first pulse of a modulation event is wide (>50% duty cycle), and the second pulse is narrow (<50% duty cycle).				
	[1:0]	Auxiliary REF2 demodulator sensitivity		Auxiliary REF2 Demodulator Sensitivity. This 2-bit unsigned value (default = 0, maximum sensitivity) sets the sensitivity of the demodulator. Modulation events having a small pulse width variation require greater relative sensitivity.	0x0	R/W	Live	No
			0	Level 0 sensitivity (maximum) (default).				
			1	Level 1 sensitivity.				
			2	Level 2 sensitivity.				
			3	Level 3 sensitivity (minimum).				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x030F	7	Enable Auxiliary REF3 demodulator polarity		Auxiliary REF3 Demodulator Automatic Polarity Detect Enable. This bit selects between manual (default) and automatic polarity detection. Manual detection relies on Register 0x030F, Bit 2.	0	R/W	Live	No
			0	Manual (default).				
			1	Automatic.				
	6	Enable Auxiliary REF3 demodulator persist		Auxiliary REF3 Demodulator Persistence Enable. This bit (default = 0) selects if the demodulated clock output persists after received modulation events cease.	1	R/W	Live	No
			0	Disabled (default). The demodulated clock output triggers with each demodulated modulation event, which means the TDC associated with Auxiliary REF3 generates demodulation tags strictly on detection of modulation events.				
			1	Enabled. The demodulator learns the rate of input modulation events and generates a demodulated clock output at the learned rate. At least five consecutive, periodic, on grid modulation events are necessary for the demodulator to learn the rate. The demodulated clock output causes the TDC associated with Auxiliary REF3 to generate demodulation tags at the learned rate, even when modulation events cease (or intermittently occur off grid).				
	[5:4]	Auxiliary REF3 demodulator sync edge		Auxiliary REF3 Demodulator Synchronization Edge Select. This 2-bit unsigned value, SYNC_EDGE (default = 0), allows the user to delay the demodulated clock output edge by an integer number of carrier periods. The first rising carrier edge following the second pulse of a modulation event constitutes the base edge. The demodulated clock output edge occurs SYNC_EDGE + 1 carrier periods after the base edge. The default value is invalid. Thus, the user must program SYNC_EDGE > 0.	0x0	R/W	Live	No
			0	SYNC_EDGE = 0 (invalid) (default).				
			1	SYNC_EDGE = 1.				
			2	SYNC_EDGE = 2.				
			3	SYNC_EDGE = 3.				
	3	Enable Auxiliary REF3 demodulator		Auxiliary REF3 Demodulator Enable.	0	R/W	Live	No
			0	Disabled (default).				
			1	Enabled.				
	2	Auxiliary REF3 demodulator event polarity		Auxiliary REF3 Demodulator Polarity. This bit declares the expected polarity of a received modulation event. This bit is only meaningful when Register 0x030F, Bit 7 = 0.	0	R/W	Live	No
			0	The first pulse of a modulation event is narrow (<50% duty cycle), and the second pulse is wide (>50% duty cycle).				
			1	The first pulse of a modulation event is wide (>50% duty cycle), and the second pulse is narrow (<50% duty cycle).				
	[1:0]	Auxiliary REF3 demodulator sensitivity		Auxiliary REF3 Demodulator Sensitivity. This 2-bit unsigned value (default = 0, maximum sensitivity) sets the sensitivity of the demodulator. Modulation events having a small pulse width variation require greater relative sensitivity.	0x0	R/W	Live	No
			0	Level 0 sensitivity (maximum) (default).				
			1	Level 1 sensitivity.				
			2	Level 2 sensitivity.				
			3	Level 3 sensitivity (minimum).				

REFERENCE INPUT PARAMETERS: REFA—REGISTER 0x0400 TO REGISTER 0x0414

Table 14. Reference Input Parameters: REFA Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0400	[7:0]	REFA R Divide Ratio[7:0]		REFA Input Divider. This 30-bit unsigned value, RDIV (default = 0), sets the division factor, R, for the reference input divider, where R relates to RDIV as follows: $R = RDIV + 1$ For example, RDIV = 0 equates to R = 1.	0x00	R/W	Live	No
0x0401	[7:0]	REFA R Divide Ratio[15:8]		Continuation of the REFA R divide ratio bit field. See the REFA R Divide Ratio[7:0] description.	0x00	R/W	Live	No
0x0402	[7:0]	REFA R Divide Ratio[23:16]		Continuation of the REFA R divide ratio bit field. See the REFA R Divide Ratio[7:0] description.	0x00	R/W	Live	No
0x0403	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	[5:0]	REFA R Divide Ratio[29:24]		Continuation of the REFA R divide ratio bit field. See the REFA R Divide Ratio[7:0] description.	0x00	R/W	Live	No
0x0404	[7:0]	REFA Nominal Period[7:0]		REFA Nominal Reference Period. This 60-bit unsigned value, $PERIOD_A$ (default = 0) in units of attoseconds (10^{-18} sec), constitutes the declaration by the user of the nominal reference input period, t_{REF}, where $t_{REF} = 1/f_{REF}$. $PERIOD_A$ (rounded to the nearest integer) relates to f_{REF} as follows: $PERIOD_A = 10^{18}/f_{REF}$ For example, given f_{REF} = 2.048 MHz, then $PERIOD_A$ = 488,281,250,000 (0x71 AFD4 98D0).	0x00	R/W	Live	No
0x0405	[7:0]	REFA Nominal Period[15:8]		Continuation of the REFA nominal period bit field. See the REFA Nominal Period[7:0] description.	0x00	R/W	Live	No
0x0406	[7:0]	REFA Nominal Period[23:16]		Continuation of the REFA nominal period bit field. See the REFA Nominal Period[7:0] description.	0x00	R/W	Live	No
0x0407	[7:0]	REFA Nominal Period[31:24]		Continuation of the REFA nominal period bit field. See the REFA Nominal Period[7:0] description.	0x00	R/W	Live	No
0x0408	[7:0]	REFA Nominal Period[39:32]		Continuation of the REFA nominal period bit field. See the REFA Nominal Period[7:0] description.	0x00	R/W	Live	No
0x0409	[7:0]	REFA Nominal Period[47:40]		Continuation of the REFA nominal period bit field. See the REFA Nominal Period[7:0] description.	0x00	R/W	Live	No
0x040A	[7:0]	REFA Nominal Period[55:48]		Continuation of the REFA nominal period bit field. See the REFA Nominal Period[7:0] description.	0x00	R/W	Live	No
0x040B	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	[3:0]	REFA Nominal Period[59:56]		Continuation of the REFA nominal period bit field. See the REFA Nominal Period[7:0] description.	0x0	R/W	Live	No
0x040C	[7:0]	REFA Offset Limit[7:0]		REFA Maximum Reference Period Deviation. This 24-bit unsigned value, threshold, in units of parts per billion (ppb) (default = 100,000), constitutes a fractional value with a maximum of 2^{24} ppb (~1.68%) and the default value equating to 100 ppm. Threshold is the magnitude of the relative deviation of the input period from t_{REF} beyond which the reference monitor declares a nonfaulted reference as out of tolerance (that is, slow or fast). Relative period deviation, δp, relates to relative frequency deviation, δf, as follows: $\delta p = (-\delta f)/(1 + \delta f)$ Because threshold is unsigned, it relates to δf as follows: $Threshold = |\delta f/(1 + \delta f)| \times 10^9$ For example, given a maximum desired relative frequency deviation of $\delta f = 75 \times 10^{-6}$ (that is, 75 ppm), threshold = 74994 (0x01 24F2) rounded to the nearest integer.	0x160	R/W	Live	No
0x040D	[7:0]	REFA Offset Limit[15:8]		Continuation of the REFA offset limit bit field. See the REFA Offset Limit[7:0] description.	0x134	R/W	Live	No
0x040E	[7:0]	REFA Offset Limit[23:16]		Continuation of the REFA offset limit bit field. See the REFA Offset Limit[7:0] description.	0x01	R/W	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x040F	[7:3]	Reserved		Reserved.	0x00	R	Live	No
	[2:0]	REFA monitor hysteresis		REFA Reference Monitor Hysteresis. This 3-bit code (default = 3) selects a scale factor, SF, that together with threshold defines a certain amount of hysteresis given by *SF* × *Threshold* For example, given threshold = 74994 ppb and SF = 6.25%, the amount of hysteresis is 4687 ppb. The smaller the amount of hysteresis, the more likely the reference monitor chatters if the input reference period is near the limit of the allowable period error (threshold).	0x3	R/W	Live	No
			0	No hysteresis.				
			1	3.125%.				
			2	6.25%.				
			3	12.5% (default).				
			4	25%.				
			5	50%.				
			6	75%.				
			7	87.5%.				
0x0410	[7:0]	REFA Validation Timer[7:0]		REFA Reference Validation Time. This 20-bit unsigned value, validation time in units of milliseconds (default = 10), defines a minimum time interval, t_{VALID} (units of seconds), for which a faulted reference must remain unfaulted before the reference monitor indicates the reference as valid. Validation time relates to t_{VALID} as follows: *Validation Time* = 1000 × t_{VALID} For example, for a validation time of t_{VALID} = 10 min (600 sec), then validation time = 600,000 (0x927C0). The default value yields t_{VALID} = 10 ms. The maximum value of validation time equates to t_{VALID} = 1048.755 sec (~17.5 min).	0x10	R/W	Live	No
0x0411	[7:0]	REFA Validation Timer[15:8]		Continuation of the REFA validation timer bit field. See the REFA Validation Timer[7:0] description.	0x00	R/W	Live	No
0x0412	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	[3:0]	REFA Validation Timer[19:16]		Continuation of the REFA validation timer bit field. See the REFA Validation Timer[7:0] description.	0x0	R/W	Live	No
0x0413	[7:0]	REFA Jitter Tolerance[7:0]		REFA Reference Jitter Tolerance. This 16-bit unsigned value, jitter tolerance in units of nanoseconds (default = 0), defines the maximum rms jitter the reference monitor accepts before indicating an excess jitter condition. Jitter tolerance relates to the maximum acceptable rms jitter, t_{J_MAX} (units of seconds), as follows: *Jitter Tolerance* = t_{J_MAX} × 10^9 For example, given t_{J_MAX} = 75 × 10^{-9} sec rms (75 ns), then jitter tolerance = 75 (0x004B). Jitter Tolerance = 0 prevents the reference monitor from including its estimation of jitter as part of the excess noise status decision, but the reference monitor continues to perform jitter estimation to continue making out of tolerance decisions.	0x00	R/W	Live	No
0x0414	[7:0]	REFA Jitter Tolerance[15:8]		Continuation of the REFA jitter tolerance bit field. See the REFA Jitter Tolerance[7:0] description.	0x00	R/W	Live	No

REFERENCE INPUT PARAMETERS: REFAA—REGISTER 0x0420 TO REGISTER 0x0434

Table 15. Reference Input Parameters: REFAA Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0420	[7:0]	REFAA R Divide Ratio[7:0]		REFAA Input Divider. This 30-bit unsigned value, RDIV (default = 0), sets the division factor, R, for the reference input divider, where R relates to RDIV as follows: $R = RDIV + 1$ For example, RDIV = 0 equates to R = 1.	0x00	R/W	Live	No
0x0421	[7:0]	REFAA R Divide Ratio[15:8]		Continuation of the REFAA R divide ratio bit field. See the REFAA R Divide Ratio[7:0] description.	0x00	R/W	Live	No
0x0422	[7:0]	REFAA R Divide Ratio[23:16]		Continuation of the REFAA R divide ratio bit field. See the REFAA R Divide Ratio[7:0] description.	0x00	R/W	Live	No
0x0423	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	[5:0]	REFAA R Divide Ratio[29:24]		Continuation of the REFAA R divide ratio bit field. See the REFAA R Divide Ratio[7:0] description.	0x00	R/W	Live	No
0x0424	[7:0]	REFAA Nominal Period[7:0]		REFAA Nominal Reference Period. This 60-bit unsigned value, $PERIOD_{AA}$ (default = 0) in units of attoseconds (10^{-18} sec), constitutes the declaration by the user of the nominal reference input period, t_{REF}, where $t_{REF} = 1/f_{REF}$. $PERIOD_{AA}$ (rounded to the nearest integer) relates to f_{REF} as follows: $PERIOD_{AA} = 10^{18}/f_{REF}$ For example, given f_{REF} = 2.048 MHz, then $PERIOD_{AA}$ = 488,281,250,000 (0x71 AFD4 98D0).	0x00	R/W	Live	No
0x0425	[7:0]	REFAA Nominal Period[15:8]		Continuation of the REFAA nominal period bit field. See the REFAA Nominal Period[7:0] description.	0x00	R/W	Live	No
0x0426	[7:0]	REFAA Nominal Period[23:16]		Continuation of the REFAA nominal period bit field. See the REFAA Nominal Period[7:0] description.	0x00	R/W	Live	No
0x0427	[7:0]	REFAA Nominal Period[31:24]		Continuation of the REFAA nominal period bit field. See the REFAA Nominal Period[7:0] description.	0x00	R/W	Live	No
0x0428	[7:0]	REFAA Nominal Period[39:32]		Continuation of the REFAA nominal period bit field. See the REFAA Nominal Period[7:0] description.	0x00	R/W	Live	No
0x0429	[7:0]	REFAA Nominal Period[47:40]		Continuation of the REFAA nominal period bit field. See the REFAA Nominal Period[7:0] description.	0x00	R/W	Live	No
0x042A	[7:0]	REFAA Nominal Period[55:48]		Continuation of the REFAA nominal period bit field. See the REFAA Nominal Period[7:0] description.	0x00	R/W	Live	No
0x042B	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	[3:0]	REFAA Nominal Period[59:56]		Continuation of the REFAA nominal period bit field. See the REFAA Nominal Period[7:0] description.	0x0	R/W	Live	No
0x042C	[7:0]	REFAA Offset Limit[7:0]		REFAA Maximum Reference Period Deviation. This 24-bit unsigned value, threshold, in units of parts per billion (ppb) (default = 100,000), constitutes a fractional value with a maximum of 2^{24} ppb (~1.68%) and the default value equating to 100 ppm. Threshold is the magnitude of the relative deviation of the input period from t_{REF} beyond which the reference monitor declares a nonfaulted reference as out of tolerance (that is, slow or fast). Relative period deviation, δp, relates to relative frequency deviation, δf, as follows: $\delta p = (-\delta f)/(1 + \delta f)$ Because threshold is unsigned, it relates to δf as follows: $Threshold = |\delta f/(1 + \delta f)| \times 10^9$ For example, given a maximum desired relative frequency deviation of $\delta f = 75 \times 10^{-6}$ (that is, 75 ppm), threshold = 74994 (0x01 24F2) rounded to the nearest integer.	0x160	R/W	Live	No
0x042D	[7:0]	REFAA Offset Limit[15:8]		Continuation of the REFAA offset limit bit field. See the REFAA Offset Limit[7:0] description.	0x134	R/W	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x042E	[7:0]	REFAA Offset Limit[23:16]		Continuation of the REFAA offset limit bit field. See the REFAA Offset Limit[7:0] description.	0x01	R/W	Live	No
0x042F	[7:3]	Reserved		Reserved.	0x00	R	Live	No
	[2:0]	REFAA monitor hysteresis		REFAA Reference Monitor Hysteresis. This 3-bit code (default = 3) selects a scale factor, SF, that together with threshold defines a certain amount of hysteresis given by *SF* × *Threshold* For example, given threshold = 74994 ppb and SF = 6.25%, the amount of hysteresis is 4687 ppb. The smaller the amount of hysteresis, the more likely the reference monitor chatters if the input reference period is near the limit of the allowable period error (threshold).	0x3	R/W	Live	No
			0	No hysteresis.				
			1	3.125%.				
			2	6.25%.				
			3	12.5% (default).				
			4	25%.				
			5	50%.				
			6	75%.				
			7	87.5%.				
0x0430	[7:0]	REFAA Validation Timer[7:0]		REFAA Reference Validation Time. This 20-bit unsigned value, validation time in units of milliseconds (default = 10), defines a minimum time interval, t_{VALID} (units of seconds), for which a faulted reference must remain unfaulted before the reference monitor indicates the reference as valid. Validation time relates to t_{VALID} as follows: *Validation Time* = 1000 × t_{VALID} For example, for a validation time of t_{VALID} = 10 min (600 sec), then validation time = 600,000 (0x927C0). The default value yields t_{VALID} = 10 ms. The maximum value of validation time equates to t_{VALID} = 1048.755 sec (~17.5 min).	0x10	R/W	Live	No
0x0431	[7:0]	REFAA Validation Timer[15:8]		Continuation of the REFAA validation timer bit field. See the REFAA Validation Timer[7:0] description.	0x00	R/W	Live	No
0x0432	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	[3:0]	REFAA Validation Timer[19:16]		Continuation of the REFAA validation timer bit field. See the REFAA Validation Timer[7:0] description.	0x0	R/W	Live	No
0x0433	[7:0]	REFAA Jitter Tolerance[7:0]		REFAA Reference Jitter Tolerance. This 16-bit unsigned value, jitter tolerance in units of nanoseconds (default = 0), defines the maximum rms jitter the reference monitor accepts before indicating an excess jitter condition. Jitter tolerance relates to the maximum acceptable rms jitter, t_{J_MAX} (units of seconds), as follows: *Jitter Tolerance* = $t_{J\_MAX} \times 10^{9}$ For example, given $t_{J\_MAX} = 75 \times 10^{-9}$ sec rms (75 ns), then jitter tolerance = 75 (0x004B). Jitter Tolerance = 0 prevents the reference monitor from including its estimation of jitter as part of the excess noise status decision, but the reference monitor continues to perform jitter estimation to continue making out of tolerance decisions.	0x00	R/W	Live	No
0x0434	[7:0]	REFAA Jitter Tolerance[15:8]		Continuation of the REFAA jitter tolerance bit field. See the REFAA Jitter Tolerance[7:0] description.	0x00	R/W	Live	No

REFERENCE INPUT PARAMETERS: REFB—REGISTER 0x0440 TO REGISTER 0x0454

Table 16. Reference Input Parameters: REFB Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0440	[7:0]	REFB R Divide Ratio[7:0]		REFB Input Divider. This 30-bit unsigned value, RDIV (default = 0), sets the division factor, R, for the reference input divider, where R relates to RDIV as follows: $R = RDIV + 1$ For example, RDIV = 0 equates to R = 1.	0x00	R/W	Live	No
0x0441	[7:0]	REFB R Divide Ratio[15:8]		Continuation of the REFB R divide ratio bit field. See the REFB R Divide Ratio[7:0] description.	0x00	R/W	Live	No
0x0442	[7:0]	REFB R Divide Ratio[23:16]		Continuation of the REFB R divide ratio bit field. See the REFB R Divide Ratio[7:0] description.	0x00	R/W	Live	No
0x0443	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	[5:0]	REFB R Divide Ratio[29:24]		Continuation of the REFB R divide ratio bit field. See the REFB R Divide Ratio[7:0] description.	0x00	R/W	Live	No
0x0444	[7:0]	REFB Nominal Period[7:0]		REFB Nominal Reference Period. This 60-bit unsigned value, $PERIOD_B$ (default = 0) in units of attoseconds (10^{-18} sec), constitutes the declaration by the user of the nominal reference input period, t_{REF}, where $t_{REF} = 1/f_{REF}$. $PERIOD_B$ (rounded to the nearest integer) relates to f_{REF} as follows: $PERIOD_B = 10^{18}/f_{REF}$ For example, given f_{REF} = 2.048 MHz, then $PERIOD_B$ = 488,281,250,000 (0x71 AFD4 98D0).	0x00	R/W	Live	No
0x0445	[7:0]	REFB Nominal Period[15:8]		Continuation of the REFB nominal period bit field. See the REFB Nominal Period[7:0] description.	0x00	R/W	Live	No
0x0446	[7:0]	REFB Nominal Period[23:16]		Continuation of the REFB nominal period bit field. See the REFB Nominal Period[7:0] description.	0x00	R/W	Live	No
0x0447	[7:0]	REFB Nominal Period[31:24]		Continuation of the REFB nominal period bit field. See the REFB Nominal Period[7:0] description.	0x00	R/W	Live	No
0x0448	[7:0]	REFB Nominal Period[39:32]		Continuation of the REFB nominal period bit field. See the REFB Nominal Period[7:0] description.	0x00	R/W	Live	No
0x0449	[7:0]	REFB Nominal Period[47:40]		Continuation of the REFB nominal period bit field. See the REFB Nominal Period[7:0] description.	0x00	R/W	Live	No
0x044A	[7:0]	REFB Nominal Period[55:48]		Continuation of the REFB nominal period bit field. See the REFB Nominal Period[7:0] description.	0x00	R/W	Live	No
0x044B	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	[3:0]	REFB Nominal Period[59:56]		Continuation of the REFB nominal period bit field. See the REFB Nominal Period[7:0] description.	0x0	R/W	Live	No
0x044C	[7:0]	REFB Offset Limit[7:0]		REFB Maximum Reference Period Deviation. This 24-bit unsigned value, threshold, in units of parts per billion (ppb) (default = 100,000), constitutes a fractional value with a maximum of 2^{24} ppb (~1.68%) and the default value equating to 100 ppm. Threshold is the magnitude of the relative deviation of the input period from t_{REF} beyond which the reference monitor declares a nonfaulted reference as out of tolerance (that is, slow or fast). Relative period deviation, δp, relates to relative frequency deviation, δf, as follows: $\delta p = (-\delta f)/(1 + \delta f)$ Because threshold is unsigned, it relates to δf as follows: $Threshold = |\delta f/(1 + \delta f)| \times 10^9$ For example, given a maximum desired relative frequency deviation of $\delta f = 75 \times 10^{-6}$ (that is, 75 ppm), threshold = 74994 (0x01 24F2) rounded to the nearest integer.	0x160	R/W	Live	No
0x044D	[7:0]	REFB Offset Limit[15:8]		Continuation of the REFB offset limit bit field. See the REFB Offset Limit[7:0] description.	0x134	R/W	Live	No
0x044E	[7:0]	REFB Offset Limit[23:16]		Continuation of the REFB offset limit bit field. See the REFB Offset Limit[7:0] description.	0x01	R/W	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x044F	[7:3]	Reserved		Reserved.	0x00	R	Live	No
	[2:0]	REFB monitor hysteresis		REFB Reference Monitor Hysteresis. This 3-bit code (default = 3) selects a scale factor, SF, that together with threshold defines a certain amount of hysteresis given by *SF* × *Threshold* For example, given threshold = 74994 ppb and SF = 6.25%, the amount of hysteresis is 4687 ppb. The smaller the amount of hysteresis, the more likely the reference monitor chatters if the input reference period is near the limit of the allowable period error (threshold).	0x3	R/W	Live	No
			0	No hysteresis.				
			1	3.125%.				
			2	6.25%.				
			3	12.5% (default).				
			4	25%.				
			5	50%.				
			6	75%.				
			7	87.5%.				
0x0450	[7:0]	REFB Validation Timer[7:0]		REFB Reference Validation Time. This 20-bit unsigned value, validation time in units of milliseconds (default = 10), defines a minimum time interval, t_{VALID} (units of seconds), for which a faulted reference must remain unfaulted before the reference monitor indicates the reference as valid. Validation time relates to t_{VALID} as follows: *Validation Time* = 1000 × t_{VALID} For example, for a validation time of t_{VALID} = 10 min (600 sec), then validation time = 600,000 (0x927C0). The default value yields t_{VALID} = 10 ms. The maximum value of validation time equates to t_{VALID} = 1048.755 sec (~17.5 min).	0x10	R/W	Live	No
0x0451	[7:0]	REFB Validation Timer[15:8]		Continuation of the REFB validation timer bit field. See the REFB Validation Timer[7:0] description.	0x00	R/W	Live	No
0x0452	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	[3:0]	REFB Validation Timer[19:16]		Continuation of the REFB validation timer bit field. See the REFB Validation Timer[7:0] description.	0x0	R/W	Live	No
0x0453	[7:0]	REFB Jitter Tolerance[7:0]		REFB Reference Jitter Tolerance. This 16-bit unsigned value, jitter tolerance in units of nanoseconds (default = 0), defines the maximum rms jitter the reference monitor accepts before indicating an excess jitter condition. Jitter tolerance relates to the maximum acceptable rms jitter, t_{J_MAX} (units of seconds), as follows: *Jitter Tolerance* = $t_{J\_MAX} \times 10^9$ For example, given $t_{J\_MAX} = 75 \times 10^{-9}$ sec rms (75 ns), then jitter tolerance = 75 (0x004B). Jitter Tolerance = 0 prevents the reference monitor from including its estimation of jitter as part of the excess noise status decision, but the reference monitor continues to perform jitter estimation to continue making out of tolerance decisions.	0x00	R/W	Live	No
0x0454	[7:0]	REFB Jitter Tolerance[15:8]		Continuation of the REFB jitter tolerance bit field. See the REFB Jitter Tolerance[7:0] description.	0x00	R/W	Live	No

REFERENCE INPUT PARAMETERS: REFBB—REGISTER 0x0460 TO REGISTER 0x0474

Table 17. Reference Input Parameters: REFBB Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0460	[7:0]	REFBB R Divide Ratio[7:0]		REFBB Input Divider. This 30-bit unsigned value, RDIV (default = 0), sets the division factor, R, for the reference input divider, where R relates to RDIV as follows: $R = RDIV + 1$ For example, RDIV = 0 equates to R = 1.	0x00	R/W	Live	No
0x0461	[7:0]	REFBB R Divide Ratio[15:8]		Continuation of the REFBB R divide ratio bit field. See the REFBB R Divide Ratio[7:0] description.	0x00	R/W	Live	No
0x0462	[7:0]	REFBB R Divide Ratio[23:16]		Continuation of the REFBB R divide ratio bit field. See the REFBB R Divide Ratio[7:0] description.	0x00	R/W	Live	No
0x0463	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	[5:0]	REFBB R Divide Ratio[29:24]		Continuation of the REFBB R divide ratio bit field. See the REFBB R Divide Ratio[7:0] description.	0x00	R/W	Live	No
0x0464	[7:0]	REFBB Nominal Period[7:0]		REFBB Nominal Reference Period. This 60-bit unsigned value, $PERIOD_{BB}$ (default = 0) in units of attoseconds (10^{-18} sec), constitutes the declaration by the user of the nominal reference input period, t_{REF}, where $t_{REF} = 1/f_{REF}$. $PERIOD_{BB}$ (rounded to the nearest integer) relates to f_{REF} as follows: $PERIOD_{BB} = 10^{18}/f_{REF}$ For example, given f_{REF} = 2.048 MHz, then $PERIOD_{BB}$ = 488,281,250,000 (0x71 AFD4 98D0).	0x00	R/W	Live	No
0x0465	[7:0]	REFBB Nominal Period[15:8]		Continuation of the REFBB nominal period bit field. See the REFBB Nominal Period[7:0] description.	0x00	R/W	Live	No
0x0466	[7:0]	REFBB Nominal Period[23:16]		Continuation of the REFBB nominal period bit field. See the REFBB Nominal Period[7:0] description.	0x00	R/W	Live	No
0x0467	[7:0]	REFBB Nominal Period[31:24]		Continuation of the REFBB nominal period bit field. See the REFBB Nominal Period[7:0] description.	0x00	R/W	Live	No
0x0468	[7:0]	REFBB Nominal Period[39:32]		Continuation of the REFBB nominal period bit field. See the REFBB Nominal Period[7:0] description.	0x00	R/W	Live	No
0x0469	[7:0]	REFBB Nominal Period[47:40]		Continuation of the REFBB nominal period bit field. See the REFBB Nominal Period[7:0] description.	0x00	R/W	Live	No
0x046A	[7:0]	REFBB Nominal Period[55:48]		Continuation of the REFBB nominal period bit field. See the REFBB Nominal Period[7:0] description.	0x00	R/W	Live	No
0x046B	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	[3:0]	REFBB Nominal Period[59:56]		Continuation of the REFBB nominal period bit field. See the REFBB Nominal Period[7:0] description.	0x0	R/W	Live	No
0x046C	[7:0]	REFBB Offset Limit[7:0]		REFBB Maximum Reference Period Deviation. This 24-bit unsigned value, threshold, in units of parts per billion (ppb) (default = 100,000), constitutes a fractional value with a maximum of 2^{24} ppb (~1.68%) and the default value equating to 100 ppm. Threshold is the magnitude of the relative deviation of the input period from t_{REF} beyond which the reference monitor declares a nonfaulted reference as out of tolerance (that is, slow or fast). Relative period deviation, δp, relates to relative frequency deviation, δf, as follows: $\delta p = (-\delta f)/(1 + \delta f)$ Because threshold is unsigned, it relates to δf as follows: $Threshold = |\delta f/(1 + \delta f)| \times 10^9$ For example, given a maximum desired relative frequency deviation of $\delta f = 75 \times 10^{-6}$ (that is, 75 ppm), threshold = 74994 (0x01 24F2) rounded to the nearest integer.	0x160	R/W	Live	No
0x046D	[7:0]	REFBB Offset Limit[15:8]		Continuation of the REFBB offset limit bit field. See the REFBB Offset Limit[7:0] description.	0x134	R/W	Live	No
0x046E	[7:0]	REFBB Offset Limit[23:16]		Continuation of the REFBB offset limit bit field. See the REFBB Offset Limit[7:0] description.	0x01	R/W	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x046F	[7:3]	Reserved		Reserved.	0x00	R	Live	No
	[2:0]	REFBB monitor hysteresis		REFBB Reference Monitor Hysteresis. This 3-bit code (default = 3) selects a scale factor, SF, that together with threshold defines a certain amount of hysteresis given by *SF* × *Threshold* For example, given threshold = 74994 ppb and SF = 6.25%, the amount of hysteresis is 4687 ppb. The smaller the amount of hysteresis, the more likely the reference monitor chatters if the input reference period is near the limit of the allowable period error (threshold).	0x3	R/W	Live	No
			0	No hysteresis.				
			1	3.125%.				
			2	6.25%.				
			3	12.5% (default).				
			4	25%.				
			5	50%.				
			6	75%.				
			7	87.5%.				
0x0470	[7:0]	REFBB Validation Timer[7:0]		REFBB Reference Validation Time. This 20-bit unsigned value, validation time in units of milliseconds (default = 10), defines a minimum time interval, t_{VALID} (units of seconds), for which a faulted reference must remain unfaulted before the reference monitor indicates the reference as valid. Validation time relates to t_{VALID} as follows: *Validation Time* = 1000 × t_{VALID} For example, for a validation time of t_{VALID} = 10 min (600 sec), then validation time = 600,000 (0x927C0). The default value yields t_{VALID} = 10 ms. The maximum value of validation time equates to t_{VALID} = 1048.755 sec (~17.5 min).	0x10	R/W	Live	No
0x0471	[7:0]	REFBB Validation Timer[15:8]		Continuation of the REFBB validation timer bit field. See the REFBB Validation Timer[7:0] description.	0x00	R/W	Live	No
0x0472	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	[3:0]	REFBB Validation Timer[19:16]		Continuation of the REFBB validation timer bit field. See the REFBB Validation Timer[7:0] description.	0x0	R/W	Live	No
0x0473	[7:0]	REFBB Jitter Tolerance[7:0]		REFBB Reference Jitter Tolerance. This 16-bit unsigned value, jitter tolerance in units of nanoseconds (default = 0), defines the maximum rms jitter the reference monitor accepts before indicating an excess jitter condition. Jitter tolerance relates to the maximum acceptable rms jitter, t_{J_MAX} (units of seconds), as follows: *Jitter Tolerance* = $t_{J\_MAX} \times 10^9$ For example, given $t_{J\_MAX} = 75 \times 10^{-9}$ sec rms (75 ns), then jitter tolerance = 75 (0x004B). Jitter Tolerance = 0 prevents the reference monitor from including its estimation of jitter as part of the excess noise status decision, but the reference monitor continues to perform jitter estimation to continue making out of tolerance decisions.	0x00	R/W	Live	No
0x0474	[7:0]	REFBB Jitter Tolerance[15:8]		Continuation of the REFBB jitter tolerance bit field. See the REFBB Jitter Tolerance[7:0] description.	0x00	R/W	Live	No

REFERENCE INPUT PARAMETERS: AUXILIARY REF0—REGISTER 0x0480 TO REGISTER 0x0494

Table 18. Reference Input Parameters: Auxiliary REF0 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0480	[7:0]	Auxiliary REF0 R Divide Ratio[7:0]		Auxiliary REF0 Input Divider. This 30-bit unsigned value, RDIV (default = 0), sets the division factor, R, for the reference input divider, where R relates to RDIV as follows: $R = RDIV + 1$ For example, RDIV = 0 equates to R = 1.	0x00	R/W	Live	No
0x0481	[7:0]	Auxiliary REF0 R Divide Ratio[15:8]		Continuation of the Auxiliary REF0 R divide ratio bit field. See the Auxiliary REF0 R Divide Ratio[7:0] description.	0x00	R/W	Live	No
0x0482	[7:0]	Auxiliary REF0 R Divide Ratio[23:16]		Continuation of the Auxiliary REF0 R divide ratio bit field. See the Auxiliary REF0 R Divide Ratio[7:0] description.	0x00	R/W	Live	No
0x0483	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	[5:0]	Auxiliary REF0 R Divide Ratio[29:24]		Continuation of the Auxiliary REF0 R divide ratio bit field. See the Auxiliary REF0 R Divide Ratio[7:0] description.	0x00	R/W	Live	No
0x0484	[7:0]	Auxiliary REF0 Nominal Period[7:0]		Auxiliary REF0 Nominal Reference Period. This 60-bit unsigned value, $PERIOD_{AUX0}$ (default = 0) in units of attoseconds (10^{-18} sec), constitutes the declaration by the user of the nominal reference input period, t_{REF}, where $t_{REF} = 1/f_{REF}$. $PERIOD_{AUX0}$ (rounded to the nearest integer) relates to f_{REF} as follows: $PERIOD_{AUX0} = 10^{18}/f_{REF}$ For example, given f_{REF} = 2.048 MHz, then $PERIOD_{AUX0}$ = 488,281,250,000 (0x71 AFD4 98D0).	0x00	R/W	Live	No
0x0485	[7:0]	Auxiliary REF0 Nominal Period[15:8]		Continuation of the Auxiliary REF0 nominal period bit field. See the Auxiliary REF0 Nominal Period[7:0] description.	0x00	R/W	Live	No
0x0486	[7:0]	Auxiliary REF0 Nominal Period[23:16]		Continuation of the Auxiliary REF0 nominal period bit field. See the Auxiliary REF0 Nominal Period[7:0] description.	0x00	R/W	Live	No
0x0487	[7:0]	Auxiliary REF0 Nominal Period[31:24]		Continuation of the Auxiliary REF0 nominal period bit field. See the Auxiliary REF0 Nominal Period[7:0] description.	0x00	R/W	Live	No
0x0488	[7:0]	Auxiliary REF0 Nominal Period[39:32]		Continuation of the Auxiliary REF0 nominal period bit field. See the Auxiliary REF0 Nominal Period[7:0] description.	0x00	R/W	Live	No
0x0489	[7:0]	Auxiliary REF0 Nominal Period[47:40]		Continuation of the Auxiliary REF0 nominal period bit field. See the Auxiliary REF0 Nominal Period[7:0] description.	0x00	R/W	Live	No
0x048A	[7:0]	Auxiliary REF0 Nominal Period[55:48]		Continuation of the Auxiliary REF0 nominal period bit field. See the Auxiliary REF0 Nominal Period[7:0] description.	0x00	R/W	Live	No
0x048B	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	[3:0]	Auxiliary REF0 Nominal Period[59:56]		Continuation of the Auxiliary REF0 nominal period bit field. See the Auxiliary REF0 Nominal Period[7:0] description.	0x0	R/W	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x048C	[7:0]	Auxiliary REF0 Offset Limit[7:0]		Auxiliary REF0 Maximum Reference Period Deviation. This 24-bit unsigned value, threshold, in units of parts per billion (ppb) (default = 100,000), constitutes a fractional value with a maximum of 2^{24} ppb (~1.68%) and the default value equating to 100 ppm. Threshold is the magnitude of the relative deviation of the input period from t_{REF} beyond which the reference monitor declares a nonfaulted reference as out of tolerance (that is, slow or fast). Relative period deviation, δp, relates to relative frequency deviation, δf, as follows: $\delta p = (-\delta f)/(1 + \delta f)$ Because threshold is unsigned, it relates to δf as follows: $Threshold = |\delta f/(1 + \delta f)| \times 10^9$ For example, given a maximum desired relative frequency deviation of $\delta f = 75 \times 10^{-6}$ (that is, 75 ppm), threshold = 74994 (0x01 24F2) rounded to the nearest integer.	0x160	R/W	Live	No
0x048D	[7:0]	Auxiliary REF0 Offset Limit[15:8]		Continuation of the Auxiliary REF0 offset limit bit field. See the Auxiliary REF0 Offset Limit[7:0] description.	0x134	R/W	Live	No
0x048E	[7:0]	Auxiliary REF0 Offset Limit[23:16]		Continuation of the Auxiliary REF0 offset limit bit field. See the Auxiliary REF0 Offset Limit[7:0] description.	0x01	R/W	Live	No
0x048F	[7:3]	Reserved		Reserved.	0x00	R	Live	No
	[2:0]	Auxiliary REF0 monitor hysteresis		Auxiliary REF0 Reference Monitor Hysteresis. This 3-bit code (default = 3) selects a scale factor, SF, that together with threshold defines a certain amount of hysteresis given by $SF \times Threshold$ For example, given threshold = 74994 ppb and SF = 6.25%, the amount of hysteresis is 4687 ppb. The smaller the amount of hysteresis, the more likely the reference monitor chatters if the input reference period is near the limit of the allowable period error (threshold).	0x3	R/W	Live	No
			0	No hysteresis.				
			1	3.125%.				
			2	6.25%.				
			3	12.5% (default).				
			4	25%.				
			5	50%.				
			6	75%.				
			7	87.5%.				
0x0490	[7:0]	Auxiliary REF0 Validation Timer[7:0]		Auxiliary REF0 Reference Validation Time. This 20-bit unsigned value, validation time in units of milliseconds (default = 10), defines a minimum time interval, t_{VALID} (units of seconds), for which a faulted reference must remain unfaulted before the reference monitor indicates the reference as valid. Validation time relates to t_{VALID} as follows: $Validation\ Time = 1000 \times t_{VALID}$ For example, for a validation time of t_{VALID} = 10 min (600 sec), then validation time = 600,000 (0x927C0). The default value yields t_{VALID} = 10 ms. The maximum value of validation time equates to t_{VALID} = 1048.755 sec (~17.5 min).	0x10	R/W	Live	No
0x0491	[7:0]	Auxiliary REF0 Validation Timer[15:8]		Continuation of the Auxiliary REF0 validation timer bit field. See the Auxiliary REF0 Validation Timer[7:0] description.	0x00	R/W	Live	No
0x0492	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	[3:0]	Auxiliary REF0 Validation Timer[19:16]		Continuation of the Auxiliary REF0 validation timer bit field. See the Auxiliary REF0 Validation Timer[7:0] description.	0x0	R/W	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0493	[7:0]	Auxiliary REF0 Jitter Tolerance[7:0]		Auxiliary REF0 Reference Jitter Tolerance. This 16-bit unsigned value, jitter tolerance in units of nanoseconds (default = 0), defines the maximum rms jitter the reference monitor accepts before indicating an excess jitter condition. Jitter tolerance relates to the maximum acceptable rms jitter, t_{J_MAX} (units of seconds), as follows: $Jitter\ Tolerance = t_{J\_MAX} \times 10^{9}$ For example, given $t_{J\_MAX} = 75 \times 10^{-9}$ sec rms (75 ns), then jitter tolerance = 75 (0x004B). Jitter Tolerance = 0 prevents the reference monitor from including its estimation of jitter as part of the excess noise status decision, but the reference monitor continues to perform jitter estimation to continue making out of tolerance decisions.	0x00	R/W	Live	No
0x0494	[7:0]	Auxiliary REF0 Jitter Tolerance[15:8]		Continuation of the Auxiliary REF0 jitter tolerance bit field. See the Auxiliary REF0 Jitter Tolerance[7:0] description.	0x00	R/W	Live	No

REFERENCE INPUT PARAMETERS: AUXILIARY REF1—REGISTER 0x04A0 TO REGISTER 0x04B4

Table 19. Reference Input Parameters: Auxiliary REF1 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x04A0	[7:0]	Auxiliary REF1 R Divide Ratio[7:0]		Auxiliary REF1 Input Divider. This 30-bit unsigned value, RDIV (default = 0), sets the division factor, R, for the reference input divider, where R relates to RDIV as follows: $R = RDIV + 1$ For example, RDIV = 0 equates to R = 1.	0x00	R/W	Live	No
0x04A1	[7:0]	Auxiliary REF1 R Divide Ratio[15:8]		Continuation of the Auxiliary REF1 R divide ratio bit field. See the Auxiliary REF1 R Divide Ratio[7:0] description.	0x00	R/W	Live	No
0x04A2	[7:0]	Auxiliary REF1 R Divide Ratio[23:16]		Continuation of the Auxiliary REF1 R divide ratio bit field. See the Auxiliary REF1 R Divide Ratio[7:0] description.	0x00	R/W	Live	No
0x04A3	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	[5:0]	Auxiliary REF1 R Divide Ratio[29:24]		Continuation of the Auxiliary REF1 R divide ratio bit field. See the Auxiliary REF1 R Divide Ratio[7:0] description.	0x00	R/W	Live	No
0x04A4	[7:0]	Auxiliary REF1 Nominal Period[7:0]		Auxiliary REF1 Nominal Reference Period. This 60-bit unsigned value, $PERIOD_{AUX1}$ (default = 0) in units of attoseconds (10^{-18} sec), constitutes the declaration by the user of the nominal reference input period, t_{REF}, where $t_{REF} = 1/f_{REF}$. $PERIOD_{AUX1}$ (rounded to the nearest integer) relates to f_{REF} as follows: $PERIOD_{AUX1} = 10^{18}/f_{REF}$ For example, given f_{REF} = 2.048 MHz, then $PERIOD_{AUX1}$ = 488,281,250,000 (0x71 AFD4 98D0).	0x00	R/W	Live	No
0x04A5	[7:0]	Auxiliary REF1 Nominal Period[15:8]		Continuation of the Auxiliary REF1 nominal period bit field. See the Auxiliary REF1 Nominal Period[7:0] description.	0x00	R/W	Live	No
0x04A6	[7:0]	Auxiliary REF1 Nominal Period[23:16]		Continuation of the Auxiliary REF1 nominal period bit field. See the Auxiliary REF1 Nominal Period[7:0] description.	0x00	R/W	Live	No
0x04A7	[7:0]	Auxiliary REF1 Nominal Period[31:24]		Continuation of the Auxiliary REF1 nominal period bit field. See the Auxiliary REF1 Nominal Period[7:0] description.	0x00	R/W	Live	No
0x04A8	[7:0]	Auxiliary REF1 Nominal Period[39:32]		Continuation of the Auxiliary REF1 nominal period bit field. See the Auxiliary REF1 Nominal Period[7:0] description.	0x00	R/W	Live	No
0x04A9	[7:0]	Auxiliary REF1 Nominal Period[47:40]		Continuation of the Auxiliary REF1 nominal period bit field. See the Auxiliary REF1 Nominal Period[7:0] description.	0x00	R/W	Live	No
0x04AA	[7:0]	Auxiliary REF1 Nominal Period[55:48]		Continuation of the Auxiliary REF1 nominal period bit field. See the Auxiliary REF1 Nominal Period[7:0] description.	0x00	R/W	Live	No
0x04AB	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	[3:0]	Auxiliary REF1 Nominal Period[59:56]		Continuation of the Auxiliary REF1 nominal period bit field. See the Auxiliary REF1 Nominal Period[7:0] description.	0x0	R/W	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x04AC	[7:0]	Auxiliary REF1 Offset Limit[7:0]		Auxiliary REF1 Maximum Reference Period Deviation. This 24-bit unsigned value, threshold, in units of parts per billion (ppb) (default = 100,000), constitutes a fractional value with a maximum of 2^{24} ppb (~1.68%) and the default value equating to 100 ppm. Threshold is the magnitude of the relative deviation of the input period from t_{REF} beyond which the reference monitor declares a nonfaulted reference as out of tolerance (that is, slow or fast). Relative period deviation, δp, relates to relative frequency deviation, δf, as follows: $\delta p = (-\delta f)/(1 + \delta f)$ Because threshold is unsigned, it relates to δf as follows: $Threshold = |\delta f/(1 + \delta f)| \times 10^9$ For example, given a maximum desired relative frequency deviation of $\delta f = 75 \times 10^{-6}$ (that is, 75 ppm), threshold = 74994 (0x01 24F2) rounded to the nearest integer.	0x160	R/W	Live	No
0x04AD	[7:0]	Auxiliary REF1 Offset Limit[15:8]		Continuation of the Auxiliary REF1 offset limit bit field. See the Auxiliary REF1 Offset Limit[7:0] description.	0x134	R/W	Live	No
0x04AE	[7:0]	Auxiliary REF1 Offset Limit[23:16]		Continuation of the Auxiliary REF1 offset limit bit field. See the Auxiliary REF1 Offset Limit[7:0] description.	0x01	R/W	Live	No
0x04AF	[7:3]	Reserved		Reserved.	0x00	R	Live	No
	[2:0]	Auxiliary REF1 monitor hysteresis		Auxiliary REF1 Reference Monitor Hysteresis. This 3-bit code (default = 3) selects a scale factor, SF, that together with threshold defines a certain amount of hysteresis given by $SF \times Threshold$ For example, given threshold = 74994 ppb and SF = 6.25%, the amount of hysteresis is 4687 ppb. The smaller the amount of hysteresis, the more likely the reference monitor chatters if the input reference period is near the limit of the allowable period error (threshold).	0x3	R/W	Live	No
			0	No hysteresis.				
			1	3.125%.				
			2	6.25%.				
			3	12.5% (default).				
			4	25%.				
			5	50%.				
			6	75%.				
			7	87.5%.				
0x04B0	[7:0]	Auxiliary REF1 Validation Timer[7:0]		Auxiliary REF1 Reference Validation Time. This 20-bit unsigned value, validation time in units of milliseconds (default = 10), defines a minimum time interval, t_{VALID} (units of seconds), for which a faulted reference must remain unfaulted before the reference monitor indicates the reference as valid. Validation time relates to t_{VALID} as follows: $Validation\ Time = 1000 \times t_{VALID}$ For example, for a validation time of t_{VALID} = 10 min (600 sec), then validation time = 600,000 (0x927C0). The default value yields t_{VALID} = 10 ms. The maximum value of validation time equates to t_{VALID} = 1048.755 sec (~17.5 min).	0x10	R/W	Live	No
0x04B1	[7:0]	Auxiliary REF1 Validation Timer[15:8]		Continuation of the Auxiliary REF1 validation timer bit field. See the Auxiliary REF1 Validation Timer[7:0] description.	0x00	R/W	Live	No
0x04B2	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	[3:0]	Auxiliary REF1 Validation Timer[19:16]		Continuation of the Auxiliary REF1 validation timer bit field. See the Auxiliary REF1 Validation Timer[7:0] description.	0x0	R/W	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x04B3	[7:0]	Auxiliary REF1 Jitter Tolerance[7:0]		Auxiliary REF1 Reference Jitter Tolerance. This 16-bit unsigned value, jitter tolerance in units of nanoseconds (default = 0), defines the maximum rms jitter the reference monitor accepts before indicating an excess jitter condition. Jitter tolerance relates to the maximum acceptable rms jitter, t_{J_MAX} (units of seconds), as follows: $Jitter\ Tolerance = t_{J\_MAX} \times 10^{9}$ For example, given $t_{J\_MAX} = 75 \times 10^{-9}$ sec rms (75 ns), then jitter tolerance = 75 (0x004B). Jitter Tolerance = 0 prevents the reference monitor from including its estimation of jitter as part of the excess noise status decision, but the reference monitor continues to perform jitter estimation to continue making out of tolerance decisions.	0x00	R/W	Live	No
0x04B4	[7:0]	Auxiliary REF1 Jitter Tolerance[15:8]		Continuation of the Auxiliary REF1 jitter tolerance bit field. See the Auxiliary REF1 Jitter Tolerance[7:0] description.	0x00	R/W	Live	No

REFERENCE INPUT PARAMETERS: AUXILIARY REF2—REGISTER 0x04C0 TO REGISTER 0x04D4

Table 20. Reference Input Parameters: Auxiliary REF2 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x04C0	[7:0]	Auxiliary REF2 R Divide Ratio[7:0]		Auxiliary REF2 Input Divider. This 30-bit unsigned value, RDIV (default = 0), sets the division factor, R, for the reference input divider, where R relates to RDIV as follows: $R = RDIV + 1$ For example, RDIV = 0 equates to R = 1.	0x00	R/W	Live	No
0x04C1	[7:0]	Auxiliary REF2 R Divide Ratio[15:8]		Continuation of the Auxiliary REF2 R divide ratio bit field. See the Auxiliary REF2 R Divide Ratio[7:0] description.	0x00	R/W	Live	No
0x04C2	[7:0]	Auxiliary REF2 R Divide Ratio[23:16]		Continuation of the Auxiliary REF2 R divide ratio bit field. See the Auxiliary REF2 R Divide Ratio[7:0] description.	0x00	R/W	Live	No
0x04C3	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	[5:0]	Auxiliary REF2 R Divide Ratio[29:24]		Continuation of the Auxiliary REF2 R divide ratio bit field. See the Auxiliary REF2 R Divide Ratio[7:0] description.	0x00	R/W	Live	No
0x04C4	[7:0]	Auxiliary REF2 Nominal Period[7:0]		Auxiliary REF2 Nominal Reference Period. This 60-bit unsigned value, $PERIOD_{AUX2}$ (default = 0) in units of attoseconds (10^{-18} sec), constitutes the declaration by the user of the nominal reference input period, t_{REF}, where $t_{REF} = 1/f_{REF}$. $PERIOD_{AUX2}$ (rounded to the nearest integer) relates to f_{REF} as follows: $PERIOD_{AUX2} = 10^{18}/f_{REF}$ For example, given f_{REF} = 2.048 MHz, then $PERIOD_{AUX2}$ = 488,281,250,000 (0x71 AFD4 98D0).	0x00	R/W	Live	No
0x04C5	[7:0]	Auxiliary REF2 Nominal Period[15:8]		Continuation of the Auxiliary REF2 nominal period bit field. See the Auxiliary REF2 Nominal Period[7:0] description.	0x00	R/W	Live	No
0x04C6	[7:0]	Auxiliary REF2 Nominal Period[23:16]		Continuation of the Auxiliary REF2 nominal period bit field. See the Auxiliary REF2 Nominal Period[7:0] description.	0x00	R/W	Live	No
0x04C7	[7:0]	Auxiliary REF2 Nominal Period[31:24]		Continuation of the Auxiliary REF2 nominal period bit field. See the Auxiliary REF2 Nominal Period[7:0] description.	0x00	R/W	Live	No
0x04C8	[7:0]	Auxiliary REF2 Nominal Period[39:32]		Continuation of the Auxiliary REF2 nominal period bit field. See the Auxiliary REF2 Nominal Period[7:0] description.	0x00	R/W	Live	No
0x04C9	[7:0]	Auxiliary REF2 Nominal Period[47:40]		Continuation of the Auxiliary REF2 nominal period bit field. See the Auxiliary REF2 Nominal Period[7:0] description.	0x00	R/W	Live	No
0x04CA	[7:0]	Auxiliary REF2 Nominal Period[55:48]		Continuation of the Auxiliary REF2 nominal period bit field. See the Auxiliary REF2 Nominal Period[7:0] description.	0x00	R/W	Live	No
0x04CB	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	[3:0]	Auxiliary REF2 Nominal Period[59:56]		Continuation of the Auxiliary REF2 nominal period bit field. See the Auxiliary REF2 Nominal Period[7:0] description.	0x0	R/W	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x04CC	[7:0]	Auxiliary REF2 Offset Limit[7:0]		Auxiliary REF2 Maximum Reference Period Deviation. This 24-bit unsigned value, threshold, in units of parts per billion (ppb) (default = 100,000), constitutes a fractional value with a maximum of 2^{24} ppb (~1.68%) and the default value equating to 100 ppm. Threshold is the magnitude of the relative deviation of the input period from t_{REF} beyond which the reference monitor declares a nonfaulted reference as out of tolerance (that is, slow or fast). Relative period deviation, δp, relates to relative frequency deviation, δf, as follows: $\delta p = (-\delta f)/(1 + \delta f)$ Because threshold is unsigned, it relates to δf as follows: $Threshold = |\delta f/(1 + \delta f)| \times 10^9$ For example, given a maximum desired relative frequency deviation of $\delta f = 75 \times 10^{-6}$ (that is, 75 ppm), threshold = 74994 (0x01 24F2) rounded to the nearest integer.	0x160	R/W	Live	No
0x04CD	[7:0]	Auxiliary REF2 Offset Limit[15:8]		Continuation of the Auxiliary REF2 offset limit bit field. See the Auxiliary REF2 Offset Limit[7:0] description.	0x134	R/W	Live	No
0x04CE	[7:0]	Auxiliary REF2 Offset Limit[23:16]		Continuation of the Auxiliary REF2 offset limit bit field. See the Auxiliary REF2 Offset Limit[7:0] description.	0x01	R/W	Live	No
0x04CF	[7:3]	Reserved		Reserved.	0x00	R	Live	No
	[2:0]	Auxiliary REF2 monitor hysteresis		Auxiliary REF2 Reference Monitor Hysteresis. This 3-bit code (default = 3) selects a scale factor, SF, that together with threshold defines a certain amount of hysteresis given by $SF \times Threshold$ For example, given threshold = 74994 ppb and SF = 6.25%, the amount of hysteresis is 4687 ppb. The smaller the amount of hysteresis, the more likely the reference monitor chatters if the input reference period is near the limit of the allowable period error (threshold).	0x3	R/W	Live	No
			0	No hysteresis.				
			1	3.125%.				
			2	6.25%.				
			3	12.5% (default).				
			4	25%.				
			5	50%.				
			6	75%.				
			7	87.5%.				
0x04D0	[7:0]	Auxiliary REF2 Validation Timer[7:0]		Auxiliary REF2 Reference Validation Time. This 20-bit unsigned value, validation time in units of milliseconds (default = 10), defines a minimum time interval, t_{VALID} (units of seconds), for which a faulted reference must remain unfaulted before the reference monitor indicates the reference as valid. Validation time relates to t_{VALID} as follows: $Validation\ Time = 1000 \times t_{VALID}$ For example, for a validation time of t_{VALID} = 10 min (600 sec), then validation time = 600,000 (0x927C0). The default value yields t_{VALID} = 10 ms. The maximum value of validation time equates to t_{VALID} = 1048.755 sec (~17.5 min).	0x10	R/W	Live	No
0x04D1	[7:0]	Auxiliary REF2 Validation Timer[15:8]		Continuation of the Auxiliary REF2 validation timer bit field. See the Auxiliary REF0 Validation Timer[7:0] description.	0x00	R/W	Live	No
0x04D2	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	[3:0]	Auxiliary REF2 Validation Timer[19:16]		Continuation of the Auxiliary REF0 validation timer bit field. See the Auxiliary REF2 Validation Timer[7:0] description.	0x0	R/W	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x04D3	[7:0]	Auxiliary REF2 Jitter Tolerance[7:0]		Auxiliary REF2 Reference Jitter Tolerance. This 16-bit unsigned value, jitter tolerance in units of nanoseconds (default = 0), defines the maximum rms jitter the reference monitor accepts before indicating an excess jitter condition. Jitter tolerance relates to the maximum acceptable rms jitter, t_{J_MAX} (units of seconds), as follows: $Jitter\ Tolerance = t_{J\_MAX} \times 10^{9}$ For example, given $t_{J\_MAX} = 75 \times 10^{-9}$ sec rms (75 ns), then jitter tolerance = 75 (0x004B). Jitter Tolerance = 0 prevents the reference monitor from including its estimation of jitter as part of the excess noise status decision, but the reference monitor continues to perform jitter estimation to continue making out of tolerance decisions.	0x00	R/W	Live	No
0x04D4	[7:0]	Auxiliary REF2 Jitter Tolerance[15:8]		Continuation of the Auxiliary REF2 jitter tolerance bit field. See the Auxiliary REF2 Jitter Tolerance[7:0] description.	0x00	R/W	Live	No

REFERENCE INPUT PARAMETERS: AUXILIARY REF3—REGISTER 0x04E0 TO REGISTER 0x04F4

Table 21. Reference Input Parameters: Auxiliary REF3 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x04E0	[7:0]	Auxiliary REF3 R Divide Ratio[7:0]		Auxiliary REF3 Input Divider. This 30-bit unsigned value, RDIV (default = 0), sets the division factor, R, for the reference input divider, where R relates to RDIV as follows: $R = RDIV + 1$ For example, RDIV = 0 equates to R = 1.	0x00	R/W	Live	No
0x04E1	[7:0]	Auxiliary REF3 R Divide Ratio[15:8]		Continuation of the Auxiliary REF3 R divide ratio bit field. See the Auxiliary REF3 R Divide Ratio[7:0] description.	0x00	R/W	Live	No
0x04E2	[7:0]	Auxiliary REF3 R Divide Ratio[23:16]		Continuation of the Auxiliary REF3 R divide ratio bit field. See the Auxiliary REF3 R Divide Ratio[7:0] description.	0x00	R/W	Live	No
0x04E3	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	[5:0]	Auxiliary REF3 R Divide Ratio[29:24]		Continuation of the Auxiliary REF3 R divide ratio bit field. See the Auxiliary REF3 R Divide Ratio[7:0] description.	0x00	R/W	Live	No
0x04E4	[7:0]	Auxiliary REF3 Nominal Period[7:0]		Auxiliary REF3 Nominal Reference Period. This 60-bit unsigned value, $PERIOD_{AUX3}$ (default = 0) in units of attoseconds (10^{-18} sec), constitutes the declaration by the user of the nominal reference input period, t_{REF}, where $t_{REF} = 1/f_{REF}$. $PERIOD_{AUX3}$ (rounded to the nearest integer) relates to f_{REF} as follows: $PERIOD_{AUX3} = 10^{18}/f_{REF}$ For example, given f_{REF} = 2.048 MHz, then $PERIOD_{AUX3}$ = 488,281,250,000 (0x71 AFD4 98D0).	0x00	R/W	Live	No
0x04E5	[7:0]	Auxiliary REF3 Nominal Period[15:8]		Continuation of the Auxiliary REF3 nominal period bit field. See the Auxiliary REF3 Nominal Period[7:0] description.	0x00	R/W	Live	No
0x04E6	[7:0]	Auxiliary REF3 Nominal Period[23:16]		Continuation of the Auxiliary REF3 nominal period bit field. See the Auxiliary REF3 Nominal Period[7:0] description.	0x00	R/W	Live	No
0x04E7	[7:0]	Auxiliary REF3 Nominal Period[31:24]		Continuation of the Auxiliary REF3 nominal period bit field. See the Auxiliary REF3 Nominal Period[7:0] description.	0x00	R/W	Live	No
0x04E8	[7:0]	Auxiliary REF3 Nominal Period[39:32]		Continuation of the Auxiliary REF3 nominal period bit field. See the Auxiliary REF3 Nominal Period[7:0] description.	0x00	R/W	Live	No
0x04E9	[7:0]	Auxiliary REF3 Nominal Period[47:40]		Continuation of the Auxiliary REF3 nominal period bit field. See the Auxiliary REF3 Nominal Period[7:0] description.	0x00	R/W	Live	No
0x04EA	[7:0]	Auxiliary REF3 Nominal Period[55:48]		Continuation of the Auxiliary REF3 nominal period bit field. See the Auxiliary REF3 Nominal Period[7:0] description.	0x00	R/W	Live	No
0x04EB	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	[3:0]	Auxiliary REF3 Nominal Period[59:56]		Continuation of the Auxiliary REF3 nominal period bit field. See the Auxiliary REF3 Nominal Period[7:0] description.	0x0	R/W	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x04EC	[7:0]	Auxiliary REF3 Offset Limit[7:0]		Auxiliary REF3 Maximum Reference Period Deviation. This 24-bit unsigned value, threshold, in units of parts per billion (ppb) (default = 100,000), constitutes a fractional value with a maximum of 2^{24} ppb (~1.68%) and the default value equating to 100 ppm. Threshold is the magnitude of the relative deviation of the input period from t_{REF} beyond which the reference monitor declares a nonfaulted reference as out of tolerance (that is, slow or fast). Relative period deviation, δp, relates to relative frequency deviation, δf, as follows: $\delta p = (-\delta f)/(1 + \delta f)$ Because threshold is unsigned, it relates to δf as follows: $Threshold = |\delta f/(1 + \delta f)| \times 10^9$ For example, given a maximum desired relative frequency deviation of $\delta f = 75 \times 10^{-6}$ (that is, 75 ppm), threshold = 74994 (0x01 24F2) rounded to the nearest integer.	0x160	R/W	Live	No
0x04ED	[7:0]	Auxiliary REF3 Offset Limit[15:8]		Continuation of the Auxiliary REF3 offset limit bit field. See the Auxiliary REF3 Offset Limit[7:0] description.	0x134	R/W	Live	No
0x04EE	[7:0]	Auxiliary REF3 Offset Limit[23:16]		Continuation of the Auxiliary REF3 offset limit bit field. See the Auxiliary REF3 Offset Limit[7:0] description.	0x01	R/W	Live	No
0x04EF	[7:3]	Reserved		Reserved.	0x00	R	Live	No
	[2:0]	Auxiliary REF3 monitor hysteresis		Auxiliary REF0 Reference Monitor Hysteresis. This 3-bit code (default = 3) selects a scale factor, SF, that together with threshold defines a certain amount of hysteresis given by $SF \times Threshold$ For example, given threshold = 74994 ppb and SF = 6.25%, the amount of hysteresis is 4687 ppb. The smaller the amount of hysteresis, the more likely the reference monitor chatters if the input reference period is near the limit of the allowable period error (threshold).	0x3	R/W	Live	No
			0	No hysteresis.				
			1	3.125%.				
			2	6.25%.				
			3	12.5% (default).				
			4	25%.				
			5	50%.				
			6	75%.				
			7	87.5%.				
0x04F0	[7:0]	Auxiliary REF3 Validation Timer[7:0]		Auxiliary REF3 Reference Validation Time. This 20-bit unsigned value, validation time in units of milliseconds (default = 10), defines a minimum time interval, t_{VALID} (units of seconds), for which a faulted reference must remain unfaulted before the reference monitor indicates the reference as valid. Validation time relates to t_{VALID} as follows: $Validation\ Time = 1000 \times t_{VALID}$ For example, for a validation time of t_{VALID} = 10 min (600 sec), then validation time = 600,000 (0x927C0). The default value yields t_{VALID} = 10 ms. The maximum value of validation time equates to t_{VALID} = 1048.755 sec (~17.5 min).	0x10	R/W	Live	No
0x04F1	[7:0]	Auxiliary REF3 Validation Timer[15:8]		Continuation of the Auxiliary REF3 validation timer bit field. See the Auxiliary REF0 Validation Timer[7:0] description.	0x00	R/W	Live	No
0x04F2	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	[3:0]	Auxiliary REF3 Validation Timer[19:16]		Continuation of the Auxiliary REF3 validation timer bit field. See the Auxiliary REF0 Validation Timer[7:0] description.	0x0	R/W	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x04F3	[7:0]	Auxiliary REF3 Jitter Tolerance[7:0]		Auxiliary REF3 Reference Jitter Tolerance. This 16-bit unsigned value, jitter tolerance in units of nanoseconds (default = 0), defines the maximum rms jitter the reference monitor accepts before indicating an excess jitter condition. Jitter tolerance relates to the maximum acceptable rms jitter, t_{J_MAX} (units of seconds), as follows: $Jitter\ Tolerance = t_{J\_MAX} \times 10^9$ For example, given $t_{J\_MAX} = 75 \times 10^{-9}$ sec rms (75 ns), then jitter tolerance = 75 (0x004B). Jitter Tolerance = 0 prevents the reference monitor from including its estimation of jitter as part of the excess noise status decision, but the reference monitor continues to perform jitter estimation to continue making out of tolerance decisions.	0x00	R/W	Live	No
0x04F4	[7:0]	Auxiliary REF3 Jitter Tolerance[15:8]		Continuation of the Auxiliary REF3 jitter tolerance bit field. See the Auxiliary REF3 Jitter Tolerance[7:0] description.	0x00	R/W	Live	No

SOURCE PROFILE: REFA—REGISTER 0x0800 TO REGISTER 0x0811

Table 22. Source Profile: REFA Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0800	[7:0]	REFA Phase Lock Threshold[7:0]		REFA Phase Lock Threshold. Synopsis: The digital phase detector delivers time error samples (ε) to the phase lock detector, where ε is the difference in time between the rising edge of the reference and feedback inputs to the PFD of the DPLL. The phase lock detector compares the magnitude of each time sample (|ε|) to a user defined time threshold (t_{THRESH}). The comparison triggers a fill or drain event. Fill events (|ε| ≤ t_{THRESH}) steer the phase lock detector toward lock status. Drain events (|ε| > t_{THRESH}) steer the phase lock detector toward unlock status. This 24-bit unsigned value, phase lock threshold in units of picoseconds (default = 700), constitutes a time threshold, t_{THRESH} (seconds). Phase Lock Threshold (rounded to the nearest integer) relates to t_{THRESH} as follows: *Phase Lock Threshold* = $t_{THRESH} \times 10^{12}$ For example, for a desired value of $t_{THRESH} = 10^{-9}$ sec (1 ns), then Phase Lock Threshold = 1000 (0x 00 03E8). When the phase slew limiter is actively in the process of phase slew limiting, the phase lock detector inhibits fill events (only drain events can occur during phase slew limiting).	0x188	R/W	Live	No
0x0801	[7:0]	REFA Phase Lock Threshold[15:8]		Continuation of the REFA phase lock threshold bit field. See the REFA Phase Lock Threshold[7:0] description.	0x02	R/W	Live	No
0x0802	[7:0]	REFA Phase Lock Threshold[23:16]		Continuation of the REFA phase lock threshold bit field. See the REFA Phase Lock Threshold[7:0] description.	0x00	R/W	Live	No
0x0803	[7:0]	REFA phase lock fill rate		REFA Phase Lock Fill Rate. This 8-bit unsigned value, phase lock fill rate (default = 10), constitutes the size associated with a phase lock detector fill event. Phase Lock Fill Rate = 0 forces the DPLL to indicate phase lock status.	0x10	R/W	Live	No
0x0804	[7:0]	REFA phase lock drain rate		REFA Phase Lock Drain Rate. This 8-bit unsigned value, Phase Lock Drain Rate (default = 10), constitutes the size associated with a phase lock detector drain event. Phase Lock Drain Rate = 0 forces the DPLL to indicate phase unlock status.	0x10	R/W	Live	No
0x0805	[7:0]	REFA Frequency Lock Threshold[7:0]		REFA Frequency Lock Threshold. Synopsis: The digital frequency detector delivers time error samples (t_{DEV}) to the frequency lock detector, where t_{DEV} is the difference in period between the reference and feedback inputs to the PFD of the DPLL. The frequency lock detector compares the magnitude of each t_{DEV} sample to a user defined period error threshold (t_{P_ERR}). The comparison triggers a fill or drain event. Fill events (|t_{DEV}| ≤ t_{P_ERR}) steer the frequency lock detector toward lock status. Drain events (|t_{DEV}| > t_{P_ERR}) steer the frequency lock detector toward unlock status. This 24-bit unsigned value, Frequency Lock Threshold in units of picoseconds (default = 700), constitutes a period error threshold, t_{P_ERR} (seconds). Frequency Lock Threshold (rounded to the nearest integer) relates to t_{P_ERR} as follows: *Frequency Lock Threshold* = $t_{P\_ERR} \times 10^{12}$	0x188	R/W	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
				In practice, it is convenient to specify an offset frequency, Δf, as a frequency lock threshold, where Δf is relative to the nominal reference frequency, f_R, at the input to the PFD. Frequency Lock Threshold (rounded to the nearest integer) relates to Δf and f_R as follows: *Frequency Lock Threshold* = $(\Delta f/f_R)(1/(f_R + \Delta f)) \times 10^{12}$ For example, given $f_R = 8 \times 10^4$ (80 kHz) and Δf = 100 Hz, then Frequency Lock Threshold = 15,605 (0x 00 3CF5). The phase slew limiter has no effect on the operation of the frequency lock detector.				
0x0806	[7:0]	REFA Frequency Lock Threshold[15:8]		Continuation of the REFA frequency lock threshold bit field. See the REFA Frequency Lock Threshold[7:0] description.	0x02	R/W	Live	No
0x0807	[7:0]	REFA Frequency Lock Threshold[23:16]		Continuation of the REFA frequency lock threshold bit field. See the REFA Frequency Lock Threshold[7:0] description.	0x00	R/W	Live	No
0x0808	[7:0]	REFA frequency lock fill rate		REFA Frequency Lock Fill Rate. This 8-bit unsigned value, Frequency Lock Fill Rate (default = 10), constitutes the size associated with a frequency lock detector fill event. Frequency Lock Fill Rate = 0 forces the DPLL to indicate frequency lock status.	0x10	R/W	Live	No
0x0809	[7:0]	REFA frequency lock drain rate		REFA Frequency Lock Drain Rate. This 8-bit unsigned value, Frequency Lock Drain Rate (default = 10), constitutes the size associated with a frequency lock detector drain event. Frequency Lock Drain Rate = 0 forces the DPLL to indicate frequency unlock status.	0x10	R/W	Live	No
0x080A	[7:0]	REFA Phase Step Threshold[7:0]		REFA Phase Step Detector Threshold. This 32-bit unsigned value, Phase Step Threshold in units of picoseconds (default = 0), sets the time threshold (Φ_{THRESH} (seconds)) at which the DPLL declares that an input reference phase step has occurred. Phase Step Threshold = 0 (default) disables the phase step detector. Phase Step Threshold (rounded to the nearest integer) relates to Φ_{THRESH} as follows: *Phase Step Threshold* = $\Phi_{THRESH} \times 10^{12}$ For example, given a desired time threshold of $\Phi_{THRESH} = 12 \times 10^{-9}$ (12 ns), then Phase Step Threshold = 12,000 (0x 0000 2EE0). The user must choose a large enough value for phase step threshold to ensure the phase step detector activates only as a result of a reference switching event and not during normal DPLL operation.	0x00	R/W	Live	No
0x080B	[7:0]	REFA Phase Step Threshold[15:8]		Continuation of the REFA phase step threshold bit field. See the REFA Phase Step Threshold[7:0] description.	0x00	R/W	Live	No
0x080C	[7:0]	REFA Phase Step Threshold[23:16]		Continuation of the REFA phase step threshold bit field. See the REFA Phase Step Threshold[7:0] description.	0x00	R/W	Live	No
0x080D	[7:0]	REFA Phase Step Threshold[31:24]		Continuation of the REFA phase step threshold bit field. See the REFA Phase Step Threshold[7:0] description.	0x00	R/W	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x080E	[7:0]	REFA Phase Skew[7:0]		REFA Phase Skew. This 24-bit signed value, Phase Skew in units of picoseconds (default = 0) defines a time skew for the phase skew adjustment feature. Time skew effectively constitutes a phase offset applied to the reference input associated with this source profile. Phase Skew (rounded to the nearest integer) relates to Time Skew as follows: $Phase\ Skew = Time\ Skew \times 10^{12}$ For example, given Time Skew = -35×10^{-9} (−35 ns), then Phase Skew = −35,000 (0x FF 7748). Phase Skew = 0 disables the phase skew adjustment feature.	0x00	R/W	Core clock	No
0x080F	[7:0]	REFA Phase Skew[15:8]		Continuation of the REFA phase skew bit field. See the REFA Phase Skew[7:0] description.	0x00	R/W	Core clock	No
0x0810	[7:0]	REFA Phase Skew[23:16]		Continuation of the REFA phase skew bit field. See the REFA Phase Skew[7:0] description.	0x00	R/W	Core clock	No
0x0811	[7:0]	REFA phase skew refinement steps		REFA Phase Skew Refinement Steps. This 8-bit unsigned value defines the number of DPLL PFD cycles the phase buildout processor uses in a phase buildout acquisition to assess the magnitude of phase buildout. The processor does not apply the buildout phase until the designated number of DPLL PFD cycles occurs. A value of zero (default) disables the phase skew refinement feature.	0x00	R/W	Live	No

SOURCE PROFILE: REFAA—REGISTER 0x0820 TO REGISTER 0x0831

Table 23. Source Profile: REFAA Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0820	[7:0]	REFAA Phase Lock Threshold[7:0]		REFAA Phase Lock Threshold. Synopsis: The digital phase detector delivers time error samples (ε) to the phase lock detector, where ε is the difference in time between the rising edge of the reference and feedback inputs to the PFD of the DPLL. The phase lock detector compares the magnitude of each time sample (|ε|) to a user defined time threshold (t_{THRESH}). The comparison triggers a fill or drain event. Fill events (|ε| ≤ t_{THRESH}) steer the phase lock detector toward lock status. Drain events (|ε| > t_{THRESH}) steer the phase lock detector toward unlock status. This 24-bit unsigned value, phase lock threshold in units of picoseconds (default = 700), constitutes a time threshold, t_{THRESH} (seconds). Phase Lock Threshold (rounded to the nearest integer) relates to t_{THRESH} as follows: *Phase Lock Threshold* = $t_{THRESH} \times 10^{12}$ For example, for a desired value of $t_{THRESH} = 10^{-9}$ sec (1 ns), then Phase Lock Threshold = 1000 (0x 00 03E8). When the phase slew limiter is actively in the process of phase slew limiting, the phase lock detector inhibits fill events (only drain events can occur during phase slew limiting).	0x188	R/W	Live	No
0x0821	[7:0]	REFAA Phase Lock Threshold[15:8]		Continuation of the REFAA phase lock threshold bit field. See the REFAA Phase Lock Threshold[7:0] description.	0x02	R/W	Live	No
0x0822	[7:0]	REFAA Phase Lock Threshold[23:16]		Continuation of the REFAA phase lock threshold bit field. See the REFAA Phase Lock Threshold[7:0] description.	0x00	R/W	Live	No
0x0823	[7:0]	REFAA phase lock fill rate		REFAA Phase Lock Fill Rate. This 8-bit unsigned value, phase lock fill rate (default = 10), constitutes the size associated with a phase lock detector fill event. Phase Lock Fill Rate = 0 forces the DPLL to indicate phase lock status.	0x10	R/W	Live	No
0x0824	[7:0]	REFAA phase lock drain rate		REFAA Phase Lock Drain Rate. This 8-bit unsigned value, Phase Lock Drain Rate (default = 10), constitutes the size associated with a phase lock detector drain event. Phase Lock Drain Rate = 0 forces the DPLL to indicate phase unlock status.	0x10	R/W	Live	No
0x0825	[7:0]	REFAA Frequency Lock Threshold[7:0]		REFAA Frequency Lock Threshold. Synopsis: The digital frequency detector delivers time error samples (t_{DEV}) to the frequency lock detector, where t_{DEV} is the difference in period between the reference and feedback inputs to the PFD of the DPLL. The frequency lock detector compares the magnitude of each t_{DEV} sample to a user defined period error threshold (t_{P_ERR}). The comparison triggers a fill or drain event. Fill events (|t_{DEV}| ≤ t_{P_ERR}) steer the frequency lock detector toward lock status. Drain events (|t_{DEV}| > t_{P_ERR}) steer the frequency lock detector toward unlock status. This 24-bit unsigned value, Frequency Lock Threshold in units of picoseconds (default = 700), constitutes a period error threshold, t_{P_ERR} (seconds). Frequency Lock Threshold (rounded to the nearest integer) relates to t_{P_ERR} as follows: *Frequency Lock Threshold* = $t_{P\_ERR} \times 10^{12}$	0x188	R/W	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
				In practice, it is convenient to specify an offset frequency, Δf, as a frequency lock threshold, where Δf is relative to the nominal reference frequency, f_R, at the input to the PFD. Frequency Lock Threshold (rounded to the nearest integer) relates to Δf and f_R as follows: *Frequency Lock Threshold* = $(\Delta f/f_R)(1/(f_R + \Delta f)) \times 10^{12}$ For example, given $f_R = 8 \times 10^4$ (80 kHz) and Δf = 100 Hz, then Frequency Lock Threshold = 15,605 (0x 00 3CF5). The phase slew limiter has no effect on the operation of the frequency lock detector.				
0x0826	[7:0]	REFAA Frequency Lock Threshold[15:8]		Continuation of the REFAA frequency lock threshold bit field. See the REFAA Frequency Lock Threshold[7:0] description.	0x02	R/W	Live	No
0x0827	[7:0]	REFAA Frequency Lock Threshold[23:16]		Continuation of the REFAA frequency lock threshold bit field. See the REFAA Frequency Lock Threshold[7:0] description.	0x00	R/W	Live	No
0x0828	[7:0]	REFAA frequency lock fill rate		REFAA Frequency Lock Fill Rate. This 8-bit unsigned value, Frequency Lock Fill Rate (default = 10), constitutes the size associated with a frequency lock detector fill event. Frequency Lock Fill Rate = 0 forces the DPLL to indicate frequency lock status.	0x10	R/W	Live	No
0x0829	[7:0]	REFAA frequency lock drain rate		REFAA Frequency Lock Drain Rate. This 8-bit unsigned value, Frequency Lock Drain Rate (default = 10), constitutes the size associated with a frequency lock detector drain event. Frequency Lock Drain Rate = 0 forces the DPLL to indicate frequency unlock status.	0x10	R/W	Live	No
0x082A	[7:0]	REFAA Phase Step Threshold[7:0]		REFAA Phase Step Detector Threshold. This 32-bit unsigned value, Phase Step Threshold in units of picoseconds (default = 0), sets the time threshold (Φ_{THRESH} (seconds)) at which the DPLL declares that an input reference phase step has occurred. Phase Step Threshold = 0 (default) disables the phase step detector. Phase Step Threshold (rounded to the nearest integer) relates to Φ_{THRESH} as follows: *Phase Step Threshold* = $\Phi_{THRESH} \times 10^{12}$ For example, given a desired time threshold of $\Phi_{THRESH} = 12 \times 10^{-9}$ (12 ns), then Phase Step Threshold = 12,000 (0x 0000 2EE0). The user must choose a large enough value for phase step threshold to ensure the phase step detector activates only as a result of a reference switching event and not during normal DPLL operation.	0x00	R/W	Live	No
0x082B	[7:0]	REFAA Phase Step Threshold[15:8]		Continuation of the REFAA phase step threshold bit field. See the REFAA Phase Step Threshold[7:0] description.	0x00	R/W	Live	No
0x082C	[7:0]	REFAA Phase Step Threshold[23:16]		Continuation of the REFAA phase step threshold bit field. See the REFAA Phase Step Threshold[7:0] description.	0x00	R/W	Live	No
0x082D	[7:0]	REFAA Phase Step Threshold[31:24]		Continuation of the REFAA phase step threshold bit field. See the REFAA Phase Step Threshold[7:0] description.	0x00	R/W	Live	No
0x082E	[7:0]	REFAA Phase Skew[7:0]		REFAA Phase Skew. This 24-bit signed value, Phase Skew in units of picoseconds (default = 0) defines a time skew for the phase skew adjustment feature. Time skew effectively constitutes a phase offset applied to the reference input associated with this source profile. Phase Skew (rounded to the nearest integer) relates to Time Skew as follows: *Phase Skew* = *Time Skew* $\times 10^{12}$ For example, given Time Skew = -35×10^{-9} (−35 ns), then Phase Skew = −35,000 (0x FF 7748). Phase Skew = 0 disables the phase skew adjustment feature.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x082F	[7:0]	REFAA Phase Skew[15:8]		Continuation of the REFAA phase skew bit field. See the REFAA Phase Skew[7:0] description.	0x00	R/W	Core clock	No
0x0830	[7:0]	REFAA Phase Skew[23:16]		Continuation of the REFAA phase skew bit field. See the REFAA Phase Skew[7:0] description.	0x00	R/W	Core clock	No
0x0831	[7:0]	REFAA phase skew refinement steps		REFAA Phase Skew Refinement Steps. This 8-bit unsigned value defines the number of DPLL PFD cycles the phase buildout processor uses in a phase buildout acquisition to assess the magnitude of phase buildout. The processor does not apply the buildout phase until the designated number of DPLL PFD cycles occurs. A value of zero (default) disables the phase skew refinement feature.	0x00	R/W	Live	No

SOURCE PROFILE: REFB—REGISTER 0x0840 TO REGISTER 0x0851

Table 24. Source Profile: REFB Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0840	[7:0]	REFB Phase Lock Threshold[7:0]		REFB Phase Lock Threshold. Synopsis: The digital phase detector delivers time error samples (ε) to the phase lock detector, where ε is the difference in time between the rising edge of the reference and feedback inputs to the PFD of the DPLL. The phase lock detector compares the magnitude of each time sample (|ε|) to a user defined time threshold (t_{THRESH}). The comparison triggers a fill or drain event. Fill events (|ε| ≤ t_{THRESH}) steer the phase lock detector toward lock status. Drain events (|ε| > t_{THRESH}) steer the phase lock detector toward unlock status. This 24-bit unsigned value, phase lock threshold in units of picoseconds (default = 700), constitutes a time threshold, t_{THRESH} (seconds). Phase Lock Threshold (rounded to the nearest integer) relates to t_{THRESH} as follows: *Phase Lock Threshold* = $t_{THRESH} \times 10^{12}$ For example, for a desired value of $t_{THRESH} = 10^{-9}$ sec (1 ns), then Phase Lock Threshold = 1000 (0x 00 03E8). When the phase slew limiter is actively in the process of phase slew limiting, the phase lock detector inhibits fill events (only drain events can occur during phase slew limiting).	0x188	R/W	Live	No
0x0841	[7:0]	REFB Phase Lock Threshold[15:8]		Continuation of the REFB phase lock threshold bit field. See the REFB Phase Lock Threshold[7:0] description.	0x02	R/W	Live	No
0x0842	[7:0]	REFB Phase Lock Threshold[23:16]		Continuation of the REFB phase lock threshold bit field. See the REFB Phase Lock Threshold[7:0] description.	0x00	R/W	Live	No
0x0843	[7:0]	REFB phase lock fill rate		REFB Phase Lock Fill Rate. This 8-bit unsigned value, phase lock fill rate (default = 10), constitutes the size associated with a phase lock detector fill event. Phase Lock Fill Rate = 0 forces the DPLL to indicate phase lock status.	0x10	R/W	Live	No
0x0844	[7:0]	REFB phase lock drain rate		REFB Phase Lock Drain Rate. This 8-bit unsigned value, Phase Lock Drain Rate (default = 10), constitutes the size associated with a phase lock detector drain event. Phase Lock Drain Rate = 0 forces the DPLL to indicate phase unlock status.	0x10	R/W	Live	No
0x0845	[7:0]	REFB Frequency Lock Threshold[7:0]		REFB Frequency Lock Threshold. Synopsis: The digital frequency detector delivers time error samples (t_{DEV}) to the frequency lock detector, where t_{DEV} is the difference in period between the reference and feedback inputs to the PFD of the DPLL. The frequency lock detector compares the magnitude of each t_{DEV} sample to a user defined period error threshold (t_{P_ERR}). The comparison triggers a fill or drain event. Fill events (|t_{DEV}| ≤ t_{P_ERR}) steer the frequency lock detector toward lock status. Drain events (|t_{DEV}| > t_{P_ERR}) steer the frequency lock detector toward unlock status. This 24-bit unsigned value, Frequency Lock Threshold in units of picoseconds (default = 700), constitutes a period error threshold, t_{P_ERR} (seconds). Frequency Lock Threshold (rounded to the nearest integer) relates to t_{P_ERR} as follows: *Frequency Lock Threshold* = $t_{P\_ERR} \times 10^{12}$	0x188	R/W	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
				In practice, it is convenient to specify an offset frequency, Δf, as a frequency lock threshold, where Δf is relative to the nominal reference frequency, f_R, at the input to the PFD. Frequency Lock Threshold (rounded to the nearest integer) relates to Δf and f_R as follows: *Frequency Lock Threshold* = $(\Delta f/f_R)(1/(f_R + \Delta f)) \times 10^{12}$ For example, given $f_R = 8 \times 10^4$ (80 kHz) and Δf = 100 Hz, then Frequency Lock Threshold = 15,605 (0x 00 3CF5). The phase slew limiter has no effect on the operation of the frequency lock detector.				
0x0846	[7:0]	REFB Frequency Lock Threshold[15:8]		Continuation of the REFB frequency lock threshold bit field. See the REFB Frequency Lock Threshold[7:0] description.	0x02	R/W	Live	No
0x0847	[7:0]	REFB Frequency Lock Threshold[23:16]		Continuation of the REFB frequency lock threshold bit field. See the REFB Frequency Lock Threshold[7:0] description.	0x00	R/W	Live	No
0x0848	[7:0]	REFB frequency lock fill rate		REFB Frequency Lock Fill Rate. This 8-bit unsigned value, Frequency Lock Fill Rate (default = 10), constitutes the size associated with a frequency lock detector fill event. Frequency Lock Fill Rate = 0 forces the DPLL to indicate frequency lock status.	0x10	R/W	Live	No
0x0849	[7:0]	REFB frequency lock drain rate		REFB Frequency Lock Drain Rate. This 8-bit unsigned value, Frequency Lock Drain Rate (default = 10), constitutes the size associated with a frequency lock detector drain event. Frequency Lock Drain Rate = 0 forces the DPLL to indicate frequency unlock status.	0x10	R/W	Live	No
0x084A	[7:0]	REFB Phase Step Threshold[7:0]		REFB Phase Step Detector Threshold. This 32-bit unsigned value, Phase Step Threshold in units of picoseconds (default = 0), sets the time threshold (Φ_{THRESH} (seconds)) at which the DPLL declares that an input reference phase step has occurred. Phase Step Threshold = 0 (default) disables the phase step detector. Phase Step Threshold (rounded to the nearest integer) relates to Φ_{THRESH} as follows: *Phase Step Threshold* = $\Phi_{THRESH} \times 10^{12}$ For example, given a desired time threshold of $\Phi_{THRESH} = 12 \times 10^{-9}$ (12 ns), then Phase Step Threshold = 12,000 (0x 0000 2EE0). The user must choose a large enough value for phase step threshold to ensure the phase step detector activates only as a result of a reference switching event and not during normal DPLL operation.	0x00	R/W	Live	No
0x084B	[7:0]	REFB Phase Step Threshold[15:8]		Continuation of the REFB phase step threshold bit field. See the REFB Phase Step Threshold[7:0] description.	0x00	R/W	Live	No
0x084C	[7:0]	REFB Phase Step Threshold[23:16]		Continuation of the REFB phase step threshold bit field. See the REFB Phase Step Threshold[7:0] description.	0x00	R/W	Live	No
0x084D	[7:0]	REFB Phase Step Threshold[31:24]		Continuation of the REFB phase step threshold bit field. See the REFB Phase Step Threshold[7:0] description.	0x00	R/W	Live	No
0x084E	[7:0]	REFB Phase Skew[7:0]		REFB Phase Skew. This 24-bit signed value, Phase Skew in units of picoseconds (default = 0) defines a time skew for the phase skew adjustment feature. Time skew effectively constitutes a phase offset applied to the reference input associated with this source profile. Phase Skew (rounded to the nearest integer) relates to Time Skew as follows: *Phase Skew* = *Time Skew* $\times 10^{12}$ For example, given Time Skew = -35×10^{-9} (−35 ns), then Phase Skew = −35,000 (0x FF 7748). Phase Skew = 0 disables the phase skew adjustment feature.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x084F	[7:0]	REFB Phase Skew[15:8]		Continuation of the REFB phase skew bit field. See the REFB Phase Skew[7:0] description.	0x00	R/W	Core clock	No
0x0850	[7:0]	REFB Phase Skew[23:16]		Continuation of the REFB phase skew bit field. See the REFB Phase Skew[7:0] description.	0x00	R/W	Core clock	No
0x0851	[7:0]	REFB phase skew refinement steps		REFB Phase Skew Refinement Steps. This 8-bit unsigned value defines the number of DPLL PFD cycles the phase buildout processor uses in a phase buildout acquisition to assess the magnitude of phase buildout. The processor does not apply the buildout phase until the designated number of DPLL PFD cycles occurs. A value of zero (default) disables the phase skew refinement feature.	0x00	R/W	Live	No

SOURCE PROFILE: REFBB—REGISTER 0x0860 TO REGISTER 0x0871

Table 25. Source Profile: REFBB Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0860	[7:0]	REFBB Phase Lock Threshold[7:0]		REFBB Phase Lock Threshold. Synopsis: The digital phase detector delivers time error samples (ε) to the phase lock detector, where ε is the difference in time between the rising edge of the reference and feedback inputs to the PFD of the DPLL. The phase lock detector compares the magnitude of each time sample (|ε|) to a user defined time threshold (t_{THRESH}). The comparison triggers a fill or drain event. Fill events (|ε| ≤ t_{THRESH}) steer the phase lock detector toward lock status. Drain events (|ε| > t_{THRESH}) steer the phase lock detector toward unlock status. This 24-bit unsigned value, phase lock threshold in units of picoseconds (default = 700), constitutes a time threshold, t_{THRESH} (seconds). Phase Lock Threshold (rounded to the nearest integer) relates to t_{THRESH} as follows: *Phase Lock Threshold* = $t_{THRESH} \times 10^{12}$ For example, for a desired value of $t_{THRESH} = 10^{-9}$ sec (1 ns), then Phase Lock Threshold = 1000 (0x 00 03E8). When the phase slew limiter is actively in the process of phase slew limiting, the phase lock detector inhibits fill events (only drain events can occur during phase slew limiting).	0x188	R/W	Live	No
0x0861	[7:0]	REFBB Phase Lock Threshold[15:8]		Continuation of the REFBB phase lock threshold bit field. See the REFBB Phase Lock Threshold[7:0] description.	0x02	R/W	Live	No
0x0862	[7:0]	REFBB Phase Lock Threshold[23:16]		Continuation of the REFBB phase lock threshold bit field. See the REFBB Phase Lock Threshold[7:0] description.	0x00	R/W	Live	No
0x0863	[7:0]	REFBB phase lock fill rate		REFB Phase Lock Fill Rate. This 8-bit unsigned value, phase lock fill rate (default = 10), constitutes the size associated with a phase lock detector fill event. Phase Lock Fill Rate = 0 forces the DPLL to indicate phase lock status.	0x10	R/W	Live	No
0x0864	[7:0]	REFBB phase lock drain rate		REFB Phase Lock Drain Rate. This 8-bit unsigned value, Phase Lock Drain Rate (default = 10), constitutes the size associated with a phase lock detector drain event. Phase Lock Drain Rate = 0 forces the DPLL to indicate phase unlock status.	0x10	R/W	Live	No
0x0865	[7:0]	REFBB Frequency Lock Threshold[7:0]		REFBB Frequency Lock Threshold. Synopsis: The digital frequency detector delivers time error samples (t_{DEV}) to the frequency lock detector, where t_{DEV} is the difference in period between the reference and feedback inputs to the PFD of the DPLL. The frequency lock detector compares the magnitude of each t_{DEV} sample to a user defined period error threshold (t_{P_ERR}). The comparison triggers a fill or drain event. Fill events (|t_{DEV}| ≤ t_{P_ERR}) steer the frequency lock detector toward lock status. Drain events (|t_{DEV}| > t_{P_ERR}) steer the frequency lock detector toward unlock status. This 24-bit unsigned value, Frequency Lock Threshold in units of picoseconds (default = 700), constitutes a period error threshold, t_{P_ERR} (seconds). Frequency Lock Threshold (rounded to the nearest integer) relates to t_{P_ERR} as follows: *Frequency Lock Threshold* = $t_{P\_ERR} \times 10^{12}$	0x188	R/W	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
				In practice, it is convenient to specify an offset frequency, Δf, as a frequency lock threshold, where Δf is relative to the nominal reference frequency, f_R, at the input to the PFD. Frequency Lock Threshold (rounded to the nearest integer) relates to Δf and f_R as follows: *Frequency Lock Threshold* = $(\Delta f/f_R)(1/(f_R + \Delta f)) \times 10^{12}$ For example, given $f_R = 8 \times 10^4$ (80 kHz) and Δf = 100 Hz, then Frequency Lock Threshold = 15,605 (0x 00 3CF5). The phase slew limiter has no effect on the operation of the frequency lock detector.				
0x0866	[7:0]	REFBB Frequency Lock Threshold[15:8]		Continuation of the REFBB frequency lock threshold bit field. See the REFBB Frequency Lock Threshold[7:0] description.	0x02	R/W	Live	No
0x0867	[7:0]	REFBB Frequency Lock Threshold[23:16]		Continuation of the REFBB frequency lock threshold bit field. See the REFBB Frequency Lock Threshold[7:0] description.	0x00	R/W	Live	No
0x0868	[7:0]	REFBB frequency lock fill rate		REFBB Frequency Lock Fill Rate. This 8-bit unsigned value, Frequency Lock Fill Rate (default = 10), constitutes the size associated with a frequency lock detector fill event. Frequency Lock Fill Rate = 0 forces the DPLL to indicate frequency lock status.	0x10	R/W	Live	No
0x0869	[7:0]	REFBB frequency lock drain rate		REFBB Frequency Lock Drain Rate. This 8-bit unsigned value, Frequency Lock Drain Rate (default = 10), constitutes the size associated with a frequency lock detector drain event. Frequency Lock Drain Rate = 0 forces the DPLL to indicate frequency unlock status.	0x10	R/W	Live	No
0x086A	[7:0]	REFBB Phase Step Threshold[7:0]		REFBB Phase Step Detector Threshold. This 32-bit unsigned value, Phase Step Threshold in units of picoseconds (default = 0), sets the time threshold (Φ_{THRESH} (seconds)) at which the DPLL declares that an input reference phase step has occurred. Phase Step Threshold = 0 (default) disables the phase step detector. Phase Step Threshold (rounded to the nearest integer) relates to Φ_{THRESH} as follows: *Phase Step Threshold* = $\Phi_{THRESH} \times 10^{12}$ For example, given a desired time threshold of $\Phi_{THRESH} = 12 \times 10^{-9}$ (12 ns), then Phase Step Threshold = 12,000 (0x 0000 2EE0). The user must choose a large enough value for phase step threshold to ensure the phase step detector activates only as a result of a reference switching event and not during normal DPLL operation.	0x00	R/W	Live	No
0x086B	[7:0]	REFBB Phase Step Threshold[15:8]		Continuation of the REFBB phase step threshold bit field. See the REFBB Phase Step Threshold[7:0] description.	0x00	R/W	Live	No
0x086C	[7:0]	REFBB Phase Step Threshold[23:16]		Continuation of the REFBB phase step threshold bit field. See the REFBB Phase Step Threshold[7:0] description.	0x00	R/W	Live	No
0x086D	[7:0]	REFBB Phase Step Threshold[31:24]		Continuation of the REFBB phase step threshold bit field. See the REFBB Phase Step Threshold[7:0] description.	0x00	R/W	Live	No
0x086E	[7:0]	REFBB Phase Skew[7:0]		REFBB Phase Skew. This 24-bit signed value, Phase Skew in units of picoseconds (default = 0) defines a time skew for the phase skew adjustment feature. Time skew effectively constitutes a phase offset applied to the reference input associated with this source profile. Phase Skew (rounded to the nearest integer) relates to Time Skew as follows: *Phase Skew* = *Time Skew* $\times 10^{12}$ For example, given Time Skew = -35×10^{-9} (−35 ns), then Phase Skew = −35,000 (0x FF 7748). Phase Skew = 0 disables the phase skew adjustment feature.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x086F	[7:0]	REFBB Phase Skew[15:8]		Continuation of the REFBB phase skew bit field. See the REFBB Phase Skew[7:0] description.	0x00	R/W	Core clock	No
0x0870	[7:0]	REFBB Phase Skew[23:16]		Continuation of the REFBB phase skew bit field. See the REFBB Phase Skew[7:0] description.	0x00	R/W	Core clock	No
0x0871	[7:0]	REFBB phase skew refinement steps		REFBB Phase Skew Refinement Steps. This 8-bit unsigned value defines the number of DPLL PFD cycles the phase buildout processor uses in a phase buildout acquisition to assess the magnitude of phase buildout. The processor does not apply the buildout phase until the designated number of DPLL PFD cycles occurs. A value of zero (default) disables the phase skew refinement feature.	0x00	R/W	Live	No

SOURCE PROFILE: AUXILIARY NCO 0—REGISTER 0x0880 TO REGISTER 0x0891

Table 26. Source Profile: Auxiliary NCO 0 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0880	[7:0]	Auxiliary NCO 0 Phase Lock Threshold[7:0]		Auxiliary NCO 0 Phase Lock Threshold. Synopsis: The digital phase detector delivers time error samples (ε) to the phase lock detector, where ε is the difference in time between the rising edge of the reference and feedback inputs to the PFD of the DPLL. The phase lock detector compares the magnitude of each time sample (|ε|) to a user defined time threshold (t_{THRESH}). The comparison triggers a fill or drain event. Fill events (|ε| ≤ t_{THRESH}) steer the phase lock detector toward lock status. Drain events (|ε| > t_{THRESH}) steer the phase lock detector toward unlock status. This 24-bit unsigned value, phase lock threshold in units of picoseconds (default = 700), constitutes a time threshold, t_{THRESH} (seconds). Phase Lock Threshold (rounded to the nearest integer) relates to t_{THRESH} as follows: *Phase Lock Threshold* = $t_{THRESH} \times 10^{12}$ For example, for a desired value of $t_{THRESH} = 10^{-9}$ sec (1 ns), then Phase Lock Threshold = 1000 (0x 00 03E8). When the phase slew limiter is actively in the process of phase slew limiting, the phase lock detector inhibits fill events (only drain events can occur during phase slew limiting).	0x188	R/W	Live	No
0x0881	[7:0]	Auxiliary NCO 0 Phase Lock Threshold[15:8]		Continuation of the Auxiliary NCO 0 phase lock threshold bit field. See the Auxiliary NCO 0 Phase Lock Threshold[7:0] description.	0x02	R/W	Live	No
0x0882	[7:0]	Auxiliary NCO 0 Phase Lock Threshold[23:16]		Continuation of the Auxiliary NCO 0 phase lock threshold bit field. See the Auxiliary NCO 0 Phase Lock Threshold[7:0] description.	0x00	R/W	Live	No
0x0883	[7:0]	Auxiliary NCO 0 phase lock fill rate		Auxiliary NCO 0 Phase Lock Fill Rate. This 8-bit unsigned value, phase lock fill rate (default = 10), constitutes the size associated with a phase lock detector fill event. Phase Lock Fill Rate = 0 forces the DPLL to indicate phase lock status.	0x10	R/W	Live	No
0x0884	[7:0]	Auxiliary NCO 0 phase lock drain rate		Auxiliary NCO 0 Phase Lock Drain Rate. This 8-bit unsigned value, Phase Lock Drain Rate (default = 10), constitutes the size associated with a phase lock detector drain event. Phase Lock Drain Rate = 0 forces the DPLL to indicate phase unlock status.	0x10	R/W	Live	No
0x0885	[7:0]	Auxiliary NCO 0 Frequency Lock Threshold[7:0]		Auxiliary NCO 0 Frequency Lock Threshold. Synopsis: The digital frequency detector delivers time error samples (t_{DEV}) to the frequency lock detector, where t_{DEV} is the difference in period between the reference and feedback inputs to the PFD of the DPLL. The frequency lock detector compares the magnitude of each t_{DEV} sample to a user defined period error threshold (t_{P_ERR}). The comparison triggers a fill or drain event. Fill events (|t_{DEV}| ≤ t_{P_ERR}) steer the frequency lock detector toward lock status. Drain events (|t_{DEV}| > t_{P_ERR}) steer the frequency lock detector toward unlock status. This 24-bit unsigned value, Frequency Lock Threshold in units of picoseconds (default = 700), constitutes a period error threshold, t_{P_ERR} (seconds). Frequency Lock Threshold (rounded to the nearest integer) relates to t_{P_ERR} as follows: *Frequency Lock Threshold* = $t_{P\_ERR} \times 10^{12}$	0x188	R/W	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
				In practice, it is convenient to specify an offset frequency, Δf, as a frequency lock threshold, where Δf is relative to the nominal reference frequency, f_R, at the input to the PFD. Frequency Lock Threshold (rounded to the nearest integer) relates to Δf and f_R as follows: *Frequency Lock Threshold* = $(\Delta f/f_R)(1/(f_R + \Delta f)) \times 10^{12}$ For example, given $f_R = 8 \times 10^4$ (80 kHz) and Δf = 100 Hz, then Frequency Lock Threshold = 15,605 (0x 00 3CF5). The phase slew limiter has no effect on the operation of the frequency lock detector.				
0x0886	[7:0]	Auxiliary NCO 0 Frequency Lock Threshold[15:8]		Continuation of the Auxiliary NCO 0 frequency lock threshold bit field. See the Auxiliary NCO 0 Frequency Lock Threshold[7:0] description.	0x02	R/W	Live	No
0x0887	[7:0]	Auxiliary NCO 0 Frequency Lock Threshold[23:16]		Continuation of the Auxiliary NCO 0 frequency lock threshold bit field. See the Auxiliary NCO 0 Frequency Lock Threshold[7:0] description.	0x00	R/W	Live	No
0x0888	[7:0]	Auxiliary NCO 0 frequency lock fill rate		Auxiliary NCO 0 Frequency Lock Fill Rate. This 8-bit unsigned value, Frequency Lock Fill Rate (default = 10), constitutes the size associated with a frequency lock detector fill event. Frequency Lock Fill Rate = 0 forces the DPLL to indicate frequency lock status.	0x10	R/W	Live	No
0x0889	[7:0]	Auxiliary NCO 0 frequency lock drain rate		Auxiliary NCO 0 Frequency Lock Drain Rate. This 8-bit unsigned value, Frequency Lock Drain Rate (default = 10), constitutes the size associated with a frequency lock detector drain event. Frequency Lock Drain Rate = 0 forces the DPLL to indicate frequency unlock status.	0x10	R/W	Live	No
0x088A	[7:0]	Auxiliary NCO 0 Phase Step Threshold[7:0]		Auxiliary NCO 0 Phase Step Detector Threshold. This 32-bit unsigned value, Phase Step Threshold in units of picoseconds (default = 0), sets the time threshold (Φ_{THRESH} (seconds)) at which the DPLL declares that an input reference phase step has occurred. Phase Step Threshold = 0 (default) disables the phase step detector. Phase Step Threshold (rounded to the nearest integer) relates to Φ_{THRESH} as follows: *Phase Step Threshold* = $\Phi_{THRESH} \times 10^{12}$ For example, given a desired time threshold of $\Phi_{THRESH} = 12 \times 10^{-9}$ (12 ns), then Phase Step Threshold = 12,000 (0x 0000 2EE0). The user must choose a large enough value for phase step threshold to ensure the phase step detector activates only as a result of a reference switching event and not during normal DPLL operation.	0x00	R/W	Live	No
0x088B	[7:0]	Auxiliary NCO 0 Phase Step Threshold[15:8]		Continuation of the Auxiliary NCO 0 phase step threshold bit field. See the Auxiliary NCO 0 Phase Step Threshold[7:0] description.	0x00	R/W	Live	No
0x088C	[7:0]	Auxiliary NCO 0 Phase Step Threshold[23:16]		Continuation of the Auxiliary NCO 0 phase step threshold bit field. See the Auxiliary NCO 0 Phase Step Threshold[7:0] description.	0x00	R/W	Live	No
0x088D	[7:0]	Auxiliary NCO 0 Phase Step Threshold[31:24]		Continuation of the Auxiliary NCO 0 phase step threshold bit field. See the Auxiliary NCO 0 Phase Step Threshold[7:0] description.	0x00	R/W	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x088E	[7:0]	Auxiliary NCO 0 Phase Skew[7:0]		Auxiliary NCO 0 Phase Skew. This 24-bit signed value, Phase Skew in units of picoseconds (default = 0) defines a time skew for the phase skew adjustment feature. Time skew effectively constitutes a phase offset applied to the reference input associated with this source profile. Phase Skew (rounded to the nearest integer) relates to Time Skew as follows: $Phase\ Skew = Time\ Skew \times 10^{12}$ For example, given Time Skew = -35×10^{-9} (−35 ns), then Phase Skew = −35,000 (0x FF 7748). Phase Skew = 0 disables the phase skew adjustment feature.	0x00	R/W	Core clock	No
0x088F	[7:0]	Auxiliary NCO 0 Phase Skew[15:8]		Continuation of the Auxiliary NCO 0 phase skew bit field. See the Auxiliary NCO 0 Phase Skew[7:0] description.	0x00	R/W	Core clock	No
0x0890	[7:0]	Auxiliary NCO 0 Phase Skew[23:16]		Continuation of the Auxiliary NCO 0 phase skew bit field. See the Auxiliary NCO 0 Phase Skew[7:0] description.	0x00	R/W	Core clock	No
0x0891	[7:0]	Auxiliary NCO 0 phase skew refinement steps		Auxiliary NCO 0 Phase Skew Refinement Steps. This 8-bit unsigned value defines the number of DPLL PFD cycles the phase buildout processor uses in a phase buildout acquisition to assess the magnitude of phase buildout. The processor does not apply the buildout phase until the designated number of DPLL PFD cycles occurs. A value of zero (default) disables the phase skew refinement feature.	0x00	R/W	Live	No

SOURCE PROFILE: AUXILIARY NCO 1—REGISTER 0x08A0 TO REGISTER 0x08B1

Table 27. Source Profile: Auxiliary NCO 1 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x08A0	[7:0]	Auxiliary NCO 1 Phase Lock Threshold[7:0]		Auxiliary NCO 1 Phase Lock Threshold. Synopsis: The digital phase detector delivers time error samples (ε) to the phase lock detector, where ε is the difference in time between the rising edge of the reference and feedback inputs to the PFD of the DPLL. The phase lock detector compares the magnitude of each time sample (|ε|) to a user defined time threshold (t_{THRESH}). The comparison triggers a fill or drain event. Fill events ($|\varepsilon| \leq t_{THRESH}$) steer the phase lock detector toward lock status. Drain events ($|\varepsilon| > t_{THRESH}$) steer the phase lock detector toward unlock status. This 24-bit unsigned value, phase lock threshold in units of picoseconds (default = 700), constitutes a time threshold, t_{THRESH} (seconds). Phase Lock Threshold (rounded to the nearest integer) relates to t_{THRESH} as follows: *Phase Lock Threshold* = $t_{THRESH} \times 10^{12}$ For example, for a desired value of $t_{THRESH} = 10^{-9}$ sec (1 ns), then Phase Lock Threshold = 1000 (0x 00 03E8). When the phase slew limiter is actively in the process of phase slew limiting, the phase lock detector inhibits fill events (only drain events can occur during phase slew limiting).	0x188	R/W	Live	No
0x08A1	[7:0]	Auxiliary NCO 1 Phase Lock Threshold[15:8]		Continuation of the Auxiliary NCO 1 phase lock threshold bit field. See the Auxiliary NCO 1 Phase Lock Threshold[7:0] description.	0x02	R/W	Live	No
0x08A2	[7:0]	Auxiliary NCO 1 Phase Lock Threshold[23:16]		Continuation of the Auxiliary NCO 1 phase lock threshold bit field. See the Auxiliary NCO 1 Phase Lock Threshold[7:0] description.	0x00	R/W	Live	No
0x08A3	[7:0]	Auxiliary NCO 1 phase lock fill rate		Auxiliary NCO 1 Phase Lock Fill Rate. This 8-bit unsigned value, phase lock fill rate (default = 10), constitutes the size associated with a phase lock detector fill event. Phase Lock Fill Rate = 0 forces the DPLL to indicate phase lock status.	0x10	R/W	Live	No
0x08A4	[7:0]	Auxiliary NCO 1 phase lock drain rate		Auxiliary NCO 1 Phase Lock Drain Rate. This 8-bit unsigned value, Phase Lock Drain Rate (default = 10), constitutes the size associated with a phase lock detector drain event. Phase Lock Drain Rate = 0 forces the DPLL to indicate phase unlock status.	0x10	R/W	Live	No
0x08A5	[7:0]	Auxiliary NCO 1 Frequency Lock Threshold[7:0]		Auxiliary NCO 1 Frequency Lock Threshold. Synopsis: The digital frequency detector delivers time error samples (t_{DEV}) to the frequency lock detector, where t_{DEV} is the difference in period between the reference and feedback inputs to the PFD of the DPLL. The frequency lock detector compares the magnitude of each t_{DEV} sample to a user defined period error threshold (t_{P_ERR}). The comparison triggers a fill or drain event. Fill events ($|t_{DEV}| \leq t_{P\_ERR}$) steer the frequency lock detector toward lock status. Drain events ($|t_{DEV}| > t_{P\_ERR}$) steer the frequency lock detector toward unlock status. This 24-bit unsigned value, Frequency Lock Threshold in units of picoseconds (default = 700), constitutes a period error threshold, t_{P_ERR} (seconds). Frequency Lock Threshold (rounded to the nearest integer) relates to t_{P_ERR} as follows: *Frequency Lock Threshold* = $t_{P\_ERR} \times 10^{12}$	0x188	R/W	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
				In practice, it is convenient to specify an offset frequency, Δf, as a frequency lock threshold, where Δf is relative to the nominal reference frequency, f_R, at the input to the PFD. Frequency Lock Threshold (rounded to the nearest integer) relates to Δf and f_R as follows: *Frequency Lock Threshold* = $(\Delta f/f_R)(1/(f_R + \Delta f)) \times 10^{12}$ For example, given $f_R = 8 \times 10^4$ (80 kHz) and Δf = 100 Hz, then Frequency Lock Threshold = 15,605 (0x 00 3CF5). The phase slew limiter has no effect on the operation of the frequency lock detector.				
0x08A6	[7:0]	Auxiliary NCO 1 Frequency Lock Threshold[15:8]		Continuation of the Auxiliary NCO 1 frequency lock threshold bit field. See the Auxiliary NCO 1 Frequency Lock Threshold[7:0] description.	0x02	R/W	Live	No
0x08A7	[7:0]	Auxiliary NCO 1 Frequency Lock Threshold[23:16]		Continuation of the Auxiliary NCO 1 frequency lock threshold bit field. See the Auxiliary NCO 1 Frequency Lock Threshold[7:0] description.	0x00	R/W	Live	No
0x08A8	[7:0]	Auxiliary NCO 1 frequency lock fill rate		Auxiliary NCO 1 Frequency Lock Fill Rate. This 8-bit unsigned value, Frequency Lock Fill Rate (default = 10), constitutes the size associated with a frequency lock detector fill event. Frequency Lock Fill Rate = 0 forces the DPLL to indicate frequency lock status.	0x10	R/W	Live	No
0x08A9	[7:0]	Auxiliary NCO 1 frequency lock drain rate		Auxiliary NCO 1 Frequency Lock Drain Rate. This 8-bit unsigned value, Frequency Lock Drain Rate (default = 10), constitutes the size associated with a frequency lock detector drain event. Frequency Lock Drain Rate = 0 forces the DPLL to indicate frequency unlock status.	0x10	R/W	Live	No
0x08AA	[7:0]	Auxiliary NCO 1 Phase Step Threshold[7:0]		Auxiliary NCO 1 Phase Step Detector Threshold. This 32-bit unsigned value, Phase Step Threshold in units of picoseconds (default = 0), sets the time threshold (Φ_{THRESH} (seconds)) at which the DPLL declares that an input reference phase step has occurred. Phase Step Threshold = 0 (default) disables the phase step detector. Phase Step Threshold (rounded to the nearest integer) relates to Φ_{THRESH} as follows: *Phase Step Threshold* = $\Phi_{THRESH} \times 10^{12}$ For example, given a desired time threshold of $\Phi_{THRESH} = 12 \times 10^{-9}$ (12 ns), then Phase Step Threshold = 12,000 (0x 0000 2EE0). The user must choose a large enough value for phase step threshold to ensure the phase step detector activates only as a result of a reference switching event and not during normal DPLL operation.	0x00	R/W	Live	No
0x08AB	[7:0]	Auxiliary NCO 1 Phase Step Threshold[15:8]		Continuation of the Auxiliary NCO 1 phase step threshold bit field. See the Auxiliary NCO 1 Phase Step Threshold[7:0] description.	0x00	R/W	Live	No
0x08AC	[7:0]	Auxiliary NCO 1 Phase Step Threshold[23:16]		Continuation of the Auxiliary NCO 1 phase step threshold bit field. See the Auxiliary NCO 1 Phase Step Threshold[7:0] description.	0x00	R/W	Live	No
0x08AD	[7:0]	Auxiliary NCO 1 Phase Step Threshold[31:24]		Continuation of the Auxiliary NCO 1 phase step threshold bit field. See the Auxiliary NCO 1 Phase Step Threshold[7:0] description.	0x00	R/W	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x08AE	[7:0]	Auxiliary NCO 1 Phase Skew[7:0]		Auxiliary NCO 1 Phase Skew. This 24-bit signed value, Phase Skew in units of picoseconds (default = 0) defines a time skew for the phase skew adjustment feature. Time skew effectively constitutes a phase offset applied to the reference input associated with this source profile. Phase Skew (rounded to the nearest integer) relates to Time Skew as follows: $Phase\ Skew = Time\ Skew \times 10^{12}$ For example, given Time Skew = -35×10^{-9} (−35 ns), then Phase Skew = −35,000 (0x FF 7748). Phase Skew = 0 disables the phase skew adjustment feature.	0x00	R/W	Core clock	No
0x08AF	[7:0]	Auxiliary NCO 1 Phase Skew[15:8]		Continuation of the Auxiliary NCO 1 phase skew bit field. See the Auxiliary NCO 1 Phase Skew[7:0] description.	0x00	R/W	Core clock	No
0x08B0	[7:0]	Auxiliary NCO 1 Phase Skew[23:16]		Continuation of the Auxiliary NCO 1 phase skew bit field. See the Auxiliary NCO 1 Phase Skew[7:0] description.	0x00	R/W	Core clock	No
0x08B1	[7:0]	Auxiliary NCO 1 phase skew refinement steps		Auxiliary NCO 1 Phase Skew Refinement Steps. This 8-bit unsigned value defines the number of DPLL PFD cycles the phase buildout processor uses in a phase buildout acquisition to assess the magnitude of phase buildout. The processor does not apply the buildout phase until the designated number of DPLL PFD cycles occurs. A value of zero (default) disables the phase skew refinement feature.	0x00	R/W	Live	No

SOURCE PROFILE: DPLL0—REGISTER 0x08C0 TO REGISTER 0x08D1

Table 28. Source Profile: DPLL0 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x08C0	[7:0]	DPLL0 Phase Lock Threshold[7:0]		DPLL0 Phase Lock Threshold. Synopsis: The digital phase detector delivers time error samples (ε) to the phase lock detector, where ε is the difference in time between the rising edge of the reference and feedback inputs to the PFD of the DPLL. The phase lock detector compares the magnitude of each time sample (|ε|) to a user defined time threshold (t_{THRESH}). The comparison triggers a fill or drain event. Fill events (|ε| ≤ t_{THRESH}) steer the phase lock detector toward lock status. Drain events (|ε| > t_{THRESH}) steer the phase lock detector toward unlock status. This 24-bit unsigned value, phase lock threshold in units of picoseconds (default = 700), constitutes a time threshold, t_{THRESH} (seconds). Phase Lock Threshold (rounded to the nearest integer) relates to t_{THRESH} as follows: *Phase Lock Threshold* = $t_{THRESH} \times 10^{12}$ For example, for a desired value of $t_{THRESH} = 10^{-9}$ sec (1 ns), then Phase Lock Threshold = 1000 (0x 00 03E8). When the phase slew limiter is actively in the process of phase slew limiting, the phase lock detector inhibits fill events (only drain events can occur during phase slew limiting).	0x188	R/W	Live	No
0x08C1	[7:0]	DPLL0 Phase Lock Threshold[15:8]		Continuation of the DPLL0 phase lock threshold bit field. See the DPLL0 Phase Lock Threshold[7:0] description.	0x02	R/W	Live	No
0x08C2	[7:0]	DPLL0 Phase Lock Threshold[23:16]		Continuation of the DPLL0 phase lock threshold bit field. See the DPLL0 Phase Lock Threshold[7:0] description.	0x00	R/W	Live	No
0x08C3	[7:0]	DPLL0 phase lock fill rate		DPLL0 Phase Lock Fill Rate. This 8-bit unsigned value, phase lock fill rate (default = 10), constitutes the size associated with a phase lock detector fill event. Phase Lock Fill Rate = 0 forces the DPLL to indicate phase lock status.	0x10	R/W	Live	No
0x08C4	[7:0]	DPLL0 phase lock drain rate		DPLL0 Phase Lock Drain Rate. This 8-bit unsigned value, Phase Lock Drain Rate (default = 10), constitutes the size associated with a phase lock detector drain event. Phase Lock Drain Rate = 0 forces the DPLL to indicate phase unlock status.	0x10	R/W	Live	No
0x08C5	[7:0]	DPLL0 Frequency Lock Threshold[7:0]		DPLL0 Frequency Lock Threshold. Synopsis: The digital frequency detector delivers time error samples (t_{DEV}) to the frequency lock detector, where t_{DEV} is the difference in period between the reference and feedback inputs to the PFD of the DPLL. The frequency lock detector compares the magnitude of each t_{DEV} sample to a user defined period error threshold (t_{P_ERR}). The comparison triggers a fill or drain event. Fill events (|t_{DEV}| ≤ t_{P_ERR}) steer the frequency lock detector toward lock status. Drain events (|t_{DEV}| > t_{P_ERR}) steer the frequency lock detector toward unlock status. This 24-bit unsigned value, Frequency Lock Threshold in units of picoseconds (default = 700), constitutes a period error threshold, t_{P_ERR} (seconds). Frequency Lock Threshold (rounded to the nearest integer) relates to t_{P_ERR} as follows: *Frequency Lock Threshold* = $t_{P\_ERR} \times 10^{12}$	0x188	R/W	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
				In practice, it is convenient to specify an offset frequency, Δf, as a frequency lock threshold, where Δf is relative to the nominal reference frequency, f_R, at the input to the PFD. Frequency Lock Threshold (rounded to the nearest integer) relates to Δf and f_R as follows: *Frequency Lock Threshold* = $(\Delta f/f_R)(1/(f_R + \Delta f)) \times 10^{12}$ For example, given $f_R = 8 \times 10^4$ (80 kHz) and Δf = 100 Hz, then Frequency Lock Threshold = 15,605 (0x 00 3CF5). The phase slew limiter has no effect on the operation of the frequency lock detector.				
0x08C6	[7:0]	DPLL0 Frequency Lock Threshold[15:8]		Continuation of the DPLL0 frequency lock threshold bit field. See the DPLL0 Frequency Lock Threshold[7:0] description.	0x02	R/W	Live	No
0x08C7	[7:0]	DPLL0 Frequency Lock Threshold[23:16]		Continuation of the DPLL0 frequency lock threshold bit field. See the DPLL0 Frequency Lock Threshold[7:0] description.	0x00	R/W	Live	No
0x08C8	[7:0]	DPLL0 frequency lock fill rate		DPLL0 Frequency Lock Fill Rate. This 8-bit unsigned value, Frequency Lock Fill Rate (default = 10), constitutes the size associated with a frequency lock detector fill event. Frequency Lock Fill Rate = 0 forces the DPLL to indicate frequency lock status.	0x10	R/W	Live	No
0x08C9	[7:0]	DPLL0 frequency lock drain rate		DPLL0 Frequency Lock Drain Rate. This 8-bit unsigned value, Frequency Lock Drain Rate (default = 10), constitutes the size associated with a frequency lock detector drain event. Frequency Lock Drain Rate = 0 forces the DPLL to indicate frequency unlock status.	0x10	R/W	Live	No
0x08CA	[7:0]	DPLL0 Phase Step Threshold[7:0]		DPLL0 Phase Step Detector Threshold. This 32-bit unsigned value, Phase Step Threshold in units of picoseconds (default = 0), sets the time threshold (Φ_{THRESH} (seconds)) at which the DPLL declares that an input reference phase step has occurred. Phase Step Threshold = 0 (default) disables the phase step detector. Phase Step Threshold (rounded to the nearest integer) relates to Φ_{THRESH} as follows: *Phase Step Threshold* = $\Phi_{THRESH} \times 10^{12}$ For example, given a desired time threshold of $\Phi_{THRESH} = 12 \times 10^{-9}$ (12 ns), then Phase Step Threshold = 12,000 (0x 0000 2EE0). The user must choose a large enough value for phase step threshold to ensure the phase step detector activates only as a result of a reference switching event and not during normal DPLL operation.	0x00	R/W	Live	No
0x08CB	[7:0]	DPLL0 Phase Step Threshold[15:8]		Continuation of the DPLL0 phase step threshold bit field. See the DPLL0 Phase Step Threshold[7:0] description.	0x00	R/W	Live	No
0x08CC	[7:0]	DPLL0 Phase Step Threshold[23:16]		Continuation of the DPLL0 phase step threshold bit field. See the DPLL0 Phase Step Threshold[7:0] description.	0x00	R/W	Live	No
0x08CD	[7:0]	DPLL0 Phase Step Threshold[31:24]		Continuation of the DPLL0 phase step threshold bit field. See the DPLL0 Phase Step Threshold[7:0] description.	0x00	R/W	Live	No
0x08CE	[7:0]	DPLL0 Phase Skew[7:0]		DPLL0 Phase Skew. This 24-bit signed value, Phase Skew in units of picoseconds (default = 0) defines a time skew for the phase skew adjustment feature. Time skew effectively constitutes a phase offset applied to the reference input associated with this source profile. Phase Skew (rounded to the nearest integer) relates to Time Skew as follows: *Phase Skew* = *Time Skew* $\times 10^{12}$ For example, given Time Skew = -35×10^{-9} (−35 ns), then Phase Skew = −35,000 (0x FF 7748). Phase Skew = 0 disables the phase skew adjustment feature.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x08CF	[7:0]	DPLL0 Phase Skew[15:8]		Continuation of the DPLL0 phase skew bit field. See the DPLL0 Phase Skew[7:0] description.	0x00	R/W	Core clock	No
0x08D0	[7:0]	DPLL0 Phase Skew[23:16]		Continuation of the DPLL0 phase skew bit field. See the DPLL0 Phase Skew[7:0] description.	0x00	R/W	Core clock	No
0x08D1	[7:0]	DPLL0 phase skew refinement steps		DPLL0 Phase Skew Refinement Steps. This 8-bit unsigned value defines the number of DPLL PFD cycles the phase buildout processor uses in a phase buildout acquisition to assess the magnitude of phase buildout. The processor does not apply the buildout phase until the designated number of DPLL PFD cycles occurs. A value of zero (default) disables the phase skew refinement feature.	0x00	R/W	Live	No

SOURCE PROFILE: DPLL1—REGISTER 0x08E0 TO REGISTER 0x08F1

Table 29. Source Profile: DPLL1 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x08E0	[7:0]	DPLL1 Phase Lock Threshold[7:0]		DPLL1 Phase Lock Threshold. Synopsis: The digital phase detector delivers time error samples (ε) to the phase lock detector, where ε is the difference in time between the rising edge of the reference and feedback inputs to the PFD of the DPLL. The phase lock detector compares the magnitude of each time sample (|ε|) to a user defined time threshold (t_{THRESH}). The comparison triggers a fill or drain event. Fill events (|ε| ≤ t_{THRESH}) steer the phase lock detector toward lock status. Drain events (|ε| > t_{THRESH}) steer the phase lock detector toward unlock status. This 24-bit unsigned value, phase lock threshold in units of picoseconds (default = 700), constitutes a time threshold, t_{THRESH} (seconds). Phase Lock Threshold (rounded to the nearest integer) relates to t_{THRESH} as follows: *Phase Lock Threshold* = $t_{THRESH} \times 10^{12}$ For example, for a desired value of $t_{THRESH} = 10^{-9}$ sec (1 ns), then Phase Lock Threshold = 1000 (0x 00 03E8). When the phase slew limiter is actively in the process of phase slew limiting, the phase lock detector inhibits fill events (only drain events can occur during phase slew limiting).	0x188	R/W	Live	No
0x08E1	[7:0]	DPLL1 Phase Lock Threshold[15:8]		Continuation of the DPLL1 phase lock threshold bit field. See the DPLL1 Phase Lock Threshold[7:0] description.	0x02	R/W	Live	No
0x08E2	[7:0]	DPLL1 Phase Lock Threshold[23:16]		Continuation of the DPLL1 phase lock threshold bit field. See the DPLL1 Phase Lock Threshold[7:0] description.	0x00	R/W	Live	No
0x08E3	[7:0]	DPLL1 phase lock fill rate		DPLL1 Phase Lock Fill Rate. This 8-bit unsigned value, phase lock fill rate (default = 10), constitutes the size associated with a phase lock detector fill event. Phase Lock Fill Rate = 0 forces the DPLL to indicate phase lock status.	0x10	R/W	Live	No
0x08E4	[7:0]	DPLL1 phase lock drain rate		DPLL1 Phase Lock Drain Rate. This 8-bit unsigned value, Phase Lock Drain Rate (default = 10), constitutes the size associated with a phase lock detector drain event. Phase Lock Drain Rate = 0 forces the DPLL to indicate phase unlock status.	0x10	R/W	Live	No
0x08E5	[7:0]	DPLL1 Frequency Lock Threshold[7:0]		DPLL1 Frequency Lock Threshold. Synopsis: The digital frequency detector delivers time error samples (t_{DEV}) to the frequency lock detector, where t_{DEV} is the difference in period between the reference and feedback inputs to the PFD of the DPLL. The frequency lock detector compares the magnitude of each t_{DEV} sample to a user defined period error threshold (t_{P_ERR}). The comparison triggers a fill or drain event. Fill events (|t_{DEV}| ≤ t_{P_ERR}) steer the frequency lock detector toward lock status. Drain events (|t_{DEV}| > t_{P_ERR}) steer the frequency lock detector toward unlock status. This 24-bit unsigned value, Frequency Lock Threshold in units of picoseconds (default = 700), constitutes a period error threshold, t_{P_ERR} (seconds). Frequency Lock Threshold (rounded to the nearest integer) relates to t_{P_ERR} as follows: *Frequency Lock Threshold* = $t_{P\_ERR} \times 10^{12}$	0x188	R/W	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
				In practice, it is convenient to specify an offset frequency, Δf, as a frequency lock threshold, where Δf is relative to the nominal reference frequency, f_R, at the input to the PFD. Frequency Lock Threshold (rounded to the nearest integer) relates to Δf and f_R as follows: *Frequency Lock Threshold* = $(\Delta f/f_R)(1/(f_R + \Delta f)) \times 10^{12}$ For example, given $f_R = 8 \times 10^4$ (80 kHz) and Δf = 100 Hz, then Frequency Lock Threshold = 15,605 (0x 00 3CF5). The phase slew limiter has no effect on the operation of the frequency lock detector.				
0x08E6	[7:0]	DPLL1 Frequency Lock Threshold[15:8]		Continuation of the DPLL1 frequency lock threshold bit field. See the DPLL1 Frequency Lock Threshold[7:0] description.	0x02	R/W	Live	No
0x08E7	[7:0]	DPLL1 Frequency Lock Threshold[23:16]		Continuation of the DPLL1 frequency lock threshold bit field. See the DPLL1 Frequency Lock Threshold[7:0] description.	0x00	R/W	Live	No
0x08E8	[7:0]	DPLL1 frequency lock fill rate		DPLL1 Frequency Lock Fill Rate. This 8-bit unsigned value, Frequency Lock Fill Rate (default = 10), constitutes the size associated with a frequency lock detector fill event. Frequency Lock Fill Rate = 0 forces the DPLL to indicate frequency lock status.	0x10	R/W	Live	No
0x08E9	[7:0]	DPLL1 frequency lock drain rate		DPLL1 Frequency Lock Drain Rate. This 8-bit unsigned value, Frequency Lock Drain Rate (default = 10), constitutes the size associated with a frequency lock detector drain event. Frequency Lock Drain Rate = 0 forces the DPLL to indicate frequency unlock status.	0x10	R/W	Live	No
0x08EA	[7:0]	DPLL1 Phase Step Threshold[7:0]		DPLL1 Phase Step Detector Threshold. This 32-bit unsigned value, Phase Step Threshold in units of picoseconds (default = 0), sets the time threshold (Φ_{THRESH} (seconds)) at which the DPLL declares that an input reference phase step has occurred. Phase Step Threshold = 0 (default) disables the phase step detector. Phase Step Threshold (rounded to the nearest integer) relates to Φ_{THRESH} as follows: *Phase Step Threshold* = $\Phi_{THRESH} \times 10^{12}$ For example, given a desired time threshold of $\Phi_{THRESH} = 12 \times 10^{-9}$ (12 ns), then Phase Step Threshold = 12,000 (0x 0000 2EE0). The user must choose a large enough value for phase step threshold to ensure the phase step detector activates only as a result of a reference switching event and not during normal DPLL operation.	0x00	R/W	Live	No
0x08EB	[7:0]	DPLL1 Phase Step Threshold[15:8]		Continuation of the DPLL1 phase step threshold bit field. See the DPLL1 Phase Step Threshold[7:0] description.	0x00	R/W	Live	No
0x08EC	[7:0]	DPLL1 Phase Step Threshold[23:16]		Continuation of the DPLL1 phase step threshold bit field. See the DPLL1 Phase Step Threshold[7:0] description.	0x00	R/W	Live	No
0x08ED	[7:0]	DPLL1 Phase Step Threshold[31:24]		Continuation of the DPLL1 phase step threshold bit field. See the DPLL1 Phase Step Threshold[7:0] description.	0x00	R/W	Live	No
0x08EE	[7:0]	DPLL1 Phase Skew[7:0]		DPLL1 Phase Skew. This 24-bit signed value, Phase Skew in units of picoseconds (default = 0) defines a time skew for the phase skew adjustment feature. Time skew effectively constitutes a phase offset applied to the reference input associated with this source profile. Phase Skew (rounded to the nearest integer) relates to Time Skew as follows: *Phase Skew* = *Time Skew* $\times 10^{12}$ For example, given Time Skew = -35×10^{-9} (−35 ns), then Phase Skew = −35,000 (0x FF 7748). Phase Skew = 0 disables the phase skew adjustment feature.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x08EF	[7:0]	DPLL1 Phase Skew[15:8]		Continuation of the DPLL1 phase skew bit field. See the DPLL1 Phase Skew[7:0] description.	0x00	R/W	Core clock	No
0x08F0	[7:0]	DPLL1 Phase Skew[23:16]		Continuation of the DPLL1 phase skew bit field. See the DPLL1 Phase Skew[7:0] description.	0x00	R/W	Core clock	No
0x08F1	[7:0]	DPLL1 phase skew refinement steps		DPLL1 Phase Skew Refinement Steps. This 8-bit unsigned value defines the number of DPLL PFD cycles the phase buildout processor uses in a phase buildout acquisition to assess the magnitude of phase buildout. The processor does not apply the buildout phase until the designated number of DPLL PFD cycles occurs. A value of zero (default) disables the phase skew refinement feature.	0x00	R/W	Live	No

SOURCE PROFILE: IUTS 0—REGISTER 0x0900 TO REGISTER 0x0911

Table 30. Source Profile: IUTS 0 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0900	[7:0]	IUTS 0 Phase Lock Threshold[7:0]		IUTS 0 Phase Lock Threshold. Synopsis: The digital phase detector delivers time error samples (ε) to the phase lock detector, where ε is the difference in time between the rising edge of the reference and feedback inputs to the PFD of the DPLL. The phase lock detector compares the magnitude of each time sample (|ε|) to a user defined time threshold (t_{THRESH}). The comparison triggers a fill or drain event. Fill events (|ε| ≤ t_{THRESH}) steer the phase lock detector toward lock status. Drain events (|ε| > t_{THRESH}) steer the phase lock detector toward unlock status. This 24-bit unsigned value, phase lock threshold in units of picoseconds (default = 700), constitutes a time threshold, t_{THRESH} (seconds). Phase Lock Threshold (rounded to the nearest integer) relates to t_{THRESH} as follows: *Phase Lock Threshold* = $t_{THRESH} \times 10^{12}$ For example, for a desired value of $t_{THRESH} = 10^{-9}$ sec (1 ns), then Phase Lock Threshold = 1000 (0x 00 03E8). When the phase slew limiter is actively in the process of phase slew limiting, the phase lock detector inhibits fill events (only drain events can occur during phase slew limiting).	0x188	R/W	Live	No
0x0901	[7:0]	IUTS 0 Phase Lock Threshold[15:8]		Continuation of the IUTS 0 phase lock threshold bit field. See the IUTS 0 Phase Lock Threshold[7:0] description.	0x02	R/W	Live	No
0x0902	[7:0]	IUTS 0 Phase Lock Threshold[23:16]		Continuation of the IUTS 0 phase lock threshold bit field. See the IUTS 0 Phase Lock Threshold[7:0] description.	0x00	R/W	Live	No
0x0903	[7:0]	IUTS 0 phase lock fill rate		IUTS 0 Phase Lock Fill Rate. This 8-bit unsigned value, phase lock fill rate (default = 10), constitutes the size associated with a phase lock detector fill event. Phase Lock Fill Rate = 0 forces the DPLL to indicate phase lock status.	0x10	R/W	Live	No
0x0904	[7:0]	IUTS 0 phase lock drain rate		IUTS 0 Phase Lock Drain Rate. This 8-bit unsigned value, Phase Lock Drain Rate (default = 10), constitutes the size associated with a phase lock detector drain event. Phase Lock Drain Rate = 0 forces the DPLL to indicate phase unlock status.	0x10	R/W	Live	No
0x0905	[7:0]	IUTS 0 Frequency Lock Threshold[7:0]		IUTS 0 Frequency Lock Threshold. Synopsis: The digital frequency detector delivers time error samples (t_{DEV}) to the frequency lock detector, where t_{DEV} is the difference in period between the reference and feedback inputs to the PFD of the DPLL. The frequency lock detector compares the magnitude of each t_{DEV} sample to a user defined period error threshold (t_{P_ERR}). The comparison triggers a fill or drain event. Fill events (|t_{DEV}| ≤ t_{P_ERR}) steer the frequency lock detector toward lock status. Drain events (|t_{DEV}| > t_{P_ERR}) steer the frequency lock detector toward unlock status. This 24-bit unsigned value, Frequency Lock Threshold in units of picoseconds (default = 700), constitutes a period error threshold, t_{P_ERR} (seconds). Frequency Lock Threshold (rounded to the nearest integer) relates to t_{P_ERR} as follows: *Frequency Lock Threshold* = $t_{P\_ERR} \times 10^{12}$	0x188	R/W	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
				In practice, it is convenient to specify an offset frequency, Δf, as a frequency lock threshold, where Δf is relative to the nominal reference frequency, f_R, at the input to the PFD. Frequency Lock Threshold (rounded to the nearest integer) relates to Δf and f_R as follows: *Frequency Lock Threshold* = $(\Delta f/f_R)(1/(f_R + \Delta f)) \times 10^{12}$ For example, given $f_R = 8 \times 10^4$ (80 kHz) and Δf = 100 Hz, then Frequency Lock Threshold = 15,605 (0x 00 3CF5). The phase slew limiter has no effect on the operation of the frequency lock detector.				
0x0906	[7:0]	IUTS 0 Frequency Lock Threshold[15:8]		Continuation of the IUTS 0 frequency lock threshold bit field. See the IUTS 0 Frequency Lock Threshold[7:0] description.	0x02	R/W	Live	No
0x0907	[7:0]	IUTS 0 Frequency Lock Threshold[23:16]		Continuation of the IUTS 0 frequency lock threshold bit field. See the IUTS 0 Frequency Lock Threshold[7:0] description.	0x00	R/W	Live	No
0x0908	[7:0]	IUTS 0 frequency lock fill rate		IUTS 0 Frequency Lock Fill Rate. This 8-bit unsigned value, Frequency Lock Fill Rate (default = 10), constitutes the size associated with a frequency lock detector fill event. Frequency Lock Fill Rate = 0 forces the DPLL to indicate frequency lock status.	0x10	R/W	Live	No
0x0909	[7:0]	IUTS 0 frequency lock drain rate		IUTS 0 Frequency Lock Drain Rate. This 8-bit unsigned value, Frequency Lock Drain Rate (default = 10), constitutes the size associated with a frequency lock detector drain event. Frequency Lock Drain Rate = 0 forces the DPLL to indicate frequency unlock status.	0x10	R/W	Live	No
0x090A	[7:0]	IUTS 0 Phase Step Threshold[7:0]		IUTS 0 Phase Step Detector Threshold. This 32-bit unsigned value, Phase Step Threshold in units of picoseconds (default = 0), sets the time threshold (Φ_{THRESH} (seconds)) at which the DPLL declares that an input reference phase step has occurred. Phase Step Threshold = 0 (default) disables the phase step detector. Phase Step Threshold (rounded to the nearest integer) relates to Φ_{THRESH} as follows: *Phase Step Threshold* = $\Phi_{THRESH} \times 10^{12}$ For example, given a desired time threshold of $\Phi_{THRESH} = 12 \times 10^{-9}$ (12 ns), then Phase Step Threshold = 12,000 (0x 0000 2EE0). The user must choose a large enough value for phase step threshold to ensure the phase step detector activates only as a result of a reference switching event and not during normal DPLL operation.	0x00	R/W	Live	No
0x090B	[7:0]	IUTS 0 Phase Step Threshold[15:8]		Continuation of the IUTS 0 phase step threshold bit field. See the IUTS 0 Phase Step Threshold[7:0] description.	0x00	R/W	Live	No
0x090C	[7:0]	IUTS 0 Phase Step Threshold[23:16]		Continuation of the IUTS 0 phase step threshold bit field. See the IUTS 0 Phase Step Threshold[7:0] description.	0x00	R/W	Live	No
0x090D	[7:0]	IUTS 0 Phase Step Threshold[31:24]		Continuation of the IUTS 0 phase step threshold bit field. See the IUTS 0 Phase Step Threshold[7:0] description.	0x00	R/W	Live	No
0x090E	[7:0]	IUTS 0 Phase Skew[7:0]		IUTS 0 Phase Skew. This 24-bit signed value, Phase Skew in units of picoseconds (default = 0) defines a time skew for the phase skew adjustment feature. Time skew effectively constitutes a phase offset applied to the reference input associated with this source profile. Phase Skew (rounded to the nearest integer) relates to Time Skew as follows: *Phase Skew* = *Time Skew* $\times 10^{12}$ For example, given Time Skew = -35×10^{-9} (−35 ns), then Phase Skew = −35,000 (0x FF 7748). Phase Skew = 0 disables the phase skew adjustment feature.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x090F	[7:0]	IUTS 0 Phase Skew[15:8]		Continuation of the IUTS 0 phase skew bit field. See the IUTS 0 Phase Skew[7:0] description.	0x00	R/W	Core clock	No
0x0910	[7:0]	IUTS 0 Phase Skew[23:16]		Continuation of the IUTS 0 phase skew bit field. See the IUTS 0 Phase Skew[7:0] description.	0x00	R/W	Core clock	No
0x0911	[7:0]	IUTS 0 phase skew refinement steps		IUTS 0 Phase Skew Refinement Steps. This 8-bit unsigned value defines the number of DPLL PFD cycles the phase buildout processor uses in a phase buildout acquisition to assess the magnitude of phase buildout. The processor does not apply the buildout phase until the designated number of DPLL PFD cycles occurs. A value of zero (default) disables the phase skew refinement feature.	0x00	R/W	Live	No

SOURCE PROFILE: IUTS 1—REGISTER 0x0920 TO REGISTER 0x0931

Table 31. Source Profile: IUTS 1 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0920	[7:0]	IUTS 1 Phase Lock Threshold[7:0]		IUTS 1 Phase Lock Threshold. Synopsis: The digital phase detector delivers time error samples (ε) to the phase lock detector, where ε is the difference in time between the rising edge of the reference and feedback inputs to the PFD of the DPLL. The phase lock detector compares the magnitude of each time sample (|ε|) to a user defined time threshold (t_{THRESH}). The comparison triggers a fill or drain event. Fill events (|ε| ≤ t_{THRESH}) steer the phase lock detector toward lock status. Drain events (|ε| > t_{THRESH}) steer the phase lock detector toward unlock status. This 24-bit unsigned value, phase lock threshold in units of picoseconds (default = 700), constitutes a time threshold, t_{THRESH} (seconds). Phase Lock Threshold (rounded to the nearest integer) relates to t_{THRESH} as follows: *Phase Lock Threshold* = $t_{THRESH} \times 10^{12}$ For example, for a desired value of $t_{THRESH} = 10^{-9}$ sec (1 ns), then Phase Lock Threshold = 1000 (0x 00 03E8). When the phase slew limiter is actively in the process of phase slew limiting, the phase lock detector inhibits fill events (only drain events can occur during phase slew limiting).	0x188	R/W	Live	No
0x0921	[7:0]	IUTS 1 Phase Lock Threshold[15:8]		Continuation of the IUTS 1 phase lock threshold bit field. See the IUTS 1 Phase Lock Threshold[7:0] description.	0x02	R/W	Live	No
0x0922	[7:0]	IUTS 1 Phase Lock Threshold[23:16]		Continuation of the IUTS 1 phase lock threshold bit field. See the IUTS 1 Phase Lock Threshold[7:0] description.	0x00	R/W	Live	No
0x0923	[7:0]	IUTS 1 phase lock fill rate		IUTS 1 Phase Lock Fill Rate. This 8-bit unsigned value, phase lock fill rate (default = 10), constitutes the size associated with a phase lock detector fill event. Phase Lock Fill Rate = 0 forces the DPLL to indicate phase lock status.	0x10	R/W	Live	No
0x0924	[7:0]	IUTS 1 phase lock drain rate		IUTS 1 Phase Lock Drain Rate. This 8-bit unsigned value, Phase Lock Drain Rate (default = 10), constitutes the size associated with a phase lock detector drain event. Phase Lock Drain Rate = 0 forces the DPLL to indicate phase unlock status.	0x10	R/W	Live	No
0x0925	[7:0]	IUTS 1 Frequency Lock Threshold[7:0]		IUTS 1 Frequency Lock Threshold. Synopsis: The digital frequency detector delivers time error samples (t_{DEV}) to the frequency lock detector, where t_{DEV} is the difference in period between the reference and feedback inputs to the PFD of the DPLL. The frequency lock detector compares the magnitude of each t_{DEV} sample to a user defined period error threshold (t_{P_ERR}). The comparison triggers a fill or drain event. Fill events (|t_{DEV}| ≤ t_{P_ERR}) steer the frequency lock detector toward lock status. Drain events (|t_{DEV}| > t_{P_ERR}) steer the frequency lock detector toward unlock status. This 24-bit unsigned value, Frequency Lock Threshold in units of picoseconds (default = 700), constitutes a period error threshold, t_{P_ERR} (seconds). Frequency Lock Threshold (rounded to the nearest integer) relates to t_{P_ERR} as follows: *Frequency Lock Threshold* = $t_{P\_ERR} \times 10^{12}$	0x188	R/W	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
				In practice, it is convenient to specify an offset frequency, Δf, as a frequency lock threshold, where Δf is relative to the nominal reference frequency, f_R, at the input to the PFD. Frequency Lock Threshold (rounded to the nearest integer) relates to Δf and f_R as follows: *Frequency Lock Threshold* = $(\Delta f/f_R)(1/(f_R + \Delta f)) \times 10^{12}$ For example, given $f_R = 8 \times 10^4$ (80 kHz) and Δf = 100 Hz, then Frequency Lock Threshold = 15,605 (0x 00 3CF5). The phase slew limiter has no effect on the operation of the frequency lock detector.				
0x0926	[7:0]	IUTS 1 Frequency Lock Threshold[15:8]		Continuation of the IUTS 1 frequency lock threshold bit field. See the IUTS 1 Frequency Lock Threshold[7:0] description.	0x02	R/W	Live	No
0x0927	[7:0]	IUTS 1 Frequency Lock Threshold[23:16]		Continuation of the IUTS 1 frequency lock threshold bit field. See the IUTS 1 Frequency Lock Threshold[7:0] description.	0x00	R/W	Live	No
0x0928	[7:0]	IUTS 1 frequency lock fill rate		IUTS 1 Frequency Lock Fill Rate. This 8-bit unsigned value, Frequency Lock Fill Rate (default = 10), constitutes the size associated with a frequency lock detector fill event. Frequency Lock Fill Rate = 0 forces the DPLL to indicate frequency lock status.	0x10	R/W	Live	No
0x0929	[7:0]	IUTS 1 frequency lock drain rate		IUTS 1 Frequency Lock Drain Rate. This 8-bit unsigned value, Frequency Lock Drain Rate (default = 10), constitutes the size associated with a frequency lock detector drain event. Frequency Lock Drain Rate = 0 forces the DPLL to indicate frequency unlock status.	0x10	R/W	Live	No
0x092A	[7:0]	IUTS 1 Phase Step Threshold[7:0]		IUTS 1 Phase Step Detector Threshold. This 32-bit unsigned value, Phase Step Threshold in units of picoseconds (default = 0), sets the time threshold (Φ_{THRESH} (seconds)) at which the DPLL declares that an input reference phase step has occurred. Phase Step Threshold = 0 (default) disables the phase step detector. Phase Step Threshold (rounded to the nearest integer) relates to Φ_{THRESH} as follows: *Phase Step Threshold* = $\Phi_{THRESH} \times 10^{12}$ For example, given a desired time threshold of $\Phi_{THRESH} = 12 \times 10^{-9}$ (12 ns), then Phase Step Threshold = 12,000 (0x 0000 2EE0). The user must choose a large enough value for phase step threshold to ensure the phase step detector activates only as a result of a reference switching event and not during normal DPLL operation.	0x00	R/W	Live	No
0x092B	[7:0]	IUTS 1 Phase Step Threshold[15:8]		Continuation of the IUTS 1 phase step threshold bit field. See the IUTS 1 Phase Step Threshold[7:0] description.	0x00	R/W	Live	No
0x092C	[7:0]	IUTS 1 Phase Step Threshold[23:16]		Continuation of the IUTS 1 phase step threshold bit field. See the IUTS 1 Phase Step Threshold[7:0] description.	0x00	R/W	Live	No
0x092D	[7:0]	IUTS 1 Phase Step Threshold[31:24]		Continuation of the IUTS 1 phase step threshold bit field. See the IUTS 1 Phase Step Threshold[7:0] description.	0x00	R/W	Live	No
0x092E	[7:0]	IUTS 1 Phase Skew[7:0]		IUTS 1 Phase Skew. This 24-bit signed value, Phase Skew in units of picoseconds (default = 0) defines a time skew for the phase skew adjustment feature. Time skew effectively constitutes a phase offset applied to the reference input associated with this source profile. Phase Skew (rounded to the nearest integer) relates to Time Skew as follows: *Phase Skew* = *Time Skew* $\times 10^{12}$ For example, given Time Skew = -35×10^{-9} (−35 ns), then Phase Skew = −35,000 (0x FF 7748). Phase Skew = 0 disables the phase skew adjustment feature.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x092F	[7:0]	IUTS 1 Phase Skew[15:8]		Continuation of the IUTS 1 phase skew bit field. See the IUTS 1 Phase Skew[7:0] description.	0x00	R/W	Core clock	No
0x0930	[7:0]	IUTS 1 Phase Skew[23:16]		Continuation of the IUTS 1 phase skew bit field. See the IUTS 1 Phase Skew[7:0] description.	0x00	R/W	Core clock	No
0x0931	[7:0]	IUTS 1 phase skew refinement steps		IUTS 1 Phase Skew Refinement Steps. This 8-bit unsigned value defines the number of DPLL PFD cycles the phase buildout processor uses in a phase buildout acquisition to assess the magnitude of phase buildout. The processor does not apply the buildout phase until the designated number of DPLL PFD cycles occurs. A value of zero (default) disables the phase skew refinement feature.	0x00	R/W	Live	No

SOURCE PROFILE: AUXILIARY REF0—REGISTER 0x0940 TO REGISTER 0x0951

Table 32. Source Profile: Auxiliary REF0 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0940	[7:0]	Auxiliary REF0 Phase Lock Threshold[7:0]		Auxiliary REF0 Phase Lock Threshold. Synopsis: The digital phase detector delivers time error samples (ε) to the phase lock detector, where ε is the difference in time between the rising edge of the reference and feedback inputs to the PFD of the DPLL. The phase lock detector compares the magnitude of each time sample (|ε|) to a user defined time threshold (t_{THRESH}). The comparison triggers a fill or drain event. Fill events ($|\varepsilon| \leq t_{THRESH}$) steer the phase lock detector toward lock status. Drain events ($|\varepsilon| > t_{THRESH}$) steer the phase lock detector toward unlock status. This 24-bit unsigned value, phase lock threshold in units of picoseconds (default = 700), constitutes a time threshold, t_{THRESH} (seconds). Phase Lock Threshold (rounded to the nearest integer) relates to t_{THRESH} as follows: $Phase\ Lock\ Threshold = t_{THRESH} \times 10^{12}$ For example, for a desired value of $t_{THRESH} = 10^{-9}$ sec (1 ns), then Phase Lock Threshold = 1000 (0x 00 03E8). When the phase slew limiter is actively in the process of phase slew limiting, the phase lock detector inhibits fill events (only drain events can occur during phase slew limiting).	0x188	R/W	Live	No
0x0941	[7:0]	Auxiliary REF0 Phase Lock Threshold[15:8]		Continuation of the Auxiliary REF0 phase lock threshold bit field. See the Auxiliary REF0 Phase Lock Threshold[7:0] description.	0x02	R/W	Live	No
0x0942	[7:0]	Auxiliary REF0 Phase Lock Threshold[23:16]		Continuation of the Auxiliary REF0 phase lock threshold bit field. See the Auxiliary REF0 Phase Lock Threshold[7:0] description.	0x00	R/W	Live	No
0x0943	[7:0]	Auxiliary REF0 phase lock fill rate		Auxiliary REF0 Phase Lock Fill Rate. This 8-bit unsigned value, phase lock fill rate (default = 10), constitutes the size associated with a phase lock detector fill event. Phase Lock Fill Rate = 0 forces the DPLL to indicate phase lock status.	0x10	R/W	Live	No
0x0944	[7:0]	Auxiliary REF0 phase lock drain rate		Auxiliary REF0 Phase Lock Drain Rate. This 8-bit unsigned value, Phase Lock Drain Rate (default = 10), constitutes the size associated with a phase lock detector drain event. Phase Lock Drain Rate = 0 forces the DPLL to indicate phase unlock status.	0x10	R/W	Live	No
0x0945	[7:0]	Auxiliary REF0 Frequency Lock Threshold[7:0]		Auxiliary REF0 Frequency Lock Threshold. Synopsis: The digital frequency detector delivers time error samples (t_{DEV}) to the frequency lock detector, where t_{DEV} is the difference in period between the reference and feedback inputs to the PFD of the DPLL. The frequency lock detector compares the magnitude of each t_{DEV} sample to a user defined period error threshold (t_{P_ERR}). The comparison triggers a fill or drain event. Fill events ($|t_{DEV}| \leq t_{P\_ERR}$) steer the frequency lock detector toward lock status. Drain events ($|t_{DEV}| > t_{P\_ERR}$) steer the frequency lock detector toward unlock status. This 24-bit unsigned value, Frequency Lock Threshold in units of picoseconds (default = 700), constitutes a period error threshold, t_{P_ERR} (seconds). Frequency Lock Threshold (rounded to the nearest integer) relates to t_{P_ERR} as follows: $Frequency\ Lock\ Threshold = t_{P\_ERR} \times 10^{12}$	0x188	R/W	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
				In practice, it is convenient to specify an offset frequency, Δf, as a frequency lock threshold, where Δf is relative to the nominal reference frequency, f_R, at the input to the PFD. Frequency Lock Threshold (rounded to the nearest integer) relates to Δf and f_R as follows: *Frequency Lock Threshold* = $(\Delta f/f_R)(1/(f_R + \Delta f)) \times 10^{12}$ For example, given $f_R = 8 \times 10^4$ (80 kHz) and Δf = 100 Hz, then Frequency Lock Threshold = 15,605 (0x 00 3CF5). The phase slew limiter has no effect on the operation of the frequency lock detector.				
0x0946	[7:0]	Auxiliary REF0 Frequency Lock Threshold[15:8]		Continuation of the Auxiliary REF0 frequency lock threshold bit field. See the Auxiliary REF0 Frequency Lock Threshold[7:0] description.	0x02	R/W	Live	No
0x0947	[7:0]	Auxiliary REF0 Frequency Lock Threshold[23:16]		Continuation of the Auxiliary REF0 frequency lock threshold bit field. See the Auxiliary REF0 Frequency Lock Threshold[7:0] description.	0x00	R/W	Live	No
0x0948	[7:0]	Auxiliary REF0 frequency lock fill rate		Auxiliary REF0 Frequency Lock Fill Rate. This 8-bit unsigned value, Frequency Lock Fill Rate (default = 10), constitutes the size associated with a frequency lock detector fill event. Frequency Lock Fill Rate = 0 forces the DPLL to indicate frequency lock status.	0x10	R/W	Live	No
0x0949	[7:0]	Auxiliary REF0 frequency lock drain rate		Auxiliary REF0 Frequency Lock Drain Rate. This 8-bit unsigned value, Frequency Lock Drain Rate (default = 10), constitutes the size associated with a frequency lock detector drain event. Frequency Lock Drain Rate = 0 forces the DPLL to indicate frequency unlock status.	0x10	R/W	Live	No
0x094A	[7:0]	Auxiliary REF0 Phase Step Threshold[7:0]		Auxiliary REF0 Phase Step Detector Threshold. This 32-bit unsigned value, Phase Step Threshold in units of picoseconds (default = 0), sets the time threshold (Φ_{THRESH} (seconds)) at which the DPLL declares that an input reference phase step has occurred. Phase Step Threshold = 0 (default) disables the phase step detector. Phase Step Threshold (rounded to the nearest integer) relates to Φ_{THRESH} as follows: *Phase Step Threshold* = $\Phi_{THRESH} \times 10^{12}$ For example, given a desired time threshold of $\Phi_{THRESH} = 12 \times 10^{-9}$ (12 ns), then Phase Step Threshold = 12,000 (0x 0000 2EE0). The user must choose a large enough value for phase step threshold to ensure the phase step detector activates only as a result of a reference switching event and not during normal DPLL operation.	0x00	R/W	Live	No
0x094B	[7:0]	Auxiliary REF0 Phase Step Threshold[15:8]		Continuation of the Auxiliary REF0 phase step threshold bit field. See the Auxiliary REF0 Phase Step Threshold[7:0] description.	0x00	R/W	Live	No
0x094C	[7:0]	Auxiliary REF0 Phase Step Threshold[23:16]		Continuation of the Auxiliary REF0 phase step threshold bit field. See the Auxiliary REF0 Phase Step Threshold[7:0] description.	0x00	R/W	Live	No
0x094D	[7:0]	Auxiliary REF0 Phase Step Threshold[31:24]		Continuation of the Auxiliary REF0 phase step threshold bit field. See the Auxiliary REF0 Phase Step Threshold[7:0] description.	0x00	R/W	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x094E	[7:0]	Auxiliary REF0 Phase Skew[7:0]		Auxiliary REF0 Phase Skew. This 24-bit signed value, Phase Skew in units of picoseconds (default = 0) defines a time skew for the phase skew adjustment feature. Time skew effectively constitutes a phase offset applied to the reference input associated with this source profile. Phase Skew (rounded to the nearest integer) relates to Time Skew as follows: $Phase\ Skew = Time\ Skew \times 10^{12}$ For example, given Time Skew = -35×10^{-9} (−35 ns), then Phase Skew = −35,000 (0x FF 7748). Phase Skew = 0 disables the phase skew adjustment feature.	0x00	R/W	Core clock	No
0x094F	[7:0]	Auxiliary REF0 Phase Skew[15:8]		Continuation of the Auxiliary REF0 phase skew bit field. See the Auxiliary REF0 Phase Skew[7:0] description.	0x00	R/W	Core clock	No
0x0950	[7:0]	Auxiliary REF0 Phase Skew[23:16]		Continuation of the Auxiliary REF0 phase skew bit field. See the Auxiliary REF0 Phase Skew[7:0] description.	0x00	R/W	Core clock	No
0x0951	[7:0]	Auxiliary REF0 phase skew refinement steps		Auxiliary REF0 Phase Skew Refinement Steps. This 8-bit unsigned value defines the number of DPLL PFD cycles the phase buildout processor uses in a phase buildout acquisition to assess the magnitude of phase buildout. The processor does not apply the buildout phase until the designated number of DPLL PFD cycles occurs. A value of zero (default) disables the phase skew refinement feature.	0x00	R/W	Live	No

SOURCE PROFILE: AUXILIARY REF1—REGISTER 0x0960 TO REGISTER 0x0971

Table 33. Source Profile: Auxiliary REF1 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0960	[7:0]	Auxiliary REF1 Phase Lock Threshold[7:0]		Auxiliary REF1 Phase Lock Threshold. Synopsis: The digital phase detector delivers time error samples (ε) to the phase lock detector, where ε is the difference in time between the rising edge of the reference and feedback inputs to the PFD of the DPLL. The phase lock detector compares the magnitude of each time sample (|ε|) to a user defined time threshold (t_{THRESH}). The comparison triggers a fill or drain event. Fill events (|ε| ≤ t_{THRESH}) steer the phase lock detector toward lock status. Drain events (|ε| > t_{THRESH}) steer the phase lock detector toward unlock status. This 24-bit unsigned value, phase lock threshold in units of picoseconds (default = 700), constitutes a time threshold, t_{THRESH} (seconds). Phase Lock Threshold (rounded to the nearest integer) relates to t_{THRESH} as follows: *Phase Lock Threshold* = $t_{THRESH} \times 10^{12}$ For example, for a desired value of $t_{THRESH} = 10^{-9}$ sec (1 ns), then Phase Lock Threshold = 1000 (0x 00 03E8). When the phase slew limiter is actively in the process of phase slew limiting, the phase lock detector inhibits fill events (only drain events can occur during phase slew limiting).	0x188	R/W	Live	No
0x0961	[7:0]	Auxiliary REF1 Phase Lock Threshold[15:8]		Continuation of the Auxiliary REF1 phase lock threshold bit field. See the Auxiliary REF1 Phase Lock Threshold[7:0] description.	0x02	R/W	Live	No
0x0962	[7:0]	Auxiliary REF1 Phase Lock Threshold[23:16]		Continuation of the Auxiliary REF1 phase lock threshold bit field. See the Auxiliary REF1 Phase Lock Threshold[7:0] description.	0x00	R/W	Live	No
0x0963	[7:0]	Auxiliary REF1 phase lock fill rate		Auxiliary REF1 Phase Lock Fill Rate. This 8-bit unsigned value, phase lock fill rate (default = 10), constitutes the size associated with a phase lock detector fill event. Phase Lock Fill Rate = 0 forces the DPLL to indicate phase lock status.	0x10	R/W	Live	No
0x0964	[7:0]	Auxiliary REF1 phase lock drain rate		Auxiliary REF1 Phase Lock Drain Rate. This 8-bit unsigned value, Phase Lock Drain Rate (default = 10), constitutes the size associated with a phase lock detector drain event. Phase Lock Drain Rate = 0 forces the DPLL to indicate phase unlock status.	0x10	R/W	Live	No
0x0965	[7:0]	Auxiliary REF1 Frequency Lock Threshold[7:0]		Auxiliary REF1 Frequency Lock Threshold. Synopsis: The digital frequency detector delivers time error samples (t_{DEV}) to the frequency lock detector, where t_{DEV} is the difference in period between the reference and feedback inputs to the PFD of the DPLL. The frequency lock detector compares the magnitude of each t_{DEV} sample to a user defined period error threshold (t_{P_ERR}). The comparison triggers a fill or drain event. Fill events (|t_{DEV}| ≤ t_{P_ERR}) steer the frequency lock detector toward lock status. Drain events (|t_{DEV}| > t_{P_ERR}) steer the frequency lock detector toward unlock status. This 24-bit unsigned value, Frequency Lock Threshold in units of picoseconds (default = 700), constitutes a period error threshold, t_{P_ERR} (seconds). Frequency Lock Threshold (rounded to the nearest integer) relates to t_{P_ERR} as follows: *Frequency Lock Threshold* = $t_{P\_ERR} \times 10^{12}$	0x188	R/W	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
				In practice, it is convenient to specify an offset frequency, Δf, as a frequency lock threshold, where Δf is relative to the nominal reference frequency, f_R, at the input to the PFD. Frequency Lock Threshold (rounded to the nearest integer) relates to Δf and f_R as follows: *Frequency Lock Threshold* = $(\Delta f/f_R)(1/(f_R + \Delta f)) \times 10^{12}$ For example, given $f_R = 8 \times 10^4$ (80 kHz) and Δf = 100 Hz, then Frequency Lock Threshold = 15,605 (0x 00 3CF5). The phase slew limiter has no effect on the operation of the frequency lock detector.				
0x0966	[7:0]	Auxiliary REF1 Frequency Lock Threshold[15:8]		Continuation of the Auxiliary REF1 frequency lock threshold bit field. See the Auxiliary REF1 Frequency Lock Threshold[7:0] description.	0x02	R/W	Live	No
0x0967	[7:0]	Auxiliary REF1 Frequency Lock Threshold[23:16]		Continuation of the Auxiliary REF1 frequency lock threshold bit field. See the Auxiliary REF1 Frequency Lock Threshold[7:0] description.	0x00	R/W	Live	No
0x0968	[7:0]	Auxiliary REF1 frequency lock fill rate		Auxiliary REF1 Frequency Lock Fill Rate. This 8-bit unsigned value, Frequency Lock Fill Rate (default = 10), constitutes the size associated with a frequency lock detector fill event. Frequency Lock Fill Rate = 0 forces the DPLL to indicate frequency lock status.	0x10	R/W	Live	No
0x0969	[7:0]	Auxiliary REF1 frequency lock drain rate		Auxiliary REF1 Frequency Lock Drain Rate. This 8-bit unsigned value, Frequency Lock Drain Rate (default = 10), constitutes the size associated with a frequency lock detector drain event. Frequency Lock Drain Rate = 0 forces the DPLL to indicate frequency unlock status.	0x10	R/W	Live	No
0x096A	[7:0]	Auxiliary REF1 Phase Step Threshold[7:0]		Auxiliary REF1 Phase Step Detector Threshold. This 32-bit unsigned value, Phase Step Threshold in units of picoseconds (default = 0), sets the time threshold (Φ_{THRESH} (seconds)) at which the DPLL declares that an input reference phase step has occurred. Phase Step Threshold = 0 (default) disables the phase step detector. Phase Step Threshold (rounded to the nearest integer) relates to Φ_{THRESH} as follows: *Phase Step Threshold* = $\Phi_{THRESH} \times 10^{12}$ For example, given a desired time threshold of $\Phi_{THRESH} = 12 \times 10^{-9}$ (12 ns), then Phase Step Threshold = 12,000 (0x 0000 2EE0). The user must choose a large enough value for phase step threshold to ensure the phase step detector activates only as a result of a reference switching event and not during normal DPLL operation.	0x00	R/W	Live	No
0x096B	[7:0]	Auxiliary REF1 Phase Step Threshold[15:8]		Continuation of the Auxiliary REF1 phase step threshold bit field. See the Auxiliary REF1 Phase Step Threshold[7:0] description.	0x00	R/W	Live	No
0x096C	[7:0]	Auxiliary REF1 Phase Step Threshold[23:16]		Continuation of the Auxiliary REF1 phase step threshold bit field. See the Auxiliary REF1 Phase Step Threshold[7:0] description.	0x00	R/W	Live	No
0x096D	[7:0]	Auxiliary REF1 Phase Step Threshold[31:24]		Continuation of the Auxiliary REF1 phase step threshold bit field. See the Auxiliary REF1 Phase Step Threshold[7:0] description.	0x00	R/W	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x096E	[7:0]	Auxiliary REF1 Phase Skew[7:0]		Auxiliary REF1 Phase Skew. This 24-bit signed value, Phase Skew in units of picoseconds (default = 0) defines a time skew for the phase skew adjustment feature. Time skew effectively constitutes a phase offset applied to the reference input associated with this source profile. Phase Skew (rounded to the nearest integer) relates to Time Skew as follows: $Phase\ Skew = Time\ Skew \times 10^{12}$ For example, given Time Skew = -35×10^{-9} (−35 ns), then Phase Skew = −35,000 (0x FF 7748). Phase Skew = 0 disables the phase skew adjustment feature.	0x00	R/W	Core clock	No
0x096F	[7:0]	Auxiliary REF1 Phase Skew[15:8]		Continuation of the Auxiliary REF1 phase skew bit field. See the Auxiliary REF1 Phase Skew[7:0] description.	0x00	R/W	Core clock	No
0x0970	[7:0]	Auxiliary REF1 Phase Skew[23:16]		Continuation of the Auxiliary REF1 phase skew bit field. See the Auxiliary REF1 Phase Skew[7:0] description.	0x00	R/W	Core clock	No
0x0971	[7:0]	Auxiliary REF1 phase skew refinement steps		Auxiliary REF1 Phase Skew Refinement Steps. This 8-bit unsigned value defines the number of DPLL PFD cycles the phase buildout processor uses in a phase buildout acquisition to assess the magnitude of phase buildout. The processor does not apply the buildout phase until the designated number of DPLL PFD cycles occurs. A value of zero (default) disables the phase skew refinement feature.	0x00	R/W	Live	No

SOURCE PROFILE: AUXILIARY REF2—REGISTER 0x0980 TO REGISTER 0x0991

Table 34. Source Profile: Auxiliary REF2 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0980	[7:0]	Auxiliary REF2 Phase Lock Threshold[7:0]		Auxiliary REF2 Phase Lock Threshold. Synopsis: The digital phase detector delivers time error samples (ε) to the phase lock detector, where ε is the difference in time between the rising edge of the reference and feedback inputs to the PFD of the DPLL. The phase lock detector compares the magnitude of each time sample (|ε|) to a user defined time threshold (t_{THRESH}). The comparison triggers a fill or drain event. Fill events ($|\varepsilon| \le t_{THRESH}$) steer the phase lock detector toward lock status. Drain events ($|\varepsilon| > t_{THRESH}$) steer the phase lock detector toward unlock status. This 24-bit unsigned value, phase lock threshold in units of picoseconds (default = 700), constitutes a time threshold, t_{THRESH} (seconds). Phase Lock Threshold (rounded to the nearest integer) relates to t_{THRESH} as follows: $Phase\ Lock\ Threshold = t_{THRESH} \times 10^{12}$ For example, for a desired value of $t_{THRESH} = 10^{-9}$ sec (1 ns), then Phase Lock Threshold = 1000 (0x 00 03E8). When the phase slew limiter is actively in the process of phase slew limiting, the phase lock detector inhibits fill events (only drain events can occur during phase slew limiting).	0x188	R/W	Live	No
0x0981	[7:0]	Auxiliary REF2 Phase Lock Threshold[15:8]		Continuation of the Auxiliary REF2 phase lock threshold bit field. See the Auxiliary REF2 Phase Lock Threshold[7:0] description.	0x02	R/W	Live	No
0x0982	[7:0]	Auxiliary REF2 Phase Lock Threshold[23:16]		Continuation of the Auxiliary REF2 phase lock threshold bit field. See the Auxiliary REF2 Phase Lock Threshold[7:0] description.	0x00	R/W	Live	No
0x0983	[7:0]	Auxiliary REF2 phase lock fill rate		Auxiliary REF2 Phase Lock Fill Rate. This 8-bit unsigned value, phase lock fill rate (default = 10), constitutes the size associated with a phase lock detector fill event. Phase Lock Fill Rate = 0 forces the DPLL to indicate phase lock status.	0x10	R/W	Live	No
0x0984	[7:0]	Auxiliary REF2 phase lock drain rate		Auxiliary REF2 Phase Lock Drain Rate. This 8-bit unsigned value, Phase Lock Drain Rate (default = 10), constitutes the size associated with a phase lock detector drain event. Phase Lock Drain Rate = 0 forces the DPLL to indicate phase unlock status.	0x10	R/W	Live	No
0x0985	[7:0]	Auxiliary REF2 Frequency Lock Threshold[7:0]		Auxiliary REF2 Frequency Lock Threshold. Synopsis: The digital frequency detector delivers time error samples (t_{DEV}) to the frequency lock detector, where t_{DEV} is the difference in period between the reference and feedback inputs to the PFD of the DPLL. The frequency lock detector compares the magnitude of each t_{DEV} sample to a user defined period error threshold (t_{P_ERR}). The comparison triggers a fill or drain event. Fill events ($|t_{DEV}| \le t_{P\_ERR}$) steer the frequency lock detector toward lock status. Drain events ($|t_{DEV}| > t_{P\_ERR}$) steer the frequency lock detector toward unlock status. This 24-bit unsigned value, Frequency Lock Threshold in units of picoseconds (default = 700), constitutes a period error threshold, t_{P_ERR} (seconds). Frequency Lock Threshold (rounded to the nearest integer) relates to t_{P_ERR} as follows: $Frequency\ Lock\ Threshold = t_{P\_ERR} \times 10^{12}$	0x188	R/W	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
				In practice, it is convenient to specify an offset frequency, Δf, as a frequency lock threshold, where Δf is relative to the nominal reference frequency, f_R, at the input to the PFD. Frequency Lock Threshold (rounded to the nearest integer) relates to Δf and f_R as follows: *Frequency Lock Threshold* = $(\Delta f/f_R)(1/(f_R + \Delta f)) \times 10^{12}$ For example, given $f_R = 8 \times 10^4$ (80 kHz) and Δf = 100 Hz, then Frequency Lock Threshold = 15,605 (0x 00 3CF5). The phase slew limiter has no effect on the operation of the frequency lock detector.				
0x0986	[7:0]	Auxiliary REF2 Frequency Lock Threshold[15:8]		Continuation of the Auxiliary REF2 frequency lock threshold bit field. See the Auxiliary REF2 Frequency Lock Threshold[7:0] description.	0x02	R/W	Live	No
0x0987	[7:0]	Auxiliary REF2 Frequency Lock Threshold[23:16]		Continuation of the Auxiliary REF2 frequency lock threshold bit field. See the Auxiliary REF2 Frequency Lock Threshold[7:0] description.	0x00	R/W	Live	No
0x0988	[7:0]	Auxiliary REF2 frequency lock fill rate		Auxiliary REF2 Frequency Lock Fill Rate. This 8-bit unsigned value, Frequency Lock Fill Rate (default = 10), constitutes the size associated with a frequency lock detector fill event. Frequency Lock Fill Rate = 0 forces the DPLL to indicate frequency lock status.	0x10	R/W	Live	No
0x0989	[7:0]	Auxiliary REF2 frequency lock drain rate		Auxiliary REF2 Frequency Lock Drain Rate. This 8-bit unsigned value, frequency lock drain rate (default = 10), constitutes the size associated with a frequency lock detector drain event. Frequency Lock Drain Rate = 0 forces the DPLL to indicate frequency unlock status.	0x10	R/W	Live	No
0x098A	[7:0]	Auxiliary REF2 Phase Step Threshold[7:0]		Auxiliary REF2 Phase Step Detector Threshold. This 32-bit unsigned value, Phase Step Threshold in units of picoseconds (default = 0), sets the time threshold (Φ_{THRESH} (seconds)) at which the DPLL declares that an input reference phase step has occurred. Phase Step Threshold = 0 (default) disables the phase step detector. Phase Step Threshold (rounded to the nearest integer) relates to Φ_{THRESH} as follows: *Phase Step Threshold* = $\Phi_{THRESH} \times 10^{12}$ For example, given a desired time threshold of $\Phi_{THRESH} = 12 \times 10^{-9}$ (12 ns), then Phase Step Threshold = 12,000 (0x 0000 2EE0). The user must choose a large enough value for phase step threshold to ensure the phase step detector activates only as a result of a reference switching event and not during normal DPLL operation.	0x00	R/W	Live	No
0x098B	[7:0]	Auxiliary REF2 Phase Step Threshold[15:8]		Continuation of the Auxiliary REF2 phase step threshold bit field. See the Auxiliary REF2 Phase Step Threshold[7:0] description.	0x00	R/W	Live	No
0x098C	[7:0]	Auxiliary REF2 Phase Step Threshold[23:16]		Continuation of the Auxiliary REF2 phase step threshold bit field. See the Auxiliary REF2 Phase Step Threshold[7:0] description.	0x00	R/W	Live	No
0x098D	[7:0]	Auxiliary REF2 Phase Step Threshold[31:24]		Continuation of the Auxiliary REF2 phase step threshold bit field. See the Auxiliary REF2 Phase Step Threshold[7:0] description.	0x00	R/W	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x098E	[7:0]	Auxiliary REF2 Phase Skew[7:0]		Auxiliary REF2 Phase Skew. This 24-bit signed value, Phase Skew in units of picoseconds (default = 0) defines a time skew for the phase skew adjustment feature. Time skew effectively constitutes a phase offset applied to the reference input associated with this source profile. Phase Skew (rounded to the nearest integer) relates to Time Skew as follows: $Phase\ Skew = Time\ Skew \times 10^{12}$ For example, given Time Skew = -35×10^{-9} (−35 ns), then Phase Skew = −35,000 (0x FF 7748). Phase Skew = 0 disables the phase skew adjustment feature.	0x00	R/W	Core clock	No
0x098F	[7:0]	Auxiliary REF2 Phase Skew[15:8]		Continuation of the Auxiliary REF2 phase skew bit field. See the Auxiliary REF2 Phase Skew[7:0] description.	0x00	R/W	Core clock	No
0x0990	[7:0]	Auxiliary REF2 Phase Skew[23:16]		Continuation of the Auxiliary REF2 phase skew bit field. See the Auxiliary REF2 Phase Skew[7:0] description.	0x00	R/W	Core clock	No
0x0991	[7:0]	Auxiliary REF2 phase skew refinement steps		Auxiliary REF2 Phase Skew Refinement Steps. This 8-bit unsigned value defines the number of DPLL PFD cycles the phase buildout processor uses in a phase buildout acquisition to assess the magnitude of phase buildout. The processor does not apply the buildout phase until the designated number of DPLL PFD cycles occurs. A value of zero (default) disables the phase skew refinement feature.	0x00	R/W	Live	No

SOURCE PROFILE: AUXILIARY REF3—REGISTER 0x09A0 TO REGISTER 0x09B1

Table 35. Source Profile: Auxiliary REF3 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x09A0	[7:0]	Auxiliary REF3 Phase Lock Threshold[7:0]		Auxiliary REF3 Phase Lock Threshold. Synopsis: The digital phase detector delivers time error samples (ε) to the phase lock detector, where ε is the difference in time between the rising edge of the reference and feedback inputs to the PFD of the DPLL. The phase lock detector compares the magnitude of each time sample (|ε|) to a user defined time threshold (t_{THRESH}). The comparison triggers a fill or drain event. Fill events (|ε| ≤ t_{THRESH}) steer the phase lock detector toward lock status. Drain events (|ε| > t_{THRESH}) steer the phase lock detector toward unlock status. This 24-bit unsigned value, phase lock threshold in units of picoseconds (default = 700), constitutes a time threshold, t_{THRESH} (seconds). Phase Lock Threshold (rounded to the nearest integer) relates to t_{THRESH} as follows: *Phase Lock Threshold* = $t_{THRESH} \times 10^{12}$ For example, for a desired value of $t_{THRESH} = 10^{-9}$ sec (1 ns), then Phase Lock Threshold = 1000 (0x 00 03E8). When the phase slew limiter is actively in the process of phase slew limiting, the phase lock detector inhibits fill events (only drain events can occur during phase slew limiting).	0x188	R/W	Live	No
0x09A1	[7:0]	Auxiliary REF3 Phase Lock Threshold[15:8]		Continuation of the Auxiliary REF3 phase lock threshold bit field. See the Auxiliary REF3 Phase Lock Threshold[7:0] description.	0x02	R/W	Live	No
0x09A2	[7:0]	Auxiliary REF3 Phase Lock Threshold[23:16]		Continuation of the Auxiliary REF3 phase lock threshold bit field. See the Auxiliary REF3 Phase Lock Threshold[7:0] description.	0x00	R/W	Live	No
0x09A3	[7:0]	Auxiliary REF3 phase lock fill rate		Auxiliary REF3 Phase Lock Fill Rate. This 8-bit unsigned value, phase lock fill rate (default = 10), constitutes the size associated with a phase lock detector fill event. Phase Lock Fill Rate = 0 forces the DPLL to indicate phase lock status.	0x10	R/W	Live	No
0x09A4	[7:0]	Auxiliary REF3 phase lock drain rate		Auxiliary REF3 Phase Lock Drain Rate. This 8-bit unsigned value, Phase Lock Drain Rate (default = 10), constitutes the size associated with a phase lock detector drain event. Phase Lock Drain Rate = 0 forces the DPLL to indicate phase unlock status.	0x10	R/W	Live	No
0x09A5	[7:0]	Auxiliary REF3 Frequency Lock Threshold[7:0]		Auxiliary REF3 Frequency Lock Threshold. Synopsis: The digital frequency detector delivers time error samples (t_{DEV}) to the frequency lock detector, where t_{DEV} is the difference in period between the reference and feedback inputs to the PFD of the DPLL. The frequency lock detector compares the magnitude of each t_{DEV} sample to a user defined period error threshold (t_{P_ERR}). The comparison triggers a fill or drain event. Fill events (|t_{DEV}| ≤ t_{P_ERR}) steer the frequency lock detector toward lock status. Drain events (|t_{DEV}| > t_{P_ERR}) steer the frequency lock detector toward unlock status. This 24-bit unsigned value, Frequency Lock Threshold in units of picoseconds (default = 700), constitutes a period error threshold, t_{P_ERR} (seconds). Frequency Lock Threshold (rounded to the nearest integer) relates to t_{P_ERR} as follows: *Frequency Lock Threshold* = $t_{P\_ERR} \times 10^{12}$	0x188	R/W	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
				In practice, it is convenient to specify an offset frequency, Δf, as a frequency lock threshold, where Δf is relative to the nominal reference frequency, f_R, at the input to the PFD. Frequency Lock Threshold (rounded to the nearest integer) relates to Δf and f_R as follows: *Frequency Lock Threshold* = $(\Delta f/f_R)(1/(f_R + \Delta f)) \times 10^{12}$ For example, given $f_R = 8 \times 10^4$ (80 kHz) and Δf = 100 Hz, then Frequency Lock Threshold = 15,605 (0x 00 3CF5). The phase slew limiter has no effect on the operation of the frequency lock detector.				
0x09A6	[7:0]	Auxiliary REF3 Frequency Lock Threshold[15:8]		Continuation of the Auxiliary REF3 frequency lock threshold bit field. See the Auxiliary REF3 Frequency Lock Threshold[7:0] description.	0x02	R/W	Live	No
0x09A7	[7:0]	Auxiliary REF3 Frequency Lock Threshold[23:16]		Continuation of the Auxiliary REF3 frequency lock threshold bit field. See the Auxiliary REF3 Frequency Lock Threshold[7:0] description.	0x00	R/W	Live	No
0x09A8	[7:0]	Auxiliary REF3 frequency lock fill rate		Auxiliary REF3 Frequency Lock Fill Rate. This 8-bit unsigned value, Frequency Lock Fill Rate (default = 10), constitutes the size associated with a frequency lock detector fill event. Frequency Lock Fill Rate = 0 forces the DPLL to indicate frequency lock status.	0x10	R/W	Live	No
0x09A9	[7:0]	Auxiliary REF3 frequency lock drain rate		Auxiliary REF3 Frequency Lock Drain Rate. This 8-bit unsigned value, Frequency Lock Drain Rate (default = 10), constitutes the size associated with a frequency lock detector drain event. Frequency Lock Drain Rate = 0 forces the DPLL to indicate frequency unlock status.	0x10	R/W	Live	No
0x09AA	[7:0]	Auxiliary REF3 Phase Step Threshold[7:0]		Auxiliary REF3 Phase Step Detector Threshold. This 32-bit unsigned value, Phase Step Threshold in units of picoseconds (default = 0), sets the time threshold (Φ_{THRESH} (seconds)) at which the DPLL declares that an input reference phase step has occurred. Phase Step Threshold = 0 (default) disables the phase step detector. Phase Step Threshold (rounded to the nearest integer) relates to Φ_{THRESH} as follows: *Phase Step Threshold* = $\Phi_{THRESH} \times 10^{12}$ For example, given a desired time threshold of $\Phi_{THRESH} = 12 \times 10^{-9}$ (12 ns), then Phase Step Threshold = 12,000 (0x 0000 2EE0). The user must choose a large enough value for phase step threshold to ensure the phase step detector activates only as a result of a reference switching event and not during normal DPLL operation.	0x00	R/W	Live	No
0x09AB	[7:0]	Auxiliary REF3 Phase Step Threshold[15:8]		Continuation of the Auxiliary REF3 phase step threshold bit field. See the Auxiliary REF3 Phase Step Threshold[7:0] description.	0x00	R/W	Live	No
0x09AC	[7:0]	Auxiliary REF3 Phase Step Threshold[23:16]		Continuation of the Auxiliary REF3 phase step threshold bit field. See the Auxiliary REF3 Phase Step Threshold[7:0] description.	0x00	R/W	Live	No
0x09AD	[7:0]	Auxiliary REF3 Phase Step Threshold[31:24]		Continuation of the Auxiliary REF3 phase step threshold bit field. See the Auxiliary REF3 Phase Step Threshold[7:0] description.	0x00	R/W	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x09AE	[7:0]	Auxiliary REF3 Phase Skew[7:0]		Auxiliary REF3 Phase Skew. This 24-bit signed value, Phase Skew in units of picoseconds (default = 0) defines a time skew for the phase skew adjustment feature. Time skew effectively constitutes a phase offset applied to the reference input associated with this source profile. Phase Skew (rounded to the nearest integer) relates to Time Skew as follows: $Phase\ Skew = Time\ Skew \times 10^{12}$ For example, given Time Skew = -35×10^{-9} (−35 ns), then Phase Skew = −35,000 (0x FF 7748). Phase Skew = 0 disables the phase skew adjustment feature.	0x00	R/W	Core clock	No
0x09AF	[7:0]	Auxiliary REF3 Phase Skew[15:8]		Continuation of the Auxiliary REF3 phase skew bit field. See the Auxiliary REF3 Phase Skew[7:0] description.	0x00	R/W	Core clock	No
0x09B0	[7:0]	Auxiliary REF3 Phase Skew[23:16]		Continuation of the Auxiliary REF3 phase skew bit field. See the Auxiliary REF3 Phase Skew[7:0] description.	0x00	R/W	Core clock	No
0x09B1	[7:0]	Auxiliary REF3 phase skew refinement steps		Auxiliary REF3 Phase Skew Refinement Steps. This 8-bit unsigned value defines the number of DPLL PFD cycles the phase buildout processor uses in a phase buildout acquisition to assess the magnitude of phase buildout. The processor does not apply the buildout phase until the designated number of DPLL PFD cycles occurs. A value of zero (default) disables the phase skew refinement feature.	0x00	R/W	Live	No

DPLL LOOP FILTER 0 (LF0) COEFFICIENTS—REGISTER 0x0C00 TO REGISTER 0x0C0B

Table 36. DPLL Loop Filter 0 (LF0) Coefficient Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0C00	[7:0]	Alpha 0 Significand[7:0]		Alpha 0 Significand. Synopsis: The DPLL loop filter, LF0, requires four coefficients, C_LF0_x, where x = 0 to 3. Each coefficient makes use of an integer significand (S) and an integer exponent (E) as follows: $C\_LF0_x = S \times 2^{(E-16)}$	0x194	R/W	Live	No
0x0C01	[7:0]	Alpha 0 Significand[15:8]		Continuation of the Alpha 0 significand bit field. See the Alpha 0 Significand[7:0] description.	0x240	R/W	Live	No
0x0C02	[7:0]	Alpha 0 exponent		Alpha 0 Exponent. Synopsis: see Register 0x0C00.	0x179	R/W	Live	No
0x0C03	[7:0]	Beta 0 Significand[7:0]		Beta 0 Significand. Synopsis: See Register 0x0C00.	0x85	R/W	Live	No
0x0C04	[7:0]	Beta 0 Significand[15:8]		Continuation of the Beta 0 significand bit field. See the Beta 0 Significand[7:0] description.	0x201	R/W	Live	No
0x0C05	[7:0]	Beta 0 exponent		Beta 0 Exponent. Synopsis: See Register 0x0C00.	0x251	R/W	Live	No
0x0C06	[7:0]	Gamma 0 Significand[7:0]		Gamma 0 Significand. Synopsis: See Register 0x0C00.	0x92	R/W	Live	No
0x0C07	[7:0]	Gamma 0 Significand[15:8]		Continuation of the Gamma 0 significand bit field. See the Gamma 0 Significand[7:0] description.	0x246	R/W	Live	No
0x0C08	[7:0]	Gamma 0 Exponent		Gamma 0 Exponent. Synopsis: See Register 0x0C00.	0x202	R/W	Live	No
0x0C09	[7:0]	Delta 0 Significand[7:0]		Delta 0 Significand. Synopsis: See Register 0x0C00.	0x17	R/W	Live	No
0x0C0A	[7:0]	Delta 0 Significand[15:8]		Continuation of the Delta 0 significand bit field. See the Delta 0 Significand[7:0] description.	0x223	R/W	Live	No
0x0C0B	[7:0]	Delta 0 exponent		Delta 0 Exponent. Synopsis: See Register 0x0C00.	0x204	R/W	Live	No

DPLL LOOP FILTER 1 (LF1) COEFFICIENTS—REGISTER 0x0C0C TO REGISTER 0x0C17

Table 37. DPLL Loop Filter 1 (LF1) Coefficient Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0C0C	[7:0]	Alpha 1 Significand[7:0]		Alpha 1 Significand. Synopsis: The DPLL loop filter, LF1, requires four coefficients, C_LF1_x, where x = 0 to 3. Each coefficient makes use of an integer significand (S) and an integer exponent (E) as follows: $C\_LF1_x = S \times 2^{(E-16)}$	0x169	R/W	Live	No
0x0C0D	[7:0]	Alpha 1 Significand[15:8]		Continuation of the Alpha 1 significand bit field. See the Alpha 1 Significand[7:0] description.	0x160	R/W	Live	No
0x0C0E	[7:0]	Alpha 1 exponent		Alpha 1 Exponent. Synopsis: See Register 0x0C0C.	0x183	R/W	Live	No
0x0C0F	[7:0]	Beta 1 Significand[7:0]		Beta 1 Significand. Synopsis: See Register 0x0C0C.	0x205	R/W	Live	No
0x0C10	[7:0]	Beta 1 Significand[15:8]		Continuation of the Beta 1 significand bit field. See the Beta 1 Significand[7:0] description.	0x219	R/W	Live	No
0x0C11	[7:0]	Beta 1 exponent		Beta 1 Exponent. Synopsis: See Register 0x0C0C.	0x243	R/W	Live	No
0x0C12	[7:0]	Gamma 1 Significand[7:0]		Gamma Significand 1. Synopsis: See Register 0x0C0C.	0x121	R/W	Live	No
0x0C13	[7:0]	Gamma 1 Significand[15:8]		Continuation of the Gamma 1 significand bit field. See the Gamma 1 Significand[7:0] description.	0x212	R/W	Live	No
0x0C14	[7:0]	Gamma 1 exponent		Gamma 1 Exponent. Synopsis: See Register 0x0C0C.	0x206	R/W	Live	No
0x0C15	[7:0]	Delta 1 Significand[7:0]		Delta 1 Significand. Synopsis: See Register 0x0C0C.	0x77	R/W	Live	No
0x0C16	[7:0]	Delta 1 Significand[15:8]		Continuation of the Delta 1 significand bit field. See the Delta 1 Significand[7:0] description.	0x167	R/W	Live	No
0x0C17	[7:0]	Delta 1 exponent		Delta Exponent 1. Synopsis: See Register 0x0C0C.	0x207	R/W	Live	No

COMMON CLOCK DPLL LOCK DETECTOR PARAMETERS—REGISTER 0x0D00 TO REGISTER 0x0D05

Table 38. Common Clock DPLL Lock Detector Parameter Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0D00	[7:0]	CCDPLL Lock Detector Threshold[7:0]		Common Clock DPLL Phase Lock Detector Threshold Level. Synopsis: The digital phase detector delivers time error samples (ε) to the phase lock detector, where ε is the difference in time between the rising edge of the reference and feedback inputs to the PFD of the CCDPLL. The phase lock detector compares the magnitude of each time sample (|ε|) to a user defined time threshold (t_{THRESH}). The comparison triggers a fill or drain event. Fill events (|ε| ≤ t_{THRESH}) steer the phase lock detector toward lock status. Drain events (|ε| > t_{THRESH}) steer the phase lock detector toward unlock status. This 16-bit unsigned value, Phase Lock Detector Threshold, in units of picoseconds (default = 0), constitutes a time threshold, t_{THRESH} (seconds). Phase Lock Detector Threshold (rounded to the nearest integer) relates to t_{THRESH} as follows: *Phase Lock Detector Threshold* = $t_{THRESH} \times 10^{12}$ For example, for a desired value of $t_{THRESH} = 10^{-9}$ sec (1 ns), then Phase Lock Detector Threshold = 1000 (0x 00 03E8). Phase Lock Detector Threshold > 0 enables the fill and drain featured lock detector. Otherwise, the basic, nonparametric lock detector associated with the auxiliary DPLL is in effect.	0x00	R/W	Core clock	No
0x0D01	[7:0]	CCDPLL Lock Detector Threshold[15:8]		Continuation of the CCDPLL Lock Detector Threshold bit field. See the CCDPLL Lock Detector Threshold[7:0] description.	0x00	R/W	Core clock	No
0x0D02	[7:0]	CCDPLL lock detector fill value		Common Clock DPLL Phase Lock Detector Fill Value. This 8-bit unsigned value, Phase Lock Detector Fill Value (default = 1), constitutes the size associated with a fill event for the CCDPLL phase lock detector. Phase Lock Detector Fill Value is meaningless unless Register 0x0D01 to Register 0x0D00, Bits[15:0] > 0.	0x01	R/W	Core clock	No
0x0D03	[7:0]	CCDPLL lock detector drain value		Common Clock DPLL Phase Lock Detector Drain Value. This 8-bit unsigned value, Phase Lock Detector Drain Value (default = 1), constitutes the size associated with a drain event for the CCDPLL phase lock detector. Phase Lock Detector Drain Value is meaningless unless Register 0x0D01 to Register 0x0D00, Bits[15:0] > 0.	0x01	R/W	Core clock	No
0x0D04	[7:0]	CCDPLL Lock Detector Delay[7:0]		Common Clock DPLL Phase Lock Detector Delay. This 16-bit unsigned value, Phase Lock Detector Delay, with units of milliseconds (default = 0), constitutes a time delay, t_{DLY} (seconds). The delay is how long the CCDPLL waits before indicating a locked status when the lock detector transitions from unlocked to locked. The delay mitigates spurious lock and unlock chatter by allowing the lock detector more time to settle after it transitions to a locked condition. Phase Lock Detector Delay (rounded to the nearest integer) relates to t_{DLY} as follows: *Phase Lock Detector Delay* = 1000 × t_{DLY} For example, given t_{DLY} = 0.0177 sec, then Phase Lock Detector Delay = 18 (0x 0012). Phase Lock Detector Delay = 0 bypasses the delay mechanism. Phase Lock Detector Delay is meaningless unless Register 0x0D01 to Register 0x0D00, Bits[15:0] > 0.	0x00	R/W	Core clock	No
0x0D05	[7:0]	CCDPLL Lock Detector Delay[15:8]		Continuation of the CCDPLL Lock Detector Delay bit field. See the CCDPLL Lock Detector Delay[7:0] description.	0x00	R/W	Core clock	No

COMMON CLOCK DPLL/SYNCHRONIZER SOURCE 0 (CCR0)—REGISTER 0x0D10 TO REGISTER 0x0D1D

Table 39. Common Clock DPLL/Synchronizer Source 0 (CCR0)—Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0D10	7	CCDPLL CCR0 enable		Common Clock DPLL Primary Reference Enable. By default, the CCDPLL uses Register 0x0284, Bits[4:0] (the source bit field for the auxiliary DPLL) to select a time stamp source. However, changing the default value of Register 0x0D10, Bit 7; Register 0x0D10, Bits[4:0]; Register 0x0D20, Bit 7; or Register 0x0D20, Bits[4:0] causes the CCDPLL to use the time stamp source defined by Register 0x0D10, Bits[4:0] for the primary common clock reference (CCR0) and Register 0x0D20, Bits[4:0] for the secondary common clock reference (CCR1).	0	R/W	Core clock	No
			0	Disabled.				
			1	Enabled.				
	[6:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:0]	CCDPLL CCR0 time stamp source		Common Clock DPLL Primary Time Stamp Source. This 5-bit unsigned value (default = 31) selects the primary time stamp source to the CCDPLL.	0x31	R/W	Core clock	No
			0	REFA.				
			1	REFAA.				
			2	REFB.				
			3	REFBB.				
			6	Auxiliary REF0.				
			7	Auxiliary REF1.				
			11	Auxiliary REF2.				
			12	Auxiliary REF3.				
			31	None (default).				
0x0D11	7	CCS primary time stamp source tagging		Common Clock Synchronizer Primary Time Stamp Source Tagging. This bit controls whether the CCS uses normal or tagged time stamps from its time stamp source when the primary source (CCR0) to the CCDPLL is in effect.	0	R/W	Core clock	No
			0	Normal.				
			1	Tagged.				
	[6:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:0]	CCS Time Stamp Source Sync 0		Common Clock Synchronizer Synchronization Source 0. This 5-bit unsigned value (default = 0) selects the synchronization time stamp source to the CCS (in conjunction with the primary reference (CCR0) to the CCDPLL).	0x00	R/W	Core clock	No
			0	REFA (default).				
			1	REFAA.				
			2	REFB.				
			3	REFBB.				
			6	Auxiliary REF0.				
			7	Auxiliary REF1.				
			11	Auxiliary REF2.				
			12	Auxiliary REF3.				
			30	Immediate synchronization via local time scale.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0D12	[7:0]	CCDPLL CCR0 Numerator[7:0]		Common Clock DPLL Primary Reference Numerator. This 32-bit unsigned value, NUM0 (default = 0), constitutes the numerator of a fraction, with the fraction denoting the period of the primary frequency source of the CCDPLL. For example, given a 38.88 MHz frequency source, the period expressed as a fraction is 1/38,880,000. Thus, the numerator is NUM0 = 1 (0x 0000 0001).	0x01	R/W	Core clock	No
0x0D13	[7:0]	CCDPLL CCR0 Numerator[15:8]		Continuation of the CCDPLL CCR0 numerator bit field. See the CCDPLL CCR0 Numerator[7:0] description.	0x00	R/W	Core clock	No
0x0D14	[7:0]	CCDPLL CCR0 Numerator[23:16]		Continuation of the CCDPLL CCR0 numerator bit field. See the CCDPLL CCR0 Numerator[7:0] description.	0x00	R/W	Core clock	No
0x0D15	[7:0]	CCDPLL CCR0 Numerator[31:24]		Continuation of the CCDPLL CCR0 numerator bit field. See the CCDPLL CCR0 Numerator[7:0] description.	0x00	R/W	Core clock	No
0x0D16	[7:0]	CCDPLL CCR0 Denominator[7:0]		Common Clock DPLL Primary Reference Denominator. This 40-bit unsigned value, DEN0 (default = 0), constitutes the denominator of a fraction, with the fraction denoting the period of the primary frequency source of the CCDPLL. For example, given a 38.88 MHz frequency source, the period expressed as a fraction is 1/38,880,000. Thus, the denominator is DEN0 = 38,880,000 (0x 00 0251 4300).	0x00	R/W	Core clock	No
0x0D17	[7:0]	CCDPLL CCR0 Denominator[15:8]		Continuation of the CCDPLL CCR0 denominator bit field. See the CCDPLL CCR0 Denominator[7:0] description.	0x00	R/W	Core clock	No
0x0D18	[7:0]	CCDPLL CCR0 Denominator[23:16]		Continuation of the CCDPLL CCR0 denominator bit field. See the CCDPLL CCR0 Denominator[7:0] description.	0x00	R/W	Core clock	No
0x0D19	[7:0]	CCDPLL CCR0 Denominator[31:24]		Continuation of the CCDPLL CCR0 denominator bit field. See the CCDPLL CCR0 Denominator[7:0] description.	0x00	R/W	Core clock	No
0x0D1A	[7:0]	CCDPLL CCR0 Denominator[39:32]		Continuation of the CCDPLL CCR0 denominator bit field. See the CCDPLL CCR0 Denominator[7:0] description.	0x00	R/W	Core clock	No
0x0D1B	[7:0]	CCDPLL CCR0 Skew[7:0]		Common Clock DPLL Primary Reference Skew. This 24-bit signed value, Skew in units of 2^{-48} sec (default = 0), defines a time offset, t_{SKEW} (seconds), specific to the primary reference of the CCS. Skew (rounded to the nearest integer) relates to t_{SKEW} as follows: $Skew = t_{SKEW} \times 2^{48}$ For example, given $t_{SKEW} = -5 \times 10^{-9}$ sec (−5 ns), then Skew = −1,407,375 (0x EA 8671). Skew is an adjustment to the synchronization time value the user provides to the CCS via Register 0x0F15 to Register 0x0F0A, Bits[95:0].	0x00	R/W	Core clock	No
0x0D1C	[7:0]	CCDPLL CCR0 Skew[15:8]		Continuation of the CCDPLL CCR0 skew bit field. See the CCDPLL CCR0 Skew[7:0] description.	0x00	R/W	Core clock	No
0x0D1D	[7:0]	CCDPLL CCR0 Skew[23:16]		Continuation of the CCDPLL CCR0 skew bit field. See the CCDPLL CCR0 Skew[7:0] description.	0x00	R/W	Core clock	No

COMMON CLOCK DPLL/SYNCHRONIZER SOURCE 1 (CCR1)—REGISTER 0x0D20 TO REGISTER 0x0D2D

Table 40. Common Clock DPLL/Synchronizer Source 1 (CCR1)—Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0D20	7	CCDPLL CCR1 Enable		Common Clock DPLL Secondary Reference Enable. By default, the CCDPLL uses Register 0x0284, Bits[4:0] (the source bit field for the auxiliary DPLL) to select a time stamp source. However, changing the default value of Register 0x0D10, Bit 7; Register 0x0D10, Bits[4:0]; Register 0x0D20, Bit 7; or Register 0x0D20, Bits[4:0] causes the CCDPLL to use the time stamp source defined by Register 0x0D10, Bits[4:0] for the primary common clock reference (CCR0) and Register 0x0D20, Bits[4:0] for the secondary common clock reference (CCR1).	0	R/W	Core clock	No
			0	Disabled.				
			1	Enabled.				
	[6:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:0]	CCDPLL CCR1 time stamp source		Common Clock DPLL Secondary Time Stamp Source. This 5-bit unsigned value (default = 31) selects the secondary time stamp source to the Common Clock DPLL.	0x31	R/W	Core clock	No
			0	REFA.				
			1	REFAA.				
			2	REFB.				
			3	REFBB.				
			6	Auxiliary REF0.				
			7	Auxiliary REF1.				
			11	Auxiliary REF2.				
			12	Auxiliary REF3.				
			31	None (default).				
0x0D21	7	CCS secondary time stamp source tagging		Common Clock Synchronizer Secondary Time Stamp Source Tagging. This bit controls whether the CCS uses normal or tagged time stamps from its time stamp source when the secondary source (CCR1) to the CCDPLL is in effect.	0	R/W	Core clock	No
			0	Normal.				
			1	Tagged.				
	[6:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:0]	CCS Time Stamp Source Sync 1		Common Clock Synchronizer Synchronization Source 1. This 5-bit unsigned value (default = 0) selects the synchronization time stamp source to the CCS (in conjunction with the secondary reference (CCR1) to the CCDPLL).	0x00	R/W	Core clock	No
			0	REFA (default).				
			1	REFAA.				
			2	REFB.				
			3	REFBB.				
			6	Auxiliary REF0.				
			7	Auxiliary REF1.				
			11	Auxiliary REF2.				
			12	Auxiliary REF3.				
			31	Immediate synchronization via local time scale.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0D22	[7:0]	CCDPLL CCR1 Numerator[7:0]		Common Clock DPLL Secondary Reference Numerator. This 32-bit unsigned value, NUM1 (default = 0), constitutes the numerator of a fraction, with the fraction denoting the period of the secondary frequency source of the CCDPLL. For example, given a 38.88 MHz frequency source, the period expressed as a fraction is 1/38,880,000. Thus, the numerator is NUM1 = 1 (0x 0000 0001).	0x01	R/W	Core clock	No
0x0D23	[7:0]	CCDPLL CCR1 Numerator[15:8]		Continuation of the CCDPLL CCR1 numerator bit field. See the CCDPLL CCR1 Numerator[7:0] description.	0x00	R/W	Core clock	No
0x0D24	[7:0]	CCDPLL CCR1 Numerator[23:16]		Continuation of the CCDPLL CCR1 numerator bit field. See the CCDPLL CCR1 Numerator[7:0] description.	0x00	R/W	Core clock	No
0x0D25	[7:0]	CCDPLL CCR1 Numerator[31:24]		Continuation of the CCDPLL CCR1 numerator bit field. See the CCDPLL CCR1 Numerator[7:0] description.	0x00	R/W	Core clock	No
0x0D26	[7:0]	CCDPLL CCR1 Denominator[7:0]		Common Clock DPLL Secondary Reference Denominator. This 40-bit unsigned value, DEN1 (default = 0), constitutes the denominator of a fraction, with the fraction denoting the period of the secondary frequency source of the CCDPLL. For example, given a 38.88 MHz frequency source, the period expressed as a fraction is 1/38,880,000. Thus, the denominator is DEN1 = 38,880,000 (0x 00 0251 4300).	0x00	R/W	Core clock	No
0x0D27	[7:0]	CCDPLL CCR1 Denominator[15:8]		Continuation of the CCDPLL CCR1 denominator bit field. See the CCDPLL CCR1 Denominator[7:0] description.	0x00	R/W	Core clock	No
0x0D28	[7:0]	CCDPLL CCR1 Denominator[23:16]		Continuation of the CCDPLL CCR1 denominator bit field. See the CCDPLL CCR1 Denominator[7:0] description.	0x00	R/W	Core clock	No
0x0D29	[7:0]	CCDPLL CCR1 Denominator[31:24]		Continuation of the CCDPLL CCR1 denominator bit field. See the CCDPLL CCR1 Denominator[7:0] description.	0x00	R/W	Core clock	No
0x0D2A	[7:0]	CCDPLL CCR1 Denominator[39:32]		Continuation of the CCDPLL CCR1 denominator bit field. See the CCDPLL CCR1 Denominator[7:0] description.	0x00	R/W	Core clock	No
0x0D2B	[7:0]	CCDPLL CCR1 Skew[7:0]		Common Clock DPLL Secondary Reference Skew. This 24-bit signed value, skew in units of 2^{-48} sec (default = 0), defines a time offset, t_{SKEW} (seconds), specific to the secondary reference of the CCS. Skew (rounded to the nearest integer) relates to t_{SKEW} as follows: $Skew = t_{SKEW} \times 2^{48}$ For example, given $t_{SKEW} = -5 \times 10^{-9}$ sec (−5 ns), then Skew = −1,407,375 (0x EA 8671). Skew is an adjustment to the synchronization time value the user provides to the CCS via Register 0x0F15 to Register 0x0F0A, Bits[95:0].	0x00	R/W	Core clock	No
0x0D2C	[7:0]	CCDPLL CCR1 Skew[15:8]		Continuation of the CCDPLL CCR1 skew bit field. See the CCDPLL CCR1 Skew[7:0] description.	0x00	R/W	Core clock	No
0x0D2D	[7:0]	CCDPLL CCR1 Skew[23:16]		Continuation of the CCDPLL CCR1 skew bit field. See the CCDPLL CCR1 Skew[7:0] description.	0x00	R/W	Core clock	No

COMMON CLOCK SYNCHRONIZER PARAMETERS—REGISTER 0x0D30 TO REGISTER 0x0D3C

Table 41. Common Clock Synchronizer Parameters Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0D30	[7:0]	CCS Offset Time[7:0]		Common Clock Synchronizer Offset Time. This 32-bit signed value, CCS Offset Time in units of 2^{-48} sec (default = 0), applies a time offset, t_{CCS_OFFSET} (seconds), to the common time scale generated by the CCS. CCS Offset Time (rounded to the nearest integer) relates to t_{CCS_OFFSET} as follows: *CCS Offset Time* = $t_{CCS\_OFFSET} \times 2^{48}$ For example, given $t_{CCS\_OFFSET} = 50 \times 10^{-9}$ sec (50 ns), then CCS Offset Time = 14,073,749 (0x 00D6 BF95).	0x00	R/W	Core clock	No
0x0D31	[7:0]	CCS Offset Time[15:8]		Continuation of the CCS offset time bit field. See the CCS Offset Time[7:0] description.	0x00	R/W	Core clock	No
0x0D32	[7:0]	CCS Offset Time[23:16]		Continuation of the CCS offset time bit field. See the CCS Offset Time[7:0] description.	0x00	R/W	Core clock	No
0x0D33	[7:0]	CCS Offset Time[31:24]		Continuation of the CCS offset time bit field. See the CCS Offset Time[7:0] description.	0x00	R/W	Core clock	No
0x0D34	[7:0]	CCS Slew Limit[7:0]		Common Clock Synchronizer Slew Limit. This 24-bit unsigned value, Slew Limit with units of 2^{-36} (default = 0), establishes an upper limit to the rate of change time, Δt/t (unitless), that the CCS applies to the common clock time scale upon detection of a phase jump. Δt/t equates to a constant fractional frequency offset. Slew Limit (rounded to the nearest integer) relates to Δt/t as follows: *Slew Limit* = $\Delta t/t \times 2^{36}$ For example, given Δt/t = 0.15 ppm (0.15×10^{-6}), then Slew Limit = 10,308 (0x 00 2844). Slew Limit = 0 disables slew rate limiting.	0x00	R/W	Core clock	No
0x0D35	[7:0]	CCS Slew Limit[15:8]		Continuation of the CCS slew limit bit field. See the CCS Slew Limit[7:0] description.	0x00	R/W	Core clock	No
0x0D36	[7:0]	CCS Slew Limit[23:16]		Continuation of the CCS slew limit bit field. See the CCS Slew Limit[7:0] description.	0x00	R/W	Core clock	No
0x0D37	[7:0]	CCS Guard Latency[7:0]		Common Clock Synchronizer Guard Latency. This 16-bit unsigned value, Guard Latency in units of 2^{-16} sec (default = 0), establishes the maximum time, t_G (seconds), the CCS waits for a synchronization event after receiving a synchronization time value from the user. Guard Latency (rounded to the nearest integer) relates to t_G as follows: *Guard Latency* = $t_G \times 2^{16}$ For example, given $t_G = 10^{-3}$ sec (1 ms), then Guard Latency = 66 (0x 0042). Failure of a synchronization event to occur before t_G causes the latency guard to activate. Guard Latency = 0 disables the latency guard.	0x00	R/W	Core clock	No
0x0D38	[7:0]	CCS Guard Latency[15:8]		Continuation of the CCS guard latency bit field. See the CCS Guard Latency[7:0] description.	0x00	R/W	Core clock	No
0x0D39	[7:0]	CCS Guard Adjustment[7:0]		Common Clock Synchronizer Guard Adjustment. This 20-bit unsigned value, Guard Adjustment in units of picoseconds (default = 0), establishes the smallest synchronization offset refinement value, $t_{MINOFST}$ (seconds), that causes the offset refinement guard of the CCS to activate. Guard Adjustment (rounded to the nearest integer) relates to $t_{MINOFST}$ as follows: *Guard Adjustment* = $t_{MINOFST} \times 10^{12}$ Guard Adjustment = 0 disables the offset refinement guard.	0x00	R/W	Core clock	No
0x0D3A	[7:0]	CCS Guard Adjustment[15:8]		Continuation of the CCS guard adjustment bit field. See the CCS Guard Adjustment[7:0] description.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0D3B	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	[3:0]	CCS Guard Adjustment[19:16]		Continuation of the CCS guard adjustment bit field. See the CCS Guard Adjustment[7:0] description.	0x0	R/W	Core clock	No
0x0D3C	[7:1]	Reserved		Reserved.	0x00	R	Live	No
	0	CCS guard bypass lock		Common Clock Synchronizer Guard Bypass Lock. By default, the CCS synchronization guard triggers when the CCDPLL unlocks. This bit allows the user to prevent an unlock condition from triggering the synchronization guard.	0	R/W	Core clock	No
			0	Unlock triggers the synchronization guard.				
			1	Unlock condition does not trigger the synchronization guard.				

DIGITIZED CLOCKING STATUS—REGISTER 0x0D40

Table 42. Digitized Clocking Status Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0D40	7	CCS guard status		Common Clock Synchronizer Guard Status.	0	R	Live	No
			0	The synchronization guard of the CCS has not been triggered (normal operation).				
			1	The synchronization guard of the CCS was triggered by a guard event (excessive offset refinement step, latency fault, or CCDPLL unlock).				
	6	CCS slew limiter status		Common Clock Synchronizer Slew Limiter Status.	0	R	Live	No
			0	The phase slew rate limiter of the CCS is not actively limiting slew rate.				
			1	The phase slew rate limiter of the CCS is actively limiting slew rate.				
	5	CCDPLL CCR1 status		Common Clock DPLL Secondary Frequency Source Status.	0	R	Live	No
			0	The secondary frequency source to the CCDPLL is not valid.				
			1	The secondary frequency source to the CCDPLL is valid ($\Delta f < 3.125\%$).				
	4	CCDPLL CCR0 status		Common Clock DPLL Primary Frequency Source Status.	0	R	Live	No
			0	The primary frequency source to the CCDPLL is not valid.				
			1	The primary frequency source to the CCDPLL is valid ($\Delta f < 3.125\%$).				
	3	CCDPLL active source		Common Clock DPLL Active Source ID.	0	R	Live	No
			0	The CCDPLL is using the primary reference source (CCR0).				
			1	The CCDPLL is using the secondary reference source (CCR1).				
	2	CCS ready status		Common Clock Synchronizer Ready. Status of the CCS as it relates to digitized clocking resources like the UTS and IUTS.	0	R	Live	No
			0	The CCS is not ready for use.				
			1	The CCS is ready for use.				
	1	CCDPLL phase locked status		Common Clock DPLL Phase-Locked. This bit is a duplicate of Register 0x3002, Bit 1.	0	R	Live	No
			0	The CCDPLL is not phase locked.				
			1	The CCDPLL is phase locked.				
	0	CCDPLL active status		Common Clock DPLL Active Status.	0	R	Live	No
			0	The CCDPLL is not tracking a reference source.				
			1	The CCDPLL is actively tracking a reference source.				

USER TIME STAMPER CONTROL: UTS 0—REGISTER 0x0E00 TO REGISTER 0x0E04

Table 43. User Time Stamper Control: UTS 0 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0E00	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:2]	UTS 0 flags		User Timer Stamper 0 Flags. This 3-bit flag code (default = 0) defines a three-element group of status conditions that UTS 0 attaches to a converted time code. There are eight combinations with each combination comprising three status conditions. For example, the three-element group, (tag, invalid, unlocked), is one such combination, where each element constitutes one of the following five status conditions: Invalid: the reference to the CCDPLL is invalid. Fault: the reference to the CCDPLL is faulted. Unlocked: the CCDPLL is unlocked. Tag: the state of the tag bit associated with the time stamp processed by UTS 0. Format: the state of the format bit associated with UTS 0.	0x0	R/W	Core clock	No
			0	Tag, invalid, unlocked (default).				
			1	Tag, fault, unlocked.				
			2	Format, invalid, unlocked.				
			3	Format, fault, unlocked.				
			4	Fault, invalid, unlocked.				
			5	Format, tag, unlocked or invalid.				
			6	Format, tag, unlocked or fault.				
			7	Unused.				
	1	UTS 0 format		User Timer Stamper 0 Format. This bit controls the format conversion UTS 0 applies to the time stamp it receives from its assigned time stamp source prior to storing the formatted time stamp in the UTS readback FIFO.	0	R/W	Core clock	No
			0	UTS 0 Fractional Seconds Format (default). Converts time stamps to a 96-bit word with the 48 MSBs constituting seconds and the 48 LSBs constituting a fraction of a second in units of 2^{-48} sec.				
			1	UTS 0 Precision Time Protocol (PTP) Format. Converts time stamps to a 96-bit word with the 48 MSBs constituting seconds. The 48 LSBs constitute a fraction of a second in units of 2^{-16} ns with the two uppermost LSBs unused.				
	0	UTS 0 enable		User Timer Stamper 0 Enable.	0	R/W	Core clock	No
			0	Disabled (default).				
			1	Enabled.				
0x0E01	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	UTS 0 tag		UTS 0 Time Stamp Source Tagging. This bit controls whether UTS 0 uses normal or tagged time stamps from its time stamp source.	0	R/W	Core clock	No
			0	Normal (default).				
			1	Tagged.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[4:0]	UTS 0 time stamp source		User Timer Stamper 0 Time Stamp Source. This 5-bit unsigned value (default = 0) is an index number for selecting the time stamp source to UTS 0.	0x00	R/W	Core clock	No
			0	REFA (default).				
			1	REFAA.				
			2	REFB.				
			3	REFBB.				
			4	DPLL0 feedback.				
			5	DPLL1 feedback.				
			6	Auxiliary REF0.				
			7	Auxiliary REF1.				
			8	Auxiliary NCO 0.				
			9	Auxiliary NCO 1.				
			11	Auxiliary REF2.				
			12	Auxiliary REF3.				
			13	IUTS 0.				
			14	IUTS 1.				
0x0E02	[7:0]	UTS 0 Offset Time[7:0]		User Time Stamper 0 Offset Time. This 24-bit signed value, UTS 0 Offset Time in units of 2^{-48} sec (default = 0), constitutes a time offset, t_{OFST} (seconds), to the time stamps received by UTS 0. UTS 0 Offset Time (rounded to the nearest integer) relates to t_{OFST} as follows: *UTS 0 Offset Time* = $t_{OFST} \times 2^{48}$ For example, given $t_{OFST} = -25 \times 10^{-9}$ sec (−25 ns), then UTS 0 Offset Time = −7,036,874 (0x 94 A036).	0x00	R/W	Core clock	No
0x0E03	[7:0]	UTS 0 Offset Time[15:8]		Continuation of the UTS 0 offset time bit field. See the UTS 0 Offset Time[7:0] description.	0x00	R/W	Core clock	No
0x0E04	[7:0]	UTS 0 Offset Time[23:16]		Continuation of the UTS 0 offset time bit field. See the UTS 0 Offset Time[7:0] description.	0x00	R/W	Core clock	No

USER TIME STAMPER CONTROL: UTS 1—REGISTER 0x0E05 TO REGISTER 0x0E09

Table 44. User Time Stamper Control: UTS 1 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0E05	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:2]	UTS 1 flags		User Timer Stamper 1 Flags. This 3-bit flag code (default = 0) defines a three-element group of status conditions that UTS 1 attaches to a converted time code. There are eight combinations with each combination comprising three status conditions. For example, the three-element group, (tag, invalid, unlocked), is one such combination, where each element constitutes one of the following five status conditions: Invalid: the reference to the CCDPLL is invalid. Fault: the reference to the CCDPLL is faulted. Unlocked: the CCDPLL is unlocked. Tag: the state of the tag bit associated with the time stamp processed by UTS 1. Format: the state of the format bit associated with UTS 1.	0x0	R/W	Core clock	No
			0	Tag, invalid, unlocked (default).				
			1	Tag, fault, unlocked.				
			2	Format, invalid, unlocked.				
			3	Format, fault, unlocked.				
			4	Fault, invalid, unlocked.				
			5	Format, tag, unlocked or invalid.				
			6	Format, tag, unlocked or fault.				
			7	Unused.				
	1	UTS 1 format		User Timer Stamper 1 Format. This bit controls the format conversion UTS 1 applies to the time stamp it receives from its assigned time stamp source prior to storing the formatted time stamp in the UTS readback FIFO.	0	R/W	Core clock	No
			0	UTS 1 Fractional Seconds Format (default). Converts time stamps to a 96-bit word with the 48 MSBs constituting seconds and the 48 LSBs constituting a fraction of a second in units of 2^{-48} sec.				
			1	UTS 1 PTP Format. Converts time stamps to a 96-bit word with the 48 MSBs constituting seconds. The 48 LSBs constitute a fraction of a second in units of 2^{-16} ns with the two uppermost LSBs unused.				
	0	UTS 1 enable		User Timer Stamper 1 Enable.	0	R/W	Core clock	No
			0	Disabled (default).				
			1	Enabled.				
0x0E06	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	UTS 1 tag		UTS 1 Time Stamp Source Tagging. This bit controls whether UTS 1 uses normal or tagged time stamps from its time stamp source.	0	R/W	Core clock	No
			0	Normal (default).				
			1	Tagged.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[4:0]	UTS 1 time stamp source		User Timer Stamper 1 Time Stamp Source. This 5-bit unsigned value (default = 0) is an index number for selecting the time stamp source to UTS 1.	0x00	R/W	Core clock	No
			0	REFA (default).				
			1	REFAA.				
			2	REFB.				
			3	REFBB.				
			4	DPLL0 feedback.				
			5	DPLL1 feedback.				
			6	Auxiliary REF0.				
			7	Auxiliary REF1.				
			8	Auxiliary NCO 0.				
			9	Auxiliary NCO 1.				
			11	Auxiliary REF2.				
			12	Auxiliary REF3.				
			13	IUTS 0.				
			14	IUTS 1.				
0x0E07	[7:0]	UTS 1 Offset Time[7:0]		User Time Stamper 1 Offset Time. This 24-bit signed value, UTS 1 Offset Time in units of 2^{-48} sec (default = 0), constitutes a time offset, t_{OFST} (seconds), to the time stamps received by UTS 1. UTS 1 Offset Time (rounded to the nearest integer) relates to t_{OFST} as follows: *UTS 1 Offset Time* = $t_{OFST} \times 2^{48}$ For example, given $t_{OFST} = -25 \times 10^{-9}$ sec (−25 ns), then UTS 1 Offset Time = −7,036,874 (0x 94 A036).	0x00	R/W	Core clock	No
0x0E08	[7:0]	UTS 1 Offset Time[15:8]		Continuation of the UTS 1 offset time bit field. See the UTS 1 Offset Time[7:0] description.	0x00	R/W	Core clock	No
0x0E09	[7:0]	UTS 1 Offset Time[23:16]		Continuation of the UTS 0 offset time bit field. See the UTS 1 Offset Time[7:0] description.	0x00	R/W	Core clock	No

USER TIME STAMPER CONTROL: UTS 2—REGISTER 0x0E0A TO REGISTER 0x0E0E

Table 45. User Time Stamper Control: UTS 2 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0E0A	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:2]	UTS 2 flags		User Timer Stamper 2 Flags. This 3-bit flag code (default = 0) defines a three-element group of status conditions that UTS 2 attaches to a converted time code. There are eight combinations with each combination comprising three status conditions. For example, the three-element group, (tag, invalid, unlocked), is one such combination, where each element constitutes one of the following five status conditions: Invalid: the reference to the CCDPLL is invalid. Fault: the reference to the CCDPLL is faulted. Unlocked: the CCDPLL is unlocked. Tag: the state of the tag bit associated with the time stamp processed by UTS 2. Format: the state of the format bit associated with UTS 2.	0x0	R/W	Core clock	No
			0	Tag, invalid, unlocked (default).				
			1	Tag, fault, unlocked.				
			2	Format, invalid, unlocked.				
			3	Format, fault, unlocked.				
			4	Fault, invalid, unlocked.				
			5	Format, tag, unlocked or invalid.				
			6	Format, tag, unlocked or fault.				
			7	Unused.				
	1	UTS 2 format		User Timer Stamper 2 Format. This bit controls the format conversion UTS 2 applies to the time stamp it receives from its assigned time stamp source prior to storing the formatted time stamp in the UTS readback FIFO.	0	R/W	Core clock	No
			0	UTS 2 Fractional Seconds Format (default). Converts time stamps to a 96-bit word with the 48 MSBs constituting seconds and the 48 LSBs constituting a fraction of a second in units of 2^{-48} sec.				
			1	UTS 2 PTP Format. Converts time stamps to a 96-bit word with the 48 MSBs constituting seconds. The 48 LSBs constitute a fraction of a second in units of 2^{-16} ns with the two uppermost LSBs unused.				
	0	UTS 2 enable		User Timer Stamper 2 Enable.	0	R/W	Core clock	No
			0	Disabled (default).				
			1	Enabled.				
0x0E0B	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	UTS 2 tag		UTS 2 Time Stamp Source Tagging. This bit controls whether UTS 2 uses normal or tagged time stamps from its time stamp source.	0	R/W	Core clock	No
			0	Normal (default).				
			1	Tagged.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[4:0]	UTS 2 time stamp source		User Timer Stamper 2 Time Stamp Source. This 5-bit unsigned value (default = 0) is an index number for selecting the time stamp source to UTS 2.	0x00	R/W	Core clock	No
			0	REFA (default).				
			1	REFAA.				
			2	REFB.				
			3	REFBB.				
			4	DPLL0 feedback.				
			5	DPLL1 feedback.				
			6	Auxiliary REF0.				
			7	Auxiliary REF1.				
			8	Auxiliary NCO 0.				
			9	Auxiliary NCO 1.				
			11	Auxiliary REF2.				
			12	Auxiliary REF3.				
			13	IUTS 0.				
			14	IUTS 1.				
0x0E0C	[7:0]	UTS 2 Offset Time[7:0]		User Time Stamper 2 Offset Time. This 24-bit signed value, UTS 2 Offset Time in units of 2^{-48} sec (default = 0), constitutes a time offset, t_{OFST} (seconds), to the time stamps received by UTS 2. UTS 2 Offset Time (rounded to the nearest integer) relates to t_{OFST} as follows: $UTS\ 2\ Offset\ Time = t_{OFST} \times 2^{48}$ For example, given $t_{OFST} = -25 \times 10^{-9}$ sec (−25 ns), then UTS 2 Offset Time = −7,036,874 (0x 94 A036).	0x00	R/W	Core clock	No
0x0E0D	[7:0]	UTS 2 Offset Time[15:8]		Continuation of the UTS 2 offset time bit field. See the UTS 2 Offset Time[7:0] description.	0x00	R/W	Core clock	No
0x0E0E	[7:0]	UTS 2 Offset Time[23:16]		Continuation of the UTS 2 offset time bit field. See the UTS 2 Offset Time[7:0] description.	0x00	R/W	Core clock	No

USER TIME STAMPER CONTROL: UTS 3—REGISTER 0x0E0F TO REGISTER 0x0E13

Table 46. User Time Stamper Control: UTS 3 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0E0F	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:2]	UTS 3 flags		User Timer Stamper 3 Flags. This 3-bit flag code (default = 0) defines a three-element group of status conditions that UTS 3 attaches to a converted time code. There are eight combinations with each combination comprising three status conditions. For example, the three-element group, (tag, invalid, unlocked), is one such combination, where each element constitutes one of the following five status conditions: Invalid: the reference to the CCDPLL is invalid. Fault: the reference to the CCDPLL is faulted. Unlocked: the CCDPLL is unlocked. Tag: the state of the tag bit associated with the time stamp processed by UTS 3. Format: the state of the format bit associated with UTS 3.	0x0	R/W	Core clock	No
			0	Tag, invalid, unlocked (default).				
			1	Tag, fault, unlocked.				
			2	Format, invalid, unlocked.				
			3	Format, fault, unlocked.				
			4	Fault, invalid, unlocked.				
			5	Format, tag, unlocked or invalid.				
			6	Format, tag, unlocked or fault.				
			7	Unused.				
	1	UTS 3 format		User Timer Stamper 3 Format. This bit controls the format conversion UTS 3 applies to the time stamp it receives from its assigned time stamp source prior to storing the formatted time stamp in the UTS readback FIFO.	0	R/W	Core clock	No
			0	UTS 3 Fractional Seconds Format (default). Converts time stamps to a 96-bit word with the 48 MSBs constituting seconds and the 48 LSBs constituting a fraction of a second in units of 2^{-48} sec.				
			1	UTS 3 PTP Format. Converts time stamps to a 96-bit word with the 48 MSBs constituting seconds. The 48 LSBs constitute a fraction of a second in units of 2^{-16} ns with the two uppermost LSBs unused.				
	0	UTS 3 enable		User Timer Stamper 3 Enable.	0	R/W	Core clock	No
			0	Disabled (default).				
			1	Enabled.				
0x0E10	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	UTS 3 tag		UTS 3 Time Stamp Source Tagging. This bit controls whether UTS 3 uses normal or tagged time stamps from its time stamp source.	0	R/W	Core clock	No
			0	Normal (default).				
			1	Tagged.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[4:0]	UTS 3 time stamp source		User Timer Stamper 3 Time Stamp Source. This 5-bit unsigned value (default = 0) is an index number for selecting the time stamp source to UTS 3.	0x00	R/W	Core clock	No
			0	REFA (default).				
			1	REFAA.				
			2	REFB.				
			3	REFBB.				
			4	DPLL0 feedback.				
			5	DPLL1 feedback.				
			6	Auxiliary REF0.				
			7	Auxiliary REF1.				
			8	Auxiliary NCO 0.				
			9	Auxiliary NCO 1.				
			11	Auxiliary REF2.				
			12	Auxiliary REF3.				
			13	IUTS 0.				
			14	IUTS 1.				
0x0E11	[7:0]	UTS 3 Offset Time[7:0]		User Time Stamper 3 Offset Time. This 24-bit signed value, UTS 3 Offset Time in units of 2^{-48} sec (default = 0), constitutes a time offset, t_{OFST} (seconds), to the time stamps received by UTS 3. UTS 3 Offset Time (rounded to the nearest integer) relates to t_{OFST} as follows: *UTS 3 Offset Time* = $t_{OFST} \times 2^{48}$ For example, given $t_{OFST} = -25 \times 10^{-9}$ sec (−25 ns), then UTS 3 Offset Time = −7,036,874 (0x 94 A036).	0x00	R/W	Core clock	No
0x0E12	[7:0]	UTS 3 Offset Time[15:8]		Continuation of the UTS 3 offset time bit field. See the UTS 3 Offset Time[7:0] description.	0x00	R/W	Core clock	No
0x0E13	[7:0]	UTS 3 Offset Time[23:16]		Continuation of the UTS 3 offset time bit field. See the UTS 3 Offset Time[7:0] description.	0x00	R/W	Core clock	No

USER TIME STAMPER CONTROL: UTS 4—REGISTER 0x0E14 TO REGISTER 0x0E18

Table 47. User Time Stamper Control: UTS 4 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0E14	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:2]	UTS 4 flags		User Timer Stamper 4 Flags. This 3-bit flag code (default = 0) defines a three-element group of status conditions that UTS 4 attaches to a converted time code. There are eight combinations with each combination comprising three status conditions. For example, the three-element group, (tag, invalid, unlocked), is one such combination, where each element constitutes one of the following five status conditions: Invalid: the reference to the CCDPLL is invalid. Fault: the reference to the CCDPLL is faulted. Unlocked: the CCDPLL is unlocked. Tag: the state of the tag bit associated with the time stamp processed by UTS 4. Format: the state of the format bit associated with UTS 4.	0x0	R/W	Core clock	No
			0	Tag, invalid, unlocked (default).				
			1	Tag, fault, unlocked.				
			2	Format, invalid, unlocked.				
			3	Format, fault, unlocked.				
			4	Fault, invalid, unlocked.				
			5	Format, tag, unlocked or invalid.				
			6	Format, tag, unlocked or fault.				
			7	Unused.				
	1	UTS 4 format		User Timer Stamper 4 Format. This bit controls the format conversion UTS 4 applies to the time stamp it receives from its assigned time stamp source prior to storing the formatted time stamp in the UTS readback FIFO.	0	R/W	Core clock	No
			0	UTS 4 Fractional Seconds Format (default). Converts time stamps to a 96-bit word with the 48 MSBs constituting seconds and the 48 LSBs constituting a fraction of a second in units of 2^{-48} sec.				
			1	UTS 4 PTP Format. Converts time stamps to a 96-bit word with the 48 MSBs constituting seconds. The 48 LSBs constitute a fraction of a second in units of 2^{-16} ns with the two uppermost LSBs unused.				
	0	UTS 4 enable		User Timer Stamper 4 Enable.	0	R/W	Core clock	No
			0	Disabled (default).				
			1	Enabled.				
0x0E15	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	UTS 4 tag		UTS 4 Time Stamp Source Tagging. This bit controls whether UTS 4 uses normal or tagged time stamps from its time stamp source.	0	R/W	Core clock	No
			0	Normal (default).				
			1	Tagged.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[4:0]	UTS 4 time stamp source		User Timer Stamper 4 Time Stamp Source. This 5-bit unsigned value (default = 0) is an index number for selecting the time stamp source to UTS 4.	0x00	R/W	Core clock	No
			0	REFA (default).				
			1	REFAA.				
			2	REFB.				
			3	REFBB.				
			4	DPLL0 feedback.				
			5	DPLL1 feedback.				
			6	Auxiliary REF0.				
			7	Auxiliary REF1.				
			8	Auxiliary NCO 0.				
			9	Auxiliary NCO 1.				
			11	Auxiliary REF2.				
			12	Auxiliary REF3.				
			13	IUTS 0.				
			14	IUTS 1.				
0x0E16	[7:0]	UTS 4 Offset Time[7:0]		User Time Stamper 4 Offset Time. This 24-bit signed value, UTS 4 Offset Time in units of 2^{-48} sec (default = 0), constitutes a time offset, t_{OFST} (seconds), to the time stamps received by UTS 4. UTS 4 Offset Time (rounded to the nearest integer) relates to t_{OFST} as follows: *UTS 4 Offset Time* = $t_{OFST} \times 2^{48}$ For example, given $t_{OFST} = -25 \times 10^{-9}$ sec (−25 ns), then UTS 4 Offset Time = −7,036,874 (0x 94 A036).	0x00	R/W	Core clock	No
0x0E17	[7:0]	UTS 4 Offset Time[15:8]		Continuation of the UTS 4 offset time bit field. See the UTS 4 Offset Time[7:0] description.	0x00	R/W	Core clock	No
0x0E18	[7:0]	UTS 4 Offset Time[23:16]		Continuation of the UTS 4 offset time bit field. See the UTS 4 Offset Time[7:0] description.	0x00	R/W	Core clock	No

USER TIME STAMPER CONTROL: UTS 5—REGISTER 0x0E19 TO REGISTER 0x0E1D

Table 48. User Time Stamper Control: UTS 5 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0E19	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:2]	UTS 5 flags		User Timer Stamper 5 Flags. This 3-bit flag code (default = 0) defines a three-element group of status conditions that UTS 5 attaches to a converted time code. There are eight combinations with each combination comprising three status conditions. For example, the three-element group, (tag, invalid, unlocked), is one such combination, where each element constitutes one of the following five status conditions: Invalid: the reference to the CCDPLL is invalid. Fault: the reference to the CCDPLL is faulted. Unlocked: the CCDPLL is unlocked. Tag: the state of the tag bit associated with the time stamp processed by UTS 5. Format: the state of the format bit associated with UTS 5.	0x0	R/W	Core clock	No
			0	Tag, invalid, unlocked (default).				
			1	Tag, fault, unlocked.				
			2	Format, invalid, unlocked.				
			3	Format, fault, unlocked.				
			4	Fault, invalid, unlocked.				
			5	Format, tag, unlocked or invalid.				
			6	Format, tag, unlocked or fault.				
			7	Unused.				
	1	UTS 5 format		User Timer Stamper 5 Format. This bit controls the format conversion UTS 5 applies to the time stamp it receives from its assigned time stamp source prior to storing the formatted time stamp in the UTS readback FIFO.	0	R/W	Core clock	No
			0	UTS 5 Fractional Seconds Format (default). Converts time stamps to a 96-bit word with the 48 MSBs constituting seconds and the 48 LSBs constituting a fraction of a second in units of 2^{-48} sec.				
			1	UTS 5 PTP Format. Converts time stamps to a 96-bit word with the 48 MSBs constituting seconds. The 48 LSBs constitute a fraction of a second in units of 2^{-16} ns with the two uppermost LSBs unused.				
	0	UTS 5 enable		User Timer Stamper 5 Enable	0	R/W	Core clock	No
			0	Disabled (default).				
			1	Enabled.				
0x0E1A	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	UTS 5 tag		UTS 5 Time Stamp Source Tagging. This bit controls whether UTS 5 uses normal or tagged time stamps from its time stamp source.	0	R/W	Core clock	No
			0	Normal (default).				
			1	Tagged.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[4:0]	UTS 5 time stamp source		User Timer Stamper 5 Time Stamp Source. This 5-bit unsigned value (default = 0) is an index number for selecting the time stamp source to UTS 5.	0x00	R/W	Core clock	No
			0	REFA (default).				
			1	REFAA.				
			2	REFB.				
			3	REFBB.				
			4	DPLL0 feedback.				
			5	DPLL1 feedback.				
			6	Auxiliary REF0.				
			7	Auxiliary REF1.				
			8	Auxiliary NCO 0.				
			9	Auxiliary NCO 1.				
			11	Auxiliary REF2.				
			12	Auxiliary REF3.				
			13	IUTS 0.				
			14	IUTS 1.				
0x0E1B	[7:0]	UTS 5 Offset Time[7:0]		User Time Stamper 5 Offset Time. This 24-bit signed value, UTS 5 Offset Time in units of 2^{-48} sec (default = 0), constitutes a time offset, t_{OFST} (seconds), to the time stamps received by UTS 5. UTS 5 Offset Time (rounded to the nearest integer) relates to t_{OFST} as follows: $UTS\ 5\ Offset\ Time = t_{OFST} \times 2^{48}$ For example, given $t_{OFST} = -25 \times 10^{-9}$ sec (−25 ns), then UTS 5 Offset Time = −7,036,874 (0x 94 A036).	0x00	R/W	Core clock	No
0x0E1C	[7:0]	UTS 5 Offset Time[15:8]		Continuation of the UTS 5 offset time bit field. See the UTS 5 Offset Time[7:0] description.	0x00	R/W	Core clock	No
0x0E1D	[7:0]	UTS 5 Offset Time[23:16]		Continuation of the UTS 5 offset time bit field. See the UTS 5 Offset Time[7:0] description.	0x00	R/W	Core clock	No

USER TIME STAMPER CONTROL: UTS 6—REGISTER 0x0E1E TO REGISTER 0x0E22

Table 49. User Time Stamper Control: UTS 6 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0E1E	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:2]	UTS 6 flags		User Timer Stamper 6 Flags. This 3-bit flag code (default = 0) defines a three-element group of status conditions that UTS 6 attaches to a converted time code. There are eight combinations with each combination comprising three status conditions. For example, the three-element group, (tag, invalid, unlocked), is one such combination, where each element constitutes one of the following five status conditions: Invalid: the reference to the CCDPLL is invalid. Fault: the reference to the CCDPLL is faulted. Unlocked: the CCDPLL is unlocked. Tag: the state of the tag bit associated with the time stamp processed by UTS 6. Format: the state of the format bit associated with UTS 6.	0x0	R/W	Core clock	No
			0	Tag, invalid, unlocked (default).				
			1	Tag, fault, unlocked.				
			2	Format, invalid, unlocked.				
			3	Format, fault, unlocked.				
			4	Fault, invalid, unlocked.				
			5	Format, tag, unlocked or invalid.				
			6	Format, tag, unlocked or fault.				
			7	Unused.				
	1	UTS 6 format		User Timer Stamper 6 Format. This bit controls the format conversion UTS 6 applies to the time stamp it receives from its assigned time stamp source prior to storing the formatted time stamp in the UTS readback FIFO.	0	R/W	Core clock	No
			0	UTS 6 Fractional Seconds Format (default). Converts time stamps to a 96-bit word with the 48 MSBs constituting seconds and the 48 LSBs constituting a fraction of a second in units of 2^{-48} sec.				
			1	UTS 6 PTP Format. Converts time stamps to a 96-bit word with the 48 MSBs constituting seconds. The 48 LSBs constitute a fraction of a second in units of 2^{-16} ns with the two uppermost LSBs unused.				
	0	UTS 6 enable		User Timer Stamper 6 Enable	0	R/W	Core clock	No
			0	Disabled (default).				
			1	Enabled.				
0x0E1F	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	UTS 6 tag		UTS 6 Time Stamp Source Tagging. This bit controls whether UTS 6 uses normal or tagged time stamps from its time stamp source.	0	R/W	Core clock	No
			0	Normal (default).				
			1	Tagged.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[4:0]	UTS 6 time stamp source		User Timer Stamper 6 Time Stamp Source. This 5-bit unsigned value (default = 0) is an index number for selecting the time stamp source to UTS 6.	0x00	R/W	Core clock	No
			0	REFA (default).				
			1	REFAA.				
			2	REFB.				
			3	REFBB.				
			4	DPLL0 feedback.				
			5	DPLL1 feedback.				
			6	Auxiliary REF0.				
			7	Auxiliary REF1.				
			8	Auxiliary NCO 0.				
			9	Auxiliary NCO 1.				
			11	Auxiliary REF2.				
			12	Auxiliary REF3.				
			13	IUTS 0.				
			14	IUTS 1.				
0x0E20	[7:0]	UTS 6 Offset Time[7:0]		User Time Stamper 6 Offset Time. This 24-bit signed value, UTS 6 Offset Time in units of 2^{-48} sec (default = 0), constitutes a time offset, t_{OFST} (seconds), to the time stamps received by UTS 6. UTS 6 Offset Time (rounded to the nearest integer) relates to t_{OFST} as follows: *UTS 6 Offset Time* = $t_{OFST} \times 2^{48}$ For example, given $t_{OFST} = -25 \times 10^{-9}$ sec (−25 ns), then UTS 6 Offset Time = −7,036,874 (0x 94 A036).	0x00	R/W	Core clock	No
0x0E21	[7:0]	UTS 6 Offset Time[15:8]		Continuation of the UTS 6 offset time bit field. See the UTS 6 Offset Time[7:0] description.	0x00	R/W	Core clock	No
0x0E22	[7:0]	UTS 6 Offset Time[23:16]		Continuation of the UTS 6 offset time bit field. See the UTS 6 Offset Time[7:0] description.	0x00	R/W	Core clock	No

USER TIME STAMPER CONTROL: UTS 7—REGISTER 0x0E23 TO REGISTER 0x0E27

Table 50. User Time Stamper Control: UTS 7 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0E23	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:2]	UTS 7 flags		User Timer Stamper 7 Flags. This 3-bit flag code (default = 0) defines a three-element group of status conditions that UTS 7 attaches to a converted time code. There are eight combinations with each combination comprising three status conditions. For example, the three-element group, (tag, invalid, unlocked), is one such combination, where each element constitutes one of the following five status conditions: Invalid: the reference to the CCDPLL is invalid. Fault: the reference to the CCDPLL is faulted. Unlocked: the CCDPLL is unlocked. Tag: the state of the tag bit associated with the time stamp processed by UTS 7. Format: the state of the format bit associated with UTS 7.	0x0	R/W	Core clock	No
			0	Tag, invalid, unlocked (default).				
			1	Tag, fault, unlocked.				
			2	Format, invalid, unlocked.				
			3	Format, fault, unlocked.				
			4	Fault, invalid, unlocked.				
			5	Format, tag, unlocked or invalid.				
			6	Format, tag, unlocked or fault.				
			7	Unused.				
	1	UTS 7 format		User Timer Stamper 7 Format. This bit controls the format conversion UTS 7 applies to the time stamp it receives from its assigned time stamp source prior to storing the formatted time stamp in the UTS readback FIFO.	0	R/W	Core clock	No
			0	UTS 7 Fractional Seconds Format (default). Converts time stamps to a 96-bit word with the 48 MSBs constituting seconds and the 48 LSBs constituting a fraction of a second in units of 2^{-48} sec.				
			1	UTS 7 PTP Format. Converts time stamps to a 96-bit word with the 48 MSBs constituting seconds. The 48 LSBs constitute a fraction of a second in units of 2^{-16} ns with the two uppermost LSBs unused.				
	0	UTS 7 enable		User Timer Stamper 7 Enable.	0	R/W	Core clock	No
			0	Disabled (default).				
			1	Enabled.				
0x0E24	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	UTS 7 tag		UTS 7 Time Stamp Source Tagging. This bit controls whether UTS 7 uses normal or tagged time stamps from its time stamp source.	0	R/W	Core clock	No
			0	Normal (default).				
			1	Tagged.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[4:0]	UTS 7 time stamp source		User Timer Stamper 7 Time Stamp Source. This 5-bit unsigned value (default = 0) is an index number for selecting the time stamp source to UTS 7.	0x00	R/W	Core clock	No
			0	REFA (default).				
			1	REFAA.				
			2	REFB.				
			3	REFBB.				
			4	DPLL0 feedback.				
			5	DPLL1 feedback.				
			6	Auxiliary REF0.				
			7	Auxiliary REF1.				
			8	Auxiliary NCO 0.				
			9	Auxiliary NCO 1.				
			11	Auxiliary REF2.				
			12	Auxiliary REF3.				
			13	IUTS 0.				
			14	IUTS 1.				
0x0E25	[7:0]	UTS 7 Offset Time[7:0]		User Time Stamper 7 Offset Time. This 24-bit signed value, UTS 7 Offset Time in units of 2^{-48} sec (default = 0), constitutes a time offset, t_{OFST} (seconds), to the time stamps received by UTS 7. UTS 7 Offset Time (rounded to the nearest integer) relates to t_{OFST} as follows: *UTS 7 Offset Time* = $t_{OFST} \times 2^{48}$ For example, given $t_{OFST} = -25 \times 10^{-9}$ sec (−25 ns), then UTS 7 Offset Time = −7,036,874 (0x 94 A036).	0x00	R/W	Core clock	No
0x0E26	[7:0]	UTS 7 Offset Time[15:8]		Continuation of the UTS 7 offset time bit field. See the UTS 7 Offset Time[7:0] description.	0x00	R/W	Core clock	No
0x0E27	[7:0]	UTS 7 Offset Time[23:16]		Continuation of the UTS 7 offset time bit field. See the UTS 7 Offset Time[7:0] description.	0x00	R/W	Core clock	No

USER TIME STAMPER CONTROL: UTS 8—REGISTER 0x0E28 TO REGISTER 0x0E2C

Table 51. User Time Stamper Control: UTS 8 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0E28	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:2]	UTS 8 flags		User Timer Stamper 8 Flags. This 3-bit flag code (default = 0) defines a three-element group of status conditions that UTS 8 attaches to a converted time code. There are eight combinations with each combination comprising three status conditions. For example, the three-element group, (tag, invalid, unlocked), is one such combination, where each element constitutes one of the following five status conditions: Invalid: the reference to the CCDPLL is invalid. Fault: the reference to the CCDPLL is faulted. Unlocked: the CCDPLL is unlocked. Tag: the state of the tag bit associated with the time stamp processed by UTS 8. Format: the state of the format bit associated with UTS 8.	0x0	R/W	Core clock	No
			0	Tag, invalid, unlocked (default).				
			1	Tag, fault, unlocked.				
			2	Format, invalid, unlocked.				
			3	Format, fault, unlocked.				
			4	Fault, invalid, unlocked.				
			5	Format, tag, unlocked or invalid.				
			6	Format, tag, unlocked or fault.				
			7	Unused.				
	1	UTS 8 format		User Timer Stamper 8 Format. This bit controls the format conversion UTS 8 applies to the time stamp it receives from its assigned time stamp source prior to storing the formatted time stamp in the UTS readback FIFO.	0	R/W	Core clock	No
			0	UTS 8 Fractional Seconds Format (default). Converts time stamps to a 96-bit word with the 48 MSBs constituting seconds and the 48 LSBs constituting a fraction of a second in units of 2^{-48} sec.				
			1	UTS 8 PTP Format. Converts time stamps to a 96-bit word with the 48 MSBs constituting seconds. The 48 LSBs constitute a fraction of a second in units of 2^{-16} ns with the two uppermost LSBs unused.				
	0	UTS 8 enable		User Timer Stamper 8 Enable.	0	R/W	Core clock	No
			0	Disabled (default).				
			1	Enabled.				
0x0E29	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	UTS 8 tag		UTS 8 Time Stamp Source Tagging. This bit controls whether UTS 8 uses normal or tagged time stamps from its time stamp source.	0	R/W	Core clock	No
			0	Normal (default).				
			1	Tagged.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[4:0]	UTS 8 time stamp source		User Timer Stamper 8 Time Stamp Source. This 5-bit unsigned value (default = 0) is an index number for selecting the time stamp source to UTS 8.	0x00	R/W	Core clock	No
			0	REFA (default).				
			1	REFAA.				
			2	REFB.				
			3	REFBB.				
			4	DPLL0 feedback.				
			5	DPLL1 feedback.				
			6	Auxiliary REF0.				
			7	Auxiliary REF1.				
			8	Auxiliary NCO 0.				
			9	Auxiliary NCO 1.				
			11	Auxiliary REF2.				
			12	Auxiliary REF3.				
			13	IUTS 0.				
			14	IUTS 1.				
0x0E2A	[7:0]	UTS 8 Offset Time[7:0]		User Time Stamper 8 Offset Time. This 24-bit signed value, UTS 8 Offset Time in units of 2^{-48} sec (default = 0), constitutes a time offset, t_{OFST} (seconds), to the time stamps received by UTS 8. UTS 8 Offset Time (rounded to the nearest integer) relates to t_{OFST} as follows: *UTS 8 Offset Time* = $t_{OFST} \times 2^{48}$ For example, given $t_{OFST} = -25 \times 10^{-9}$ sec (−25 ns), then UTS 8 Offset Time = −7,036,874 (0x 94 A036).	0x00	R/W	Core clock	No
0x0E2B	[7:0]	UTS 8 Offset Time[15:8]		Continuation of the UTS 8 offset time bit field. See the UTS 8 Offset Time[7:0] description.	0x00	R/W	Core clock	No
0x0E2C	[7:0]	UTS 8 Offset Time[23:16]		Continuation of the UTS 8 offset time bit field. See the UTS 8 Offset Time[7:0] description.	0x00	R/W	Core clock	No

USER TIME STAMPER FIFO—REGISTER 0x0E2D TO REGISTER 0x0E3A

Table 52. User Time Stamper FIFO Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0E2D	7	UTS FIFO overfill		User Time Stamper FIFO Overfill. This bit is a status indicator for the UTS FIFO.	0	R	Live	No
			0	Normal.				
			1	Overfill.				
	[6:0]	UTS FIFO status count		User Time Stamper FIFO Status Count. This 7-bit (unsigned) value, FIFO status count, constitutes a count code. The meaning of FIFO status count depends on the UTS FIFO overfill status (Bit 7 of this 8-bit register). When Bit 7 = 0, FIFO status count indicates the number of time code samples currently stored in the UTS FIFO. When Bit 7 = 1, FIFO status count indicates the number of lost time code samples.	0x00	R	Live	No
0x0E2E	[7:5]	UTS FIFO status flags		User Time Stamper FIFO Status Flags. This 3-bit flag code is a three-element group of status conditions associated with the current FIFO output sample, where each element has a one-to-one correspondence to the 3-bit flag code the user chose for the UTS associated with the current FIFO output sample. Deciphering the meaning of the three elements requires the user to determine which UTS associates with the source of the current FIFO output sample and the 3-bit flag code assigned to that UTS. See Register 0x0E00, Bits[4:2] for more information about the three elements.	0x0	R	Live	No
	[4:0]	UTS FIFO time stamp source		User Timer Stamper FIFO Time Stamp Source. This 5-bit unsigned value is an index number corresponding to the time stamp source associated with the current UTS FIFO output sample.	0x00	R	Live	No
			0	REFA.				
			1	REFAA.				
			2	REFB.				
			3	REFBB.				
			4	DPLL0 feedback.				
			5	DPLL1 feedback.				
			6	Auxiliary REF0.				
			7	Auxiliary REF1.				
			8	Auxiliary NCO 0.				
			9	Auxiliary NCO 1.				
			11	Auxiliary REF2.				
			12	Auxiliary REF3.				
			13	IUTS 0.				
			14	IUTS 1.				
0x0E2F	[7:0]	UTS FIFO Time Code[7:0]		User Time Stamper FIFO Time Code. This 96-bit (unsigned) value denotes a time code associated with the current FIFO output sample. Bits[95:48] constitute units of seconds. The meaning of Bits[47:0] depends on the format of the current FIFO output sample. The format of the current FIFO output sample corresponds to the format associated with UTS x (the UTS that was the source of the current FIFO output sample). When the format is fractional seconds, Bits[47:0] constitute a fraction of a second in units of 2^{-48} sec. When the format is PTP, Bits[45:0] constitute a fraction of a second in units of 2^{-16} ns with Bits[47:46] unused.	0x00	R	Live	No
0x0E30	[7:0]	UTS FIFO Time Code[15:8]		Continuation of the UTS FIFO time code bit field. See the UTS FIFO Time Code[7:0] description.	0x00	R	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0E31	[7:0]	UTS FIFO Time Code[23:16]		Continuation of the UTS FIFO time code bit field. See the UTS FIFO Time Code[7:0] description.	0x00	R	Live	No
0x0E32	[7:0]	UTS FIFO Time Code[31:24]		Continuation of the UTS FIFO time code bit field. See the UTS FIFO Time Code[7:0] description.	0x00	R	Live	No
0x0E33	[7:0]	UTS FIFO Time Code[39:32]		Continuation of the UTS FIFO time code bit field. See the UTS FIFO Time Code[7:0] description.	0x00	R	Live	No
0x0E34	[7:0]	UTS FIFO Time Code[47:40]		Continuation of the UTS FIFO time code bit field. See the UTS FIFO Time Code[7:0] description.	0x00	R	Live	No
0x0E35	[7:0]	UTS FIFO Time Code[55:48]		Continuation of the UTS FIFO time code bit field. See the UTS FIFO Time Code[7:0] description.	0x00	R	Live	No
0x0E36	[7:0]	UTS FIFO Time Code[63:56]		Continuation of the UTS FIFO time code bit field. See the UTS FIFO Time Code[7:0] description.	0x00	R	Live	No
0x0E37	[7:0]	UTS FIFO Time Code[71:64]		Continuation of the UTS FIFO time code bit field. See the UTS FIFO Time Code[7:0] description.	0x00	R	Live	No
0x0E38	[7:0]	UTS FIFO Time Code[79:72]		Continuation of the UTS FIFO time code bit field. See the UTS FIFO Time Code[7:0] description.	0x00	R	Live	No
0x0E39	[7:0]	UTS FIFO Time Code[87:80]		Continuation of the UTS FIFO time code bit field. See the UTS FIFO Time Code[7:0] description.	0x00	R	Live	No
0x0E3A	[7:0]	UTS FIFO Time Code[95:88]		Continuation of the UTS FIFO time code bit field. See the UTS FIFO Time Code[7:0] description.	0x00	R	Live	No

INVERSE USER TIME STAMPER PARAMETERS: IUTS 0—REGISTER 0x0F00 TO REGISTER 0x0F03

Table 53. IUTS 0 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0F00	[7:2]	Reserved		Reserved.	0x00	R/W	Core clock	No
	1	IUTS 0 bypass lock		Inverse User Time Stamper 0 Bypass Lock. Normally, the processing of time codes by IUTS 0 requires the CCDPLL to indicate locked status. However, this bit allows the user to remove the CCDPLL locked constraint.	0	R/W	Core clock	No
			0	Requires the CCDPLL to be locked.				
			1	Does not require the CCDPLL to be locked.				
	0	IUTS 0 valid		Inverse User Time Stamper 0 Valid. This bit allows the user to manually invalidate IUTS 0. For example, the user may be aware of a problem with the source of input time codes to IUTS 0 making IUTS 0 unsuitable as a digitized clock source to downstream resources. In this case, the user can prevent IUTS 0 from generating time stamps by invalidating it.	0	R/W	Core clock	No
			0	Invalid.				
			1	Valid.				
0x0F01	[7:0]	IUTS 0 Offset[7:0]		IUTS 0 Offset. This 24-bit signed value, IUTS 0 Time Offset with units of 2^{-48} sec (default = 0), constitutes a time offset, t_{OFST} (seconds), applied to the estimated time code generated by the period processor of IUTS 0. IUTS 0 Time Offset (rounded to the nearest integer) relates to t_{OFST} as follows: $IUTS\ 0\ Time\ Offset = t_{OFST} \times 2^{48}$ For example, given $t_{OFST} = 5 \times 10^{-9}$ sec (5 ns), then IUTS 0 Time Offset = 1,407,375 (0x 15 798F).	0x00	R/W	Core clock	No
0x0F02	[7:0]	IUTS 0 Offset[15:8]		Continuation of the IUTS 0 offset bit field. See the IUTS 0 Offset[7:0] description.	0x00	R/W	Core clock	No
0x0F03	[7:0]	IUTS 0 Offset[23:16]		Continuation of the IUTS 0 offset bit field. See the IUTS 0 Offset[7:0] description.	0x00	R/W	Core clock	No

INVERSE USER TIME STAMPER PARAMETERS: IUTS 1—REGISTER 0x0F04 TO REGISTER 0x0F07

Table 54. IUTS 1 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0F04	[7:2]	Reserved		Reserved.	0x00	R/W	Core clock	No
	1	IUTS 1 bypass lock		Inverse User Time Stamper 1 Bypass Lock. Normally, the processing of time codes by IUTS 1 requires the CCDPLL to indicate locked status. However, this bit allows the user to remove the CCDPLL locked constraint.	0	R/W	Core clock	No
			0	Requires the CCDPLL to be locked.				
			1	Does not require the CCDPLL to be locked.				
	0	IUTS 1 valid		Inverse User Time Stamper 1 Valid. This bit allows the user to manually invalidate IUTS 1. For example, the user may be aware of a problem with the source of input time codes to IUTS 1 making IUTS 1 unsuitable as a digitized clock source to downstream resources. In this case, the user can prevent IUTS 1 from generating time stamps by invalidating it.	0	R/W	Core clock	No
			0	Invalid.				
			1	Valid.				
0x0F05	[7:0]	IUTS 1 Offset[7:0]		IUTS 1 Offset. This 24-bit signed value, IUTS 1 Time Offset with units of 2^{-48} sec (default = 0), constitutes a time offset, t_{OFST} (seconds), applied to the estimated time code generated by the period processor of IUTS 1. IUTS 1 Time Offset (rounded to the nearest integer) relates to t_{OFST} as follows: $IUTS\ 1\ Time\ Offset = t_{OFST} \times 2^{48}$ For example, given $t_{OFST} = 5 \times 10^{-9}$ sec (5 ns), then IUTS 1 Time Offset = 1,407,375 (0x 15 798F).	0x00	R/W	Core clock	No
0x0F06	[7:0]	IUTS 1 Offset[15:8]		Continuation of the IUTS 1 offset bit field. See the IUTS 1 Offset[7:0] description.	0x00	R/W	Core clock	No
0x0F07	[7:0]	IUTS 1 Offset[23:16]		Continuation of the IUTS 1 offset bit field. See the IUTS 1 Offset[7:0] description.	0x00	R/W	Core clock	No

INVERSE USER TIME STAMPER: IUTS CONTROL—REGISTER 0x0F08 TO REGISTER 0x0F15

Table 55. Inverse User Time Stamper Control Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x0F08	[7:1]	Reserved		Reserved.	0x00	R	Live	No
	0	IUTS restart		IUTS Restart. This bit restarts the target resource (IUTS or CSS).	0	R/W	Live	No
			0	Normal operation.				
			1	Restart.				
0x0F09	7	IUTS format		IUTS Format. This bit defines the format of the user provided time code, which is converted to a form suitable for the target resource (IUTS or CSS).	0	R/W	Live	No
			0	Fractional Seconds Format. Defines the 96-bit time code such that Bits[95:48] constitute seconds and Bits[47:0] constitute a fraction of a second in units of 2^{-48} sec.				
			1	PTP Format. Defines the 96-bit time code such that Bits[95:48] constitute seconds and Bits[45:0] constitute a fraction of a second in units of 2^{-16} ns with Bits[47:46] unused.				
	[6:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:0]	IUTS destination		IUTS Destination. This 5-bit unsigned value is a destination index number to select the destination of the time code and restart parameters. The destinations include the CCS, which also makes use of the time code and restart parameters.	0x00	R/W	Live	No
			0 to 12	Reserved.				
			13	IUTS 0.				
			14	IUTS 1.				
			15 to 29	Reserved				
			30	CSS Sync 0 time code.				
			31	CSS Sync 1 time code.				
0x0F0A	[7:0]	IUTS Time Code[7:0]		IUTS Time Code. This 96-bit (unsigned) value denotes a time code destined for an IUTS or the CCS. Bits[95:48] constitute units of seconds. The meaning of Bits[47:0] depends on the selected format (per Register 0x0F09, Bit 7). When the format is fractional seconds, Bits[47:0] constitute a fraction of a second in units of 2^{-48} sec. When the format is PTP, Bits[45:0] constitute a fraction of a second in units of 2^{-16} ns with Bits[47:46] unused.	0x00	R/W	Live	No
0x0F0B	[7:0]	IUTS Time Code[15:8]		Continuation of the IUTS time code bit field. See the IUTS Time Code[7:0] description.	0x00	R/W	Live	No
0x0F0C	[7:0]	IUTS Time Code[23:16]		Continuation of the IUTS time code bit field. See the IUTS Time Code[7:0] description.	0x00	R/W	Live	No
0x0F0D	[7:0]	IUTS Time Code[31:24]		Continuation of the IUTS time code bit field. See the IUTS Time Code[7:0] description.	0x00	R/W	Live	No
0x0F0E	[7:0]	IUTS Time Code[39:32]		Continuation of the IUTS time code bit field. See the IUTS Time Code[7:0] description.	0x00	R/W	Live	No
0x0F0F	[7:0]	IUTS Time Code[47:40]		Continuation of the IUTS time code bit field. See the IUTS Time Code[7:0] description.	0x00	R/W	Live	No
0x0F10	[7:0]	IUTS Time Code[55:48]		Continuation of the IUTS time code bit field. See the IUTS Time Code[7:0] description.	0x00	R/W	Live	No
0x0F11	[7:0]	IUTS Time Code[63:56]		Continuation of the IUTS time code bit field. See the IUTS Time Code[7:0] description.	0x00	R/W	Live	No
0x0F12	[7:0]	IUTS Time Code[71:64]		Continuation of the IUTS time code bit field. See the IUTS Time Code[7:0] description.	0x00	R/W	Live	No
0x0F13	[7:0]	IUTS Time Code[79:72]		Continuation of the IUTS time code bit field. See the IUTS Time Code[7:0] description.	0x00	R/W	Live	No
0x0F14	[7:0]	IUTS Time Code[87:80]		Continuation of the IUTS time code bit field. See the IUTS Time Code[7:0] description.	0x00	R/W	Live	No
0x0F15	[7:0]	IUTS Time Code[95:88]		Continuation of the IUTS time code bit field. See the IUTS Time Code[7:0] description.	0x00	R/W	Live	No

DPLL0 PARAMETERS—REGISTER 0x1000 TO REGISTER 0x102A

Table 56. DPLL0 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1000	[7:0]	DPLL0 Freerun Tuning Word[7:0]		DPLL0 Freerun Tuning Word. This 46-bit unsigned value, FTW0 (default = 0), constitutes the frequency tuning word that DPLL0 uses when in freerun mode. FTW0 relates to the desired DPLL output frequency (f) and the system clock PLL VCO frequency (f_S) as follows: $FTW0 = \text{round}(2^{48} \times (f/f_S))$ To determine the output frequency generated by the DPLL NCO (f_{NCO}) when the DPLL is in freerun mode, use the following computations: $INT = \text{floor}(2^{48}/FTW0)$ where: $7 \le \text{INT} \le 13$. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction. $FRAC = 2^{-30} \times \text{round}(2^{30} \times ((2^{48}/FTW0) - INT))$ where: $0.05 \le FRAC \le 0.95$. round(x) means round x to the nearest integer. $f_{NCO} = f_S/(INT + FRAC)$ For example, given f = 305 MHz and f_S = 2400 MHz, then INT = 7, FRAC = 0.868852458894252777099609375, f_{NCO} = 305.000000004734223087702167268 34 MHz.	0x00	R/W	Core clock	No
0x1001	[7:0]	DPLL0 Freerun Tuning Word[15:8]		Continuation of the DPLL0 freerun tuning word bit field. See the DPLL0 Freerun Tuning Word[7:0] description.	0x00	R/W	Core clock	No
0x1002	[7:0]	DPLL0 Freerun Tuning Word[23:16]		Continuation of the DPLL0 freerun tuning word bit field. See the DPLL0 Freerun Tuning Word[7:0] description.	0x00	R/W	Core clock	No
0x1003	[7:0]	DPLL0 Freerun Tuning Word[31:24]		Continuation of the DPLL0 freerun tuning word bit field. See the DPLL0 Freerun Tuning Word[7:0] description.	0x00	R/W	Core clock	No
0x1004	[7:0]	DPLL0 Freerun Tuning Word[39:32]		Continuation of the DPLL0 freerun tuning word bit field. See the DPLL0 Freerun Tuning Word[7:0] description.	0x00	R/W	Core clock	No
0x1005	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	[5:0]	DPLL0 Freerun Tuning Word[45:40]		Continuation of the DPLL0 freerun tuning word bit field. See the DPLL0 Freerun Tuning Word[7:0] description.	0x00	R/W	Core clock	No
0x1006	[7:0]	DPLL0 FTW Offset Clamp[7:0]		DPLL0 FTW Offset Clamp. This 24-bit unsigned value, Frequency Clamp Value (default = 16,777,215) constitutes a frequency clamp magnitude, f_{CLAMP} (Hz), for DPLL0. Frequency Clamp Value (rounded to the nearest integer) relates to f_{CLAMP} as follows: $\text{Frequency Clamp Value} = (f_{CLAMP}/f_S) \times 2^{36}$ where f_S is the frequency at the output of the system clock PLL VCO. For example, given $f_{CLAMP} = 10^4$ Hz (10 kHz) and $f_S = 2.4 \times 10^9$ Hz (2.4 GHz), then Frequency Clamp Value = 286,331 (0x045E7B). f_{CLAMP} enforces an output frequency range (f_{RNG}) on DPLL0 such that $f_{RNG} = f_0 \pm f_{CLAMP}$, where f_0 is the value of f_{NCO} resulting from FTW0 (see Register 0x1000 for FTW0 and f_{NCO}). For f_S = 2.4 GHz, the default frequency clamp value establishes a ±586 kHz bound about f_0.	0x255	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1007	[7:0]	DPLL0 FTW Offset Clamp[15:8]		Continuation of the DPLL0 FTW offset clamp bit field. See the DPLL0 FTW Offset Clamp[7:0] description.	0x255	R/W	Core clock	No
0x1008	[7:0]	DPLL0 FTW Offset Clamp[23:16]		Continuation of the DPLL0 FTW offset clamp bit field. See the DPLL0 FTW Offset Clamp[7:0] description.	0x255	R/W	Core clock	No
0x1009	[7:4]	Reserved		Reserved.	0x0	R/W	Core clock	No
	[3:0]	DPLL0 NCO gain FTW filter bandwidth		DPLL0 NCO Gain FTW Filter Bandwidth. This 4-bit unsigned value sets the cutoff frequency (−3 dB) of a low-pass filter that applies a variable gain to the FTWs applied to the NCO of DPLL0. The variable gain compensates for the nonlinear gain associated with the Σ-Δ modulator (SDM) that comprises the NCO.	0x0	R/W	Core clock	No
			0x0	248 kHz (maximum setting) (default).				
			0x1	124 kHz.				
			0x2	62 kHz.				
			0x3	31 kHz.				
			0x4	15.5 kHz.				
			0x5	7.8 kHz.				
			0x6	3.9 kHz.				
			0x7	1.9 kHz.				
			0x8	970 Hz.				
			0x9	490 Hz.				
			0xa	240 Hz.				
			0xb	120 Hz.				
			0xc	61 Hz.				
			0xd	30 Hz.				
			0xe	15 Hz.				
			0xf	7.6 Hz (minimum setting).				
0x100A	[7:0]	DPLL0 History Accumulation Timer[7:0]		DPLL0 History Accumulation Timer. This 28-bit unsigned value, DPLL0 History Accumulation Timer in units of milliseconds (default = 10), constitutes an averaging period, t_{ACCUM} (seconds). DPLL0 History Accumulation Timer (rounded to the nearest integer) relates to t_{ACCUM} as follows: *DPLL0 History Accumulation Timer* = 1000 × t_{ACCUM} For example, given t_{ACCUM} = 900 sec (15 min), then DPLL0 History Accumulation Timer = 900,000 (0x 00D BBA0). t_{ACCUM} constitutes an averaging period for processing the holdover tuning word value. The default value sets t_{ACCUM} = 10 ms, but the available range is 1 ms to 268,435.455 sec (~74.5 hours). DPLL0 History Accumulation Timer = 0 is a special case that routes tuning word samples from the digital loop filter to both the DPLL0 NCO and Register 0x3108 to Register 0x3103, Bits[46:0] (bypassing the tuning word history processor). This makes it possible for the user to monitor tuning words applied to the DPLL NCO as they arrive from the loop filter.	0x10	R/W	Core clock	No
0x100B	[7:0]	DPLL0 History Accumulation Timer[15:8]		Continuation of the DPLL0 history accumulation timer bit field. See the DPLL0 History Accumulation Timer[7:0] description.	0x00	R/W	Core clock	No
0x100C	[7:0]	DPLL0 History Accumulation Timer[23:16]		Continuation of the DPLL0 history accumulation timer bit field. See the DPLL0 History Accumulation Timer[7:0] description.	0x00	R/W	Core clock	No
0x100D	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	[3:0]	DPLL0 History Accumulation Timer[27:24]		Continuation of the DPLL0 history accumulation timer bit field. See the DPLL0 History Accumulation Timer[7:0] description.	0x0	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x100E	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	DPLL0 delay history while slewing		DPLL0 Delay History Until Phase Slew Limit Inactive. By default, as soon as DPLL0 declares a translation profile active, the tuning word history averaging processor is reset and begins processing tuning words from the loop filter. This bit allows the user to delay the averaging process until the DPLL0 phase slew limiter is not actively slewing phase.	1	R/W	Core clock	No
			0	DPLL0 does not postpone tuning word averaging contingent on the state of the phase slew limiter.				
			1	DPLL0 postpones tuning word averaging while the phase limiter is actively slewing phase (default).				
	4	DPLL0 delay history frequency lock		DPLL0 Delay History Until Frequency Lock. By default, as soon as DPLL0 declares a translation profile active, the tuning word history averaging processor is reset and begins processing tuning words from the loop filter. This bit allows the user to delay the averaging process until DPLL0 frequency locks.	1	R/W	Core clock	No
			0	DPLL0 does not postpone tuning word averaging contingent on frequency lock status.				
			1	DPLL0 postpones tuning word averaging until frequency lock occurs (default).				
	3	DPLL0 delay history phase lock		DPLL0 Delay History Until Phase Lock. By default, as soon as DPLL0 declares a translation profile active, the tuning word history averaging processor is reset and begins processing tuning words from the loop filter. This bit allows the user to delay the averaging process until DPLL0 phase locks.	1	R/W	Core clock	No
			0	DPLL0 does not postpone tuning word averaging contingent on phase lock status.				
			1	DPLL0 postpones tuning word averaging until phase lock occurs (default).				
	2	DPLL0 quick start history		DPLL0 Quick Start History. By default, when DPLL0 is in active closed-loop operation, the available tuning word history ($FTW_{HISTORY}$) in Register 0x3103 to Register 0x3108 does not update until tuning word history averaging has run for the full duration prescribed by the history accumulation timer (t_{ACCUM}). Thus, a switch to holdover prior to t_{ACCUM} causes the DPLL to use the freerun tuning word (FTW0) because of the absence of $FTW_{HISTORY}$. This can be problematic for applications requiring large t_{ACCUM} (hours, for example), because the DPLL may switch to holdover just prior to meeting t_{ACCUM}. This bit allows the DPLL to update $FTW_{HISTORY}$ as early as 1/4 of t_{ACCUM}.	0	R/W	Core clock	No
			0	DPLL0 updates $FTW_{HISTORY}$ no earlier than t_{ACCUM}. (default).				
			1	DPLL0 updates $FTW_{HISTORY}$ as early as $t_{ACCUM}/4$.				
	1	DPLL0 single sample history		DPLL0 Single Sample History. By default, DPLL0 uses the available tuning word history ($FTW_{HISTORY}$) when switching to holdover mode from active closed-loop operation. However, if $FTW_{HISTORY}$ is unavailable, the DPLL uses the freerun tuning word (FTW0). This bit allows the DPLL to use the most recent FTW value from the loop filter instead of FTW0 when $FTW_{HISTORY}$ is unavailable.	0	R/W	Core clock	No
			0	DPLL0 uses FTW0 if $FTW_{HISTORY}$ is unavailable when switching to holdover (default).				
			1	DPLL0 uses the most recent FTW from the loop filter if $FTW_{HISTORY}$ is unavailable when switching to holdover.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	0	DPLL0 persistent history		DPLL0 Persistent History. By default, the history tuning word processor continues its history tuning word averaging process regardless of the state of DPLL0. This bit, in conjunction with Register 0x100F, Bits[2:0], allows the user to establish reset or pause conditions on the history accumulation process. 0 Reset the history tuning word averaging process (default). 1 Pause the history tuning word averaging process.	0	R/W	Core clock	No
0x100F	[7:3]	Reserved		Reserved.	0x00	R	Live	No
	2	DPLL0 pause history while slewing		DPLL0 Pause History While Phase Slew Limited. By default, the history tuning word processor continues its history tuning word averaging process regardless of the state of DPLL0. However, the user can have the averaging processor reset or pause (depending on Register 0x100E, Bit 0) based on the state of the DPLL. When this bit is Logic 1 (default = 0), it allows the tuning word averaging processor to be reset or paused while the DPLL is actively slewing phase.	0	R/W	Core clock	No
	1	DPLL0 pause history frequency lock		DPLL0 Pause History While Frequency Unlock. By default, the history tuning word processor continues its history tuning word averaging process regardless of the state of DPLL0. However, the user can have the averaging processor reset or pause (depending on Register 0x100E, Bit 0) based on the state of the DPLL. When this bit is Logic 1 (default = 0), it allows the tuning word averaging processor to be reset or paused while the DPLL is not frequency locked.	0	R/W	Core clock	No
	0	DPLL0 pause history phase lock		DPLL0 Pause History While Phase Unlock. By default, the history tuning word processor continues its history tuning word averaging process regardless of the state of DPLL0. However, the user can have the averaging processor reset or pause (depending on Register 0x100E, Bit 0) based on the state of the DPLL. When this bit is Logic 1 (default = 0), it allows the tuning word averaging processor to be reset or paused while the DPLL is not phase locked.	0	R/W	Core clock	No
0x1010	[7:0]	DPLL0 history holdoff time		DPLL0 History Holdoff Time. This 8-bit unsigned value, DPLL0 History Holdoff Time (default = 0), constitutes a holdoff period, t_{HOLD}. DPLL0 History Holdoff Time relates to t_{HOLD} as follows: $t_{HOLD} = DPLL0\ History\ Holdoff\ Time \times (t_{ACCUM}/8)$ where t_{ACCUM} is the value in Register 0x100D to Register 0x100A, Bits[27:0]. For example, given t_{ACCUM} = 16 sec and DPLL0 History Holdoff Time = 10, then t_{HOLD} = 20 sec. t_{HOLD} is the time that DPLL0 waits, after declaring a translation profile active, before allowing the tuning word history averaging processor to start its tuning word averaging process. t_{HOLD} does not take effect until the expiration of any event dependent delays prescribed by Register 0x100E, Bits[5:3].	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1011	[7:0]	DPLL0 Phase Slew Limit Rate[7:0]		DPLL0 Phase Slew Limit Rate. This 32-bit unsigned value, DPLL0 Phase Slew Limit Rate (units of picoseconds/second, or 10^{-12}), defines a maximum rate of change of phase, Δt/t, that can appear at the output of the phase detector of DPLL0. Δt/t equates to a maximum relative frequency offset of DPLL0 Phase Slew Limit Rate × 10^{-6} ppm. DPLL0 Phase Slew Limit Rate relates to Δt/t as follows: $\Delta t/t = DPLL0\ Phase\ Slew\ Limit\ Rate \times 10^{-12}$ By default, DPLL0 Phase Slew Limit Rate = 100,663,296 (0x 0600 0000), which equates to a maximum relative frequency offset of approximately 100 ppm. The maximum value of DPLL0 Phase Slew Limit Rate equates to approximately 4000 ppm.	0x00	R/W	Core clock	No
0x1012	[7:0]	DPLL0 Phase Slew Limit Rate[15:8]		Continuation of the DPLL0 phase slew limit rate bit field. See the DPLL0 Phase Slew Limit Rate[7:0] description.	0x00	R/W	Core clock	No
0x1013	[7:0]	DPLL0 Phase Slew Limit Rate[23:16]		Continuation of the DPLL0 phase slew limit rate bit field. See the DPLL0 Phase Slew Limit Rate[7:0] description.	0x00	R/W	Core clock	No
0x1014	[7:0]	DPLL0 Phase Slew Limit Rate[31:24]		Continuation of the DPLL0 phase slew limit rate bit field. See the DPLL0 Phase Slew Limit Rate[7:0] description.	0x06	R/W	Core clock	No
0x1015	[7:0]	DPLL0 Phase Offset[7:0]		DPLL0 Closed-Loop Phase Offset. This 40-bit signed value, DPLL0 Phase Offset in units of picoseconds (default = 0), defines a fixed time (phase) offset, t_{OFST} (seconds), added in the feedback path to the phase detector of DPLL0. The result is a fixed time offset, t_{OFST}, at the output of DPLL0 relative to the reference input signal. DPLL0 Phase Offset (rounded to the nearest integer) relates to t_{OFST} as follows: $DPLL0\ Phase\ Offset = t_{OFST} \times 10^{12}$ A positive DPLL0 Phase Offset causes the output signal of the DPLL to lag relative to the input reference signal.	0x00	R/W	Core clock	No
0x1016	[7:0]	DPLL0 Phase Offset[15:8]		Continuation of the DPLL0 phase offset bit field. See the DPLL0 Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x1017	[7:0]	DPLL0 Phase Offset[23:16]		Continuation of the DPLL0 phase offset bit field. See the DPLL0 Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x1018	[7:0]	DPLL0 Phase Offset[31:24]		Continuation of the DPLL0 phase offset bit field. See the DPLL0 Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x1019	[7:0]	DPLL0 Phase Offset[39:32]		Continuation of the DPLL0 phase offset bit field. See the DPLL0 Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x101A	[7:0]	DPLL0 Phase Temperature Compensation C_1 Significand[7:0]		DPLL0 Phase Temperature Compensation C_1 Significand. Synopsis: DPLL0 delay compensation injects a temperature (T) dependent correction factor (CF) as a time offset in the feedback path to the phase detector based on a fifth-order polynomial such that $CF = \Sigma(C_k \times T^k)$ (k = 1 to 5). T originates either from the on-board temperature sensor or from Register 0x2901 to Register 0x2900, Bits[15:0]. Each coefficient, C_k, takes the following form: $C_k = S_k \times 2^{Ek}$ where: S_k denotes the significand associated with C_k. E_k denotes the power of 2 exponent associated with C_k. When $C_k = 0$ or $\lvert C_k \rvert < 2^{-128}$, then $E_k = 0$ and $S_k = 0$. Detail: this 16-bit signed value, S_1 (default = 0), constitutes the significand associated with C_1. S_1 relates to C_1 as follows: $S_1 = \text{round}(C_1 \times 2^{15 - E1})$ where round(x) means round x to the nearest integer. Example: given $C_1 = -2.8927765 \times 10^{-6}$, then $E_1 = -18$ (see Register 0x101C), and thus $S_1 = -24{,}849$ (0x9EEF).	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x101B	[7:0]	DPLL0 Phase Temperature Compensation C_1 Significand[15:8]		Continuation of the DPLL0 phase temperature compensation C_1 significand bit field. See the DPLL0 Phase Temperature Compensation C_1 Significand[7:0] description.	0x00	R/W	Core clock	No
0x101C	[7:0]	DPLL0 phase temperature compensation C_1 exponent		DPLL0 Phase Temperature Compensation C_1 Exponent. Synopsis: see Register 0x101A. Detail: this 8-bit signed value, E_1 (default = 0), constitutes the power of 2 exponent associated with C_1. E_1 relates to C_1 as follows: $E_1 = \text{floor}(\log(\lvert C_1 \rvert)/\log(2)) + 1$ where floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction. Example: given $C_1 = -2.8927765 \times 10^{-6}$, then $E_1 = -18$ (0xEE).	0x00	R/W	Core clock	No
0x101D	[7:0]	DPLL0 Phase Temperature Compensation C_2 Significand[7:0]		DPLL0 Phase Temperature Compensation C_2 Significand. This 16-bit signed value, S_2 (default = 0), constitutes the significand associated with C_2. S_2 relates to C_2 as follows: $S_2 = \text{round}(C_2 \times 2^{15 - E2})$ See Register 0x101A for guidance.	0x00	R/W	Core clock	No
0x101E	[7:0]	DPLL0 Phase Temperature Compensation C_2 Significand[15:8]		Continuation of the DPLL0 phase temperature compensation C_2 significand bit field. See the DPLL0 Phase Temperature Compensation C_2 Significand[7:0] description.	0x00	R/W	Core clock	No
0x101F	[7:0]	DPLL0 phase temperature compensation C_2 exponent		DPLL0 Phase Temperature Compensation C_2 Exponent. This 8-bit signed value, E_2 (default = 0), constitutes the power of 2 exponent associated with C_2. E_2 relates to C_2 as follows: $E_2 = \text{floor}(\log(\lvert C_2 \rvert)/\log(2)) + 1$ See Register 0x101C for guidance.	0x00	R/W	Core clock	No
0x1020	[7:0]	DPLL0 Phase Temperature Compensation C_3 Significand[7:0]		DPLL0 Phase Temperature Compensation C_3 Significand. This 16-bit signed value, S_3 default = 0), constitutes the significand associated with C_3. S_3 relates to C_3 as follows: $S_3 = \text{round}(C_3 \times 2^{15 - E3})$ See Register 0x101A for guidance.	0x00	R/W	Core clock	No
0x1021	[7:0]	DPLL0 Phase Temperature Compensation C_3 Significand[15:8]		Continuation of the DPLL0 phase temperature compensation C_3 significand bit field. See the DPLL0 Phase Temperature Compensation C_3 Significand[7:0] description.	0x00	R/W	Core clock	No
0x1022	[7:0]	DPLL0 phase temperature compensation C_3 exponent		DPLL0 Phase Temperature Compensation C_3 Exponent. This 8-bit signed value, E_3 (default = 0), constitutes the power of 2 exponent associated with C_3. E_3 relates to C_3 as follows: $E_3 = \text{floor}(\log(\lvert C_3 \rvert)/\log(2)) + 1$ See Register 0x101C for guidance.	0x00	R/W	Core clock	No
0x1023	[7:0]	DPLL0 Phase Temperature Compensation C_4 Significand[7:0]		DPLL0 Phase Temperature Compensation C_4 Significand. This 16-bit signed value, S_4 (default = 0), constitutes the significand associated with C_4. S_4 relates to C_4 as follows: $S_4 = \text{round}(C_4 \times 2^{15 - E4})$ See Register 0x101A for guidance.	0x00	R/W	Core clock	No
0x1024	[7:0]	DPLL0 Phase Temperature Compensation C_4 Significand[15:8]		Continuation of the DPLL0 phase temperature compensation C_4 significand bit field. See the DPLL0 Phase Temperature Compensation C_4 Significand[7:0] description.	0x00	R/W	Core clock	No
0x1025	[7:0]	DPLL0 Phase Temperature Compensation C_4 Exponent		DPLL0 Phase Temperature Compensation C_4 Exponent. This 8-bit signed value, E_4 (default = 0), constitutes the power of 2 exponent associated with C_4. E_4 relates to C_4 as follows: $E_4 = \text{floor}(\log(\lvert C_4 \rvert)/\log(2)) + 1$ See Register 0x101C for guidance.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1026	[7:0]	DPLL0 Phase Temperature Compensation C_5 Significand[7:0]		DPLL0 Phase Temperature Compensation C_5 Significand. This 16-bit signed value, S_5 (default = 0), constitutes the significand associated with C_5. S_5 relates to C_5 as follows: $S_5 = \text{round}(C_5 \times 2^{15-E5})$ See Register 0x101A for guidance.	0x00	R/W	Core clock	No
0x1027	[7:0]	DPLL0 Phase Temperature Compensation C_5 Significand[15:8]		Continuation of the DPLL0 phase temperature compensation C_5 significand bit field. See the DPLL0 Phase Temperature Compensation C_5 Significand[7:0] description.	0x00	R/W	Core clock	No
0x1028	[7:0]	DPLL0 Phase Temperature Compensation C_5 Exponent		DPLL0 Phase Temperature Compensation C_5 Exponent. This 8-bit signed value, E_5 (default = 0), constitutes the power of 2 exponent associated with C_5. E_5 relates to C_5 as follows: $E_5 = \text{floor}(\log(\lvert C_5 \rvert)/\log(2)) + 1$ See Register 0x101C for guidance.	0x00	R/W	Core clock	No
0x1029	[7:3]	Reserved		Reserved.	0x00	R	Live	No
	[2:0]	DPLL0 phase temperature compensation filter bandwidth		DPLL0 Phase Temperature Compensation Low-Pass Filter Bandwidth. This 4-bit unsigned value sets the cutoff frequency (−3 dB) of the low-pass filter at the output of the delay compensation polynomial calculator of DPLL0. The filter serves to suppress rapid changes in the temperature compensation values.	0x0	R/W	Core clock	No
			0x0	240 Hz (maximum setting) (default).				
			0x1	120 Hz.				
			0x2	60 Hz.				
			0x3	30 Hz.				
			0x4	15 Hz.				
			0x5	7.6 Hz.				
			0x6	3.8 Hz.				
			0x7	1.9 Hz (minimum setting).				
0x102A	[7:3]	Reserved		Reserved.	0x00	R	Live	No
	[2:0]	DPLL0 inactive profile index		DPLL0 Inactive Profile Index. This 3-bit unsigned value, x (default = 0), identifies Translation Profile 0.x as the inactive profile for cascaded DPLL operation when DPLL0 switches to freerun or holdover mode.	0x0	R/W	Core clock	No

APLL0 PARAMETERS—REGISTER 0x1080 TO REGISTER 0x1083

Table 57. APLL0 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1080	7	Enable APLL0 manual charge pump current		Enables Manual Control of APLL0 Charge Pump Current. This bit controls whether the charge pump associated with the PFD of APLL0 operates in manual or automatic mode. In manual mode, the nominal charge pump current (I_{CP0}) depends on the value of Bits[6:0]. In automatic mode, I_{CP0} depends on the value, M, of the M0 divider, where I_{CP0} = 1016 µA for M ≥ 64 and I_{CP0} = M × 16 µA for M < 64.	1	R/W	Serial port clock	No
			0	Automatic.				
			1	Manual (default).				
	[6:0]	APLL0 manual charge pump current		APLL0 Manual Charge Pump Current. This 7-bit unsigned value, I_{CP} (units of 8 µA), establishes the nominal charge pump current (I_{CP0}) of the PFD associated with APLL0, but is only effective when the charge pump is configured for manual operation. I_{CP} = 20 decimal (default), yielding I_{CP0} = 160 µA.	0x20	R/W	Serial port clock	No
0x1081	[7:0]	APLL0 M0 feedback divider		APLL Multiplication Ratio. This 8-bit unsigned value, M (default = 0), constitutes the divide ratio of the M0 divider. Valid values for M are from 14 to 255. The default value is not valid. Therefore, the user must program a valid value.	0x00	R/W	Serial port clock	No
0x1082	[7:5]	APLL0 Loop Filter Zero resistor (R1)		Loop Filter R1. This 3-bit unsigned value (default = 7) selects the resistance of R1 (one of the internal components comprising the loop filter of APLL0). R1 resides between the output of the charge pump and the LF0 pin.	0x7	R/W	Serial port clock	No
			000	0 Ω.				
			001	250 Ω.				
			010	500 Ω.				
			011	750 Ω.				
			100	1.00 kΩ.				
			101	1.25 kΩ.				
			110	1.50 kΩ.				
			111	1.75 kΩ (default).				
	[4:2]	APLL0 loop filter pole capacitor (C2)		Loop Filter C2. This 3-bit unsigned value (default = 0) selects the capacitance of C2 (one of the internal components comprising the loop filter of APLL0). C2 resides between the output of the charge pump and the LDO0 pin.	0x0	R/W	Serial port clock	No
			000	8 pF (default).				
			001	24 pF.				
			010	40 pF.				
			011	56 pF.				
			100	72 pF.				
			101	88 pF.				
			110	104 pF.				
			111	120 pF.				
	[1:0]	APLL0 loop filter second pole resistor (R3)		Loop Filter R3. This 2-bit unsigned value (default = 0) selects the resistance of R3 (one of the internal components comprising the loop filter of APLL0). R3 resides between the output of the charge pump and the input to the VCO.	0x0	R/W	Serial port clock	No
			00	200 Ω (default).				
			01	250 Ω.				
			10	333 Ω.				
			11	500 Ω.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1083	[7:4]	Reserved		Reserved.	0x0	R/W	Serial port clock	No
	3	APLL0 dc offset current direction		DC Offset Current Polarity. This bit selects the polarity of I_{OFST} for APLL0. With regard to the action of the charge pump, positive polarity is in the pump up direction (default) and negative polarity is in the pump down direction.	0	R/W	Serial port clock	No
			0	Positive (default).				
			1	Negative.				
	[2:1]	APLL0 dc offset current value		I_{OFST} Magnitude. This 2-bit unsigned value (default = 1) selects a scale factor, SF, for the charge pump offset current (I_{OFST}) for APLL0, such that $I_{OFST} = SF \times I_{CP0}$. The magnitude of I_{OFST} is quantized to 8 µA.	0x1	R/W	Serial port clock	No
			00	SF = 0.5.				
			01	SF = 0.25 (default).				
			10	SF = 0.125.				
			11	SF = 0.0625.				
	0	Enable APLL0 dc offset current		DC Offset Current Enable. This bit allows the application of a supplemental constant current source (I_{OFST}) to the nominal charge pump current (I_{CP0}) of APLL0 such that $I_{CP} = I_{CP0} + I_{OFST}$.	1	R/W	Serial port clock	No
			0	Disabled.				
			1	Enabled (default).				

DISTRIBUTION CONTROL: PLL CHANNEL 0—REGISTER 0x10C0 TO REGISTER 0x10DC

Table 58. Distribution Control: PLL Channel 0 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x10C0	[7:0]	Modulation Step[7:0]		Pulse Width Modulator Duty Cycle Deviation (PLL0). This 16-bit unsigned value, Modulation Step (default = 0) in units of half-cycles of the input clock to the Q divider, controls the duty cycle deviation, D, associated with a modulation event. The value of Modulation Step is common to the A, B, and C pulse width modulators. Modulation Step relates to D as follows: $D = Modulation\ Step/(2 \times QDIV0y)$ where *QDIV0y* is the divide ratio of the applicable Q divider (*y* is A, B, or C). For example, given Modulation Step = 100 and QDIV0y = 8025.5, then D = 0.00623 (0.623%).	0x00	R/W	Serial port clock	No
0x10C1	[7:0]	Modulation Step[15:8]		Continuation of the modulation step bit field. See the Modulation Step[7:0] description	0x00	R/W	Serial port clock	No
0x10C2	[7:0]	OUT0A Modulation Counter[7:0]		OUT0A Pulse Width Modulator Modulation Counter. This 28-bit unsigned value, Modulation Counter (default = 0), establishes the modulation period (t_{MOD}) of the pulse width modulator associated with Q0A, where t_{MOD} is the time period between modulation events. Modulation Counter relates to t_{MOD} as follows: $t_{MOD} = Modulation\ Counter \times (QDIV0A/f_{IN})$ where: *QDIV0A* is the divide ratio of Q0A. f_{IN} is the input clock frequency to Q0A. For example, given f_{IN} = 1.19 GHz, QDIV0A = 107.5 and Modulation Counter = 11,070, then t_{MOD} = 1.000 ms. Modulation Counter ≥ 6 when using pulse width modulation. Modulation Counter ≥ SYNC_EDGE + 7 (see Register 0x10CE, Bits[1:0]) when using triggered pulse width modulation.	0x00	R/W	Serial port clock	No
0x10C3	[7:0]	OUT0A Modulation Counter[15:8]		Continuation of the OUT0A modulation counter bit field. See the OUT0A Modulation Counter[7:0] description.	0x00	R/W	Serial port clock	No
0x10C4	[7:0]	OUT0A Modulation Counter[23:16]		Continuation of the OUT0A modulation counter bit field. See the OUT0A Modulation Counter[7:0] description.	0x00	R/W	Serial port clock	No
0x10C5	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	[3:0]	OUT0A Modulation Counter[27:24]		Continuation of the OUT0A modulation counter bit field. See the OUT0A Modulation Counter[7:0] description.	0x0	R/W	Serial port clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x10C6	[7:0]	OUT0B Modulation Counter[7:0]		OUT0B Pulse Width Modulator Modulation Counter. This 28-bit unsigned value, Modulation Counter (default = 0), establishes the modulation period (t_{MOD}) of the pulse width modulator associated with Q0B, where t_{MOD} is the time period between modulation events. Modulation Counter relates to t_{MOD} as follows: $t_{MOD} = Modulation\ Counter \times (QDIV0B/f_{IN})$ where: *QDIV0B* is the divide ratio of Q0B. f_{IN} is the input clock frequency to Q0B. For example, given f_{IN} = 1.19 GHz, QDIV0B = 107.5 and Modulation Counter = 11,070, then t_{MOD} = 1.000 ms. Modulation Counter ≥ 6 when using pulse width modulation. Modulation Counter ≥ SYNC_EDGE + 7 (see Register 0x10CE, Bits[1:0]) when using triggered pulse width modulation.	0x00	R/W	Serial port clock	No
0x10C7	[7:0]	OUT0B Modulation Counter[15:8]		Continuation of the OUT0B modulation counter bit field. See the OUT0B Modulation Counter[7:0] description.	0x00	R/W	Serial port clock	No
0x10C8	[7:0]	OUT0B Modulation Counter[23:16]		Continuation of the OUT0B modulation counter bit field. See the OUT0B Modulation Counter[7:0] description.	0x00	R/W	Serial port clock	No
0x10C9	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	[3:0]	OUT0B Modulation Counter[27:24]		Continuation of the OUT0B modulation counter bit field. See the OUT0B Modulation Counter[7:0] description.	0x0	R/W	Serial port clock	No
0x10CA	[7:0]	OUT0C Modulation Counter[7:0]		OUT0C Pulse Width Modulator Modulation Counter. This 28-bit unsigned value, Modulation Counter (default = 0), establishes the modulation period (t_{MOD}) of the pulse width modulator associated with Q0C, where t_{MOD} is the time period between modulation events. Modulation Counter relates to t_{MOD} as follows: $t_{MOD} = Modulation\ Counter \times (QDIV0C/f_{IN})$ where: *QDIV0C* is the divide ratio of Q0C. f_{IN} is the input clock frequency to Q0C. For example, given f_{IN} = 1.19 GHz, QDIV0C = 107.5 and Modulation Counter = 11,070, then t_{MOD} = 1.000 ms. Modulation Counter ≥ 6 when using pulse width modulation. Modulation Counter ≥ SYNC_EDGE + 7 (see Register 0x10CE, Bits[1:0]) when using triggered pulse width modulation.	0x00	R/W	Serial port clock	No
0x10CB	[7:0]	OUT0C Modulation Counter[15:8]		Continuation of the OUT0C modulation counter bit field. See the OUT0C Modulation Counter[7:0] description.	0x00	R/W	Serial port clock	No
0x10CC	[7:0]	OUT0C Modulation Counter[23:16]		Continuation of the OUT0C modulation counter bit field. See the OUT0C Modulation Counter[7:0] description.	0x00	R/W	Serial port clock	No
0x10CD	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	[3:0]	OUT0C Modulation Counter[27:24]		Continuation of the OUT0C modulation counter bit field. See the OUT0C Modulation Counter[7:0] description.	0x0	R/W	Serial port clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x10CE	[7:2]	Reserved		Reserved.	0x00	R	Live	No
	[1:0]	Feedback divider sync edge		Feedback Divider Synchronization Edge. This 2-bit unsigned value, SYNC_EDGE (default = 0), assigns the number of Q divider output periods (0, 1, 2, or 3) to delay synchronization (relative to the modulation base edge) of the DPLL0 feedback divider. SYNC_EDGE = 0 is not valid. Thus, the user must program a nonzero value.	0x0	R/W	Serial port clock	No
0x10CF	[7:4]	Reserved		Reserved.	0x0	R/W	Serial port clock	No
	3	Enable OUT0A N shot modulation		OUT0A Pulse Width Modulator Trigger Type Select. This bit (default = 0) selects between immediate and triggered generation of modulation events by the pulse width modulator associated with Q0A. The following two triggering methods are possible: When Register 0x10D3, Bit 6 = 0, the trigger signal causes the pulse width modulator to generate five modulation events and then stop. When Register 0x10D3, Bit 6 = 1, the pulse width modulator continuously generates modulation events when the trigger signal is Logic 1. The Q divider N shot/PRBS controller is the source of the trigger signal and trigger controls (refer to the AD9546 data sheet for details). 0 Immediate modulation events (default). 1 Triggered modulation events.	0	R/W	Serial port clock	No
	2	Enable OUT0A single pulse modulation		OUT0A Pulse Width Modulator Balanced/Unbalanced Select. This bit selects balanced (default) or unbalanced modulation events generated by the pulse width modulator associated with Q0A. 0 Balanced (default). 1 Unbalanced.	0	R/W	Serial port clock	No
	1	OUT0A modulation polarity		OUT0A Pulse Width Modulator Polarity. This bit selects, as narrow (default) or wide, the width of the first pulse of a Q0A modulation event. For balanced modulation, the width of the second pulse of the modulation event has the opposite width of that of the first pulse. 0 First pulse narrow (default). 1 First pulse wide.	0	R/W	Serial port clock	No
	0	Enable OUT0A modulation		OUT0A Pulse Width Modulator Enable. This bit selects or bypasses the pulse width modulator (embedded clock modulator) associated with Q0A. 0 Bypass pulse width modulator (default). 1 Select pulse width modulator.	0	R/W	Serial port clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x10D0	[7:4]	Reserved		Reserved.	0x0	R/W	Serial port clock	No
	3	Enable OUT0B N shot modulation		OUT0B Pulse Width Modulator Trigger Type Select. This bit (default = 0) selects between immediate and triggered generation of modulation events by the pulse width modulator associated with Q0B. The following two triggering methods are possible: When Register 0x10D3, Bit 6 = 0, the trigger signal causes the pulse width modulator to generate five modulation events and then stop. When Register 0x10D3, Bit 6 = 1, the pulse width modulator continuously generates modulation events when the trigger signal is Logic 1. The Q divider N shot/PRBS controller is the source of the trigger signal and trigger controls (refer to the AD9546 data sheet for details).	0	R/W	Serial port clock	No
			0	Immediate modulation events (default).				
			1	Triggered modulation events.				
	2	Enable OUT0B single pulse modulation		OUT0B Pulse Width Modulator Balanced/Unbalanced Select. This bit selects balanced (default) or unbalanced modulation events generated by the pulse width modulator associated with Q0B.	0	R/W	Serial port clock	No
			0	Balanced (default).				
			1	Unbalanced.				
	1	OUT0B modulation polarity		OUT0B Pulse Width Modulator Polarity. This bit selects, as narrow (default) or wide, the width of the first pulse of a Q0B modulation event. For balanced modulation, the width of the second pulse of the modulation event has the opposite width of that of the first pulse.	0	R/W	Serial port clock	No
			0	First pulse narrow (default).				
			1	First pulse wide.				
	0	Enable OUT0B modulation		OUT0B Pulse Width Modulator Enable. This bit selects or bypasses the pulse width modulator (embedded clock modulator) associated with Q0B.	0	R/W	Serial port clock	No
			0	Bypass pulse width modulator (default).				
			1	Select pulse width modulator.				
0x10D1	[7:4]	Reserved		Reserved.	0x0	R/W	Serial port clock	No
	3	Enable OUT0C N shot modulation		OUT0C Pulse Width Modulator Trigger Type Select. This bit (default = 0) selects between immediate and triggered generation of modulation events by the pulse width modulator associated with Q0C. The following two triggering methods are possible: When Register 0x10D3, Bit 6 = 0, the trigger signal causes the pulse width modulator to generate five modulation events and then stop. When Register 0x10D3, Bit 6 = 1, the pulse width modulator continuously generates modulation events when the trigger signal is Logic 1. The Q divider N shot/PRBS controller is the source of the trigger signal and trigger controls (refer to the AD9546 data sheet for details).	0	R/W	Serial port clock	No
			0	Immediate modulation events (default).				
			1	Triggered modulation events.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	2	Enable OUT0C single pulse modulation		OUT0C Pulse Width Modulator Balanced/Unbalanced Select. This bit selects balanced (default) or unbalanced modulation events generated by the pulse width modulator associated with Q0C.	0	R/W	Serial port clock	No
			0	Balanced (default).				
			1	Unbalanced.				
	1	OUT0C modulation polarity		OUT0C Pulse Width Modulator Polarity. This bit selects, as narrow (default) or wide, the width of the first pulse of a Q0C modulation event. For balanced modulation, the width of the second pulse of the modulation event has the opposite width of that of the first pulse.	0	R/W	Serial port clock	No
			0	First pulse narrow (default).				
			1	First pulse wide.				
	0	Enable OUT0C modulation		OUT0C Pulse Width Modulator Enable. This bit selects or bypasses the pulse width modulator (embedded clock modulator) associated with Q0C.	0	R/W	Serial port clock	No
			0	Bypass pulse width modulator (default).				
			1	Select pulse width modulator.				
0x10D2	[7:0]	N shot gap		N Shot Gap (PLL0). This 8-bit unsigned value, Gap (default = 0) in units of Q divider output clock periods, defines how long the N shot generator blanks the Q divider output (that is, no rising edges) during an N shot event associated with PLL0. An N shot event consists of a pulsing interval followed by a blank interval (no pulses). N (in Register 0x10D3, Bits[5:0]) defines the pulsing interval, whereas Gap defines the blank interval. The value of Gap is common to the A, AA, B, BB, C, and CC N shot generators.	0x00	R/W	Serial port clock	No
0x10D3	7	Reserved		Reserved.	0	R/W	Serial port clock	No
	6	N shot request mode		N Shot Request Burst/Edge or Periodic/Level (PLL0). This bit (default = 0) selects between burst and periodic generation of N shot events associated with PLL0. In burst operation, the N shot generator triggers on the rising edge of the trigger signal. In periodic operation, the N shot generator produces N shot events only while the trigger signal is Logic 1. The N shot generator stalls (see the AD9546 data sheet for details) when the trigger signal is Logic 1. See Register 0x10D6, Bit 0 regarding the trigger signal. This bit is common to the A, AA, B, BB, C, and CC N shot generators and the A, B, and C pulse width modulators.	0	R/W	Serial port clock	No
			0	N shot burst operation (edge triggered).				
			1	N shot periodic operation (level triggered).				
	[5:0]	N shot		Number of Clock Pulses in an N Shot Burst (PLL0). This 6-bit unsigned value, N (default = 0) in units of Q divider output clock periods, defines how long the N shot generator is transparent to the Q divider output (that is, allows Q divider output pulses) during an N shot event associated with PLL0. An N shot event consists of a pulsing interval followed by a blank interval (no pulses). N defines the pulsing interval, whereas Gap (in Register 0x10D2, Bits[7:0]) defines the blank interval. The value of N is common to the A, AA, B, BB, C, and CC N shot generators.	0x00	R/W	Serial port clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x10D4	7	Enable PRBS Q0BB		Q0BB PRBS Enable. This bit (default = 0) enables pseudorandom binary sequence (PRBS) operation for Q0BB. When enabled, Q divider output pulses are pseudorandomly muted.	0	R/W	Serial port clock	No
			0	Disabled (default).				
			1	Enabled.				
	6	Enable Q0BB N shot		Q0BB N Shot Enable. This bit (default = 0) enables N shot (JESD204B) operation for Q0BB. When enabled, Q divider output pulses are muted until receipt of an N shot trigger (see Register 0x10D6, Bit 0).	0	R/W	Serial port clock	No
			0	Disabled (default).				
			1	Enabled.				
	5	Enable PRBS Q0B		Q0B PRBS Enable. This bit (default = 0) enables PRBS operation for Q0B. When enabled, Q divider output pulses are pseudorandomly muted.	0	R/W	Serial port clock	No
			0	Disabled (default).				
			1	Enabled.				
	4	Enable Q0B N shot		Q0B N Shot Enable. This bit (default = 0) enables N shot (JESD204B) operation for Q0B. When enabled, Q divider output pulses are muted until receipt of an N shot trigger (see Register 0x10D6, Bit 0).	0	R/W	Serial port clock	No
			0	Disabled (default).				
			1	Enabled.				
	3	Enable PRBS Q0AA		Q0AA PRBS Enable. This bit (default = 0) enables PRBS operation for Q0AA. When enabled, Q divider output pulses are pseudorandomly muted.	0	R/W	Serial port clock	No
			0	Disabled (default).				
			1	Enabled.				
	2	Enable Q0AA N shot		Q0AA N Shot Enable. This bit (default = 0) enables N shot (JESD204B) operation for Q0AA. When enabled, Q divider output pulses are muted until receipt of an N shot trigger (see Register 0x10D6, Bit 0).	0	R/W	Serial port clock	No
			0	Disabled (default).				
			1	Enabled.				
	1	Enable PRBS Q0A		Q0A PRBS Enable. This bit (default = 0) enables PRBS operation for Q0A. When enabled, Q divider output pulses are pseudorandomly muted.	0	R/W	Serial port clock	No
			0	Disabled (default).				
			1	Enabled.				
	0	Enable Q0A N shot		Q0A N Shot Enable. This bit (default = 0) enables N shot (JESD204B) operation for Q0A. When enabled, Q divider output pulses are muted until receipt of an N shot trigger (see Register 0x10D6, Bit 0).	0	R/W	Serial port clock	No
			0	Disabled (default).				
			1	Enabled.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x10D5	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	3	Enable PRBS Q0CC		Q0CC PRBS Enable. This bit (default = 0) enables pseudorandom binary sequence (PRBS) operation for Q0CC. When enabled, Q divider output pulses are pseudorandomly muted.	0	R/W	Serial port clock	No
			0	Disabled (default).				
			1	Enabled.				
	2	Enable Q0CC N shot		Q0CC N Shot Enable. This bit (default = 0) enables N shot (JESD204B) operation for Q0CC. When enabled, Q divider output pulses are muted until receipt of an N shot trigger (see Register 0x10D6, Bit 0).	0	R/W	Serial port clock	No
			0	Disabled (default).				
			1	Enabled.				
	1	Enable PRBS Q0C		Q0C PRBS Enable. This bit (default = 0) enables pseudorandom binary sequence (PRBS) operation for Q0C. When enabled, Q divider output pulses are pseudorandomly muted.	0	R/W	Serial port clock	No
			0	Disabled (default).				
			1	Enabled.				
	0	Enable Q0C N shot		Q0C N Shot Enable. This bit (default = 0) enables N shot (JESD204B) operation for Q0C. When enabled, Q divider output pulses are muted until receipt of an N shot trigger (see Register 0x10D6, Bit 0).	0	R/W	Serial port clock	No
			0	Disabled (default).				
			1	Enabled.				
0x10D6	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	4	Enable N shot retime to modulation		Enable Modulation Trigger Retiming (PLL0). This bit (only meaningful when Register 0x10D6, Bit 0 = 1) selects retimed N shot triggering relative to Q divider carrier clock edges (default) or modulation events (when modulation is active). This bit is common to the A, AA, B, BB, C, and CC N shot generators and the A, B, and C pulse width modulators.	0	R/W	Serial port clock	No
			0	Carrier clock edge N shot trigger retiming (default), which only applies to N shot enabled Q dividers.				
			1	Modulation event N shot trigger retiming, which only applies to modulation enabled Q dividers.				
	[3:1]	Reserved		Reserved.	0x0	R/W	Serial port clock	No
	0	Enable N shot retime		Enable N Shot Trigger Retiming (PLL0). This bit selects direct (default) or retimed triggering to the N shot generators and pulse width modulators. Trigger retiming stalls the trigger event such that trigger enabled Q dividers start together on a common rising edge. The trigger signal can originate from an appropriately configured Mx pin or from Register 0x2101, Bit 0. This bit is common to the A, AA, B, BB, C, and CC N shot generators and the A, B, and C pulse width modulators.	0	R/W	Serial port clock	No
			0	Direct N shot triggering (default).				
			1	Retimed N shot triggering.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x10D7	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	Bypass mute retiming Channel A		Bypass OUT0AP/OUT0AN Mute Retiming. This bit (default = 0) allows the user to bypass the mute retiming block associated with OUT0AP/OUT0AN. By default, the mute controller retimes a mute command to prevent runt pulses at the output. With the retiming block bypassed, the output mutes immediately upon receipt of a mute command.	0	R/W	Serial port clock	No
			0	Mute Retiming Active (default).				
			1	Mute Retiming Bypassed.				
	[4:3]	OUT0A driver mode		Q0A/Q0AA Divider and OUT0AP/OUT0AN Driver Connectivity. This 2-bit unsigned value (default = 0) selects the connectivity between the Q dividers and the output drivers associated with OUT0Ax.	0x0	R/W	Serial port clock	No
			0	Single divider, differential drivers (default). The OUT0Ax signal is differential. The normal output of Divider Q0A connects to the OUT0AP driver. The inverted output of Divider Q0A connects to the OUT0AN driver.				
			1	Single divider, single-ended drivers. The OUT0AP and OUT0AN signals are single-ended replicas of one another. The normal output of Divider Q0A connects to both the OUT0AP driver and the OUT0AN driver.				
			2	Dual divider, single-ended drivers. The OUT0AP and OUT0AN signals are single-ended and independent. The normal output of Divider Q0A connects to the OUT0AP driver. The normal output of Divider Q0AA connects to the OUT0AN driver. Although the user can program different divide ratios for Q0A and Q0AA, the recommendation is to program the same divide ratio to mitigate crosstalk between the OUT0AP and OUT0AN pins.				
	[2:1]	OUT0A driver current		OUT0AP/OUT0AN Output Driver Current. This 2-bit unsigned value (default = 0) selects the magnitude of the source or sink current associated with both output drivers associated with OUT0Ax.	0x0	R/W	Serial port clock	No
			0	7.5 mA (default).				
			1	12.5 mA.				
			2	15 mA.				
	0	Enable OUT0A HCSL		OUT0AP/OUT0AN Current Source or Sink Mode Select. This bit (default = 1) sets the direction of current flow for both output drivers associated with OUT0A. See the AD9546 data sheet for details about input/output termination recommendations.	1	R/W	Serial port clock	No
			0	Current sink—CML.				
			1	Current source—HCSL (default).				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x10D8	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	Bypass mute retiming Channel B		Bypass OUT0BP/OUT0BN Mute Retiming. This bit (default = 0) allows the user to bypass the mute retiming block associated with OUT0BP/OUT0BN. By default, the mute controller retimes a mute command to prevent runt pulses at the output. With the retiming block bypassed, the output mutes immediately upon receipt of a mute command.	0	R/W	Serial port clock	No
			0	Mute Retiming Active (default).				
			1	Mute Retiming Bypassed.				
	[4:3]	OUT0B driver mode		Q0B/Q0BB Divider and OUT0BP/OUT0BN Driver Connectivity. This 2-bit unsigned value (default = 0) selects the connectivity between the Q dividers and the output drivers associated with OUT0Bx.	0x0	R/W	Serial port clock	No
			0	Single divider, differential drivers (default). The OUT0Bx signal is differential. The normal output of Divider Q0B connects to the OUT0BP driver. The inverted output of Divider Q0B connects to the OUT0BN driver.				
			1	Single divider, single-ended drivers. The OUT0BP and OUT0BN signals are single-ended replicas of one another. The normal output of Divider Q0B connects to both the OUT0BP driver and the OUT0BN driver.				
			2	Dual divider, single-ended drivers. The OUT0BP and OUT0BN signals are single-ended and independent. The normal output of Divider Q0B connects to the OUT0BP driver. The normal output of Divider Q0BB connects to the OUT0BN driver. Although the user can program different divide ratios for Q0B and Q0BB, the recommendation is to program the same divide ratio to mitigate crosstalk between the OUT0BP and OUT0BN pins.				
	[2:1]	OUT0B driver current		OUT0BP/OUT0BN Output Driver Current. This 2-bit unsigned value (default = 0) selects the magnitude of the source or sink current associated with both output drivers associated with OUT0Bx.	0x0	R/W	Serial port clock	No
			0	7.5 mA (default).				
			1	12.5 mA.				
			2	15 mA.				
	0	Enable OUT0B HCSL		OUT0BP/OUT0BN Current Source or Sink Mode Select. This bit (default = 1) sets the direction of current flow for both output drivers associated with OUT0B. See the AD9546 data sheet for details about input/output termination recommendations.	1	R/W	Serial port clock	No
			0	Current sink—CML.				
			1	Current source—HCSL (default).				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x10D9	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	Bypass mute retiming Channel C		Bypass OUT0CP/OUT0CN Mute Retiming. This bit (default = 0) allows the user to bypass the mute retiming block associated with OUT0CP/OUT0CN. By default, the mute controller retimes a mute command to prevent runt pulses at the output. With the retiming block bypassed, the output mutes immediately upon receipt of a mute command.	0	R/W	Serial port clock	No
			0	Mute Retiming Active (default).				
			1	Mute Retiming Bypassed.				
	[4:3]	OUT0C driver mode		Q0C/Q0CC Divider and OUT0CP/OUT0CN Driver Connectivity. This 2-bit unsigned value (default = 0) selects the connectivity between the Q dividers and the output drivers associated with OUT0Cx.	0x0	R/W	Serial port clock	No
			0	Single divider, differential drivers (default). The OUT0C signal is differential. The normal output of Divider Q0C connects to the OUT0CP driver. The inverted output of Divider Q0C connects to the OUT0CN driver.				
			1	Single divider, single-ended drivers. The OUT0CP and OUT0CN signals are single-ended replicas of one another. The normal output of Divider Q0C connects to both the OUT0CP driver and the OUT0CN driver.				
			2	Dual divider, single-ended drivers. The OUT0CP and OUT0CN signals are single-ended and independent. The normal output of Divider Q0C connects to the OUT0CP driver. The normal output of Divider Q0CC connects to the OUT0CN driver. Although the user can program different divide ratios for Q0C and Q0CC, the recommendation is to program the same divide ratio to mitigate crosstalk between the OUT0CP and OUT0CN pins.				
	[2:1]	OUT0C Driver Current		OUT0BP/OUT0BN Output Driver Current. This 2-bit unsigned value (default = 0) selects the magnitude of the source or sink current associated with both output drivers associated with OUT0Cx.	0x0	R/W	Serial port clock	No
			0	7.5 mA (default).				
			1	12.5 mA.				
			2	15 mA.				
	0	Enable OUT0C HCSL		OUT0BP/OUT0BN Current Source or Sink Mode Select. This bit (default = 1) sets the direction of current flow for both output drivers associated with OUT0C. See the AD9546 data sheet for details about input/output termination recommendations.	1	R/W	Serial port clock	No
			0	Current sink—CML.				
			1	Current source—HCSL (default).				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x10DA	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	3	Enable SYSCLK Channel 0C		OUT0C Q Divider Clock Source Select. This bit (default = 0) selects the input clock source to both the Q0C and Q0CC divider.	0	R/W	Core clock	No
			0	1/2 APLL0 VCO Frequency (default).				
			1	System Clock PLL VCO Frequency.				
	2	Enable SYSCLK Channel 0B		OUT0B Q Divider Clock Source Select. This bit (default = 0) selects the input clock source to both the Q0B and Q0BB divider.	0	R/W	Core clock	No
			0	1/2 APLL0 VCO Frequency (default).				
			1	System Clock PLL VCO Frequency.				
	1	Enable SYSCLK Channel 0A		OUT0A Q Divider Clock Source Select. This bit (default = 0) selects the input clock source to both the Q0A and Q0AA divider.	0	R/W	Core clock	No
			0	1/2 APLL0 VCO Frequency (default).				
			1	System Clock PLL VCO Frequency.				
	0	Enable SYSCLK sync mask		SYSCLK Driven Q Divider Synchronization Mask Enable (PLL0). This bit (default = 0) allows the user to prevent synchronization events from disrupting the outputs of all Q dividers associated with PLL0 having the system clock selected as the input clock source (see Bits[3:1]). This feature is particularly useful when an output is the clock source to a microprocessor, for example. In this case, the synchronization mask prevents disruption of the microprocessor clock, which can otherwise occur following a synchronization event. The system clock PLL must be configured and stable prior to setting this bit.	0	R/W	Core clock	No
			0	SYSCLK Synchronization Mask Disabled (default).				
			1	SYSCLK Synchronization Mask Enabled.				
0x10DB	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	3	Enable Channel 0 coupled mode sync		Enable Channel 0 Coupled Mode Sync. This bit is normally set to zero. If Logic 1, this bit allows output autosynchronization to occur on the slave channel in cascaded DPLL mode before the master DPLL locks and synchronizes.	0	R/W	Core clock	No
	2	Enable DPLL0 reference sync		Distribution Synchronization on Reference Input Edge (PLL0). This bit (default = 0) allows the user to synchronize the outputs associated with PLL0 coincident with the rising edge of the input reference signal to DPLL0. The reference synchronization feature requires an active hitless profile for DPLL0.	0	R/W	Core clock	No
			0	Reference Synchronization Disabled (default).				
			1	Reference Synchronization Enabled.				
	[1:0]	Autosync mode		Distribution Autosynchronization Mode (PLL0). This 2-bit unsigned value (default = 0) selects one of the synchronization modes for the distribution outputs associated with PLL0. The output drivers do not toggle until a synchronization event occurs.	0x0	R/W	Core clock	No
			0	Manual Distribution Synchronization (default). Manual distribution synchronization is via one of the following: Register 0x2000, Bit 3 for all outputs; Register 0x2101, Bit 3 for outputs associated with PLL0; or implementation of one of the previous items via an appropriately configured Mx control pin.				
			1	Immediate Distribution Synchronization (the system clock PLL must be locked).				
			2	Distribution Synchronization on DPLL0 Phase Lock.				
			3	Distribution Synchronization on DPLL0 Frequency Lock.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x10DC	7	Mask OUT0CN auto unmute		OUT0CN Automatic Unmute Mask. This bit (default = 0) allows the user to opt out of (that is, mask) automatic unmute of the OUT0CN driver. This functionality only applies when automatic unmuting is in effect (that is, Register 0x10DC, Bits[1:0] > 0).	0	R/W	Core clock	No
			0	Normal Automatic Unmute Operation.				
			1	No Automatic Unmute.				
	6	Mask OUT0CP auto unmute		OUT0CP Automatic Unmute Mask. This bit (default = 0) allows the user to opt out of (that is, mask) automatic unmute of the OUT0CP driver. This functionality only applies when automatic unmuting is in effect (that is, Register 0x10DC, Bits[1:0] > 0).	0	R/W	Core clock	No
			0	Normal Automatic Unmute Operation.				
			1	No Automatic Unmute.				
	5	Mask OUT0BN auto unmute		OUT0BN Automatic Unmute Mask. This bit (default = 0) allows the user to opt out of (that is, mask) automatic unmute of the OUT0BN driver. This functionality only applies when automatic unmuting is in effect (that is, Register 0x10DC, Bits[1:0] > 0).	0	R/W	Core clock	No
			0	Normal Automatic Unmute Operation.				
			1	No Automatic Unmute.				
	4	Mask OUT0BP auto unmute		OUT0BP Automatic Unmute Mask. This bit (default = 0) allows the user to opt out of (that is, mask) automatic unmute of the OUT0BP driver. This functionality only applies when automatic unmuting is in effect (that is, Register 0x10DC, Bits[1:0] > 0).	0	R/W	Core clock	No
			0	Normal Automatic Unmute Operation.				
			1	No Automatic Unmute.				
	3	Mask OUT0AN auto unmute		OUT0AN Automatic Unmute Mask. This bit (default = 0) allows the user to opt out of (that is, mask) automatic unmute of the OUT0AN driver. This functionality only applies when automatic unmuting is in effect (that is, Register 0x10DC, Bits[1:0] > 0).	0	R/W	Core clock	No
			0	Normal Automatic Unmute Operation.				
			1	No Automatic Unmute.				
	2	Mask OUT0AP auto unmute		OUT0AP Automatic Unmute Mask. This bit (default = 0) allows the user to opt out of (that is, mask) automatic unmute of the OUT0AP driver. This functionality only applies when automatic unmuting is in effect (that is, Register 0x10DC, Bits[1:0] > 0).	0	R/W	Core clock	No
			0	Normal Automatic Unmute Operation.				
			1	No Automatic Unmute.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[1:0]	DPLL0 auto unmute mode		Distribution Unmute Mode Select (PLL0). This 2-bit unsigned value (default = 0) selects the mode of distribution driver unmute functionality for outputs associated with PLL0.	0x0	R/W	Core clock	No
			0	Immediate Distribution Unmute (default). Occurs immediately upon release of a synchronization request.				
			1	Distribution Unmute Subject to Hitless Profile Activation. Unmute occurs upon release of a synchronization request, but subject to activation of a hitless DPLL0 profile.				
			2	Distribution Unmute Subject to DPLL0 Phase Lock. Unmute occurs upon release of a synchronization request, but subject to DPLL0 phase lock (applies only to a hitless DPLL0 profile).				
			3	Distribution Unmute Subject to DPLL0 Frequency Lock. Unmute occurs upon release of a synchronization request, but subject to DPLL0 frequency lock (applies only to a hitless DPLL0 profile).				

DISTRIBUTION PARAMETERS: Q0A—REGISTER 0x1100 TO REGISTER 0x1108

Table 59. Distribution Parameters: Q0A Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1100	[7:0]	Q0A Divide Ratio[7:0]		Q0A Integer Divide Ratio. This 32-bit unsigned value, Q0A_int (default = 0), is the integer portion of the divide factor (QDIV0A) for Q Divider Q0A. 0 and 1 are invalid values for Q0A_int. Because the default value is 0, the user must program a valid value. When using the associated N shot generator or pulse width modulator, the following constraint applies: Q0A_int ≥ 8.	0x00	R/W	Core clock	No
0x1101	[7:0]	Q0A Divide Ratio[15:8]		Continuation of the Q0A divide ratio bit field. See the Q0A Divide Ratio[7:0] description.	0x00	R/W	Core clock	No
0x1102	[7:0]	Q0A Divide Ratio[23:16]		Continuation of the Q0A divide ratio bit field. See the Q0A Divide Ratio[7:0] description.	0x00	R/W	Core clock	No
0x1103	[7:0]	Q0A Divide Ratio[31:24]		Continuation of the Q0A divide ratio bit field. See the Q0A Divide Ratio[7:0] description.	0x00	R/W	Core clock	No
0x1104	[7:0]	Q0A Phase Offset[7:0]		Q0A Phase Offset or Pulse Width Magnitude. This 33-bit unsigned value, Phase Offset (default = 0), establishes either a phase offset or a pulse width for the Q0A divider. The maximum usable value of Phase Offset ($OFST_{MAX}$) is as follows: $OFST_{MAX} = 2 \times QDIV0A - 1$ where *QDIV0A* is the total divide ratio of Q Divider Q0A. The Q divider interprets the value of Phase Offset differently depending on whether phase offset or pulse width mode is in effect per Register 0x1108, Bit 4. Two categories of phase offset activation exist: initial and subsequent. An initial phase offset activates immediately following a device power-up or a reset, followed by completion of a distribution synchronization request. Subsequent phase offsets result from completed distribution synchronization requests that occur after completion of an initial phase offset.	0x00	R/W	Core clock	No
0x1105	[7:0]	Q0A Phase Offset[15:8]		Continuation of the Q0A phase offset bit field. See the Q0A Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x1106	[7:0]	Q0A Phase Offset[23:16]		Continuation of the Q0A phase offset bit field. See the Q0A Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x1107	[7:0]	Q0A Phase Offset[31:24]		Continuation of the Q0A phase offset bit field. See the Q0A Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x1108	7	Reserved		Reserved.	0	R	Live	No
	6	Q0A Phase Offset[32]		Continuation of the Q0A phase offset bit field. See the Q0A Phase Offset[7:0] description.	0	R/W	Core clock	No
	5	Enable half divide		Q0A Half Integer Enable. This bit (default = 0) adds 0 or 0.5 to the integer portion of Q Divider Q0A.	0	R/W	Core clock	No
			0	QDIV0A = Q0A_int.				
			1	QDIV0A = Q0A_int + 0.5.				
	4	Enable pulse width control		Q0A Phase Offset or Pulse Width Mode Select. This bit (default = 0) selects between phase offset mode and pulse width mode with regard to the interpretation of the value of Phase Offset in Register 0x1104. The value of Phase Offset relates to the total division factor, QDIV0A, of the Q divider (QDIV0A includes the integer and half integer parts).	0	R/W	Core clock	No
			1	Pulse Width Mode. Pulse width mode controls the duty cycle of the output clock signal. Duty cycle resolution, DC_0, is a function of QDIV0A as DC_0 (%) = 50/QDIV0A. Duty cycle relates to Phase Offset as $DC_0 \times$ Phase Offset. For example, given QDIV0A = 101.5 and Phase Offset = 10, then DC_0 = 0.493% and duty cycle = 4.93%. Duty cycle constitutes a fraction of one Q divider output cycle from rising edge to falling edge. Subsequent phase offsets do not cause activation of the phase slew limiting function of the Q divider.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
			0	Phase Offset Mode (default). Phase resolution, θ_0, is a function of QDIV0A as θ_0 (degrees)= 180/QDIV0A. Phase, θ, is a function of Phase Offset as $\theta = \theta_0 \times$ Phase Offset. For example, given QDIV0A = 101.5 and Phase Offset = 10, then $\theta_0 = 1.773°$ and $\theta = 17.73°$. Subsequent phase offsets activate the phase slew limiting function of the Q divider.				
	3	Q0A phase slew mode		Q0A Phase Slew Mode. This bit (default = 0) selects between phase slewing modes.	0	R/W	Core clock	No
			0	Lag Mode (default). Phase slewing steps (Δθ) are always in the −Δθ/Δt direction. Thus, while phase slewing, the output frequency decreases in accordance with the sign of Δθ/Δt.				
			1	Minimum Steps Mode. Phase slewing steps (Δθ) are in the direction requiring the least number of steps to accomplish the specified phase offset. Thus, while phase slewing, the output frequency increases or decreases in accordance with the sign of Δθ/Δt necessary to satisfy the least number of steps requirement.				
	[2:0]	Maximum phase slew step		Q0A Maximum Phase Slew Step. This 3-bit value (default = 7) selects a maximum phase step size (θ_{MAX}) for phase slewing, where θ_{MAX} relates to the total division factor, QDIV0A, of the Q divider (QDIV0A includes the integer and half integer parts).	0x7	R/W	Core clock	No
			0	1 Q divider input half-cycle. θ_{MAX} = 180/QDIV0A (degrees).				
			1	1 Q divider input cycle. θ_{MAX} = 90/QDIV0A (degrees).				
			2	~1/32 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV0A/16)/QDIV0A. The user must ensure floor(QDIV0A/16) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			3	~1/16 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV0A/8)/QDIV0A. The user must ensure floor(QDIV0A/8) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			4	~1/8 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV0A/4)/QDIV0A. The user must ensure floor(QDIV0A/4) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			5	~1/4 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV0A/2)/QDIV0A. The user must ensure floor(QDIV0A/2) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			6	~1/2 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV0A)/QDIV0A. The user must ensure floor(QDIV0A) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			7	~1 Q divider output cycle (default). θ_{MAX} (degrees) = 180 × (2 × QDIV0A − 1)/QDIV0A. This setting results in the phase slewing function being effectively disabled and causes phase slewing to execute as though Bit 3 = 0 (even when Bit 3 = 1).				

DISTRIBUTION PARAMETERS: Q0AA—REGISTER 0x1109 TO REGISTER 0x1111

Table 60. Distribution Parameters: Q0AA Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1109	[7:0]	Q0AA Divide Ratio[7:0]		Q0AA Integer Divide Ratio. This 32-bit unsigned value, Q0AA_int (default = 0), is the integer portion of the divide factor (QDIV0AA) for Q Divider Q0AA. 0 and 1 are invalid values for Q0AA_int. Because the default value is 0, the user must program a valid value. When using the associated N shot generator or pulse width modulator, the following constraint applies: Q0AA_int ≥ 8.	0x00	R/W	Core clock	No
0x110A	[7:0]	Q0AA Divide Ratio[15:8]		Continuation of the Q0AA divide ratio bit field. See the Q0AA Divide Ratio[7:0] description.	0x00	R/W	Core clock	No
0x110B	[7:0]	Q0AA Divide Ratio[23:16]		Continuation of the Q0AA divide ratio bit field. See the Q0AA Divide Ratio[7:0] description.	0x00	R/W	Core clock	No
0x110C	[7:0]	Q0AA Divide Ratio[31:24]		Continuation of the Q0AA divide ratio bit field. See the Q0AA Divide Ratio[7:0] description.	0x00	R/W	Core clock	No
0x110D	[7:0]	Q0AA Phase Offset[7:0]		Q0AA Phase Offset or Pulse Width Magnitude. This 33-bit unsigned value, Phase Offset (default = 0), establishes either a phase offset or a pulse width for the Q0AA divider. The maximum usable value of Phase Offset ($OFST_{MAX}$) is as follows: $OFST_{MAX} = 2 \times QDIV0AA - 1$ where *QDIV0AA* is the total divide ratio of Q Divider Q0AA. The Q divider interprets the value of Phase Offset differently depending on whether phase offset or pulse width mode is in effect per Register 0x1111, Bit 4. Two categories of phase offset activation exist: initial and subsequent. An initial phase offset activates immediately following a device power-up or a reset, followed by completion of a distribution synchronization request. Subsequent phase offsets result from completed distribution synchronization requests that occur after completion of an initial phase offset.	0x00	R/W	Core clock	No
0x110E	[7:0]	Q0AA Phase Offset[15:8]		Continuation of the Q0AA phase offset bit field. See the Q0AA Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x110F	[7:0]	Q0AA Phase Offset[23:16]		Continuation of the Q0AA phase offset bit field. See the Q0AA Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x1110	[7:0]	Q0AA Phase Offset[31:24]		Continuation of the Q0AA phase offset bit field. See the Q0AA Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x1111	7	Reserved		Reserved.	0	R	Live	No
	6	Q0AA Phase Offset[32]		Continuation of the Q0AA phase offset bit field. See the Q0AA Phase Offset[7:0] description.	0	R/W	Core clock	No
	5	Enable half divide		Q0AA Half Integer Enable. This bit (default = 0) adds 0 or 0.5 to the integer portion of Q Divider Q0AA.	0	R/W	Core clock	No
			0	QDIV0AA = Q0AA_int.				
			1	QDIV0AA = Q0AA_int + 0.5.				
	4	Enable pulse width control		Q0AA Phase Offset or Pulse Width Mode Select. This bit (default = 0) selects between phase offset mode and pulse width mode with regard to the interpretation of the value of Phase Offset in Register 0x110D. The value of Phase Offset relates to the total division factor, QDIV0AA, of the Q divider (QDIV0AA includes the integer and half integer parts).	0	R/W	Core clock	No
			1	Pulse Width Mode. Pulse width mode controls the duty cycle of the output clock signal. Duty cycle resolution, DC_0, is a function of QDIV0AA as DC_0 (%) = 50/QDIV0AA. Duty cycle relates to Phase Offset as $DC_0 \times$ Phase Offset. For example, given QDIV0AA = 101.5 and Phase Offset = 10, then DC_0 = 0.493% and duty cycle = 4.93%. Duty cycle constitutes a fraction of one Q divider output cycle from rising edge to falling edge. Subsequent phase offsets do not cause activation of the phase slew limiting function of the Q divider.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
			0	Phase Offset Mode (default). Phase resolution, θ_0, is a function of QDIV0AA as θ_0 (degrees)= 180/QDIV0AA. Phase, θ, is a function of Phase Offset as $\theta = \theta_0 \times$ Phase Offset. For example, given QDIV0AA = 101.5 and Phase Offset = 10, then $\theta_0 = 1.773°$ and $\theta = 17.73°$. Subsequent phase offsets activate the phase slew limiting function of the Q divider.				
	3	Q0AA phase slew mode		Q0AA Phase Slew Mode. This bit (default = 0) selects between phase slewing modes.	0	R/W	Core clock	No
			0	Lag Mode (default). Phase slewing steps (Δθ) are always in the −Δθ/Δt direction. Thus, while phase slewing, the output frequency decreases in accordance with the sign of Δθ/Δt.				
			1	Minimum Steps Mode. Phase slewing steps (Δθ) are in the direction requiring the least number of steps to accomplish the specified phase offset. Thus, while phase slewing, the output frequency increases or decreases in accordance with the sign of Δθ/Δt necessary to satisfy the least number of steps requirement.				
	[2:0]	Maximum phase slew step		Q0AA Maximum Phase Slew Step. This 3-bit value (default = 7) selects a maximum phase step size (θ_{MAX}) for phase slewing, where θ_{MAX} relates to the total division factor, QDIV0AA, of the Q divider (QDIV0AA includes the integer and half integer parts).	0x7	R/W	Core clock	No
			0	1 Q divider input half-cycle. θ_{MAX} = 180/QDIV0AA (degrees).				
			1	1 Q divider input cycle. θ_{MAX} = 90/QDIV0AA (degrees).				
			2	~1/32 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV0AA/16)/QDIV0AA. The user must ensure floor(QDIV0AA/16) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			3	~1/16 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV0AA/8)/QDIV0AA. The user must ensure floor(Q0AA/8) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			4	~1/8 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV0AA/4)/QDIV0AA. The user must ensure floor(QDIV0AA/4) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			5	~1/4 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV0AA/2)/QDIV0AA. The user must ensure floor(QDIV0AA/2) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			6	~1/2 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV0AA)/QDIV0AA. The user must ensure floor(QDIV0AA) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			7	~1 Q divider output cycle (default). θ_{MAX} (degrees) = 180 × (2 × QDIV0AA − 1)/QDIV0AA. This setting results in the phase slewing function being effectively disabled and causes phase slewing to execute as though Bit 3 = 0 (even when Bit 3 = 1).				

DISTRIBUTION PARAMETERS: Q0B—REGISTER 0x1112 TO REGISTER 0x111A

Table 61. Distribution Parameters: Q0B Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1112	[7:0]	Q0B Divide Ratio[7:0]		Q0B Integer Divide Ratio. This 32-bit unsigned value, Q0B_int (default = 0), is the integer portion of the divide factor (QDIV0B) for Q Divider Q0B. 0 and 1 are invalid values for Q0B_int. Because the default value is 0, the user must program a valid value. When using the associated N shot generator or pulse width modulator, the following constraint applies: Q0B_int ≥ 8.	0x00	R/W	Core clock	No
0x1113	[7:0]	Q0B Divide Ratio[15:8]		Continuation of the Q0B divide ratio bit field. See the Q0B Divide Ratio[7:0] description.	0x00	R/W	Core clock	No
0x1114	[7:0]	Q0B Divide Ratio[23:16]		Continuation of the Q0B divide ratio bit field. See the Q0B Divide Ratio[7:0] description.	0x00	R/W	Core clock	No
0x1115	[7:0]	Q0B Divide Ratio[31:24]		Continuation of the Q0B divide ratio bit field. See the Q0B Divide Ratio[7:0] description.	0x00	R/W	Core clock	No
0x1116	[7:0]	Q0B Phase Offset[7:0]		Q0B Phase Offset or Pulse Width Magnitude. This 33-bit unsigned value, Phase Offset (default = 0), establishes either a phase offset or a pulse width for the Q0B divider. The maximum usable value of Phase Offset ($OFST_{MAX}$) is as follows: $OFST_{MAX} = 2 \times QDIV0B - 1$ where *QDIV0B* is the total divide ratio of Q Divider Q0B. The Q divider interprets the value of Phase Offset differently depending on whether phase offset or pulse width mode is in effect per Register 0x111A, Bit 4. Two categories of phase offset activation exist: initial and subsequent. An initial phase offset activates immediately following a device power-up or a reset, followed by completion of a distribution synchronization request. Subsequent phase offsets result from completed distribution synchronization requests that occur after completion of an initial phase offset.	0x00	R/W	Core clock	No
0x1117	[7:0]	Q0B Phase Offset[15:8]		Continuation of the Q0B phase offset bit field. See the Q0B Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x1118	[7:0]	Q0B Phase Offset[23:16]		Continuation of the Q0B phase offset bit field. See the Q0B Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x1119	[7:0]	Q0B Phase Offset[31:24]		Continuation of the Q0B phase offset bit field. See the Q0B Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x111A	7	Reserved		Reserved.	0	R	Live	No
	6	Q0B Phase Offset[32]		Continuation of the Q0B phase offset bit field. See the Q0B Phase Offset[7:0] description.	0	R/W	Core clock	No
	5	Enable half divide		Q0B Half Integer Enable. This bit (default = 0) adds 0 or 0.5 to the integer portion of Q Divider Q0B.	0	R/W	Core clock	No
			0	QDIV0B = Q0B_int.				
			1	QDIV0B = Q0B_int + 0.5.				
	4	Enable pulse width control		Q0B Phase Offset or Pulse Width Mode Select. This bit (default = 0) selects between phase offset mode and pulse width mode with regard to the interpretation of the value of Phase Offset in Register 0x1116. The value of Phase Offset relates to the total division factor, QDIV0B, of the Q divider (QDIV0B includes the integer and half integer parts).	0	R/W	Core clock	No
			1	Pulse Width Mode. Pulse width mode controls the duty cycle of the output clock signal. Duty cycle resolution, DC_0, is a function of QDIV0B as DC_0 (%) = 50/QDIV0B. Duty cycle relates to Phase Offset as $DC_0 \times$ Phase Offset. For example, given QDIV0B = 101.5 and Phase Offset = 10, then DC_0 = 0.493% and duty cycle = 4.93%. Duty cycle constitutes a fraction of one Q divider output cycle from rising edge to falling edge. Subsequent phase offsets do not cause activation of the phase slew limiting function of the Q divider.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
			0	Phase Offset Mode (default). Phase resolution, θ_0, is a function of QDIV0B as θ_0 (degrees)= 180/QDIV0B. Phase, θ, is a function of Phase Offset as $\theta = \theta_0 \times$ Phase Offset. For example, given QDIV0B = 101.5 and Phase Offset = 10, then $\theta_0 = 1.773°$ and $\theta = 17.73°$. Subsequent phase offsets activate the phase slew limiting function of the Q divider.				
	3	Q0B phase slew mode		Q0B Phase Slew Mode. This bit (default = 0) selects between phase slewing modes.	0	R/W	Core clock	No
			0	Lag Mode (default). Phase slewing steps (Δθ) are always in the −Δθ/Δt direction. Thus, while phase slewing, the output frequency decreases in accordance with the sign of Δθ/Δt.				
			1	Minimum Steps Mode. Phase slewing steps (Δθ) are in the direction requiring the least number of steps to accomplish the specified phase offset. Thus, while phase slewing, the output frequency increases or decreases in accordance with the sign of Δθ/Δt necessary to satisfy the least number of steps requirement.				
	[2:0]	Maximum phase slew step		Q0B Maximum Phase Slew Step. This 3-bit value (default = 7) selects a maximum phase step size (θ_{MAX}) for phase slewing, where θ_{MAX} relates to the total division factor, QDIV0B, of the Q divider (QDIV0B includes the integer and half integer parts).	0x7	R/W	Core clock	No
			0	1 Q divider input half-cycle. θ_{MAX} = 180/QDIV0B (degrees).				
			1	1 Q divider input cycle. θ_{MAX} = 90/QDIV0B (degrees).				
			2	~1/32 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV0B/16)/QDIV0B. The user must ensure floor(QDIV0B/16) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			3	~1/16 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV0B/8)/QDIV0B. The user must ensure floor(QDIV0B/8) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			4	~1/8 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV0B/4)/QDIV0B. The user must ensure floor(QDIV0B/4) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			5	~1/4 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV0B/2)/QDIV0B. The user must ensure floor(QDIV0B/2) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			6	~1/2 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV0B)/QDIV0B. The user must ensure floor(QDIV0B) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			7	~1 Q divider output cycle (default). θ_{MAX} (degrees) = 180 × (2 × QDIV0B − 1)/QDIV0B. This setting results in the phase slewing function being effectively disabled and causes phase slewing to execute as though Bit 3 = 0 (even when Bit 3 = 1).				

DISTRIBUTION PARAMETERS: Q0BB—REGISTER 0x111B TO REGISTER 0x1123

Table 62. Distribution Parameters: Q0BB Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x111B	[7:0]	Q0BB Divide Ratio[7:0]		Q0BB Integer Divide Ratio. This 32-bit unsigned value, Q0BB_int (default = 0), is the integer portion of the divide factor (QDIV0BB) for Q Divider Q0BB. 0 and 1 are invalid values for Q0BB_int. Because the default value is 0, the user must program a valid value. When using the associated N shot generator or pulse width modulator, the following constraint applies: Q0BB_int ≥ 8.	0x00	R/W	Core clock	No
0x111C	[7:0]	Q0BB Divide Ratio[15:8]		Continuation of the Q0BB divide ratio bit field. See the Q0BB Divide Ratio[7:0] description.	0x00	R/W	Core clock	No
0x111D	[7:0]	Q0BB Divide Ratio[23:16]		Continuation of the Q0BB divide ratio bit field. See the Q0BB Divide Ratio[7:0] description.	0x00	R/W	Core clock	No
0x111E	[7:0]	Q0BB Divide Ratio[31:24]		Continuation of the Q0BB divide ratio bit field. See the Q0BB Divide Ratio[7:0] description.	0x00	R/W	Core clock	No
0x111F	[7:0]	Q0BB Phase Offset[7:0]		Q0BB Phase Offset or Pulse Width Magnitude. This 33-bit unsigned value, Phase Offset (default = 0), establishes either a phase offset or a pulse width for the Q0BB divider. The maximum usable value of Phase Offset ($OFST_{MAX}$) is as follows: $OFST_{MAX} = 2 \times QDIV0BB - 1$ where *QDIV0BB* is the total divide ratio of Q Divider Q0BB. The Q divider interprets the value of Phase Offset differently depending on whether phase offset or pulse width mode is in effect per Register 0x1123, Bit 4. Two categories of phase offset activation exist: initial and subsequent. An initial phase offset activates immediately following a device power-up or a reset, followed by completion of a distribution synchronization request. Subsequent phase offsets result from completed distribution synchronization requests that occur after completion of an initial phase offset.	0x00	R/W	Core clock	No
0x1120	[7:0]	Q0BB Phase Offset[15:8]		Continuation of the Q0BB phase offset bit field. See the Q0BB Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x1121	[7:0]	Q0BB Phase Offset[23:16]		Continuation of the Q0BB phase offset bit field. See the Q0BB Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x1122	[7:0]	Q0BB Phase Offset[31:24]		Continuation of the Q0BB phase offset bit field. See the Q0BB Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x1123	7	Reserved		Reserved.	0	R	Live	No
	6	Q0BB Phase Offset[32]		Continuation of the Q0BB phase offset bit field. See the Q0BB Phase Offset[7:0] description.	0	R/W	Core clock	No
	5	Enable half divide		Q0BB Half Integer Enable. This bit (default = 0) adds 0 or 0.5 to the integer portion of Q Divider Q0BB.	0	R/W	Core clock	No
			0	QDIV0BB = Q0BB_int.				
			1	QDIV0BB = Q0BB_int + 0.5.				
	4	Enable PW Control		Q0BB Phase Offset or Pulse Width Mode Select. This bit (default = 0) selects between phase offset mode and pulse width mode with regard to the interpretation of the value of Phase Offset in Register 0x111F. The value of Phase Offset relates to the total division factor, QDIV0BB, of the Q divider (QDIV0BB includes the integer and half integer parts).	0	R/W	Core clock	No
			1	Pulse Width Mode. Pulse width mode controls the duty cycle of the output clock signal. Duty cycle resolution, DC_0, is a function of QDIV0BB as DC_0 (%) = 50/QDIV0BB. Duty cycle relates to Phase Offset as $DC_0 \times$ Phase Offset. For example, given QDIV0BB = 101.5 and Phase Offset = 10, then DC_0 = 0.493% and duty cycle = 4.93%. Duty cycle constitutes a fraction of one Q divider output cycle from rising edge to falling edge. Subsequent phase offsets do not cause activation of the phase slew limiting function of the Q divider.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
			0	Phase Offset Mode (default). Phase resolution, θ_0, is a function of QDIV0BB as θ_0 (degrees)= 180/QDIV0BB. Phase, θ, is a function of Phase Offset as $\theta = \theta_0 \times$ Phase Offset. For example, given QDIV0BB = 101.5 and Phase Offset = 10, then $\theta_0 = 1.773°$ and $\theta = 17.73°$. Subsequent phase offsets activate the phase slew limiting function of the Q divider.				
	3	Q0BB phase slew mode		Q0BB Phase Slew Mode. This bit (default = 0) selects between phase slewing modes.	0	R/W	Core clock	No
			0	Lag Mode (default). Phase slewing steps (Δθ) are always in the −Δθ/Δt direction. Thus, while phase slewing, the output frequency decreases in accordance with the sign of Δθ/Δt.				
			1	Minimum Steps Mode. Phase slewing steps (Δθ) are in the direction requiring the least number of steps to accomplish the specified phase offset. Thus, while phase slewing, the output frequency increases or decreases in accordance with the sign of Δθ/Δt necessary to satisfy the least number of steps requirement.				
	[2:0]	Maximum phase slew step		Q0BB Maximum Phase Slew Step. This 3-bit value (default = 7) selects a maximum phase step size (θ_{MAX}) for phase slewing, where θ_{MAX} relates to the total division factor, QDIV0BB, of the Q divider (QDIV0BB includes the integer and half integer parts).	0x7	R/W	Core clock	No
			0	1 Q divider input half-cycle. θ_{MAX} = 180/QDIV0BB (degrees).				
			1	1 Q divider input cycle. θ_{MAX} = 90/QDIV0BB (degrees).				
			2	~1/32 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV0BB/16)/QDIV0BB. The user must ensure floor(QDIV0BB/16) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			3	~1/16 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV0BB/8)/QDIV0BB. The user must ensure floor(QDIV0BB/8) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			4	~1/8 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV0BB/4)/QDIV0BB. The user must ensure floor(QDIV0BB/4) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			5	~1/4 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV0BB/2)/QDIV0BB. The user must ensure floor(QDIV0BB/2) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			6	~1/2 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV0BB)/QDIV0BB. The user must ensure floor(QDIV0BB) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			7	~1 Q divider output cycle (default). θ_{MAX} (degrees) = 180 × (2 × QDIV0BB − 1)/QDIV0BB. This setting results in the phase slewing function being effectively disabled and causes phase slewing to execute as though Bit 3 = 0 (even when Bit 3 = 1).				

DISTRIBUTION PARAMETERS: Q0C—REGISTER 0x1124 TO REGISTER 0x112C

Table 63. Distribution Parameters: Q0C Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1124	[7:0]	Q0C Divide Ratio[7:0]		Q0C Integer Divide Ratio. This 32-bit unsigned value, Q0C_int (default = 0), is the integer portion of the divide factor (QDIV0C) for Q Divider Q0C. 0 and 1 are invalid values for Q0C_int. Because the default value is 0, the user must program a valid value. When using the associated N shot generator or pulse width modulator, the following constraint applies: Q0C_int ≥ 8.	0x00	R/W	Core clock	No
0x1125	[7:0]	Q0C Divide Ratio[15:8]		Continuation of the Q0C divide ratio bit field. See the Q0C Divide Ratio[7:0] description.	0x00	R/W	Core clock	No
0x1126	[7:0]	Q0C Divide Ratio[23:16]		Continuation of the Q0C divide ratio bit field. See the Q0C Divide Ratio[7:0] description.	0x00	R/W	Core clock	No
0x1127	[7:0]	Q0C Divide Ratio[31:24]		Continuation of the Q0C divide ratio bit field. See the Q0C Divide Ratio[7:0] description.	0x00	R/W	Core clock	No
0x1128	[7:0]	Q0C Phase Offset[7:0]		Q0C Phase Offset or Pulse Width Magnitude. This 33-bit unsigned value, Phase Offset (default = 0), establishes either a phase offset or a pulse width for the Q0C divider. The maximum usable value of Phase Offset ($OFST_{MAX}$) is as follows: $OFST_{MAX} = 2 \times QDIV0C - 1$ where *QDIV0C* is the total divide ratio of Q Divider Q0C. The Q divider interprets the value of Phase Offset differently depending on whether phase offset or pulse width mode is in effect per Register 0x112C, Bit 4. Two categories of phase offset activation exist: initial and subsequent. An initial phase offset activates immediately following a device power-up or a reset, followed by completion of a distribution synchronization request. Subsequent phase offsets result from completed distribution synchronization requests that occur after completion of an initial phase offset.	0x00	R/W	Core clock	No
0x1129	[7:0]	Q0C Phase Offset[15:8]		Continuation of the Q0C phase offset bit field. See the Q0C Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x112A	[7:0]	Q0C Phase Offset[23:16]		Continuation of the Q0C phase offset bit field. See the Q0C Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x112B	[7:0]	Q0C Phase Offset[31:24]		Continuation of the Q0C phase offset bit field. See the Q0C Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x112C	7	Reserved		Reserved.	0	R	Live	No
	6	Q0C Phase Offset[32]		Continuation of the Q0C phase offset bit field. See the Q0C Phase Offset[7:0] description.	0	R/W	Core clock	No
	5	Enable half divide		Q0C Half Integer Enable. This bit (default = 0) adds 0 or 0.5 to the integer portion of Q Divider Q0C.	0	R/W	Core clock	No
			0	QDIV0C = Q0C_int.				
			1	QDIV0C = Q0C_int + 0.5.				
	4	Enable pulse width control		Q0C Phase Offset or Pulse Width Mode Select. This bit (default = 0) selects between phase offset mode and pulse width mode with regard to the interpretation of the value of Phase Offset in Register 0x1128. The value of Phase Offset relates to the total division factor, QDIV0C, of the Q divider (QDIV0C includes the integer and half integer parts).	0	R/W	Core clock	No
			1	Pulse Width Mode. Pulse width mode controls the duty cycle of the output clock signal. Duty cycle resolution, DC_0, is a function of QDIV0C as DC_0 (%) = 50/QDIV0C. Duty cycle relates to Phase Offset as $DC_0 \times$ Phase Offset. For example, given QDIV0C = 101.5 and Phase Offset = 10, then DC_0 = 0.493% and duty cycle = 4.93%. Duty cycle constitutes a fraction of one Q divider output cycle from rising edge to falling edge. Subsequent phase offsets do not cause activation of the phase slew limiting function of the Q divider.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
			0	Phase Offset Mode (default). Phase resolution, θ_0, is a function of QDIV0C as θ_0 (degrees)= 180/QDIV0C. Phase, θ, is a function of Phase Offset as $\theta = \theta_0 \times$ Phase Offset. For example, given QDIV0C = 101.5 and Phase Offset = 10, then $\theta_0 = 1.773°$ and $\theta = 17.73°$. Subsequent phase offsets activate the phase slew limiting function of the Q divider.				
	3	Q0C phase slew mode		Q0C Phase Slew Mode. This bit (default = 0) selects between phase slewing modes.	0	R/W	Core clock	No
			0	Lag Mode (default). Phase slewing steps (Δθ) are always in the −Δθ/Δt direction. Thus, while phase slewing, the output frequency decreases in accordance with the sign of Δθ/Δt.				
			1	Minimum Steps Mode. Phase slewing steps (Δθ) are in the direction requiring the least number of steps to accomplish the specified phase offset. Thus, while phase slewing, the output frequency increases or decreases in accordance with the sign of Δθ/Δt necessary to satisfy the least number of steps requirement.				
	[2:0]	Maximum phase slew step		Q0C Maximum Phase Slew Step. This 3-bit value (default = 7) selects a maximum phase step size (θ_{MAX}) for phase slewing, where θ_{MAX} relates to the total division factor, QDIV0C, of the Q divider (QDIV0C includes the integer and half integer parts).	0x7	R/W	Core clock	No
			0	1 Q divider input half-cycle. θ_{MAX} = 180/QDIV0C (degrees).				
			1	1 Q divider input cycle. θ_{MAX} = 90/QDIV0C (degrees).				
			2	~1/32 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV0C/16)/QDIV0C. The user must ensure floor(QDIV0C/16) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			3	~1/16 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV0C/8)/QDIV0C. The user must ensure floor(QDIV0C/8) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			4	~1/8 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV0C/4)/QDIV0C. The user must ensure floor(QDIV0C/4) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			5	~1/4 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV0C/2)/QDIV0C. The user must ensure floor(QDIV0C /2) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			6	~1/2 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV0C)/QDIV0C. The user must ensure floor(QDIV0C) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			7	~1 Q divider output cycle (default). θ_{MAX} (degrees) = 180 × (2 × QDIV0C − 1)/QDIV0C. This setting results in the phase slewing function being effectively disabled and causes phase slewing to execute as though Bit 3 = 0 (even when Bit 3 = 1).				

DISTRIBUTION PARAMETERS: Q0CC—REGISTER 0x112D TO REGISTER 0x1135

Table 64. Distribution Parameters: Q0CC Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x112D	[7:0]	Q0CC Divide Ratio[7:0]		Q0CC Integer Divide Ratio. This 32-bit unsigned value, Q0CC_int (default = 0), is the integer portion of the divide factor (QDIV0CC) for Q Divider Q0CC. 0 and 1 are invalid values for Q0CC_int. Because the default value is 0, the user must program a valid value. When using the associated N shot generator or pulse width modulator, the following constraint applies: Q0CC_int ≥ 8.	0x00	R/W	Core clock	No
0x112E	[7:0]	Q0CC Divide Ratio[15:8]		Continuation of the Q0CC divide ratio bit field. See the Q0CC Divide Ratio[7:0] description.	0x00	R/W	Core clock	No
0x112F	[7:0]	Q0CC Divide Ratio[23:16]		Continuation of the Q0CC divide ratio bit field. See the Q0CC Divide Ratio[7:0] description.	0x00	R/W	Core clock	No
0x1130	[7:0]	Q0CC Divide Ratio[31:24]		Continuation of the Q0CC divide ratio bit field. See the Q0CC Divide Ratio[7:0] description.	0x00	R/W	Core clock	No
0x1131	[7:0]	Q0CC Phase Offset[7:0]		Q0CC Phase Offset or Pulse Width Magnitude. This 33-bit unsigned value, Phase Offset (default = 0), establishes either a phase offset or a pulse width for the Q0CC divider. The maximum usable value of Phase Offset ($OFST_{MAX}$) is as follows: $OFST_{MAX} = 2 \times QDIV0CC - 1$ where *QDIV0CC* is the total divide ratio of Q Divider Q0CC. The Q divider interprets the value of Phase Offset differently depending on whether phase offset or pulse width mode is in effect per Register 0x1135, Bit 4. Two categories of phase offset activation exist: initial and subsequent. An initial phase offset activates immediately following a device power-up or a reset, followed by completion of a distribution synchronization request. Subsequent phase offsets result from completed distribution synchronization requests that occur after completion of an initial phase offset.	0x00	R/W	Core clock	No
0x1132	[7:0]	Q0CC Phase Offset[15:8]		Continuation of the Q0CC phase offset bit field. See the Q0CC Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x1133	[7:0]	Q0CC Phase Offset[23:16]		Continuation of the Q0CC phase offset bit field. See the Q0CC Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x1134	[7:0]	Q0CC Phase Offset[31:24]		Continuation of the Q0CC phase offset bit field. See the Q0CC Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x1135	7	Reserved		Reserved.	0	R	Live	No
	6	Q0CC Phase Offset[32]		Continuation of the Q0CC phase offset bit field. See the Q0CC Phase Offset[7:0] description.	0	R/W	Core clock	No
	5	Enable half divide		Q0CC Half Integer Enable. This bit (default = 0) adds 0 or 0.5 to the integer portion of Q Divider Q0CC.	0	R/W	Core clock	No
			0	QDIV0CC = Q0CC_int.				
			1	QDIV0CC = Q0CC_int + 0.5.				
	4	Enable pulse width control		Q0CC Phase Offset or Pulse Width Mode Select. This bit (default = 0) selects between phase offset mode and pulse width mode with regard to the interpretation of the value of Phase Offset in Register 0x1131. The value of Phase Offset relates to the total division factor, QDIV0CC, of the Q divider (QDIV0CC includes the integer and half integer parts).	0	R/W	Core clock	No
			1	Pulse Width Mode. Pulse width mode controls the duty cycle of the output clock signal. Duty cycle resolution, DC_0, is a function of QDIV0CC as DC_0 (%) = 50/QDIV0CC. Duty cycle relates to Phase Offset as $DC_0 \times$ Phase Offset. For example, given QDIV0CC = 101.5 and Phase Offset = 10, then DC_0 = 0.493% and duty cycle = 4.93%. Duty cycle constitutes a fraction of one Q divider output cycle from rising edge to falling edge. Subsequent phase offsets do not cause activation of the phase slew limiting function of the Q divider.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
			0	Phase Offset Mode (default). Phase resolution, θ_0, is a function of QDIV0CC as θ_0 (degrees)= 180/QDIV0CC. Phase, θ, is a function of Phase Offset as $\theta = \theta_0 \times$ Phase Offset. For example, given QDIV0CC = 101.5 and Phase Offset = 10, then $\theta_0 = 1.773°$ and $\theta = 17.73°$. Subsequent phase offsets activate the phase slew limiting function of the Q divider.				
	3	Q0CC phase slew mode		Q0CC Phase Slew Mode. This bit (default = 0) selects between phase slewing modes.	0	R/W	Core clock	No
			0	Lag Mode (default). Phase slewing steps (Δθ) are always in the −Δθ/Δt direction. Thus, while phase slewing, the output frequency decreases in accordance with the sign of Δθ/Δt.				
			1	Minimum Steps Mode. Phase slewing steps (Δθ) are in the direction requiring the least number of steps to accomplish the specified phase offset. Thus, while phase slewing, the output frequency increases or decreases in accordance with the sign of Δθ/Δt necessary to satisfy the least number of steps requirement.				
	[2:0]	Maximum phase slew step		Q0CC Maximum Phase Slew Step. This 3-bit value (default = 7) selects a maximum phase step size (θ_{MAX}) for phase slewing, where θ_{MAX} relates to the total division factor, QDIV0CC, of the Q divider (QDIV0CC includes the integer and half integer parts).	0x7	R/W	Core clock	No
			0	1 Q divider input half-cycle. θ_{MAX} = 180/QDIV0CC (degrees).				
			1	1 Q divider input cycle. θ_{MAX} = 90/QDIV0CC (degrees).				
			2	~1/32 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV0CC/16)/QDIV0CC. The user must ensure floor(QDIV0CC/16) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			3	~1/16 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV0CC/8)/QDIV0CC. The user must ensure floor(QDIV0CC/8) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			4	~1/8 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV0CC/4)/QDIV0CC. The user must ensure floor(QDIV0CC/4) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			5	~1/4 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV0CC/2)/QDIV0CC. The user must ensure floor(QDIV0CC/2) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			6	~1/2 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV0CC)/QDIV0CC. The user must ensure floor(QDIV0CC) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			7	~1 Q divider output cycle (default). θ_{MAX} (degrees) = 180 × (2 × QDIV0CC − 1)/QDIV0CC. This setting results in the phase slewing function being effectively disabled and causes phase slewing to execute as though Bit 3 = 0 (even when Bit 3 = 1).				

TRANSLATION PROFILE 0.0 PARAMETERS—REGISTER 0x1200 TO REGISTER 0x1217

Table 65. Translation Profile 0.0 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1200	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	[5:1]	Translation Profile 0.0 selection priority		Translation Profile 0.0 Priority Value. This 5-bit unsigned value (default = 0) allows the user to assign a priority level to Translation Profile 0.0. Priority assignment (highest priority = 0, lowest priority = 31) allows DPLL0 to select one translation profile over another when reference switching.	0x00	R/W	Core clock	No
	0	Enable Translation Profile 0.0		Translation Profile 0.0 Enable. This bit enables Translation Profile 0.0 as a usable translation profile for DPLL0.	0	R/W	Core clock	No
			0	Disabled (default).				
			1	Enabled.				
0x1201	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:0]	Translation Profile 0.0 reference source selection		DPLL0 Reference Source Selection. This 5-bit unsigned value (default = 0) assigns a time stamp source as the input to DPLL0 when the DPLL activates Translation Profile 0.0.	0x00	R/W	Core clock	No
			0	REFA (default).				
			1	REFAA.				
			2	REFB.				
			3	REFBB.				
			5	Feedback from DPLL1.				
			6	Auxiliary REF0.				
			7	Auxiliary REF1.				
			8	Auxiliary NCO 0.				
			9	Auxiliary NCO 1.				
			11	Auxiliary REF2.				
			12	Auxiliary REF3.				
			13	Inverse User Time Stamper 0.				
			14	Inverse User Time Stamper 1.				
0x1202	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:0]	External zero delay feedback path		DPLL0 External Zero-Delay Feedback Path. This 5-bit field (default = 0) selects a reference input as the feedback return path for DPLL0 when Translation Profile 0.0 is configured as a hitless external zero-delay profile. The selections of the reference input as the DPLL feedback are meaningless unless Register 0x1203, Bits[1:0] = 11 (binary).	0x00	R/W	Core clock	No
			0	REFA (default). When REFA is configured as a differential input, use this selection (not the REFAA selection).				
			1	REFAA.				
			2	REFB. When REFB is configured as a differential input, use this selection (not the REFBB selection).				
			3	REFBB.				
			4	Auxiliary REF0.				
			5	Auxiliary REF1.				
			6	Auxiliary REF2.				
			7	Auxiliary REF3.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[4:0]	Internal zero-delay feedback path		DPLL0 Internal Zero-Delay Feedback Path. This 5-bit field (default = 0) selects a Q divider output as the feedback return path for DPLL0 when Translation Profile 0.0 is configured as a hitless internal zero-delay profile. The selections of the Q divider output as the DPLL feedback return path are meaningless unless Register 0x1203, Bits[1:0] = 01 (binary).	0x00	R/W	Core clock	No
			0	Q0A Output as DPLL0 Feedback (default). When OUT0A is configured for differential mode, use this selection (not the Q0AA feedback selection).				
			1	Q0AA Output as DPLL0 Feedback.				
			2	Q0B Output as DPLL0 Feedback. When OUT0B is configured for differential mode, use this selection (not the Q0BB feedback selection).				
			3	Q0BB Output as DPLL0 Feedback.				
			4	Q0C Output as DPLL0 Feedback. When OUT0C is configured for differential mode, use this selection (not the Q0CC feedback selection).				
			5	Q0CC Output as DPLL0 Feedback.				
0x1203	7	Translation Profile 0.0 loop filter base		DPLL0 Loop Filter Base. This bit (default = 0) assigns one of the loop filter base coefficient sets (LFx) to DPLL0.	0	R/W	Core clock	No
			0	LF0 (default). Nominal 70° phase margin.				
			1	LF1. Nominal 88.5° phase margin (use this setting for applications requiring the response of the closed-loop transfer function of DPLL0 to have <0.1 dB peaking).				
	[6:5]	Reserved		Reserved.	0x0	R/W	Core clock	No
	[4:2]	Translation Profile 0.0 tag mode		DPLL0 Tag Modes. This 3-bit unsigned value (default = 0) selects the DPLL0 tag mode for Translation Profile 0.0.	0x0	R/W	Core clock	No
			0	No tagged time stamps in the reference or feedback path of DPLL0 (default).				
			1	Tagged time stamps only in the reference path of DPLL0.				
			2	Tagged time stamps only in the feedback path of DPLL0.				
			3	Tagged time stamps in the reference and feedback paths of DPLL0, but the untagged rates differ.				
			4	Tagged time stamps in the reference and feedback paths of DPLL0, but the untagged rates are equal.				
	[1:0]	Translation Profile 0.0 loop mode		DPLL0 Frequency Translation Mode. This 2-bit unsigned value (default = 0) establishes the frequency translation mode for DPLL0.	0x0	R/W	Core clock	No
			0	Phase buildout mode (default).				
			1	Hitless, internal zero delay mode.				
			3	Hitless, external zero delay mode.				
0x1204	[7:0]	Translation Profile 0.0 Loop Bandwidth[7:0]		DPLL0 Loop Bandwidth Scale Factor. This 32-bit unsigned value (default = 0) constitutes a scale factor (SF) applied to the base loop bandwidth (LBW_0) associated with the coefficients of Loop Filter LF0 or LF1. The resulting loop bandwidth (LBW) is LBW = SF × LBW_0. The default coefficients of LF0 and LF1 yield LBW_0 = 1 µHz (10^{-6} Hz). For example, given SF = 50,000,000, then LBW = 50 Hz for LF0 or LF1.	0x00	R/W	Core clock	No
0x1205	[7:0]	Translation Profile 0.0 Loop Bandwidth[15:8]		Continuation of the Translation Profile 0.0 loop bandwidth bit field. See the Translation Profile 0.0 Loop Bandwidth[7:0] description.	0x00	R/W	Core clock	No
0x1206	[7:0]	Translation Profile 0.0 Loop Bandwidth[23:16]		Continuation of the Translation Profile 0.0 loop bandwidth bit field. See the Translation Profile 0.0 Loop Bandwidth[7:0] description.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1207	[7:0]	Translation Profile 0.0 Loop Bandwidth[31:24]		Continuation of the Translation Profile 0.0 loop bandwidth bit field. See the Translation Profile 0.0 Loop Bandwidth[7:0] description.	0x00	R/W	Core clock	No
0x1208	[7:0]	Translation Profile 0.0 Hitless N Divider[7:0]		DPLL0 Feedback Divider (N): Hitless Zero-Delay Operation. This 32-bit unsigned value, N Hitless (default = 4000), sets the divide ratio, N, for the feedback divider of DPLL0 when the DPLL operates in internal hitless zero delay mode. $N = N\ Hitless + 1$ Thus, the default value yields N = 4001. A translation profile configured for external zero delay hitless DPLL operation uses Register 0x120F to Register 0x120C, Bits[31:0] instead of this register.	0x160	R/W	Core clock	No
0x1209	[7:0]	Translation Profile 0.0 Hitless N Divider[15:8]		Continuation of the Translation Profile 0.0 hitless N divider bit field. See the Translation Profile 0.0 Hitless N Divider[7:0] description.	0x15	R/W	Core clock	No
0x120A	[7:0]	Translation Profile 0.0 Hitless N Divider[23:16]		Continuation of the Translation Profile 0.0 hitless N divider bit field. See the Translation Profile 0.0 Hitless N Divider[7:0] description.	0x00	R/W	Core clock	No
0x120B	[7:0]	Translation Profile 0.0 Hitless N Divider[31:24]		Continuation of the Translation Profile 0.0 hitless N divider bit field. See the Translation Profile 0.0 Hitless N Divider[7:0] description.	0x00	R/W	Core clock	No
0x120C	[7:0]	Translation Profile 0.0 Buildout N Divider[7:0]		DPLL0 Feedback Divider (N_int): Phase Buildout Operation. This 32-bit unsigned value, $N\_int_{BUILDOUT}$ (default = 4000), sets the integer part of the divide ratio, N, for the feedback divider of DPLL0 when the DPLL operates in phase buildout mode. $N = N\_int_{BUILDOUT} + 1$ Thus, the default value yields N = 4001.	0x160	R/W	Core clock	No
0x120D	[7:0]	Translation Profile 0.0 Buildout N Divider[15:8]		Continuation of the Translation Profile 0.0 buildout N divider bit field. See the Translation Profile 0.0 Buildout N Divider[7:0] description.	0x15	R/W	Core clock	No
0x120E	[7:0]	Translation Profile 0.0 Buildout N Divider[23:16]		Continuation of the Translation Profile 0.0 buildout N divider bit field. See the Translation Profile 0.0 Buildout N Divider[7:0] description.	0x00	R/W	Core clock	No
0x120F	[7:0]	Translation Profile 0.0 Buildout N Divider[31:24]		Continuation of the Translation Profile 0.0 buildout N divider bit field. See the Translation Profile 0.0 Buildout N Divider[7:0] description.	0x00	R/W	Core clock	No
0x1210	[7:0]	Translation Profile 0.0 Buildout FRAC[7:0]		DPLL0 Feedback Divider (N_num): Phase Buildout Operation. This 24-bit unsigned value, $N\_num_{BUILDOUT}$ (default = 0), is the numerator of the fractional portion of the feedback divider of DPLL0 when the DPLL operates in phase buildout mode. The total divide ratio is as follows: $N\_total = (N\_int_{BUILDOUT} + 1) + (N\_num/N\_den)$ where: *N_den* is the denominator of the fractional portion of the feedback divider, which resides in Register 0x1215 to Register 0x1213, Bits[23:0]. $N\_num < N\_den$. To make N_total an integer, program N_num = 0 and N_den = 0.	0x00	R/W	Core clock	No
0x1211	[7:0]	Translation Profile 0.0 Buildout FRAC[15:8]		Continuation of the Translation Profile 0.0 buildout FRAC bit field. See the Translation Profile 0.0 Buildout FRAC[7:0] description.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1212	[7:0]	Translation Profile 0.0 Buildout FRAC[23:16]		Continuation of the Translation Profile 0.0 buildout FRAC bit field. See the Translation Profile 0.0 Buildout FRAC[7:0] description.	0x00	R/W	Core clock	No
0x1213	[7:0]	Translation Profile 0.0 Buildout MOD[7:0]		DPLL0 Feedback Divider (N_den): Phase Buildout Operation. This 24-bit unsigned value, $N\_den_{BUILDOUT}$ (default = 0), is the denominator of the fractional portion of the feedback divider of DPLL0 when the DPLL operates in phase buildout mode. The total divide ratio is as follows: $N\_total = (N\_int_{BUILDOUT} + 1) + (N\_num/N\_den)$ where *N_num* is the numerator of the fractional portion of the feedback divider, which resides in Register 0x1212 to Register 0x1210, Bits[23:0]. *N_num* < *N_den*. To make the N divider divide ratio an integer, program *N_num* = 0 and *N_den* = 0.	0x00	R/W	Core clock	No
0x1214	[7:0]	Translation Profile 0.0 Buildout MOD[15:8]		Continuation of the Translation Profile 0.0 buildout MOD bit field. See the Translation Profile 0.0 Buildout MOD[7:0] description.	0x00	R/W	Core clock	No
0x1215	[7:0]	Translation Profile 0.0 Buildout MOD[23:16]		Continuation of the Translation Profile 0.0 buildout MOD bit field. See the Translation Profile 0.0 Buildout MOD[7:0] description.	0x00	R/W	Core clock	No
0x1216	[7:4]	Reserved		Reserved.	0x0	R/W	Core clock	No
	[3:0]	Translation Profile 0.0 fast acquisition excess bandwidth		DPLL0 Fast Acquisition Excess Bandwidth Factor. This 3-bit unsigned value, ESF (default = 0), controls the behavior of the fast acquisition option for DPLL0, where ESF= 0 disables the fast acquisition feature. ESF constitutes an exponential scale factor applied to the nominal loop bandwidth of the DPLL (BW_0) to yield an excess bandwidth, EBW, as follows: $EBW = BW_0 \times 2^{ESF}$ The fast acquisition controller sets the loop bandwidth of the DPLL to EBW at the start of an acquisition sequence. When the DPLL indicates phase lock, the fast acquisition controller halves the loop bandwidth. The fast acquisition controller again waits for the DPLL to indicate phase lock. When the DPLL indicates phase lock, the fast acquisition controller again halves the loop bandwidth. The process repeats until the DPLL loop bandwidth reaches BW_0. The fast acquisition controller sets Register 0x3102, Bit 4 = 1 while sequencing through the loop bandwidth reduction steps to indicate its active status. 0 Fast acquisition controller disabled (default). 1 ESF = 1. 2 ESF = 2. 3 ESF = 3. 4 ESF = 4. 5 ESF = 5. 6 ESF = 6. 7 ESF = 7. 8 ESF = 8. 9 ESF = 9. 10 ESF = 10.	0x0	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1217	7	Reserved		Reserved.	0	R	Live	No
	[6:4]	Translation Profile 0.0 fast acquisition timeout		DPLL0 Fast Acquisition Timeout. This 3-bit unsigned value puts a time limit (t_{MAX}) on how long the fast acquisition controller waits for chatter free DPLL phase lock status to occur during each loop bandwidth reduction step. If the phase lock guard timer (see Bits[2:0]) fails to time out by t_{MAX}, the fast acquisition controller automatically moves on to the next loop bandwidth reduction step even though chatter free phase lock failed to occur. The fast acquisition controller indicates completion of the fast acquisition process by setting Register 0x3102, Bit 5 = 1 only when the fast acquisition controller is in its final bandwidth reduction step and the t_{MAX} timer fails to expire.	0x0	R/W	Core clock	No
			0	t_{MAX} = 10 ms (default).				
			1	t_{MAX} = 50 ms.				
			2	t_{MAX} = 100 ms.				
			3	t_{MAX} = 500 ms.				
			4	t_{MAX} = 1 sec.				
			5	t_{MAX} = 10 sec.				
			6	t_{MAX} = 50 sec.				
			7	t_{MAX} = 100 sec.				
	3	Reserved		Reserved.	0	R	Live	No
	[2:0]	Translation Profile 0.0 fast acquisition lock settle time		DPLL0 Fast Acquisition Phase Lock Guard Time. This 3-bit unsigned value, GUARD_TIME (default = 0), sets the period (t_{GUARD}) of a countdown timer used by the fast acquisition controller. The countdown timer starts when the DPLL indicates phase lock, but the fast acquisition controller reloads the countdown timer with a value per GUARD_TIME whenever the DPLL indicates phase unlock. It is only upon timeout of the countdown timer that the fast acquisition controller moves on to its next bandwidth reduction step. t_{GUARD} constitutes the minimum amount of time the fast acquisition controller must observe chatter free DPLL phase lock status during each loop bandwidth reduction step.	0x0	R/W	Core clock	No
			0	t_{GUARD} = 1 ms (default).				
			1	t_{GUARD} = 10 ms.				
			2	t_{GUARD} = 50 ms.				
			3	t_{GUARD} = 100 ms.				
			4	t_{GUARD} = 500 ms.				
			5	t_{GUARD} = 1 sec.				
			6	t_{GUARD} = 10 sec.				
			7	t_{GUARD} = 50 sec.				

TRANSLATION PROFILE 0.1 PARAMETERS—REGISTER 0x1220 TO REGISTER 0x1237

Table 66. Translation Profile 0.1 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1220	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	[5:1]	Translation Profile 0.1 selection priority		Translation Profile 0.1 Priority Value. This 5-bit unsigned value (default = 0) allows the user to assign a priority level to Translation Profile 0.1. Priority assignment (highest priority = 0, lowest priority = 31) allows DPLL0 to select one translation profile over another when reference switching.	0x00	R/W	Core clock	No
	0	Enable Translation Profile 0.1		Translation Profile 0.1 Enable. This bit enables Translation Profile 0.1 as a usable translation profile for DPLL0.	0	R/W	Core clock	No
			0	Disabled (default).				
			1	Enabled.				
0x1221	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:0]	Translation Profile 0.1 reference source selection		DPLL0 Reference Source Selection. This 5-bit unsigned value (default = 0) assigns a time stamp source as the input to DPLL0 when the DPLL activates Translation Profile 0.1.	0x00	R/W	Core clock	No
			0	REFA (default).				
			1	REFAA.				
			2	REFB.				
			3	REFBB.				
			5	Feedback from DPLL1.				
			6	Auxiliary REF0.				
			7	Auxiliary REF1.				
			8	Auxiliary NCO 0.				
			9	Auxiliary NCO 1.				
			11	Auxiliary REF2.				
			12	Auxiliary REF3.				
			13	Inverse User Time Stamper 0.				
			14	Inverse User Time Stamper 1.				
0x1222	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:0]	External zero delay feedback path		DPLL0 External Zero-Delay Feedback Path. This 5-bit field (default = 0) selects a reference input as the feedback return path for DPLL0 when Translation Profile 0.1 is configured as a hitless external zero-delay profile. The selections of the reference input as the DPLL feedback are meaningless unless Register 0x1223, Bits[1:0] = 11 (binary).	0x00	R/W	Core clock	No
			0	REFA (default). When REFA is configured as a differential input, use this selection (not the REFAA selection).				
			1	REFAA.				
			2	REFB. When REFB is configured as a differential input, use this selection (not the REFBB selection).				
			3	REFBB.				
			4	Auxiliary REF0.				
			5	Auxiliary REF1.				
			6	Auxiliary REF2.				
			7	Auxiliary REF3.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[4:0]	Internal zero-delay feedback path		DPLL0 Internal Zero-Delay Feedback Path. This 5-bit field (default = 0) selects a Q divider output as the feedback return path for DPLL0 when Translation Profile 0.1 is configured as a hitless internal zero-delay profile. The selections of the Q divider output as the DPLL feedback return path are meaningless unless Register 0x1223, Bits[1:0] = 01 (binary).	0x00	R/W	Core clock	No
			0	Q0A Output as DPLL0 Feedback (default). When OUT0A is configured for differential mode, use this selection (not the Q0AA feedback selection).				
			1	Q0AA Output as DPLL0 Feedback.				
			2	Q0B Output as DPLL0 Feedback. When OUT0B is configured for differential mode, use this selection (not the Q0BB feedback selection).				
			3	Q0BB Output as DPLL0 Feedback.				
			4	Q0C Output as DPLL0 Feedback. When OUT0C is configured for differential mode, use this selection (not the Q0CC feedback selection).				
			5	Q0CC Output as DPLL0 Feedback.				
0x1223	7	Translation Profile 0.1 loop filter base		DPLL0 Loop Filter Base. This bit (default = 0) assigns one of the loop filter base coefficient sets (LFx) to DPLL0.	0	R/W	Core clock	No
			0	LF0 (default). Nominal 70° phase margin.				
			1	LF1. Nominal 88.5° phase margin (use this setting for applications requiring the response of the closed-loop transfer function of DPLL0 to have <0.1 dB peaking).				
	[6:5]	Reserved		Reserved.	0x0	R/W	Core clock	No
	[4:2]	Translation Profile 0.1 tag mode		DPLL0 Tag Modes. This 3-bit unsigned value (default = 0) selects the DPLL0 tag mode for Translation Profile 0.1.	0x0	R/W	Core clock	No
			0	No tagged time stamps in the reference or feedback path of DPLL0 (default).				
			1	Tagged time stamps only in the reference path of DPLL0.				
			2	Tagged time stamps only in the feedback path of DPLL0.				
			3	Tagged time stamps in the reference and feedback paths of DPLL0, but the untagged rates differ.				
			4	Tagged time stamps in the reference and feedback paths of DPLL0, but the untagged rates are equal.				
	[1:0]	Translation Profile 0.1 loop mode		DPLL0 Frequency Translation Mode. This 2-bit unsigned value (default = 0) establishes the frequency translation mode for DPLL0.	0x0	R/W	Core clock	No
			0	Phase buildout mode (default).				
			1	Hitless, internal zero delay mode.				
			3	Hitless, external zero delay mode.				
0x1224	[7:0]	Translation Profile 0.1 Loop Bandwidth[7:0]		DPLL0 Loop Bandwidth Scale Factor. This 32-bit unsigned value (default = 0) constitutes a scale factor (SF) applied to the base loop bandwidth (LBW_0) associated with the coefficients of Loop Filter LF0 or LF1. The resulting loop bandwidth (LBW) is LBW = SF × LBW_0. The default coefficients of LF0 and LF1 yield LBW_0 = 1 µHz (10^{-6} Hz). For example, given SF = 50,000,000, then LBW = 50 Hz for LF0 or LF1.	0x00	R/W	Core clock	No
0x1225	[7:0]	Translation Profile 0.1 Loop Bandwidth[15:8]		Continuation of the Translation Profile 0.1 loop bandwidth bit field. See the Translation Profile 0.1 Loop Bandwidth[7:0] description.	0x00	R/W	Core clock	No
0x1226	[7:0]	Translation Profile 0.1 Loop Bandwidth[23:16]		Continuation of the Translation Profile 0.1 loop bandwidth bit field. See the Translation Profile 0.1 Loop Bandwidth[7:0] description.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1227	[7:0]	Translation Profile 0.1 Loop Bandwidth[31:24]		Continuation of the Translation Profile 0.1 loop bandwidth bit field. See the Translation Profile 0.1 Loop Bandwidth[7:0] description.	0x00	R/W	Core clock	No
0x1228	[7:0]	Translation Profile 0.1 Hitless N Divider[7:0]		DPLL0 Feedback Divider (N): Hitless Zero-Delay Operation. This 32-bit unsigned value, N Hitless (default = 4000), sets the divide ratio, N, for the feedback divider of DPLL0 when the DPLL operates in internal hitless zero delay mode. $N = N\ Hitless + 1$ Thus, the default value yields N = 4001. A translation profile configured for external zero delay hitless DPLL operation uses Register 0x122F to Register, 0x122C, Bits[31:0] instead of this register.	0x160	R/W	Core clock	No
0x1229	[7:0]	Translation Profile 0.1 Hitless N Divider[15:8]		Continuation of the Translation Profile 0.1 hitless N divider bit field. See the Translation Profile 0.1 Hitless N Divider[7:0] description.	0x15	R/W	Core clock	No
0x122A	[7:0]	Translation Profile 0.1 Hitless N Divider[23:16]		Continuation of the Translation Profile 0.1 hitless N divider bit field. See the Translation Profile 0.1 Hitless N Divider[7:0] description.	0x00	R/W	Core clock	No
0x122B	[7:0]	Translation Profile 0.1 Hitless N Divider[31:24]		Continuation of the Translation Profile 0.1 hitless N divider bit field. See the Translation Profile 0.1 Hitless N Divider[7:0] description.	0x00	R/W	Core clock	No
0x122C	[7:0]	Translation Profile 0.1 Buildout N Divider[7:0]		DPLL0 Feedback Divider (N_int): Phase Buildout Operation. This 32-bit unsigned value, $N\_int_{BUILDOUT}$ (default = 4000), sets the integer part of the divide ratio, N, for the feedback divider of DPLL0 when the DPLL operates in phase buildout mode. $N = N\_int_{BUILDOUT} + 1$ Thus, the default value yields N = 4001.	0x160	R/W	Core clock	No
0x122D	[7:0]	Translation Profile 0.1 Buildout N Divider[15:8]		Continuation of the Translation Profile 0.1 buildout N divider bit field. See the Translation Profile 0.1 Buildout N Divider[7:0] description.	0x15	R/W	Core clock	No
0x122E	[7:0]	Translation Profile 0.1 Buildout N Divider[23:16]		Continuation of the Translation Profile 0.1 buildout N divider bit field. See the Translation Profile 0.1 Buildout N Divider[7:0] description.	0x00	R/W	Core clock	No
0x122F	[7:0]	Translation Profile 0.1 Buildout N Divider[31:24]		Continuation of the Translation Profile 0.1 buildout N divider bit field. See the Translation Profile 0.1 Buildout N Divider[7:0] description.	0x00	R/W	Core clock	No
0x1230	[7:0]	Translation Profile 0.1 Buildout FRAC[7:0]		DPLL0 Feedback Divider (N_num): Phase Buildout Operation. This 24-bit unsigned value, $N\_num_{BUILDOUT}$ (default = 0), is the numerator of the fractional portion of the feedback divider of DPLL0 when the DPLL operates in phase buildout mode. The total divide ratio is as follows: $N\_total = (N\_int_{BUILDOUT} + 1) + (N\_num/N\_den)$ where: *N_den* is the denominator of the fractional portion of the feedback divider, which resides in Register 0x1235 to Register 0x1233, Bits[23:0]. $N\_num < N\_den$. To make N_total an integer, program N_num = 0 and N_den = 0.	0x00	R/W	Core clock	No
0x1231	[7:0]	Translation Profile 0.1 Buildout FRAC[15:8]		Continuation of the Translation Profile 0.1 buildout FRAC bit field. See the Translation Profile 0.1 Buildout FRAC[7:0] description.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1232	[7:0]	Translation Profile 0.1 Buildout FRAC[23:16]		Continuation of the Translation Profile 0.1 buildout FRAC bit field. See the Translation Profile 0.1 Buildout FRAC[7:0] description.	0x00	R/W	Core clock	No
0x1233	[7:0]	Translation Profile 0.1 Buildout MOD[7:0]		DPLL0 Feedback Divider (N_den): Phase Buildout Operation. This 24-bit unsigned value, $N\_den_{BUILDOUT}$ (default = 0), is the denominator of the fractional portion of the feedback divider of DPLL0 when the DPLL operates in phase buildout mode. The total divide ratio is as follows: $N\_total = (N\_int_{BUILDOUT} + 1) + (N\_num/N\_den)$ where *N_num* is the numerator of the fractional portion of the feedback divider, which resides in Register 0x1232 to Register 0x1230, Bits[23:0]. *N_num* < *N_den*. To make the N divider divide ratio an integer, program *N_num* = 0 and *N_den* = 0.	0x00	R/W	Core clock	No
0x1234	[7:0]	Translation Profile 0.1 Buildout MOD[15:8]		Continuation of the Translation Profile 0.1 buildout MOD bit field. See the Translation Profile 0.1 Buildout MOD[7:0] description.	0x00	R/W	Core clock	No
0x1235	[7:0]	Translation Profile 0.1 Buildout MOD[23:16]		Continuation of the Translation Profile 0.1 buildout MOD bit field. See the Translation Profile 0.1 Buildout MOD[7:0] description.	0x00	R/W	Core clock	No
0x1236	[7:4]	Reserved		Reserved.	0x0	R/W	Core clock	No
	[3:0]	Translation Profile 0.1 fast acquisition excess bandwidth		DPLL0 Fast Acquisition Excess Bandwidth Factor. This 3-bit unsigned value, ESF (default = 0), controls the behavior of the fast acquisition option for DPLL0, where ESF = 0 disables the fast acquisition feature. ESF constitutes an exponential scale factor applied to the nominal loop bandwidth of the DPLL (BW_0) to yield an excess bandwidth, EBW, as follows: $EBW = BW_0 \times 2^{ESF}$ The fast acquisition controller sets the loop bandwidth of the DPLL to EBW at the start of an acquisition sequence. When the DPLL indicates phase lock, the fast acquisition controller halves the loop bandwidth. The fast acquisition controller again waits for the DPLL to indicate phase lock. When the DPLL indicates phase lock, the fast acquisition controller again halves the loop bandwidth. The process repeats until the DPLL loop bandwidth reaches BW_0. The fast acquisition controller sets Register 0x3102, Bit 4 = 1 while sequencing through the loop bandwidth reduction steps to indicate its active status. 0 Fast acquisition controller disabled (default). 1 ESF = 1. 2 ESF = 2. 3 ESF = 3. 4 ESF = 4. 5 ESF = 5. 6 ESF = 6. 7 ESF = 7. 8 ESF = 8. 9 ESF = 9. 10 ESF = 10.	0x0	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1237	7	Reserved		Reserved.	0	R	Live	No
	[6:4]	Translation Profile 0.1 fast acquisition timeout		DPLL0 Fast Acquisition Timeout. This 3-bit unsigned value puts a time limit (t_{MAX}) on how long the fast acquisition controller waits for chatter free DPLL phase lock status to occur during each loop bandwidth reduction step. If the phase lock guard timer (see Bits[2:0]) fails to time out by t_{MAX}, the fast acquisition controller automatically moves on to the next loop bandwidth reduction step even though chatter free phase lock failed to occur. The fast acquisition controller indicates completion of the fast acquisition process by setting Register 0x3102, Bit 5 = 1 only when the fast acquisition controller is in its final bandwidth reduction step and the t_{MAX} timer fails to expire.	0x0	R/W	Core clock	No
			0	t_{MAX} = 10 ms (default).				
			1	t_{MAX} = 50 ms.				
			2	t_{MAX} = 100 ms.				
			3	t_{MAX} = 500 ms.				
			4	t_{MAX} = 1 sec.				
			5	t_{MAX} = 10 sec.				
			6	t_{MAX} = 50 sec.				
			7	t_{MAX} = 100 sec.				
	3	Reserved		Reserved.	0	R	Live	No
	[2:0]	Translation Profile 0.1 fast acquisition lock settle time		DPLL0 Fast Acquisition Phase Lock Guard Time. This 3-bit unsigned value, GUARD_TIME (default = 0), sets the period (t_{GUARD}) of a countdown timer used by the fast acquisition controller. The countdown timer starts when the DPLL indicates phase lock, but the fast acquisition controller reloads the countdown timer with a value per GUARD_TIME whenever the DPLL indicates phase unlock. It is only upon timeout of the countdown timer that the fast acquisition controller moves on to its next bandwidth reduction step. t_{GUARD} constitutes the minimum amount of time the fast acquisition controller must observe chatter free DPLL phase lock status during each loop bandwidth reduction step.	0x0	R/W	Core clock	No
			0	t_{GUARD} = 1 ms (default).				
			1	t_{GUARD} = 10 ms.				
			2	t_{GUARD} = 50 ms.				
			3	t_{GUARD} = 100 ms.				
			4	t_{GUARD} = 500 ms.				
			5	t_{GUARD} = 1 sec.				
			6	t_{GUARD} = 10 sec.				
			7	t_{GUARD} = 50 sec.				

TRANSLATION PROFILE 0.2 PARAMETERS—REGISTER 0x1240 TO REGISTER 0x1257

Table 67. Translation Profile 0.2 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1240	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	[5:1]	Translation Profile 0.2 selection priority		Translation Profile 0.2 Priority Value. This 5-bit unsigned value (default = 0) allows the user to assign a priority level to Translation Profile 0.2. Priority assignment (highest priority = 0, lowest priority = 31) allows DPLL0 to select one translation profile over another when reference switching.	0x00	R/W	Core clock	No
	0	Enable Translation Profile 0.2		Translation Profile 0.2 Enable. This bit enables Translation Profile 0.2 as a usable translation profile for DPLL0.	0	R/W	Core clock	No
			0	Disabled (default).				
			1	Enabled.				
0x1241	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:0]	Translation Profile 0.2 reference source selection		DPLL0 Reference Source Selection. This 5-bit unsigned value (default = 0) assigns a time stamp source as the input to DPLL0 when the DPLL activates Translation Profile 0.2.	0x00	R/W	Core clock	No
			0	REFA (default).				
			1	REFAA.				
			2	REFB.				
			3	REFBB.				
			5	Feedback from DPLL1.				
			6	Auxiliary REF0.				
			7	Auxiliary REF1.				
			8	Auxiliary NCO 0.				
			9	Auxiliary NCO 1.				
			11	Auxiliary REF2.				
			12	Auxiliary REF3.				
			13	Inverse User Time Stamper 0.				
			14	Inverse User Time Stamper 1.				
0x1242	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:0]	External zero delay feedback path		DPLL0 External Zero-Delay Feedback Path. This 5-bit field (default = 0) selects a reference input as the feedback return path for DPLL0 when Translation Profile 0.2 is configured as a hitless external zero-delay profile. The selections of the reference input as the DPLL feedback are meaningless unless Register 0x1243, Bits[1:0] = 11 (binary).	0x00	R/W	Core clock	No
			0	REFA (default). When REFA is configured as a differential input, use this selection (not the REFAA selection).				
			1	REFAA.				
			2	REFB. When REFB is configured as a differential input, use this selection (not the REFBB selection).				
			3	REFBB.				
			4	Auxiliary REF0.				
			5	Auxiliary REF1.				
			6	Auxiliary REF2.				
			7	Auxiliary REF3.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[4:0]	Internal zero-delay feedback path		DPLL0 Internal Zero-Delay Feedback Path. This 5-bit field (default = 0) selects a Q divider output as the feedback return path for DPLL0 when Translation Profile 0.2 is configured as a hitless internal zero-delay profile. The selections of the Q divider output as the DPLL feedback return path are meaningless unless Register 0x1243, Bits[1:0] = 01 (binary).	0x00	R/W	Core clock	No
			0	Q0A Output as DPLL0 Feedback (default). When OUT0A is configured for differential mode, use this selection (not the Q0AA feedback selection).				
			1	Q0AA Output as DPLL0 Feedback.				
			2	Q0B Output as DPLL0 Feedback. When OUT0B is configured for differential mode, use this selection (not the Q0BB feedback selection).				
			3	Q0BB Output as DPLL0 Feedback.				
			4	Q0C Output as DPLL0 Feedback. When OUT0C is configured for differential mode, use this selection (not the Q0CC feedback selection).				
			5	Q0CC Output as DPLL0 Feedback.				
0x1243	7	Translation Profile 0.2 loop filter base		DPLL0 Loop Filter Base. This bit (default = 0) assigns one of the loop filter base coefficient sets (LFx) to DPLL0.	0	R/W	Core clock	No
			0	LF0 (default). Nominal 70° phase margin.				
			1	LF1. Nominal 88.5° phase margin (use this setting for applications requiring the response of the closed-loop transfer function of DPLL0 to have <0.1 dB peaking).				
	[6:5]	Reserved		Reserved.	0x0	R/W	Core clock	No
	[4:2]	Translation Profile 0.2 tag mode		DPLL0 Tag Modes. This 3-bit unsigned value (default = 0) selects the DPLL0 tag mode for Translation Profile 0.2.	0x0	R/W	Core clock	No
			0	No tagged time stamps in the reference or feedback path of DPLL0 (default).				
			1	Tagged time stamps only in the reference path of DPLL0.				
			2	Tagged time stamps only in the feedback path of DPLL0.				
			3	Tagged time stamps in the reference and feedback paths of DPLL0, but the untagged rates differ.				
			4	Tagged time stamps in the reference and feedback paths of DPLL0, but the untagged rates are equal.				
	[1:0]	Translation Profile 0.2 loop mode		DPLL0 Frequency Translation Mode. This 2-bit unsigned value (default = 0) establishes the frequency translation mode for DPLL0.	0x0	R/W	Core clock	No
			0	Phase buildout mode (default).				
			1	Hitless, internal zero delay mode.				
			3	Hitless, external zero delay mode.				
0x1244	[7:0]	Translation Profile 0.2 Loop Bandwidth[7:0]		DPLL0 Loop Bandwidth Scale Factor. This 32-bit unsigned value (default = 0) constitutes a scale factor (SF) applied to the base loop bandwidth (LBW_0) associated with the coefficients of Loop Filter LF0 or LF1. The resulting loop bandwidth (LBW) is LBW = SF × LBW_0. The default coefficients of LF0 and LF1 yield LBW_0 = 1 µHz (10^{-6} Hz). For example, given SF = 50,000,000, then LBW = 50 Hz for LF0 or LF1.	0x00	R/W	Core clock	No
0x1245	[7:0]	Translation Profile 0.2 Loop Bandwidth[15:8]		Continuation of the Translation Profile 0.2 loop bandwidth bit field. See the Translation Profile 0.2 Loop Bandwidth[7:0] description.	0x00	R/W	Core clock	No
0x1246	[7:0]	Translation Profile 0.2 Loop Bandwidth[23:16]		Continuation of the Translation Profile 0.2 loop bandwidth bit field. See the Translation Profile 0.2 Loop Bandwidth[7:0] description.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1247	[7:0]	Translation Profile 0.2 Loop Bandwidth[31:24]		Continuation of the Translation Profile 0.2 loop bandwidth bit field. See the Translation Profile 0.2 Loop Bandwidth[7:0] description.	0x00	R/W	Core clock	No
0x1248	[7:0]	Translation Profile 0.2 Hitless N Divider[7:0]		DPLL0 Feedback Divider (N): Hitless Zero-Delay Operation. This 32-bit unsigned value, N Hitless (default = 4000), sets the divide ratio, N, for the feedback divider of DPLL0 when the DPLL operates in internal hitless zero delay mode. $N = N\ Hitless + 1$ Thus, the default value yields N = 4001. A translation profile configured for external zero delay hitless DPLL operation uses Register 0x124F to Register 0x124C, Bits[31:0] instead of this register.	0x160	R/W	Core clock	No
0x1249	[7:0]	Translation Profile 0.2 Hitless N Divider[15:8]		Continuation of the Translation Profile 0.2 hitless N divider bit field. See the Translation Profile 0.2 Hitless N Divider[7:0] description.	0x15	R/W	Core clock	No
0x124A	[7:0]	Translation Profile 0.2 Hitless N Divider[23:16]		Continuation of the Translation Profile 0.2 hitless N divider bit field. See the Translation Profile 0.2 Hitless N Divider[7:0] description.	0x00	R/W	Core clock	No
0x124B	[7:0]	Translation Profile 0.2 Hitless N Divider[31:24]		Continuation of the Translation Profile 0.2 hitless N divider bit field. See the Translation Profile 0.2 Hitless N Divider[7:0] description.	0x00	R/W	Core clock	No
0x124C	[7:0]	Translation Profile 0.2 Buildout N Divider[7:0]		DPLL0 Feedback Divider (N_int): Phase Buildout Operation. This 32-bit unsigned value, $N\_int_{BUILDOUT}$ (default = 4000), sets the integer part of the divide ratio, N, for the feedback divider of DPLL0 when the DPLL operates in phase buildout mode. $N = N\_int_{BUILDOUT} + 1$ Thus, the default value yields N = 4001.	0x160	R/W	Core clock	No
0x124D	[7:0]	Translation Profile 0.2 Buildout N Divider[15:8]		Continuation of the Translation Profile 0.2 buildout N divider bit field. See the Translation Profile 0.2 Buildout N Divider[7:0] description.	0x15	R/W	Core clock	No
0x124E	[7:0]	Translation Profile 0.2 Buildout N Divider[23:16]		Continuation of the Translation Profile 0.2 buildout N divider bit field. See the Translation Profile 0.2 Buildout N Divider[7:0] description.	0x00	R/W	Core clock	No
0x124F	[7:0]	Translation Profile 0.2 Buildout N Divider[31:24]		Continuation of the Translation Profile 0.2 buildout N divider bit field. See the Translation Profile 0.2 Buildout N Divider[7:0] description.	0x00	R/W	Core clock	No
0x1250	[7:0]	Translation Profile 0.2 Buildout FRAC[7:0]		DPLL0 Feedback Divider (N_num): Phase Buildout Operation. This 24-bit unsigned value, $N\_num_{BUILDOUT}$ (default = 0), is the numerator of the fractional portion of the feedback divider of DPLL0 when the DPLL operates in phase buildout mode. The total divide ratio is as follows: $N\_total = (N\_int_{BUILDOUT} + 1) + (N\_num/N\_den)$ where: *N_den* is the denominator of the fractional portion of the feedback divider, which resides in Register 0x1255 to Register 0x1253, Bits[23:0]. $N\_num < N\_den$. To make N_total an integer, program N_num = 0 and N_den = 0.	0x00	R/W	Core clock	No
0x1251	[7:0]	Translation Profile 0.2 Buildout FRAC[15:8]		Continuation of the Translation Profile 0.2 buildout FRAC bit field. See the Translation Profile 0.2 Buildout FRAC[7:0] description.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1252	[7:0]	Translation Profile 0.2 Buildout FRAC[23:16]		Continuation of the Translation Profile 0.2 buildout FRAC bit field. See the Translation Profile 0.2 Buildout FRAC[7:0] description.	0x00	R/W	Core clock	No
0x1253	[7:0]	Translation Profile 0.2 Buildout MOD[7:0]		DPLL0 Feedback Divider (N_den): Phase Buildout Operation. This 24-bit unsigned value, $N\_den_{BUILDOUT}$ (default = 0), is the denominator of the fractional portion of the feedback divider of DPLL0 when the DPLL operates in phase buildout mode. The total divide ratio is as follows: $N\_total = (N\_int_{BUILDOUT} + 1) + (N\_num/N\_den)$ where *N_num* is the numerator of the fractional portion of the feedback divider, which resides in Register 0x1252 to Register 0x1250, Bits[23:0]. *N_num* < *N_den*. To make the N divider divide ratio an integer, program *N_num* = 0 and *N_den* = 0.	0x00	R/W	Core clock	No
0x1254	[7:0]	Translation Profile 0.2 Buildout MOD[15:8]		Continuation of the Translation Profile 0.2 buildout MOD bit field. See the Translation Profile 0.2 Buildout MOD[7:0] description.	0x00	R/W	Core clock	No
0x1255	[7:0]	Translation Profile 0.2 Buildout MOD[23:16]		Continuation of the Translation Profile 0.2 buildout MOD bit field. See the Translation Profile 0.2 Buildout MOD[7:0] description.	0x00	R/W	Core clock	No
0x1256	[7:4]	Reserved		Reserved.	0x0	R/W	Core clock	No
	[3:0]	Translation Profile 0.2 fast acquisition excess bandwidth		DPLL0 Fast Acquisition Excess Bandwidth Factor. This 3-bit unsigned value, ESF (default = 0), controls the behavior of the fast acquisition option for DPLL0, where ESF = 0 disables the fast acquisition feature. ESF constitutes an exponential scale factor applied to the nominal loop bandwidth of the DPLL (BW_0) to yield an excess bandwidth, EBW, as follows: $EBW = BW_0 \times 2^{ESF}$ The fast acquisition controller sets the loop bandwidth of the DPLL to EBW at the start of an acquisition sequence. When the DPLL indicates phase lock, the fast acquisition controller halves the loop bandwidth. The fast acquisition controller again waits for the DPLL to indicate phase lock. When the DPLL indicates phase lock, the fast acquisition controller again halves the loop bandwidth. The process repeats until the DPLL loop bandwidth reaches BW_0. The fast acquisition controller sets Register 0x3102, Bit 4 = 1 while sequencing through the loop bandwidth reduction steps to indicate its active status. 0 Fast acquisition controller disabled (default). 1 ESF = 1. 2 ESF = 2. 3 ESF = 3. 4 ESF = 4. 5 ESF = 5. 6 ESF = 6. 7 ESF = 7. 8 ESF = 8. 9 ESF = 9. 10 ESF = 10.	0x0	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1257	7	Reserved		Reserved.	0	R	Live	No
	[6:4]	Translation Profile 0.2 fast acquisition timeout		DPLL0 Fast Acquisition Timeout. This 3-bit unsigned value puts a time limit (t_{MAX}) on how long the fast acquisition controller waits for chatter free DPLL phase lock status to occur during each loop bandwidth reduction step. If the phase lock guard timer (see Bits[2:0]) fails to time out by t_{MAX}, the fast acquisition controller automatically moves on to the next loop bandwidth reduction step even though chatter free phase lock failed to occur. The fast acquisition controller indicates completion of the fast acquisition process by setting Register 0x3102, Bit 5 = 1 only when the fast acquisition controller is in its final bandwidth reduction step and the t_{MAX} timer fails to expire.	0x0	R/W	Core clock	No
			0	t_{MAX} = 10 ms (default).				
			1	t_{MAX} = 50 ms.				
			2	t_{MAX} = 100 ms.				
			3	t_{MAX} = 500 ms.				
			4	t_{MAX} = 1 sec.				
			5	t_{MAX} = 10 sec.				
			6	t_{MAX} = 50 sec.				
			7	t_{MAX} = 100 sec.				
	3	Reserved		Reserved.	0	R	Live	No
	[2:0]	Translation Profile 0.2 fast acquisition lock settle time		DPLL0 Fast Acquisition Phase Lock Guard Time. This 3-bit unsigned value, GUARD_TIME (default = 0), sets the period (t_{GUARD}) of a countdown timer used by the fast acquisition controller. The countdown timer starts when the DPLL indicates phase lock, but the fast acquisition controller reloads the countdown timer with a value per GUARD_TIME whenever the DPLL indicates phase unlock. It is only upon timeout of the countdown timer that the fast acquisition controller moves on to its next bandwidth reduction step. t_{GUARD} constitutes the minimum amount of time the fast acquisition controller must observe chatter free DPLL phase lock status during each loop bandwidth reduction step.	0x0	R/W	Core clock	No
			0	t_{GUARD} = 1 ms (default).				
			1	t_{GUARD} = 10 ms.				
			2	t_{GUARD} = 50 ms.				
			3	t_{GUARD} = 100 ms.				
			4	t_{GUARD} = 500 ms.				
			5	t_{GUARD} = 1 sec.				
			6	t_{GUARD} = 10 sec.				
			7	t_{GUARD} = 50 sec.				

TRANSLATION PROFILE 0.3 PARAMETERS—REGISTER 0x1260 TO REGISTER 0x1277

Table 68. Translation Profile 0.3 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1260	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	[5:1]	Translation Profile 0.3 selection priority		Translation Profile 0.3 Priority Value. This 5-bit unsigned value (default = 0) allows the user to assign a priority level to Translation Profile 0.3. Priority assignment (highest priority = 0, lowest priority = 31) allows DPLL0 to select one translation profile over another when reference switching.	0x00	R/W	Core clock	No
	0	Enable Translation Profile 0.3		Translation Profile 0.3 Enable. This bit enables Translation Profile 0.3 as a usable translation profile for DPLL0.	0	R/W	Core clock	No
			0	Disabled (default).				
			1	Enabled.				
0x1261	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:0]	Translation Profile 0.3 reference source selection		DPLL0 Reference Source Selection. This 5-bit unsigned value (default = 0) assigns a time stamp source as the input to DPLL0 when the DPLL activates Translation Profile 0.3.	0x00	R/W	Core clock	No
			0	REFA (default).				
			1	REFAA.				
			2	REFB.				
			3	REFBB.				
			5	Feedback from DPLL1.				
			6	Auxiliary REF0.				
			7	Auxiliary REF1.				
			8	Auxiliary NCO 0.				
			9	Auxiliary NCO 1.				
			11	Auxiliary REF2.				
			12	Auxiliary REF3.				
			13	Inverse User Time Stamper 0.				
			14	Inverse User Time Stamper 1.				
0x1262	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:0]	External zero delay feedback path		DPLL0 External Zero-Delay Feedback Path. This 5-bit field (default = 0) selects a reference input as the feedback return path for DPLL0 when Translation Profile 0.3 is configured as a hitless external zero-delay profile. The selections of the reference input as the DPLL feedback are meaningless unless Register 0x1263, Bits[1:0] = 11 (binary).	0x00	R/W	Core clock	No
			0	REFA (default). When REFA is configured as a differential input, use this selection (not the REFAA selection).				
			1	REFAA.				
			2	REFB. When REFB is configured as a differential input, use this selection (not the REFBB selection).				
			3	REFBB.				
			4	Auxiliary REF0.				
			5	Auxiliary REF1.				
			6	Auxiliary REF2.				
			7	Auxiliary REF3.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[4:0]	Internal zero-delay feedback path		DPLL0 Internal Zero-Delay Feedback Path. This 5-bit field (default = 0) selects a Q divider output as the feedback return path for DPLL0 when Translation Profile 0.3 is configured as a hitless internal zero-delay profile. The selections of the Q divider output as the DPLL feedback return path are meaningless unless Register 0x1263, Bits[1:0] = 01 (binary).	0x00	R/W	Core clock	No
			0	Q0A Output as DPLL0 Feedback (default). When OUT0A is configured for differential mode, use this selection (not the Q0AA feedback selection).				
			1	Q0AA Output as DPLL0 Feedback.				
			2	Q0B Output as DPLL0 Feedback. When OUT0B is configured for differential mode, use this selection (not the Q0BB feedback selection).				
			3	Q0BB Output as DPLL0 Feedback.				
			4	Q0C Output as DPLL0 Feedback. When OUT0C is configured for differential mode, use this selection (not the Q0CC feedback selection).				
			5	Q0CC Output as DPLL0 Feedback.				
0x1263	7	Translation Profile 0.3 loop filter base		DPLL0 Loop Filter Base. This bit (default = 0) assigns one of the loop filter base coefficient sets (LFx) to DPLL0.	0	R/W	Core clock	No
			0	LF0 (default). Nominal 70° phase margin.				
			1	LF1. Nominal 88.5° phase margin (use this setting for applications requiring the response of the closed-loop transfer function of DPLL0 to have <0.1 dB peaking).				
	[6:5]	Reserved		Reserved.	0x0	R/W	Core clock	No
	[4:2]	Translation Profile 0.3 tag mode		DPLL0 Tag Modes. This 3-bit unsigned value (default = 0) selects the DPLL0 tag mode for Translation Profile 0.3.	0x0	R/W	Core clock	No
			0	No tagged time stamps in the reference or feedback path of DPLL0 (default).				
			1	Tagged time stamps only in the reference path of DPLL0.				
			2	Tagged time stamps only in the feedback path of DPLL0.				
			3	Tagged time stamps in the reference and feedback paths of DPLL0, but the untagged rates differ.				
			4	Tagged time stamps in the reference and feedback paths of DPLL0, but the untagged rates are equal.				
	[1:0]	Translation Profile 0.3 loop mode		DPLL0 Frequency Translation Mode. This 2-bit unsigned value (default = 0) establishes the frequency translation mode for DPLL0.	0x0	R/W	Core clock	No
			0	Phase buildout mode (default).				
			1	Hitless, internal zero delay mode.				
			3	Hitless, external zero delay mode.				
0x1264	[7:0]	Translation Profile 0.3 Loop Bandwidth[7:0]		DPLL0 Loop Bandwidth Scale Factor. This 32-bit unsigned value (default = 0) constitutes a scale factor (SF) applied to the base loop bandwidth (LBW_0) associated with the coefficients of Loop Filter LF0 or LF1. The resulting loop bandwidth (LBW) is LBW = SF × LBW_0. The default coefficients of LF0 and LF1 yield LBW_0 = 1 µHz (10^{-6} Hz). For example, given SF = 50,000,000, then LBW = 50 Hz for LF0 or LF1.	0x00	R/W	Core clock	No
0x1265	[7:0]	Translation Profile 0.3 Loop Bandwidth[15:8]		Continuation of the Translation Profile 0.3 loop bandwidth bit field. See the Translation Profile 0.3 Loop Bandwidth[7:0] description.	0x00	R/W	Core clock	No
0x1266	[7:0]	Translation Profile 0.3 Loop Bandwidth[23:16]		Continuation of the Translation Profile 0.3 loop bandwidth bit field. See the Translation Profile 0.3 Loop Bandwidth[7:0] description.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1267	[7:0]	Translation Profile 0.3 Loop Bandwidth[31:24]		Continuation of the Translation Profile 0.3 loop bandwidth bit field. See the Translation Profile 0.3 Loop Bandwidth[7:0] description.	0x00	R/W	Core clock	No
0x1268	[7:0]	Translation Profile 0.3 Hitless N Divider[7:0]		DPLL0 Feedback Divider (N): Hitless Zero-Delay Operation. This 32-bit unsigned value, N Hitless (default = 4000), sets the divide ratio, N, for the feedback divider of DPLL0 when the DPLL operates in internal hitless zero delay mode. $N = N\,Hitless + 1$ Thus, the default value yields N = 4001. A translation profile configured for external zero delay hitless DPLL operation uses Register 0x126F to Register 0x126C, Bits[31:0] instead of this register.	0x160	R/W	Core clock	No
0x1269	[7:0]	Translation Profile 0.3 Hitless N Divider[15:8]		Continuation of the Translation Profile 0.3 hitless N divider bit field. See the Translation Profile 0.3 Hitless N Divider[7:0] description.	0x15	R/W	Core clock	No
0x126A	[7:0]	Translation Profile 0.3 Hitless N Divider[23:16]		Continuation of the Translation Profile 0.3 hitless N divider bit field. See the Translation Profile 0.3 Hitless N Divider[7:0] description.	0x00	R/W	Core clock	No
0x126B	[7:0]	Translation Profile 0.3 Hitless N Divider[31:24]		Continuation of the Translation Profile 0.3 hitless N divider bit field. See the Translation Profile 0.3 Hitless N Divider[7:0] description.	0x00	R/W	Core clock	No
0x126C	[7:0]	Translation Profile 0.3 Buildout N Divider[7:0]		DPLL0 Feedback Divider (N_int): Phase Buildout Operation. This 32-bit unsigned value, $N\_int_{BUILDOUT}$ (default = 4000), sets the integer part of the divide ratio, N, for the feedback divider of DPLL0 when the DPLL operates in phase buildout mode. $N = N\_int_{BUILDOUT} + 1$ Thus, the default value yields N = 4001.	0x160	R/W	Core clock	No
0x126D	[7:0]	Translation Profile 0.3 Buildout N Divider[15:8]		Continuation of the Translation Profile 0.3 buildout N divider bit field. See the Translation Profile 0.3 Buildout N Divider[7:0] description.	0x15	R/W	Core clock	No
0x126E	[7:0]	Translation Profile 0.3 Buildout N Divider[23:16]		Continuation of the Translation Profile 0.3 buildout N divider bit field. See the Translation Profile 0.3 Buildout N Divider[7:0] description.	0x00	R/W	Core clock	No
0x126F	[7:0]	Translation Profile 0.3 Buildout N Divider[31:24]		Continuation of the Translation Profile 0.3 buildout N divider bit field. See the Translation Profile 0.3 Buildout N Divider[7:0] description.	0x00	R/W	Core clock	No
0x1270	[7:0]	Translation Profile 0.3 Buildout FRAC[7:0]		DPLL0 Feedback Divider (N_num): Phase Buildout Operation. This 24-bit unsigned value, $N\_num_{BUILDOUT}$ (default = 0), is the numerator of the fractional portion of the feedback divider of DPLL0 when the DPLL operates in phase buildout mode. The total divide ratio is as follows: $N\_total = (N\_int_{BUILDOUT} + 1) + (N\_num/N\_den)$ where: *N_den* is the denominator of the fractional portion of the feedback divider, which resides in Register 0x1275 to Register 0x1273, Bits[23:0]. $N\_num < N\_den$. To make N_total an integer, program N_num = 0 and N_den = 0.	0x00	R/W	Core clock	No
0x1271	[7:0]	Translation Profile 0.3 Buildout FRAC[15:8]		Continuation of the Translation Profile 0.3 buildout FRAC bit field. See the Translation Profile 0.3 Buildout FRAC[7:0] description.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1272	[7:0]	Translation Profile 0.3 Buildout FRAC[23:16]		Continuation of the Translation Profile 0.3 buildout FRAC bit field. See the Translation Profile 0.3 Buildout FRAC[7:0] description.	0x00	R/W	Core clock	No
0x1273	[7:0]	Translation Profile 0.3 Buildout MOD[7:0]		DPLL0 Feedback Divider (N_den): Phase Buildout Operation. This 24-bit unsigned value, $N\_den_{BUILDOUT}$ (default = 0), is the denominator of the fractional portion of the feedback divider of DPLL0 when the DPLL operates in phase buildout mode. The total divide ratio is as follows: $N\_total = (N\_int_{BUILDOUT} + 1) + (N\_num/N\_den)$ where *N_num* is the numerator of the fractional portion of the feedback divider, which resides in Register 0x1272 to Register 0x1270, Bits[23:0]. *N_num* < *N_den*. To make the N divider divide ratio an integer, program *N_num* = 0 and *N_den* = 0.	0x00	R/W	Core clock	No
0x1274	[7:0]	Translation Profile 0.3 Buildout MOD[15:8]		Continuation of the Translation Profile 0.3 buildout MOD bit field. See the Translation Profile 0.3 Buildout MOD[7:0] description.	0x00	R/W	Core clock	No
0x1275	[7:0]	Translation Profile 0.3 Buildout MOD[23:16]		Continuation of the Translation Profile 0.3 buildout MOD bit field. See the Translation Profile 0.3 Buildout MOD[7:0] description.	0x00	R/W	Core clock	No
0x1276	[7:4]	Reserved		Reserved.	0x0	R/W	Core clock	No
	[3:0]	Translation Profile 0.3 fast acquisition excess bandwidth		DPLL0 Fast Acquisition Excess Bandwidth Factor. This 3-bit unsigned value, ESF (default = 0), controls the behavior of the fast acquisition option for DPLL0, where ESF = 0 disables the fast acquisition feature. ESF constitutes an exponential scale factor applied to the nominal loop bandwidth of the DPLL (BW_0) to yield an excess bandwidth, EBW, as follows: $EBW = BW_0 \times 2^{ESF}$ The fast acquisition controller sets the loop bandwidth of the DPLL to EBW at the start of an acquisition sequence. When the DPLL indicates phase lock, the fast acquisition controller halves the loop bandwidth. The fast acquisition controller again waits for the DPLL to indicate phase lock. When the DPLL indicates phase lock, the fast acquisition controller again halves the loop bandwidth. The process repeats until the DPLL loop bandwidth reaches BW_0. The fast acquisition controller sets Register 0x3102, Bit 4 = 1 while sequencing through the loop bandwidth reduction steps to indicate its active status.	0x0	R/W	Core clock	No
			0	Fast acquisition controller disabled (default).				
			1	ESF = 1.				
			2	ESF = 2.				
			3	ESF = 3.				
			4	ESF = 4.				
			5	ESF = 5.				
			6	ESF = 6.				
			7	ESF = 7.				
			8	ESF = 8.				
			9	ESF = 9.				
			10	ESF = 10.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1277	7	Reserved		Reserved.	0	R	Live	No
	[6:4]	Translation Profile 0.3 fast acquisition timeout		DPLL0 Fast Acquisition Timeout. This 3-bit unsigned value puts a time limit (t_{MAX}) on how long the fast acquisition controller waits for chatter free DPLL phase lock status to occur during each loop bandwidth reduction step. If the phase lock guard timer (see Bits[2:0]) fails to time out by t_{MAX}, the fast acquisition controller automatically moves on to the next loop bandwidth reduction step even though chatter free phase lock failed to occur. The fast acquisition controller indicates completion of the fast acquisition process by setting Register 0x3102, Bit 5 = 1 only when the fast acquisition controller is in its final bandwidth reduction step and the t_{MAX} timer fails to expire.	0x0	R/W	Core clock	No
			0	t_{MAX} = 10 ms (default).				
			1	t_{MAX} = 50 ms.				
			2	t_{MAX} = 100 ms.				
			3	t_{MAX} = 500 ms.				
			4	t_{MAX} = 1 sec.				
			5	t_{MAX} = 10 sec.				
			6	t_{MAX} = 50 sec.				
			7	t_{MAX} = 100 sec.				
	3	Reserved		Reserved.	0	R	Live	No
	[2:0]	Translation Profile 0.3 fast acquisition lock settle time		DPLL0 Fast Acquisition Phase Lock Guard Time. This 3-bit unsigned value, GUARD_TIME (default = 0), sets the period (t_{GUARD}) of a countdown timer used by the fast acquisition controller. The countdown timer starts when the DPLL indicates phase lock, but the fast acquisition controller reloads the countdown timer with a value per GUARD_TIME whenever the DPLL indicates phase unlock. It is only upon timeout of the countdown timer that the fast acquisition controller moves on to its next bandwidth reduction step. t_{GUARD} constitutes the minimum amount of time the fast acquisition controller must observe chatter free DPLL phase lock status during each loop bandwidth reduction step.	0x0	R/W	Core clock	No
			0	t_{GUARD} = 1 ms (default).				
			1	t_{GUARD} = 10 ms.				
			2	t_{GUARD} = 50 ms.				
			3	t_{GUARD} = 100 ms.				
			4	t_{GUARD} = 500 ms.				
			5	t_{GUARD} = 1 sec.				
			6	t_{GUARD} = 10 sec.				
			7	t_{GUARD} = 50 sec.				

TRANSLATION PROFILE 0.4 PARAMETERS—REGISTER 0x1280 TO REGISTER 0x1297

Table 69. Translation Profile 0.4 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1280	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	[5:1]	Translation Profile 0.4 selection priority		Translation Profile 0.4 Priority Value. This 5-bit unsigned value (default = 0) allows the user to assign a priority level to Translation Profile 0.4. Priority assignment (highest priority = 0, lowest priority = 31) allows DPLL0 to select one translation profile over another when reference switching.	0x00	R/W	Core clock	No
	0	Enable Translation Profile 0.4		Translation Profile 0.4 Enable. This bit enables Translation Profile 0.4 as a usable translation profile for DPLL0.	0	R/W	Core clock	No
			0	Disabled (default).				
			1	Enabled.				
0x1281	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:0]	Translation Profile 0.4 reference source selection		DPLL0 Reference Source Selection. This 5-bit unsigned value (default = 0) assigns a time stamp source as the input to DPLL0 when the DPLL activates Translation Profile 0.4.	0x00	R/W	Core clock	No
			0	REFA (default).				
			1	REFAA.				
			2	REFB.				
			3	REFBB.				
			5	Feedback from DPLL1.				
			6	Auxiliary REF0.				
			7	Auxiliary REF1.				
			8	Auxiliary NCO 0.				
			9	Auxiliary NCO 1.				
			11	Auxiliary REF2.				
			12	Auxiliary REF3.				
			13	Inverse User Time Stamper 0.				
			14	Inverse User Time Stamper 1.				
0x1282	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:0]	External zero delay feedback path		DPLL0 External Zero-Delay Feedback Path. This 5-bit field (default = 0) selects a reference input as the feedback return path for DPLL0 when Translation Profile 0.4 is configured as a hitless external zero-delay profile. The selections of the reference input as the DPLL feedback are meaningless unless Register 0x1283, Bits[1:0] = 11 (binary).	0x00	R/W	Core clock	No
			0	REFA (default). When REFA is configured as a differential input, use this selection (not the REFAA selection).				
			1	REFAA.				
			2	REFB. When REFB is configured as a differential input, use this selection (not the REFBB selection).				
			3	REFBB.				
			4	Auxiliary REF0.				
			5	Auxiliary REF1.				
			6	Auxiliary REF2.				
			7	Auxiliary REF3.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[4:0]	Internal zero-delay feedback path		DPLL0 Internal Zero-Delay Feedback Path. This 5-bit field (default = 0) selects a Q divider output as the feedback return path for DPLL0 when Translation Profile 0.4 is configured as a hitless internal zero-delay profile. The selections of the Q divider output as the DPLL feedback return path are meaningless unless Register 0x1283, Bits[1:0] = 01 (binary).	0x00	R/W	Core clock	No
			0	Q0A Output as DPLL0 Feedback (default). When OUT0A is configured for differential mode, use this selection (not the Q0AA feedback selection).				
			1	Q0AA Output as DPLL0 Feedback.				
			2	Q0B Output as DPLL0 Feedback. When OUT0B is configured for differential mode, use this selection (not the Q0BB feedback selection).				
			3	Q0BB Output as DPLL0 Feedback.				
			4	Q0C Output as DPLL0 Feedback. When OUT0C is configured for differential mode, use this selection (not the Q0CC feedback selection).				
			5	Q0CC Output as DPLL0 Feedback.				
0x1283	7	Translation Profile 0.4 loop filter base		DPLL0 Loop Filter Base. This bit (default = 0) assigns one of the loop filter base coefficient sets (LFx) to DPLL0.	0	R/W	Core clock	No
			0	LF0 (default). Nominal 70° phase margin.				
			1	LF1. Nominal 88.5° phase margin (use this setting for applications requiring the response of the closed-loop transfer function of DPLL0 to have <0.1 dB peaking).				
	[6:5]	Reserved		Reserved.	0x0	R/W	Core clock	No
	[4:2]	Translation Profile 0.4 tag mode		DPLL0 Tag Modes. This 3-bit unsigned value (default = 0) selects the DPLL0 tag mode for Translation Profile 0.4.	0x0	R/W	Core clock	No
			0	No tagged time stamps in the reference or feedback path of DPLL0 (default).				
			1	Tagged time stamps only in the reference path of DPLL0.				
			2	Tagged time stamps only in the feedback path of DPLL0.				
			3	Tagged time stamps in the reference and feedback paths of DPLL0, but the untagged rates differ.				
			4	Tagged time stamps in the reference and feedback paths of DPLL0, but the untagged rates are equal.				
	[1:0]	Translation Profile 0.4 loop mode		DPLL0 Frequency Translation Mode. This 2-bit unsigned value (default = 0) establishes the frequency translation mode for DPLL0.	0x0	R/W	Core clock	No
			0	Phase buildout mode (default).				
			1	Hitless, internal zero delay mode.				
			3	Hitless, external zero delay mode.				
0x1284	[7:0]	Translation Profile 0.4 Loop Bandwidth[7:0]		DPLL0 Loop Bandwidth Scale Factor. This 32-bit unsigned value (default = 0) constitutes a scale factor (SF) applied to the base loop bandwidth (LBW_0) associated with the coefficients of Loop Filter LF0 or LF1. The resulting loop bandwidth (LBW) is LBW = SF × LBW_0. The default coefficients of LF0 and LF1 yield LBW_0 = 1 µHz (10^{-6} Hz). For example, given SF = 50,000,000, then LBW = 50 Hz for LF0 or LF1.	0x00	R/W	Core clock	No
0x1285	[7:0]	Translation Profile 0.4 Loop Bandwidth[15:8]		Continuation of the Translation Profile 0.4 loop bandwidth bit field. See the Translation Profile 0.4 Loop Bandwidth[7:0] description.	0x00	R/W	Core clock	No
0x1286	[7:0]	Translation Profile 0.4 Loop Bandwidth[23:16]		Continuation of the Translation Profile 0.4 loop bandwidth bit field. See the Translation Profile 0.4 Loop Bandwidth[7:0] description.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1287	[7:0]	Translation Profile 0.4 Loop Bandwidth[31:24]		Continuation of the Translation Profile 0.4 loop bandwidth bit field. See the Translation Profile 0.4 Loop Bandwidth[7:0] description.	0x00	R/W	Core clock	No
0x1288	[7:0]	Translation Profile 0.4 Hitless N Divider[7:0]		DPLL0 Feedback Divider (N): Hitless Zero-Delay Operation. This 32-bit unsigned value, N Hitless (default = 4000), sets the divide ratio, N, for the feedback divider of DPLL0 when the DPLL operates in internal hitless zero delay mode. $N = N\ Hitless + 1$ Thus, the default value yields N = 4001. A translation profile configured for external zero delay hitless DPLL operation uses Register 0x128F to Register 0x128C, Bits[31:0] instead of this register.	0x160	R/W	Core clock	No
0x1289	[7:0]	Translation Profile 0.4 Hitless N Divider[15:8]		Continuation of the Translation Profile 0.4 hitless N divider bit field. See the Translation Profile 0.4 Hitless N Divider[7:0] description.	0x15	R/W	Core clock	No
0x128A	[7:0]	Translation Profile 0.4 Hitless N Divider[23:16]		Continuation of the Translation Profile 0.4 hitless N divider bit field. See the Translation Profile 0.4 Hitless N Divider[7:0] description.	0x00	R/W	Core clock	No
0x128B	[7:0]	Translation Profile 0.4 Hitless N Divider[31:24]		Continuation of the Translation Profile 0.4 hitless N divider bit field. See the Translation Profile 0.4 Hitless N Divider[7:0] description.	0x00	R/W	Core clock	No
0x128C	[7:0]	Translation Profile 0.4 Buildout N Divider[7:0]		DPLL0 Feedback Divider (N_int): Phase Buildout Operation. This 32-bit unsigned value, $N\_int_{BUILDOUT}$ (default = 4000), sets the integer part of the divide ratio, N, for the feedback divider of DPLL0 when the DPLL operates in phase buildout mode. $N = N\_int_{BUILDOUT} + 1$ Thus, the default value yields N = 4001.	0x160	R/W	Core clock	No
0x128D	[7:0]	Translation Profile 0.4 Buildout N Divider[15:8]		Continuation of the Translation Profile 0.4 buildout N divider bit field. See the Translation Profile 0.4 Buildout N Divider[7:0] description.	0x15	R/W	Core clock	No
0x128E	[7:0]	Translation Profile 0.4 Buildout N Divider[23:16]		Continuation of the Translation Profile 0.4 buildout N divider bit field. See the Translation Profile 0.4 Buildout N Divider[7:0] description.	0x00	R/W	Core clock	No
0x128F	[7:0]	Translation Profile 0.4 Buildout N Divider[31:24]		Continuation of the Translation Profile 0.4 buildout N divider bit field. See the Translation Profile 0.4 Buildout N Divider[7:0] description.	0x00	R/W	Core clock	No
0x1290	[7:0]	Translation Profile 0.4 Buildout FRAC[7:0]		DPLL0 Feedback Divider (N_num): Phase Buildout Operation. This 24-bit unsigned value, $N\_num_{BUILDOUT}$ (default = 0), is the numerator of the fractional portion of the feedback divider of DPLL0 when the DPLL operates in phase buildout mode. The total divide ratio is as follows: $N\_total = (N\_int_{BUILDOUT} + 1) + (N\_num/N\_den)$ where: *N_den* is the denominator of the fractional portion of the feedback divider, which resides in Register 0x1295 to Register 0x1293, Bits[23:0]. $N\_num < N\_den$. To make N_total an integer, program N_num = 0 and N_den = 0.	0x00	R/W	Core clock	No
0x1291	[7:0]	Translation Profile 0.4 Buildout FRAC[15:8]		Continuation of the Translation Profile 0.4 buildout FRAC bit field. See the Translation Profile 0.4 Buildout FRAC[7:0] description.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1292	[7:0]	Translation Profile 0.4 Buildout FRAC[23:16]		Continuation of the Translation Profile 0.4 buildout FRAC bit field. See the Translation Profile 0.4 Buildout FRAC[7:0] description.	0x00	R/W	Core clock	No
0x1293	[7:0]	Translation Profile 0.4 Buildout MOD[7:0]		DPLL0 Feedback Divider (N_den): Phase Buildout Operation. This 24-bit unsigned value, $N\_den_{BUILDOUT}$ (default = 0), is the denominator of the fractional portion of the feedback divider of DPLL0 when the DPLL operates in phase buildout mode. The total divide ratio is as follows: $N\_total = (N\_int_{BUILDOUT} + 1) + (N\_num/N\_den)$ where *N_num* is the numerator of the fractional portion of the feedback divider, which resides in Register 0x1292 to Register 0x1290, Bits[23:0]. *N_num* < *N_den*. To make the N divider divide ratio an integer, program *N_num* = 0 and *N_den* = 0.	0x00	R/W	Core clock	No
0x1294	[7:0]	Translation Profile 0.4 Buildout MOD[15:8]		Continuation of the Translation Profile 0.4 buildout MOD bit field. See the Translation Profile 0.4 Buildout MOD[7:0] description.	0x00	R/W	Core clock	No
0x1295	[7:0]	Translation Profile 0.4 Buildout MOD[23:16]		Continuation of the Translation Profile 0.4 buildout MOD bit field. See the Translation Profile 0.4 Buildout MOD[7:0] description.	0x00	R/W	Core clock	No
0x1296	[7:4]	Reserved		Reserved.	0x0	R/W	Core clock	No
	[3:0]	Translation Profile 0.4 fast acquisition excess bandwidth		DPLL0 Fast Acquisition Excess Bandwidth Factor. This 3-bit unsigned value, ESF (default = 0), controls the behavior of the fast acquisition option for DPLL0, where ESF = 0 disables the fast acquisition feature. ESF constitutes an exponential scale factor applied to the nominal loop bandwidth of the DPLL (BW_0) to yield an excess bandwidth, EBW, as follows: $EBW = BW_0 \times 2^{ESF}$ The fast acquisition controller sets the loop bandwidth of the DPLL to EBW at the start of an acquisition sequence. When the DPLL indicates phase lock, the fast acquisition controller halves the loop bandwidth. The fast acquisition controller again waits for the DPLL to indicate phase lock. When the DPLL indicates phase lock, the fast acquisition controller again halves the loop bandwidth. The process repeats until the DPLL loop bandwidth reaches BW_0. The fast acquisition controller sets Register 0x3102, Bit 4 = 1 while sequencing through the loop bandwidth reduction steps to indicate its active status. 0 Fast acquisition controller disabled (default). 1 ESF = 1. 2 ESF = 2. 3 ESF = 3. 4 ESF = 4. 5 ESF = 5. 6 ESF = 6. 7 ESF = 7. 8 ESF = 8. 9 ESF = 9. 10 ESF = 10.	0x0	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1297	7	Reserved		Reserved.	0	R	Live	No
	[6:4]	Translation Profile 0.4 fast acquisition timeout		DPLL0 Fast Acquisition Timeout. This 3-bit unsigned value puts a time limit (t_{MAX}) on how long the fast acquisition controller waits for chatter free DPLL phase lock status to occur during each loop bandwidth reduction step. If the phase lock guard timer (see Bits[2:0]) fails to time out by t_{MAX}, the fast acquisition controller automatically moves on to the next loop bandwidth reduction step even though chatter free phase lock failed to occur. The fast acquisition controller indicates completion of the fast acquisition process by setting Register 0x3102, Bit 5 = 1 only when the fast acquisition controller is in its final bandwidth reduction step and the t_{MAX} timer fails to expire.	0x0	R/W	Core clock	No
			0	t_{MAX} = 10 ms (default).				
			1	t_{MAX} = 50 ms.				
			2	t_{MAX} = 100 ms.				
			3	t_{MAX} = 500 ms.				
			4	t_{MAX} = 1 sec.				
			5	t_{MAX} = 10 sec.				
			6	t_{MAX} = 50 sec.				
			7	t_{MAX} = 100 sec.				
	3	Reserved		Reserved.	0	R	Live	No
	[2:0]	Translation Profile 0.4 fast acquisition lock settle time		DPLL0 Fast Acquisition Phase Lock Guard Time. This 3-bit unsigned value, GUARD_TIME (default = 0), sets the period (t_{GUARD}) of a countdown timer used by the fast acquisition controller. The countdown timer starts when the DPLL indicates phase lock, but the fast acquisition controller reloads the countdown timer with a value per GUARD_TIME whenever the DPLL indicates phase unlock. It is only upon timeout of the countdown timer that the fast acquisition controller moves on to its next bandwidth reduction step. t_{GUARD} constitutes the minimum amount of time the fast acquisition controller must observe chatter free DPLL phase lock status during each loop bandwidth reduction step.	0x0	R/W	Core clock	No
			0	t_{GUARD} = 1 ms (default).				
			1	t_{GUARD} = 10 ms.				
			2	t_{GUARD} = 50 ms.				
			3	t_{GUARD} = 100 ms.				
			4	t_{GUARD} = 500 ms.				
			5	t_{GUARD} = 1 sec.				
			6	t_{GUARD} = 10 sec.				
			7	t_{GUARD} = 50 sec.				

TRANSLATION PROFILE 0.5 PARAMETERS—REGISTER 0x12A0 TO REGISTER 0x12B7

Table 70. Translation Profile 0.5 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x12A0	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	[5:1]	Translation Profile 0.5 selection priority		Translation Profile 0.5 Priority Value. This 5-bit unsigned value (default = 0) allows the user to assign a priority level to Translation Profile 0.5. Priority assignment (highest priority = 0, lowest priority = 31) allows DPLL0 to select one translation profile over another when reference switching.	0x00	R/W	Core clock	No
	0	Enable Translation Profile 0.5		Translation Profile 0.5 Enable. This bit enables Translation Profile 0.5 as a usable translation profile for DPLL0.	0	R/W	Core clock	No
			0	Disabled (default).				
			1	Enabled.				
0x12A1	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:0]	Translation Profile 0.5 reference source selection		DPLL0 Reference Source Selection. This 5-bit unsigned value (default = 0) assigns a time stamp source as the input to DPLL0 when the DPLL activates Translation Profile 0.5.	0x00	R/W	Core clock	No
			0	REFA (default).				
			1	REFAA.				
			2	REFB.				
			3	REFBB.				
			5	Feedback from DPLL1.				
			6	Auxiliary REF0.				
			7	Auxiliary REF1.				
			8	Auxiliary NCO 0.				
			9	Auxiliary NCO 1.				
			11	Auxiliary REF2.				
			12	Auxiliary REF3.				
			13	Inverse User Time Stamper 0.				
			14	Inverse User Time Stamper 1.				
0x12A2	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:0]	External zero-delay feedback path		DPLL0 External Zero-Delay Feedback Path. This 5-bit field (default = 0) selects a reference input as the feedback return path for DPLL0 when Translation Profile 0.5 is configured as a hitless external zero-delay profile. The selections of the reference input as the DPLL feedback are meaningless unless Register 0x12A3, Bits[1:0] = 11 (binary).	0x00	R/W	Core clock	No
			0	REFA (default). When REFA is configured as a differential input, use this selection (not the REFAA selection).				
			1	REFAA.				
			2	REFB. When REFB is configured as a differential input, use this selection (not the REFBB selection).				
			3	REFBB.				
			4	Auxiliary REF0.				
			5	Auxiliary REF1.				
			6	Auxiliary REF2.				
			7	Auxiliary REF3.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[4:0]	Internal zero-delay feedback path		DPLL0 Internal Zero-Delay Feedback Path. This 5-bit field (default = 0) selects a Q divider output as the feedback return path for DPLL0 when Translation Profile 0.5 is configured as a hitless internal zero-delay profile. The selections of the Q divider output as the DPLL feedback return path are meaningless unless Register 0x12A3, Bits[1:0] = 01 (binary).	0x00	R/W	Core clock	No
			0	Q0A Output as DPLL0 Feedback (default). When OUT0A is configured for differential mode, use this selection (not the Q0AA feedback selection).				
			1	Q0AA Output as DPLL0 Feedback.				
			2	Q0B Output as DPLL0 Feedback. When OUT0B is configured for differential mode, use this selection (not the Q0BB feedback selection).				
			3	Q0BB Output as DPLL0 Feedback.				
			4	Q0C Output as DPLL0 Feedback. When OUT0C is configured for differential mode, use this selection (not the Q0CC feedback selection).				
			5	Q0CC Output as DPLL0 Feedback.				
0x12A3	7	Translation Profile 0.5 loop filter base		DPLL0 Loop Filter Base. This bit (default = 0) assigns one of the loop filter base coefficient sets (LFx) to DPLL0.	0	R/W	Core clock	No
			0	LF0 (default). Nominal 70° phase margin.				
			1	LF1. Nominal 88.5° phase margin (use this setting for applications requiring the response of the closed-loop transfer function of DPLL0 to have <0.1 dB peaking).				
	[6:5]	Reserved		Reserved.	0x0	R/W	Core clock	No
	[4:2]	Translation Profile 0.5 tag mode		DPLL0 Tag Modes. This 3-bit unsigned value (default = 0) selects the DPLL0 tag mode for Translation Profile 0.5.	0x0	R/W	Core clock	No
			0	No tagged time stamps in the reference or feedback path of DPLL0 (default).				
			1	Tagged time stamps only in the reference path of DPLL0.				
			2	Tagged time stamps only in the feedback path of DPLL0.				
			3	Tagged time stamps in the reference and feedback paths of DPLL0, but the untagged rates differ.				
			4	Tagged time stamps in the reference and feedback paths of DPLL0, but the untagged rates are equal.				
	[1:0]	Translation Profile 0.5 loop mode		DPLL0 Frequency Translation Mode. This 2-bit unsigned value (default = 0) establishes the frequency translation mode for DPLL0.	0x0	R/W	Core clock	No
			0	Phase buildout mode (default).				
			1	Hitless, internal zero delay mode.				
			3	Hitless, external zero delay mode.				
0x12A4	[7:0]	Translation Profile 0.5 Loop Bandwidth[7:0]		DPLL0 Loop Bandwidth Scale Factor. This 32-bit unsigned value (default = 0) constitutes a scale factor (SF) applied to the base loop bandwidth (LBW_0) associated with the coefficients of Loop Filter LF0 or LF1. The resulting loop bandwidth (LBW) is LBW = SF × LBW_0. The default coefficients of LF0 and LF1 yield LBW_0 = 1 µHz (10^{-6} Hz). For example, given SF = 50,000,000, then LBW = 50 Hz for LF0 or LF1.	0x00	R/W	Core clock	No
0x12A5	[7:0]	Translation Profile 0.5 Loop Bandwidth[15:8]		Continuation of the Translation Profile 0.5 loop bandwidth bit field. See the Translation Profile 0.5 Loop Bandwidth[7:0] description.	0x00	R/W	Core clock	No
0x12A6	[7:0]	Translation Profile 0.5 Loop Bandwidth[23:16]		Continuation of the Translation Profile 0.5 loop bandwidth bit field. See the Translation Profile 0.5 Loop Bandwidth[7:0] description.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x12A7	[7:0]	Translation Profile 0.5 Loop Bandwidth[31:24]		Continuation of the Translation Profile 0.5 loop bandwidth bit field. See the Translation Profile 0.5 Loop Bandwidth[7:0] description.	0x00	R/W	Core clock	No
0x12A8	[7:0]	Translation Profile 0.5 Hitless N Divider[7:0]		DPLL0 Feedback Divider (N): Hitless Zero-Delay Operation. This 32-bit unsigned value, N Hitless (default = 4000), sets the divide ratio, N, for the feedback divider of DPLL0 when the DPLL operates in internal hitless zero delay mode. $N = N\,Hitless + 1$ Thus, the default value yields N = 4001. A translation profile configured for external zero delay hitless DPLL operation uses Register 0x12AF to Register 0x12AC, Bits[31:0] instead of this register.	0x160	R/W	Core clock	No
0x12A9	[7:0]	Translation Profile 0.5 Hitless N Divider[15:8]		Continuation of the Translation Profile 0.5 hitless N divider bit field. See the Translation Profile 0.5 Hitless N Divider[7:0] description.	0x15	R/W	Core clock	No
0x12AA	[7:0]	Translation Profile 0.5 Hitless N Divider[23:16]		Continuation of the Translation Profile 0.5 hitless N divider bit field. See the Translation Profile 0.5 Hitless N Divider[7:0] description.	0x00	R/W	Core clock	No
0x12AB	[7:0]	Translation Profile 0.5 Hitless N Divider[31:24]		Continuation of the Translation Profile 0.5 hitless N divider bit field. See the Translation Profile 0.5 Hitless N Divider[7:0] description.	0x00	R/W	Core clock	No
0x12AC	[7:0]	Translation Profile 0.5 Buildout N Divider[7:0]		DPLL0 Feedback Divider (N_int): Phase Buildout Operation. This 32-bit unsigned value, $N\_int_{BUILDOUT}$ (default = 4000), sets the integer part of the divide ratio, N, for the feedback divider of DPLL0 when the DPLL operates in phase buildout mode. $N = N\_int_{BUILDOUT} + 1$ Thus, the default value yields N = 4001.	0x160	R/W	Core clock	No
0x12AD	[7:0]	Translation Profile 0.5 Buildout N Divider[15:8]		Continuation of the Translation Profile 0.5 buildout N divider bit field. See the Translation Profile 0.5 Buildout N Divider[7:0] description.	0x15	R/W	Core clock	No
0x12AE	[7:0]	Translation Profile 0.5 Buildout N Divider[23:16]		Continuation of the Translation Profile 0.5 buildout N divider bit field. See the Translation Profile 0.5 Buildout N Divider[7:0] description.	0x00	R/W	Core clock	No
0x12AF	[7:0]	Translation Profile 0.5 Buildout N Divider[31:24]		Continuation of the Translation Profile 0.5 buildout N divider bit field. See the Translation Profile 0.5 Buildout N Divider[7:0] description.	0x00	R/W	Core clock	No
0x12B0	[7:0]	Translation Profile 0.5 Buildout FRAC[7:0]		DPLL0 Feedback Divider (N_num): Phase Buildout Operation. This 24-bit unsigned value, $N\_num_{BUILDOUT}$ (default = 0), is the numerator of the fractional portion of the feedback divider of DPLL0 when the DPLL operates in phase buildout mode. The total divide ratio is as follows: $N\_total = (N\_int_{BUILDOUT} + 1) + (N\_num/N\_den)$ where: *N_den* is the denominator of the fractional portion of the feedback divider, which resides in Register 0x12B5 to Register 0x12B3, Bits[23:0]. $N\_num < N\_den$. To make N_total an integer, program N_num = 0 and N_den = 0.	0x00	R/W	Core clock	No
0x12B1	[7:0]	Translation Profile 0.5 Buildout FRAC[15:8]		Continuation of the Translation Profile 0.5 buildout FRAC bit field. See the Translation Profile 0.5 Buildout FRAC[7:0] description.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x12B2	[7:0]	Translation Profile 0.5 Buildout FRAC[23:16]		Continuation of the Translation Profile 0.5 buildout FRAC bit field. See the Translation Profile 0.5 Buildout FRAC[7:0] description.	0x00	R/W	Core clock	No
0x12B3	[7:0]	Translation Profile 0.5 Buildout MOD[7:0]		DPLL0 Feedback Divider (N_den): Phase Buildout Operation. This 24-bit unsigned value, $N\_den_{BUILDOUT}$ (default = 0), is the denominator of the fractional portion of the feedback divider of DPLL0 when the DPLL operates in phase buildout mode. The total divide ratio is as follows: $N\_total = (N\_int_{BUILDOUT} + 1) + (N\_num/N\_den)$ where *N_num* is the numerator of the fractional portion of the feedback divider, which resides in Register 0x12B2 to Register 0x12B0, Bits[23:0]. *N_num* < *N_den*. To make the N divider divide ratio an integer, program *N_num* = 0 and *N_den* = 0.	0x00	R/W	Core clock	No
0x12B4	[7:0]	Translation Profile 0.5 Buildout MOD[15:8]		Continuation of the Translation Profile 0.5 buildout MOD bit field. See the Translation Profile 0.5 Buildout MOD[7:0] description.	0x00	R/W	Core clock	No
0x12B5	[7:0]	Translation Profile 0.5 Buildout MOD[23:16]		Continuation of the Translation Profile 0.5 buildout MOD bit field. See the Translation Profile 0.5 Buildout MOD[7:0] description.	0x00	R/W	Core clock	No
0x12B6	[7:4]	Reserved		Reserved.	0x0	R/W	Core clock	No
	[3:0]	Translation Profile 0.5 fast acquisition excess bandwidth		DPLL0 Fast Acquisition Excess Bandwidth Factor. This 3-bit unsigned value, ESF (default = 0), controls the behavior of the fast acquisition option for DPLL0, where ESF = 0 disables the fast acquisition feature. ESF constitutes an exponential scale factor applied to the nominal loop bandwidth of the DPLL (BW_0) to yield an excess bandwidth, EBW, as follows: $EBW = BW_0 \times 2^{ESF}$ The fast acquisition controller sets the loop bandwidth of the DPLL to EBW at the start of an acquisition sequence. When the DPLL indicates phase lock, the fast acquisition controller halves the loop bandwidth. The fast acquisition controller again waits for the DPLL to indicate phase lock. When the DPLL indicates phase lock, the fast acquisition controller again halves the loop bandwidth. The process repeats until the DPLL loop bandwidth reaches BW_0. The fast acquisition controller sets Register 0x3102, Bit 4 = 1 while sequencing through the loop bandwidth reduction steps to indicate its active status.	0x0	R/W	Core clock	No
			0	Fast acquisition controller disabled (default).				
			1	ESF = 1.				
			2	ESF = 2.				
			3	ESF = 3.				
			4	ESF = 4.				
			5	ESF = 5.				
			6	ESF = 6.				
			7	ESF = 7.				
			8	ESF = 8.				
			9	ESF = 9.				
			10	ESF = 10.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x12B7	7	Reserved		Reserved.	0	R	Live	No
	[6:4]	Translation Profile 0.5 fast acquisition timeout		DPLL0 Fast Acquisition Timeout. This 3-bit unsigned value puts a time limit (t_{MAX}) on how long the fast acquisition controller waits for chatter free DPLL phase lock status to occur during each loop bandwidth reduction step. If the phase lock guard timer (see Bits[2:0]) fails to time out by t_{MAX}, the fast acquisition controller automatically moves on to the next loop bandwidth reduction step even though chatter free phase lock failed to occur. The fast acquisition controller indicates completion of the fast acquisition process by setting Register 0x3102, Bit 5 = 1 only when the fast acquisition controller is in its final bandwidth reduction step and the t_{MAX} timer fails to expire.	0x0	R/W	Core clock	No
			0	t_{MAX} = 10 ms (default).				
			1	t_{MAX} = 50 ms.				
			2	t_{MAX} = 100 ms.				
			3	t_{MAX} = 500 ms.				
			4	t_{MAX} = 1 sec.				
			5	t_{MAX} = 10 sec.				
			6	t_{MAX} = 50 sec.				
			7	t_{MAX} = 100 sec.				
	3	Reserved		Reserved.	0	R	Live	No
	[2:0]	Translation Profile 0.5 fast acquisition lock settle time		DPLL0 Fast Acquisition Phase Lock Guard Time. This 3-bit unsigned value, GUARD_TIME (default = 0), sets the period (t_{GUARD}) of a countdown timer used by the fast acquisition controller. The countdown timer starts when the DPLL indicates phase lock, but the fast acquisition controller reloads the countdown timer with a value per GUARD_TIME whenever the DPLL indicates phase unlock. It is only upon timeout of the countdown timer that the fast acquisition controller moves on to its next bandwidth reduction step. t_{GUARD} constitutes the minimum amount of time the fast acquisition controller must observe chatter free DPLL phase lock status during each loop bandwidth reduction step.	0x0	R/W	Core clock	No
			0	t_{GUARD} = 1 ms (default).				
			1	t_{GUARD} = 10 ms.				
			2	t_{GUARD} = 50 ms.				
			3	t_{GUARD} = 100 ms.				
			4	t_{GUARD} = 500 ms.				
			5	t_{GUARD} = 1 sec.				
			6	t_{GUARD} = 10 sec.				
			7	t_{GUARD} = 50 sec.				

DPLL1 PARAMETERS—REGISTER 0x1400 TO REGISTER 0x142A

Table 71. DPLL1 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1400	[7:0]	DPLL1 Freerun Tuning Word[7:0]		DPLL1 Freerun Tuning Word. This 46-bit unsigned value, FTW0 (default = 0), constitutes the frequency tuning word that DPLL1 uses when in freerun mode. FTW0 relates to the desired DPLL output frequency (f) and the system clock PLL VCO frequency (f_S) as follows: $FTW0 = \text{round}(2^{48} \times (f/f_S))$ To determine the output frequency generated by the DPLL NCO (f_{NCO}) when the DPLL is in freerun mode, use the following computations: $INT = \text{floor}(2^{48}/FTW0)$ where: $7 \le \text{INT} \le 13$. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction. $FRAC = 2^{-30} \times \text{round}(2^{30} \times ((2^{48}/FTW0) - INT))$ where: $0.05 \le FRAC \le 0.95$. round(x) means round x to the nearest integer. $f_{NCO} = f_S/(INT + FRAC)$ For example, given f = 305 MHz and f_S = 2400 MHz, then INT = 7, FRAC = 0.868852458894252777099609375, f_{NCO} = 305.000000004734223087702167268 34 MHz.	0x00	R/W	Core clock	No
0x1401	[7:0]	DPLL1 Freerun Tuning Word[15:8]		Continuation of the DPLL1 freerun tuning word bit field. See the DPLL1 Freerun Tuning Word[7:0] description.	0x00	R/W	Core clock	No
0x1402	[7:0]	DPLL1 Freerun Tuning Word[23:16]		Continuation of the DPLL1 freerun tuning word bit field. See the DPLL1 Freerun Tuning Word[7:0] description.	0x00	R/W	Core clock	No
0x1403	[7:0]	DPLL1 Freerun Tuning Word[31:24]		Continuation of the DPLL1 freerun tuning word bit field. See the DPLL1 Freerun Tuning Word[7:0] description.	0x00	R/W	Core clock	No
0x1404	[7:0]	DPLL1 Freerun Tuning Word[39:32]		Continuation of the DPLL1 freerun tuning word bit field. See the DPLL1 Freerun Tuning Word[7:0] description.	0x00	R/W	Core clock	No
0x1405	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	[5:0]	DPLL1 Freerun Tuning Word[45:40]		Continuation of the DPLL1 freerun tuning word bit field. See the DPLL1 Freerun Tuning Word[7:0] description.	0x00	R/W	Core clock	No
0x1406	[7:0]	DPLL1 FTW Offset Clamp[7:0]		DPLL1 FTW Offset Clamp. This 24-bit unsigned value, Frequency Clamp Value (default = 16,777,215) constitutes a frequency clamp magnitude, f_{CLAMP} (Hz), for DPLL1. Frequency Clamp Value (rounded to the nearest integer) relates to f_{CLAMP} as follows: $\text{Frequency Clamp Value} = (f_{CLAMP}/f_S) \times 2^{36}$ where f_S is the frequency at the output of the system clock PLL VCO. For example, given $f_{CLAMP} = 10^4$ Hz (10 kHz) and $f_S = 2.4 \times 10^9$ Hz (2.4 GHz), then Frequency Clamp Value = 286,331 (0x045E7B). f_{CLAMP} enforces an output frequency range (f_{RNG}) on DPLL1 such that $f_{RNG} = f_0 \pm f_{CLAMP}$, where f_0 is the value of f_{NCO} resulting from FTW0 (see Register 0x1400 for f_{NCO} and FTW0). For f_S = 2.4 GHz, the default frequency clamp value establishes a ±586 kHz bound about f_0.	0x255	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1407	[7:0]	DPLL1 FTW Offset Clamp[15:8]		Continuation of the DPLL1 FTW offset clamp bit field. See the DPLL1 FTW Offset Clamp[7:0] description.	0x255	R/W	Core clock	No
0x1408	[7:0]	DPLL1 FTW Offset Clamp[23:16]		Continuation of the DPLL1 FTW offset clamp bit field. See the DPLL1 FTW Offset Clamp[7:0] description.	0x255	R/W	Core clock	No
0x1409	[7:4]	Reserved		Reserved.	0x0	R/W	Core clock	No
	[3:0]	DPLL1 NCO gain FTW filter bandwidth		DPLL1 NCO Gain FTW Filter Bandwidth. This 4-bit unsigned value sets the cutoff frequency (−3 dB) of a low-pass filter that applies a variable gain to the FTWs applied to the NCO of DPLL1. The variable gain compensates for the nonlinear gain associated with the SDM that comprises the NCO.	0x0	R/W	Core clock	No
			0x0	248 kHz (maximum setting) (default).				
			0x1	124 kHz.				
			0x2	62 kHz.				
			0x3	31 kHz.				
			0x4	15.5 kHz.				
			0x5	7.8 kHz.				
			0x6	3.9 kHz.				
			0x7	1.9 kHz.				
			0x8	970 Hz.				
			0x9	490 Hz.				
			0xa	240 Hz.				
			0xb	120 Hz.				
			0xc	61 Hz.				
			0xd	30 Hz.				
			0xe	15 Hz.				
			0xf	7.6 Hz (minimum setting).				
0x140A	[7:0]	DPLL1 History Accumulation Timer[7:0]		DPLL1 History Accumulation Timer. This 28-bit unsigned value, DPLL1 History Accumulation Timer in units of milliseconds (default = 10), constitutes an averaging period, t_{ACCUM} (seconds). DPLL1 History Accumulation Timer (rounded to the nearest integer) relates to t_{ACCUM} as follows: $DPLL1\ History\ Accumulation\ Timer = 1000 \times t_{ACCUM}$ For example, given t_{ACCUM} = 900 sec (15 min), then DPLL1 History Accumulation Timer = 900,000 (0x 00D BBA0). t_{ACCUM} constitutes an averaging period for processing the holdover tuning word value. The default value sets t_{ACCUM} = 10 ms, but the available range is 1 ms to 268,435.455 sec (~74.5 hours). DPLL1 History Accumulation Timer = 0 is a special case that routes tuning word samples from the digital loop filter to both the DPLL1 NCO and Register 0x3108 to Register 0x3103, Bits[46:0] (bypassing the tuning word history processor). This makes it possible for the user to monitor tuning words applied to the DPLL NCO as they arrive from the loop filter.	0x10	R/W	Core clock	No
0x140B	[7:0]	DPLL1 History Accumulation Timer[15:8]		Continuation of the DPLL1 history accumulation timer bit field. See the DPLL1 History Accumulation Timer[7:0] description.	0x00	R/W	Core clock	No
0x140C	[7:0]	DPLL1 History Accumulation Timer[23:16]		Continuation of the DPLL1 history accumulation timer bit field. See the DPLL1 History Accumulation Timer[7:0] description.	0x00	R/W	Core clock	No
0x140D	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	[3:0]	DPLL1 History Accumulation Timer[27:24]		Continuation of the DPLL1 history accumulation timer bit field. See the DPLL1 History Accumulation Timer[7:0] description.	0x0	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x140E	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	DPLL1 delay history while slewing		DPLL1 Delay History Until Phase Slew Limit Inactive. By default, as soon as DPLL1 declares a translation profile active, the tuning word history averaging processor is reset and begins processing tuning words from the loop filter. This bit allows the user to delay the averaging process until DPLL1 phase slew limiter is not actively slewing phase.	1	R/W	Core clock	No
			0	DPLL1 does not postpone tuning word averaging contingent on the state of the phase slew limiter.				
			1	DPLL1 postpones tuning word averaging while the phase limiter is actively slewing phase (default).				
	4	DPLL1 delay history frequency lock		DPLL1 Delay History Until Frequency Lock. By default, as soon as DPLL1 declares a translation profile active, the tuning word history averaging processor is reset and begins processing tuning words from the loop filter. This bit allows the user to delay the averaging process until DPLL1 frequency locks.	1	R/W	Core clock	No
			0	DPLL1 does not postpone tuning word averaging contingent on frequency lock status.				
			1	DPLL1 postpones tuning word averaging until frequency lock occurs (default).				
	3	DPLL1 delay history phase lock		DPLL1 Delay History Until Phase Lock. By default, as soon as DPLL1 declares a translation profile active, the tuning word history averaging processor is reset and begins processing tuning words from the loop filter. This bit allows the user to delay the averaging process until DPLL1 phase locks.	1	R/W	Core clock	No
			0	DPLL1 does not postpone tuning word averaging contingent on phase lock status.				
			1	DPLL1 postpones tuning word averaging until phase lock occurs (default).				
	2	DPLL1 quick start history		DPLL1 Quick Start History. By default, when DPLL1 is in active closed-loop operation, the available tuning word history ($FTW_{HISTORY}$) in Register 0x3203 to Register 0x3208 does not update until tuning word history averaging has run for the full duration prescribed by the history accumulation timer (t_{ACCUM}). Thus, a switch to holdover prior to t_{ACCUM} causes the DPLL to use the freerun tuning word (FTW0) because of the absence of $FTW_{HISTORY}$. This can be problematic for applications requiring large t_{ACCUM} (hours, for example), because the DPLL may switch to holdover just prior to meeting t_{ACCUM}. This bit allows the DPLL to update $FTW_{HISTORY}$ as early as 1/4 of t_{ACCUM}.	0	R/W	Core clock	No
			0	DPLL1 updates $FTW_{HISTORY}$ no earlier than t_{ACCUM}. (default)				
			1	DPLL1 updates $FTW_{HISTORY}$ as early as $t_{ACCUM}/4$.				
	1	DPLL1 single sample history		DPLL1 Single Sample History. By default, DPLL1 uses the available tuning word history ($FTW_{HISTORY}$) when switching to holdover mode from active closed-loop operation. However, if $FTW_{HISTORY}$ is unavailable, the DPLL uses the freerun tuning word (FTW0). This bit allows the DPLL to use the most recent FTW value from the loop filter instead of FTW0 when $FTW_{HISTORY}$ is unavailable.	0	R/W	Core clock	No
			0	DPLL1 uses FTW0 if $FTW_{HISTORY}$ is unavailable when switching to holdover (default).				
			1	DPLL1 uses the most recent FTW from the loop filter if $FTW_{HISTORY}$ is unavailable when switching to holdover.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	0	DPLL1 persistent history		DPLL1 Persistent History. By default, the history tuning word processor continues its history tuning word averaging process regardless of the state of DPLL1. This bit, in conjunction with Register 0x140F, Bits[2:0], allows the user to establish reset or pause conditions on the history accumulation process. 0 Reset the history tuning word averaging process. (default) 1 Pause the history tuning word averaging process.	0	R/W	Core clock	No
0x140F	[7:3]	Reserved		Reserved.	0x00	R	Live	No
	2	DPLL1 pause history while slewing		DPLL1 Pause History While Phase Slew Limited. By default, the history tuning word processor continues its history tuning word averaging process regardless of the state of DPLL1. However, the user can have the averaging processor reset or pause (depending on Register 0x140E, Bit 0) based on the state of the DPLL. When this bit is Logic 1 (default = 0), it allows the tuning word averaging processor to be reset or paused while the DPLL is actively slewing phase.	0	R/W	Core clock	No
	1	DPLL1 pause history frequency lock		DPLL1 Pause History While Frequency Unlock. By default, the history tuning word processor continues its history tuning word averaging process regardless of the state of DPLL1. However, the user can have the averaging processor reset or pause (depending on Register 0x140E, Bit 0) based on the state of the DPLL. When this bit is Logic 1 (default = 0), it allows the tuning word averaging processor to be reset or paused while the DPLL is not frequency locked.	0	R/W	Core clock	No
	0	DPLL1 pause history phase lock		DPLL1 Pause History While Phase Unlock. By default, the history tuning word processor continues its history tuning word averaging process regardless of the state of DPLL1. However, the user can have the averaging processor reset or pause (depending on Register 0x140E, Bit 0) based on the state of the DPLL. When this bit is Logic 1 (default = 0), it allows the tuning word averaging processor to be reset or paused while the DPLL is not phase locked.	0	R/W	Core clock	No
0x1410	[7:0]	DPLL1 history holdoff time		DPLL1 History Holdoff Time. This 8-bit unsigned value, DPLL1 History Holdoff Time (default = 0), constitutes a holdoff period, t_{HOLD}. DPLL1 History Holdoff Time relates to t_{HOLD} as follows: $t_{HOLD} = DPLL1\ History\ Holdoff\ Time \times (t_{ACCUM}/8)$ where t_{ACCUM} is the value in Register 0x140D to Register 0x140A, Bits[27:0]. For example, given t_{ACCUM} = 16 sec and DPLL1 History Holdoff Time = 10, then t_{HOLD} = 20 sec. t_{HOLD} is the time that DPLL1 waits, after declaring a translation profile active, before allowing the tuning word history averaging processor to start its tuning word averaging process. t_{HOLD} does not take effect until the expiration of any event dependent delays prescribed by Register 0x140E, Bits[5:3].	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1411	[7:0]	DPLL1 Phase Slew Limit Rate[7:0]		DPLL1 Phase Slew Limit Rate. This 32-bit unsigned value, DPLL1 Phase Slew Limit Rate (units of picoseconds/second, or 10^{-12}), defines a maximum rate of change of phase, Δt/t, that can appear at the output of the phase detector of DPLL1. Δt/t equates to a maximum relative frequency offset of DPLL1 Phase Slew Limit Rate × 10^{-6} ppm. DPLL1 Phase Slew Limit Rate relates to Δt/t as follows: $\Delta t/t = DPLL1\ Phase\ Slew\ Limit\ Rate \times 10^{-12}$ By default, DPLL1 Phase Slew Limit Rate = 100,663,296 (0x 0600 0000), which equates to a maximum relative frequency offset of approximately 100 ppm. The maximum value of DPLL1 Phase Slew Limit Rate equates to approximately 4000 ppm.	0x00	R/W	Core clock	No
0x1412	[7:0]	DPLL1 Phase Slew Limit Rate[15:8]		Continuation of the DPLL1 phase slew limit rate bit field. See the DPLL1 Phase Slew Limit Rate[7:0] description.	0x00	R/W	Core clock	No
0x1413	[7:0]	DPLL1 Phase Slew Limit Rate[23:16]		Continuation of the DPLL1 phase slew limit rate bit field. See the DPLL1 Phase Slew Limit Rate[7:0] description.	0x00	R/W	Core clock	No
0x1414	[7:0]	DPLL1 Phase Slew Limit Rate[31:24]		Continuation of the DPLL1 phase slew limit rate bit field. See the DPLL1 Phase Slew Limit Rate[7:0] description.	0x06	R/W	Core clock	No
0x1415	[7:0]	DPLL1 Phase Offset[7:0]		DPLL1 Closed-Loop Phase Offset. This 40-bit signed value, DPLL1 Phase Offset in units of picoseconds (default = 0), defines a fixed time (phase) offset, t_{OFST} (seconds), added in the feedback path to the phase detector of DPLL1. The result is a fixed time offset, t_{OFST}, at the output of DPLL1 relative to the reference input signal. DPLL1 Phase Offset (rounded to the nearest integer) relates to t_{OFST} as follows: $DPLL1\ Phase\ Offset = t_{OFST} \times 10^{12}$ A positive DPLL1 Phase Offset causes the output signal of the DPLL to lag relative to the input reference signal.	0x00	R/W	Core clock	No
0x1416	[7:0]	DPLL1 Phase Offset[15:8]		Continuation of the DPLL1 phase offset bit field. See the DPLL1 Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x1417	[7:0]	DPLL1 Phase Offset[23:16]		Continuation of the DPLL1 phase offset bit field. See the DPLL1 Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x1418	[7:0]	DPLL1 Phase Offset[31:24]		Continuation of the DPLL1 phase offset bit field. See the DPLL1 Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x1419	[7:0]	DPLL1 Phase Offset[39:32]		Continuation of the DPLL1 phase offset bit field. See the DPLL1 Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x141A	[7:0]	DPLL1 Phase Temperature Compensation C_1 Significand[7:0]		DPLL1 Temperature Compensation C_1 Significand. Synopsis: DPLL1 delay compensation injects a temperature (T) dependent correction factor (CF) as a time offset in the feedback path to the phase detector based on a fifth-order polynomial such that $CF = \Sigma(C_k \times T^k)$ (k = 1 to 5). T originates either from the on-board temperature sensor or from Register 0x2901 to Register 0x2900, Bits[15:0]. Each coefficient, C_k, takes the following form: $C_k = S_k \times 2^{Ek}$ where: S_k denotes the significand associated with C_k. E_k denotes the power of 2 exponent associated with C_k. When $C_k = 0$ or $\lvert C_k \rvert < 2^{-128}$, then $E_k = 0$ and $S_k = 0$.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
				Detail: this 16-bit signed value, S_1 (default = 0), constitutes the significand associated with C_1. S_1 relates to C_1 as follows: $S_1 = \text{round}(C_1 \times 2^{15-E1})$ where round(x) means round x to the nearest integer. Example: given $C_1 = -2.8927765 \times 10^{-6}$, then $E_1 = -18$ (see Register 0x141C), and thus $S_1 = -24{,}849$ (0x9EEF).				
0x141B	[7:0]	DPLL1 Phase Temperature Compensation C_1 Significand[15:8]		Continuation of the DPLL1 phase temperature compensation C_1 significand bit field. See the DPLL1 Phase Temperature Compensation C_1 Significand[7:0] description.	0x00	R/W	Core clock	No
0x141C	[7:0]	DPLL1 phase temperature compensation C_1 exponent		DPLL1 Phase Temperature Compensation C_1 Exponent. Synopsis: see Register 0x141A. Detail: this 8-bit signed value, E_1 (default = 0), constitutes the power of 2 exponent associated with C_1. E_1 relates to C_1 as follows: $E_1 = \text{floor}(\log(\lvert C_1 \rvert)/\log(2)) + 1$ where floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction. Example: given $C_1 = -2.8927765 \times 10^{-6}$, then $E_1 = -18$ (0xEE).	0x00	R/W	Core clock	No
0x141D	[7:0]	DPLL1 Phase Temperature Compensation C_2 Significand[7:0]		DPLL1 Phase Temperature Compensation C_2 Significand. This 16-bit signed value, S_2 (default = 0), constitutes the significand associated with C_2. S_2 relates to C_2 as follows: $S_2 = \text{round}(C_2 \times 2^{15-E2})$ See Register 0x141A for guidance.	0x00	R/W	Core clock	No
0x141E	[7:0]	DPLL1 Phase Temperature Compensation C_2 Significand[15:8]		Continuation of the DPLL1 phase temperature compensation C_2 significand bit field. See the DPLL1 Phase Temperature Compensation C_2 Significand[7:0] description.	0x00	R/W	Core clock	No
0x141F	[7:0]	DPLL1 phase temperature Compensation C_2 exponent		DPLL1 Phase Temperature Compensation C_2 Exponent. This 8-bit signed value, E_2 (default = 0), constitutes the power of 2 exponent associated with C_2. E_2 relates to C_2 as follows: $E_2 = \text{floor}(\log(\lvert C_2 \rvert)/\log(2)) + 1$ See Register 0x141C for guidance.	0x00	R/W	Core clock	No
0x1420	[7:0]	DPLL1 Phase Temperature Compensation C_3 Significand[7:0]		DPLL1 Temperature Compensation C_3 Significand. This 16-bit signed value, S_3 default = 0), constitutes the significand associated with C_3. S_3 relates to C_3 as follows: $S_3 = \text{round}(C_3 \times 2^{15-E3})$ See Register 0x141A for guidance.	0x00	R/W	Core clock	No
0x1421	[7:0]	DPLL1 Phase Temperature Compensation C_3 Significand[15:8]		Continuation of the DPLL1 phase temperature compensation C_3 significand bit field. See the DPLL1 Phase Temperature Compensation C_3 Significand[7:0] description.	0x00	R/W	Core clock	No
0x1422	[7:0]	DPLL1 phase temperature compensation C_3 exponent		DPLL1 Phase Temperature Compensation C_3 Exponent. This 8-bit signed value, E_3 (default = 0), constitutes the power of 2 exponent associated with C_3. E_3 relates to C_3 as follows: $E_3 = \text{floor}(\log(\lvert C_3 \rvert)/\log(2)) + 1$ See Register 0x141C for guidance.	0x00	R/W	Core clock	No
0x1423	[7:0]	DPLL1 Phase Temperature Compensation C_4 Significand[7:0]		DPLL1 Phase Temperature Compensation C_4 Significand. This 16-bit signed value, S_4 (default = 0), constitutes the significand associated with C_4. S_4 relates to C_4 as follows: $S_4 = \text{round}(C_4 \times 2^{15-E4})$ See Register 0x141A for guidance.	0x00	R/W	Core clock	No
0x1424	[7:0]	DPLL1 Phase Temperature Compensation C_4 Significand[15:8]		Continuation of the DPLL1 phase temperature compensation C_4 significand bit field. See the DPLL1 Phase Temperature Compensation C_4 Significand[7:0] description.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1425	[7:0]	DPLL1 Phase Temperature Compensation C_4 exponent		DPLL1 Temperature Compensation C_4 Exponent. This 8-bit signed value, E_4 (default = 0), constitutes the power of 2 exponent associated with C_4. E_4 relates to C_4 as follows: $E_4 = \text{floor}(\log(\lvert C_4 \rvert)/\log(2)) + 1$ See Register 0x141C for guidance.	0x00	R/W	Core clock	No
0x1426	[7:0]	DPLL1 Phase Temperature Compensation C_5 Significand[7:0]		DPLL1 Phase Temperature Compensation C_5 Significand. This 16-bit signed value, S_5 (default = 0), constitutes the significand associated with C_5. S_5 relates to C_5 as follows: $S_5 = \text{round}(C_5 \times 2^{15 - E5})$ See Register 0x141A for guidance.	0x00	R/W	Core clock	No
0x1427	[7:0]	DPLL1 Phase Temperature Compensation C_5 Significand[15:8]		Continuation of the DPLL1 phase temperature compensation C_5 significand bit field. See the DPLL1 Phase Temperature Compensation C_5 Significand[7:0] description.	0x00	R/W	Core clock	No
0x1428	[7:0]	DPLL1 Phase Temperature Compensation C_5 exponent		DPLL1 Phase Temperature Compensation C_5 Exponent. This 8-bit signed value, E_5 (default = 0), constitutes the power of 2 exponent associated with C_5. E_5 relates to C_5 as follows: $E_5 = \text{floor}(\log(\lvert C_5 \rvert)/\log(2)) + 1$ See Register 0x141C for guidance.	0x00	R/W	Core clock	No
0x1429	[7:3]	Reserved		Reserved.	0x00	R	Live	No
	[2:0]	DPLL1 phase temperature compensation filter bandwidth		DPLL1 Phase Temperature Compensation Low-Pass Filter Bandwidth. This 4-bit unsigned value sets the cutoff frequency (−3 dB) of the low-pass filter at the output of the delay compensation polynomial calculator of DPLL1. The filter serves to suppress rapid changes in the temperature compensation values.	0x0	R/W	Core clock	No
			0x0	240 Hz (maximum setting) (default).				
			0x1	120 Hz.				
			0x2	60 Hz.				
			0x3	30 Hz.				
			0x4	15 Hz.				
			0x5	7.6 Hz.				
			0x6	3.8 Hz.				
			0x7	1.9 Hz (minimum setting).				
0x142A	[7:3]	Reserved		Reserved.	0x00	R	Live	No
	[2:0]	DPLL1 inactive profile index		DPLL1 Inactive Profile Index. This 3-bit unsigned value, x (default = 0), identifies Translation Profile 1.x as the inactive profile for cascaded DPLL operation when DPLL1 switches to freerun or holdover mode.	0x0	R/W	Core clock	No

APLL1 PARAMETERS—REGISTER 0x1480 TO REGISTER 0x1483

Table 72. APLL1 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1480	7	Enable APLL1 manual charge pump current		Enables Manual Control of APLL1 Charge Pump Current. This bit controls whether the charge pump associated with the PFD of APLL1 operates in manual or automatic mode. In manual mode, the nominal charge pump current (I_{CP0}) depends on the value of Bits[6:0]. In automatic mode, I_{CP0} depends on the value, M, of the M0 divider, where I_{CP0} = 1016 µA for M ≥ 64 and I_{CP0} = M × 16 µA for M < 64.	1	R/W	Serial port clock	No
			0	Automatic.				
			1	Manual (default).				
	[6:0]	APLL1 manual charge pump current		APLL1 Manual Charge Pump Current. This 7-bit unsigned value, I_{CP} (units of 8 µA), establishes the nominal charge pump current (I_{CP0}) of the PFD associated with APLL1, but is only effective when the charge pump is configured for manual operation. I_{CP} = 20 decimal (default), yielding I_{CP0} = 160 µA.	0x16	R/W	Serial port clock	No
0x1481	[7:0]	APLL1 M1 feedback divider		APLL Multiplication Ratio. This 8-bit unsigned value, M (default = 0), constitutes the divide ratio of the M1 divider. Valid values for M are from 14 to 255. The default value is not valid. Therefore, the user must program a valid value.	0x00	R/W	Serial port clock	No
0x1482	[7:5]	APLL1 Loop Filter Zero resistor (R1)		Loop Filter R1. This 3-bit unsigned value (default = 7) selects the resistance of R1 (one of the internal components comprising the loop filter of APLL1). R1 resides between the output of the charge pump and the LF1 pin.	0x7	R/W	Serial port clock	No
			000	0 Ω.				
			001	250 Ω.				
			010	500 Ω.				
			011	750 Ω.				
			100	1.00 kΩ.				
			101	1.25 kΩ.				
			110	1.50 kΩ.				
			111	1.75 kΩ (default).				
	[4:2]	APLL1 loop filter pole capacitor (C2)		Loop Filter C2. This 3-bit unsigned value (default = 0) selects the capacitance of C2 (one of the internal components comprising the loop filter of APLL1). C2 resides between the output of the charge pump and the LDO1 pin.	0x0	R/W	Serial port clock	No
			000	8 pF (default).				
			001	24 pF.				
			010	40 pF.				
			011	56 pF.				
			100	72 pF.				
			101	88 pF.				
			110	104 pF.				
			111	120 pF.				
	[1:0]	APLL1 loop filter second pole resistor (R3)		Loop Filter R3. This 2-bit unsigned value (default = 0) selects the resistance of R3 (one of the internal components comprising the loop filter of APLL1). R3 resides between the output of the charge pump and the input to the VCO.	0x0	R/W	Serial port clock	No
			00	200 Ω (default).				
			01	250 Ω.				
			10	333 Ω.				
			11	500 Ω.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1483	[7:4]	Reserved		Reserved.	0x0	R/W	Serial port clock	No
	3	APLL1 dc offset current direction		DC Offset Current Polarity. This bit selects the polarity of I_{OFST} for APLL1. With regard to the action of the charge pump, positive polarity is in the pump up direction (default) and negative polarity is in the pump down direction.	0	R/W	Serial port clock	No
			0	Positive (default).				
			1	Negative.				
	[2:1]	APLL1 dc offset current value		I_{OFST} Magnitude. This 2-bit unsigned value (default = 1) selects a scale factor, SF, for the charge pump offset current (I_{OFST}) for APLL1, such that $I_{OFST} = SF \times I_{CP0}$. The magnitude of I_{OFST} is quantized to 8 µA.	0x1	R/W	Serial port clock	No
			00	SF = 0.5.				
			01	SF = 0.25 (default).				
			10	SF = 0.125.				
			11	SF = 0.0625.				
	0	Enable APLL1 dc offset current		DC Offset Current Enable. This bit allows the application of a supplemental constant current source (I_{OFST}) to the nominal charge pump current (I_{CP0}) of APLL1 such that $I_{CP} = I_{CP0} + I_{OFST}$.	1	R/W	Serial port clock	No
			0	Disabled.				
			1	Enabled (default).				

DISTRIBUTION CONTROL: PLL CHANNEL 1—REGISTER 0x14C0 TO REGISTER 0x14DC

Table 73. Distribution Control 1 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x14C0	[7:0]	Modulation Step[7:0]		Pulse Width Modulator Duty Cycle Deviation (PLL1). This 16-bit unsigned value, Modulation Step (default = 0) in units of half-cycles of the input clock to the Q divider, controls the duty cycle deviation, D, associated with a modulation event. The value of Modulation Step is common to the A and B pulse width modulators. Modulation Step relates to D as follows: $D = Modulation\ Step/(2 \times QDIV1y)$ where *QDIV1y* is the divide ratio of the applicable Q divider (*y* is A or B). For example, given Modulation Step = 100 and QDIV1y = 8025.5, then D = 0.00623 (0.623%).	0x00	R/W	Serial port clock	No
0x14C1	[7:0]	Modulation Step[15:8]		Continuation of the modulation step bit field. See the Modulation Step[7:0] description	0x00	R/W	Serial port clock	No
0x14C2	[7:0]	OUT1A Modulation Counter[7:0]		OUT1A Pulse Width Modulator Modulation Counter. This 28-bit unsigned value, Modulation Counter (default = 0), establishes the modulation period (t_{MOD}) of the pulse width modulator associated with Q1A, where t_{MOD} is the time period between modulation events. Modulation Counter relates to t_{MOD} as follows: $t_{MOD} = Modulation\ Counter \times (QDIV1A/f_{IN})$ where: *QDIV1A* is the divide ratio of Q1A. f_{IN} is the input clock frequency to Q1A. For example, given f_{IN} = 1.19 GHz, QDIV1A = 107.5 and Modulation Counter = 11,070, then t_{MOD} = 1.000 ms. Modulation Counter ≥ 6 when using pulse width modulation. Modulation Counter ≥ SYNC_EDGE + 7 (see Register 0x14CE, Bits[1:0]) when using triggered pulse width modulation.	0x00	R/W	Serial port clock	No
0x14C3	[7:0]	OUT1A Modulation Counter[15:8]		Continuation of the OUT1A modulation counter bit field. See the OUT1A Modulation Counter[7:0] description.	0x00	R/W	Serial port clock	No
0x14C4	[7:0]	OUT1A Modulation Counter[23:16]		Continuation of the OUT1A modulation counter bit field. See the OUT1A Modulation Counter[7:0] description.	0x00	R/W	Serial port clock	No
0x14C5	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	[3:0]	OUT1A Modulation Counter[27:24]		Continuation of the OUT1A modulation counter bit field. See the OUT1A Modulation Counter[7:0] description.	0x0	R/W	Serial port clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x14C6	[7:0]	OUT1B Modulation Counter[7:0]		OUT1B Pulse Width Modulator Modulation Counter. This 28-bit unsigned value, Modulation Counter (default = 0), establishes the modulation period (t_{MOD}) of the pulse width modulator associated with Q1B, where t_{MOD} is the time period between modulation events. Modulation Counter relates to t_{MOD} as follows: $t_{MOD} = Modulation\ Counter \times (QDIV1B/f_{IN})$ where: *QDIV1B* is the divide ratio of Q1B. f_{IN} is the input clock frequency to Q1B. For example, given f_{IN} = 1.19 GHz, QDIV1B = 107.5 and Modulation Counter = 11,070, then t_{MOD} = 1.000 ms. Modulation Counter ≥ 6 when using pulse width modulation. Modulation Counter ≥ SYNC_EDGE + 7 (see Register 0x14CE, Bits[1:0]) when using triggered pulse width modulation.	0x00	R/W	Serial port clock	No
0x14C7	[7:0]	OUT1B Modulation Counter[15:8]		Continuation of the OUT1B modulation counter bit field. See the OUT1B Modulation Counter[7:0] description.	0x00	R/W	Serial port clock	No
0x14C8	[7:0]	OUT1B Modulation Counter[23:16]		Continuation of the OUT1B modulation counter bit field. See the OUT1B Modulation Counter[7:0] description.	0x00	R/W	Serial port clock	No
0x14C9	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	[3:0]	OUT1B Modulation Counter[27:24]		Continuation of the OUT1B modulation counter bit field. See the OUT1B Modulation Counter[7:0] description.	0x0	R/W	Serial port clock	No
0x14CE	[7:2]	Reserved		Reserved.	0x00	R	Live	No
	[1:0]	Feedback divider sync edge		Feedback Divider Synchronization Edge. This 2-bit unsigned value, SYNC_EDGE (default = 0), assigns the number of Q divider output periods (0, 1, 2, or 3) to delay synchronization (relative to the modulation base edge) of the DPLL1 feedback divider. SYNC_EDGE = 0 is not valid. Thus, the user must program a nonzero value.	0x0	R/W	Serial port clock	No
0x14CF	[7:4]	Reserved		Reserved.	0x0	R/W	Serial port clock	No
	3	Enable OUT1A N shot modulation		OUT1A Pulse Width Modulator Trigger Type Select. This bit (default = 0) selects between immediate and triggered generation of modulation events by the pulse width modulator associated with Q1A. The following two triggering methods are possible: When Register 0x14D3, Bit 6 = 0, the trigger signal causes the pulse width modulator to generate five modulation events and then stop. When Register 0x14D3, Bit 6 = 1, the pulse width modulator continuously generates modulation events when the trigger signal is Logic 1. The Q divider N shot/PRBS controller is the source of the trigger signal and trigger controls (refer to the AD9546 data sheet for details). 0 Immediate modulation events (default). 1 Triggered modulation events.	0	R/W	Serial port clock	No
	2	Enable OUT1A single pulse modulation		OUT1A Pulse Width Modulator Balanced/Unbalanced Select. This bit selects balanced (default) or unbalanced modulation events generated by the pulse width modulator associated with Q1A. 0 Balanced (default). 1 Unbalanced.	0	R/W	Serial port clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	1	OUT1A modulation polarity		OUT1A Pulse Width Modulator Polarity. This bit selects, as narrow (default) or wide, the width of the first pulse of a Q1A modulation event. For balanced modulation, the width of the second pulse of the modulation event has the opposite width of that of the first pulse.	0	R/W	Serial port clock	No
			0	First pulse narrow (default).				
			1	First pulse wide.				
	0	Enable OUT1A modulation		OUT1A Pulse Width Modulator Enable. This bit selects or bypasses the pulse width modulator (embedded clock modulator) associated with Q1A.	0	R/W	Serial port clock	No
			0	Bypass pulse width modulator (default).				
			1	Select pulse width modulator.				
0x14D0	[7:4]	Reserved		Reserved.	0x0	R/W	Serial port clock	No
	3	Enable OUT1B N shot modulation		OUT1B Pulse Width Modulator Trigger Type Select. This bit (default = 0) selects between immediate and triggered generation of modulation events by the pulse width modulator associated with Q1B. The following two triggering methods are possible:	0	R/W	Serial port clock	No
				When Register 0x14D3, Bit 6 = 0, the trigger signal causes the pulse width modulator to generate five modulation events and then stop.				
				When Register 0x14D3, Bit 6 = 1, the pulse width modulator continuously generates modulation events when the trigger signal is Logic 1. The Q divider N shot/PRBS controller is the source of the trigger signal and trigger controls (refer to the AD9546 data sheet for details).				
			0	Immediate modulation events (default).				
			1	Triggered modulation events.				
	2	Enable OUT1B single pulse modulation		OUT1B Pulse Width Modulator Balanced/Unbalanced Select. This bit selects balanced (default) or unbalanced modulation events generated by the pulse width modulator associated with Q1B.	0	R/W	Serial port clock	No
			0	Balanced (default).				
			1	Unbalanced.				
	1	OUT1B modulation polarity		OUT1B Pulse Width Modulator Polarity. This bit selects, as narrow (default) or wide, the width of the first pulse of a Q1B modulation event. For balanced modulation, the width of the second pulse of the modulation event has the opposite width of that of the first pulse.	0	R/W	Serial port clock	No
			0	First pulse narrow (default).				
			1	First pulse wide.				
	0	Enable OUT1B modulation		OUT1B Pulse Width Modulator Enable. This bit selects or bypasses the pulse width modulator (embedded clock modulator) associated with Q1B.	0	R/W	Serial port clock	No
			0	Bypass pulse width modulator (default).				
			1	Select pulse width modulator.				
0x14D2	[7:0]	N shot gap		N Shot Gap (PLL1). This 8-bit unsigned value, Gap (default = 0) in units of Q divider output clock periods, defines how long the N shot generator blanks the Q divider output (that is, no rising edges) during an N shot event associated with PLL1. An N shot event consists of a pulsing interval followed by a blank interval (no pulses). N (in Register 0x14D3, Bits[5:0]) defines the pulsing interval, whereas Gap defines the blank interval. The value of Gap is common to the A, AA, B, and BB N shot generators.	0x00	R/W	Serial port clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x14D3	7	Reserved		Reserved.	0	R/W	Serial port clock	No
	6	N shot request mode		N Shot Request Burst/Edge or Periodic/Level (PLL1). This bit (default = 0) selects between burst and periodic generation of N shot events associated with PLL1. In burst operation, the N shot generator triggers on the rising edge of the trigger signal. In periodic operation, the N shot generator produces N shot events only while the trigger signal is Logic 1. The N shot generator stalls (see the AD9546 data sheet for details) when the trigger signal is Logic 1. See Register 0x14D6, Bit 0 regarding the trigger signal. This bit is common to the A, AA, B and BB N shot generators and the A and B pulse width modulators. 0 N shot burst operation (edge triggered). 1 N shot periodic operation (level triggered).	0	R/W	Serial port clock	No
	[5:0]	N shot		Number of Clock Pulses in an N Shot Burst (PLL1). This 6-bit unsigned value, N (default = 0) in units of Q divider output clock periods, defines how long the N shot generator is transparent to the Q divider output (that is, allows Q divider output pulses) during an N shot event associated with PLL1. An N shot event consists of a pulsing interval followed by a blank interval (no pulses). N defines the pulsing interval, whereas Gap (in Register 0x14D2, Bits[7:0]) defines the blank interval. The value of N is common to the A, AA, B, and BB N shot generators.	0x00	R/W	Serial port clock	No
0x14D4	7	Enable PRBS Q1BB		Q1BB PRBS Enable. This bit (default = 0) enables PRBS operation for Q1BB. When enabled, Q divider output pulses are pseudorandomly muted. 0 Disabled (default). 1 Enabled.	0	R/W	Serial port clock	No
	6	Enable Q1BB N shot		Q1BB N Shot Enable. This bit (default = 0) enables N shot (JESD204B) operation for Q1BB. When enabled, Q divider output pulses are muted until receipt of an N shot trigger (see Register 0x14D6, Bit 0). 0 Disabled (default). 1 Enabled.	0	R/W	Serial port clock	No
	5	Enable PRBS Q1B		Q1B PRBS Enable. This bit (default = 0) enables PRBS operation for Q1B. When enabled, Q divider output pulses are pseudorandomly muted. 0 Disabled (default). 1 Enabled.	0	R/W	Serial port clock	No
	4	Enable Q1B N shot		Q1B N Shot Enable. This bit (default = 0) enables N shot (JESD204B) operation for Q1B. When enabled, Q divider output pulses are muted until receipt of an N shot trigger (see Register 0x14D6, Bit 0). 0 Disabled (default). 1 Enabled.	0	R/W	Serial port clock	No
	3	Enable PRBS Q1AA		Q1AA PRBS Enable. This bit (default = 0) enables PRBS operation for Q1AA. When enabled, Q divider output pulses are pseudorandomly muted. 0 Disabled (default). 1 Enabled.	0	R/W	Serial port clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	2	Enable Q1AA N shot		Q1AA N Shot Enable. This bit (default = 0) enables N shot (JESD204B) operation for Q1AA. When enabled, Q divider output pulses are muted until receipt of an N shot trigger (see Register 0x14D6, Bit 0).	0	R/W	Serial port clock	No
			0	Disabled (default).				
			1	Enabled.				
	1	Enable PRBS Q1A		Q1A PRBS Enable. This bit (default = 0) enables PRBS operation for Q1A. When enabled, Q divider output pulses are pseudorandomly muted.	0	R/W	Serial port clock	No
			0	Disabled (default).				
			1	Enabled.				
	0	Enable Q1A N shot		Q1A N Shot Enable. This bit (default = 0) enables N shot (JESD204B) operation for Q1A. When enabled, Q divider output pulses are muted until receipt of an N shot trigger (see Register 0x14D6, Bit 0).	0	R/W	Serial port clock	No
			0	Disabled (default).				
			1	Enabled.				
0x14D6	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	4	Enable N shot retime to modulation		Enable Modulation Trigger Retiming (PLL1). This bit (only meaningful when Register 0x14D6, Bit 0 = 1) selects retimed N shot triggering relative to Q divider carrier clock edges (default) or modulation events (when modulation is active). This bit is common to the A, AA, B and BB N shot generators and the A and B pulse width modulators.	0	R/W	Serial port clock	No
			0	Carrier clock edge N shot trigger retiming (default), which only applies to N shot enabled Q dividers.				
			1	Modulation event N shot trigger retiming, which only applies to modulation enabled Q dividers.				
	[3:1]	Reserved		Reserved.	0x0	R/W	Serial port clock	No
	0	Enable N shot retime		Enable N Shot Trigger Retiming (PLL1). This bit selects direct (default) or retimed triggering to the N shot generators and pulse width modulators. Trigger retiming stalls the trigger event such that trigger enabled Q dividers start together on a common rising edge. The trigger signal can originate from an appropriately configured Mx pin or from Register 0x2201, Bit 0. This bit is common to the A, AA, B, and BB N shot generators and the A and B pulse width modulators.	0	R/W	Serial port clock	No
			0	Direct N shot triggering (default).				
			1	Retimed N shot triggering.				
0x14D7	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	Bypass mute retiming Channel A		Bypass OUT1AP/OUT1AN Mute Retiming. This bit (default = 0) allows the user to bypass the mute retiming block associated with OUT1AP/OUT1AN. By default, the mute controller retimes a mute command to prevent runt pulses at the output. With the retiming block bypassed, the output mutes immediately upon receipt of a mute command.	0	R/W	Serial port clock	No
			0	Mute Retiming Active (default).				
			1	Mute Retiming Bypassed.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[4:3]	OUT1A driver mode		Q1A/Q1AA Divider and OUT1AP/OUT1AN Driver Connectivity. This 2-bit unsigned value (default = 0) selects the connectivity between the Q dividers and the output drivers associated with OUT1Ax.	0x0	R/W	Serial port clock	No
			0	Single divider, differential drivers (default). The OUT1A signal is differential. The normal output of Divider Q1A connects to the OUT1AP driver. The inverted output of Divider Q1A connects to the OUT1AN driver.				
			1	Single divider, single-ended drivers. The OUT1AP and OUT1AN signals are single-ended replicas of one another. The normal output of Divider Q1A connects to both the OUT1AP driver and the OUT1AN driver.				
			2	Dual divider, single-ended drivers. The OUT1AP and OUT1AN signals are single-ended and independent. The normal output of Divider Q1A connects to the OUT1AP driver. The normal output of Divider Q1AA connects to the OUT1AN driver. Although the user can program different divide ratios for Q1A and Q1AA, the recommendation is to program the same divide ratio to mitigate crosstalk between the OUT1AP and OUT1AN pins.				
	[2:1]	OUT1A driver current		OUT1AP/OUT1AN Output Driver Current. This 2-bit unsigned value (default = 0) selects the magnitude of the source or sink current associated with both output drivers associated with OUT1Ax.	0x0	R/W	Serial port clock	No
			0	7.5 mA (default).				
			1	12.5 mA.				
			2	15 mA.				
	0	Enable OUT1A HCSL		OUT1AP/OUT1AN Current Source or Sink Mode Select. This bit (default = 1) sets the direction of current flow for both output drivers associated with OUT1A. See the AD9546 data sheet for details about input/output termination recommendations.	1	R/W	Serial port clock	No
			0	Current sink—CML.				
			1	Current source—HCSL (default).				
0x14D8	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	Bypass mute retiming Channel B		Bypass OUT1BP/OUT1BN Mute Retiming. This bit (default = 0) allows the user to bypass the mute retiming block associated with OUT1BP/OUT1BN. By default, the mute controller retimes a mute command to prevent runt pulses at the output. With the retiming block bypassed, the output mutes immediately upon receipt of a mute command.	0	R/W	Serial port clock	No
			0	Mute Retiming Active (default).				
			1	Mute Retiming Bypassed.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[4:3]	OUT1B driver mode		Q1B/Q1BB Divider and OUT1BP/OUT1BN Driver Connectivity. This 2-bit unsigned value (default = 0) selects the connectivity between the Q dividers and the output drivers associated with OUT1Bx.	0x0	R/W	Serial port clock	No
			0	Single divider, differential drivers (default). The OUT1B signal is differential. The normal output of Divider Q1B connects to the OUT1BP driver. The inverted output of Divider Q1B connects to the OUT1BN driver.				
			1	Single divider, single-ended drivers. The OUT1BP and OUT1BN signals are single-ended replicas of one another. The normal output of Divider Q1B connects to both the OUT1BP driver and the OUT1BN driver.				
			2	Dual divider, single-ended drivers. The OUT1BP and OUT1BN signals are single-ended and independent. The normal output of Divider Q1B connects to the OUT1BP driver. The normal output of Divider Q1BB connects to the OUT1BN driver. Although the user can program different divide ratios for Q1B and Q1BB, the recommendation is to program the same divide ratio to mitigate crosstalk between the OUT1BP and OUT1BN pins.				
	[2:1]	OUT1B driver current		OUT1BP/OUT1BN Output Driver Current. This 2-bit unsigned value (default = 0) selects the magnitude of the source or sink current associated with both output drivers associated with OUT1Bx.	0x0	R/W	Serial port clock	No
			0	7.5 mA (default).				
			1	12.5 mA.				
			2	15 mA.				
	0	Enable OUT1B HCSL		OUT1BP/OUT1BN Current Source or Sink Mode Select. This bit (default = 1) sets the direction of current flow for both output drivers associated with OUT1B. See the AD9546 data sheet for details about input/output termination recommendations.	1	R/W	Serial port clock	No
			0	Current sink—CML.				
			1	Current source—HCSL (default).				
0x14DA	[7:3]	Reserved		Reserved.	0x00	R	Live	No
	2	Enable SYSCLK Channel 1B		OUT1B Q divider Clock Source Select. This bit (default = 0) selects the input clock source to both the Q1B and Q1BB divider.	0	R/W	Core clock	No
			0	1/2 APLL1 VCO Frequency (default).				
			1	System Clock PLL VCO Frequency.				
	1	Enable SYSCLK Channel 1A		OUT1A Q divider Clock Source Select. This bit (default = 0) selects the input clock source to both the Q1A and Q1AA divider.	0	R/W	Core clock	No
			0	1/2 APLL1 VCO Frequency (default).				
			1	System Clock PLL VCO Frequency.				
	0	Enable SYSCLK sync mask		SYSCLK Driven Q divider Synchronization Mask Enable (PLL1). This bit (default = 0) allows the user to prevent synchronization events from disrupting the outputs of all Q dividers associated with PLL1 having the system clock selected as the input clock source (see Bits[2:1]). This feature is particularly useful when an output is the clock source to a microprocessor, for example. In this case, the synchronization mask prevents disruption of the microprocessor clock, which can otherwise occur following a synchronization event. The system clock PLL must be configured and stable prior to setting this bit.	0	R/W	Core clock	No
			0	SYSCLK Synchronization Mask Disabled (default).				
			1	SYSCLK Synchronization Mask Enabled.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x14DB	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	3	Enable Channel 1 coupled mode sync		Enable Channel 1 Coupled Mode Sync. This bit is normally set to zero. If Logic 1, this bit allows output autosynchronization to occur on the slave channel in cascaded DPLL mode before the master DPLL locks and synchronizes.	0	R/W	Core clock	No
	2	Enable DPLL1 reference sync		Distribution Synchronization on Reference Input Edge (PLL1). This bit (default = 0) allows the user to synchronize the outputs associated with PLL1 coincident with the rising edge of the input reference signal to DPLL1. The reference synchronization feature requires an active hitless profile for DPLL1.	0	R/W	Core clock	No
			0	Reference Synchronization Disabled (default).				
			1	Reference Synchronization Enabled.				
	[1:0]	Autosync mode		Distribution Autosynchronization Mode (PLL1). This 2-bit unsigned value (default = 0) selects one of the synchronization modes for the distribution outputs associated with PLL1. The output drivers do not toggle until a synchronization event occurs.	0x0	R/W	Core clock	No
			0	Manual Distribution Synchronization (default). Manual distribution synchronization is via one of the following: Register 0x2000, Bit 3 for all outputs; Register 0x2201, Bit 3 for outputs associated with PLL1; or implementation of one of the previous items via an appropriately configured Mx control pin.				
			1	Immediate Distribution Synchronization (the system clock PLL must be locked).				
			2	Distribution Synchronization on DPLL1 Phase Lock.				
			3	Distribution Synchronization on DPLL1 Frequency Lock.				
0x14DC	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	Mask OUT1BN auto unmute		OUT1BN Automatic Unmute Mask. This bit (default = 0) allows the user to opt out of (that is, mask) automatic unmute of the OUT1BN driver. This functionality only applies when automatic unmuting is in effect (that is, Register 0x14DC, Bits[1:0] > 0).	0	R/W	Core clock	No
			0	Normal Automatic Unmute Operation.				
			1	No Automatic Unmute.				
	4	Mask OUT1BP auto unmute		OUT1BP Automatic Unmute Mask. This bit (default = 0) allows the user to opt out of (that is, mask) automatic unmute of the OUT1BP driver. This functionality only applies when automatic unmuting is in effect (that is, Register 0x14DC, Bits[1:0] > 0).	0	R/W	Core clock	No
			0	Normal Automatic Unmute Operation.				
			1	No Automatic Unmute.				
	3	Mask OUT1AN auto unmute		OUT1AN Automatic Unmute Mask. This bit (default = 0) allows the user to opt out of (that is, mask) automatic unmute of the OUT1AN driver. This functionality only applies when automatic unmuting is in effect (that is, Register 0x14DC, Bits[1:0] > 0).	0	R/W	Core clock	No
			0	Normal Automatic Unmute Operation.				
			1	No Automatic Unmute.				
	2	Mask OUT1AP auto unmute		OUT1AP Automatic Unmute Mask. This bit (default = 0) allows the user to opt out of (that is, mask) automatic unmute of the OUT1AP driver. This functionality only applies when automatic unmuting is in effect (that is, Register 0x14DC, Bits[1:0] > 0).	0	R/W	Core clock	No
			0	Normal Automatic Unmute Operation.				
			1	No Automatic Unmute.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[1:0]	DPLL1 auto unmute mode		Distribution Unmute Mode Select (PLL1). This 2-bit unsigned value (default = 0) selects the mode of distribution driver unmute functionality for outputs associated with PLL1.	0x0	R/W	Core clock	No
			0	Immediate Distribution Unmute (default). Occurs immediately upon release of a synchronization request.				
			1	Distribution Unmute Subject to Hitless Profile Activation. Unmute occurs upon release of a synchronization request, but subject to activation of a hitless DPLL1 profile.				
			2	Distribution Unmute Subject to DPLL1 Phase Lock. Unmute occurs upon release of a synchronization request, but subject to DPLL1 phase lock (applies only to a hitless DPLL1 profile).				
			3	Distribution Unmute Subject to DPLL1 Frequency Lock. Unmute occurs upon release of a synchronization request, but subject to DPLL1 frequency lock (applies only to a hitless DPLL1 profile).				

DISTRIBUTION PARAMETERS: Q1A—REGISTER 0x1500 TO REGISTER 0x1508

Table 74. Distribution Parameters: Q1A Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1500	[7:0]	Q1A Divide Ratio[7:0]		Q1A Integer Divide Ratio. This 32-bit unsigned value, Q1A_int (default = 0), is the integer portion of the divide factor (QDIV1A) for Q Divider Q1A. 0 and 1 are invalid values for Q1A_int. Because the default value is 0, the user must program a valid value. When using the associated N shot generator or pulse width modulator, the following constraint applies: Q1A_int ≥ 8.	0x00	R/W	Core clock	No
0x1501	[7:0]	Q1A Divide Ratio[15:8]		Continuation of the Q1A divide ratio bit field. See the Q1A Divide Ratio[7:0] description.	0x00	R/W	Core clock	No
0x1502	[7:0]	Q1A Divide Ratio[23:16]		Continuation of the Q1A divide ratio bit field. See the Q1A Divide Ratio[7:0] description.	0x00	R/W	Core clock	No
0x1503	[7:0]	Q1A Divide Ratio[31:24]		Continuation of the Q1A divide ratio bit field. See the Q1A Divide Ratio[7:0] description.	0x00	R/W	Core clock	No
0x1504	[7:0]	Q1A Phase Offset[7:0]		Q1A Phase Offset or Pulse Width Magnitude. This 33-bit unsigned value, Phase Offset (default = 0), establishes either a phase offset or a pulse width for the Q1A divider. The maximum usable value of Phase Offset ($OFST_{MAX}$) is as follows: $OFST_{MAX} = 2 \times QDIV1A - 1$ where *QDIV1A* is the total divide ratio of Q Divider Q1A. The Q divider interprets the value of Phase Offset differently depending on whether phase offset or pulse width mode is in effect per Register 0x1508, Bit 4. Two categories of phase offset activation exist: initial and subsequent. An initial phase offset activates immediately following a device power-up or a reset, followed by completion of a distribution synchronization request. Subsequent phase offsets result from completed distribution synchronization requests that occur after completion of an initial phase offset.	0x00	R/W	Core clock	No
0x1505	[7:0]	Q1A Phase Offset[15:8]		Continuation of the Q1A phase offset bit field. See the Q1A Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x1506	[7:0]	Q1A Phase Offset[23:16]		Continuation of the Q1A phase offset bit field. See the Q1A Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x1507	[7:0]	Q1A Phase Offset[31:24]		Continuation of the Q1A phase offset bit field. See the Q1A Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x1508	7	Reserved		Reserved.	0	R	Live	No
	6	Q1A Phase Offset[32]		Continuation of the Q1A phase offset bit field. See the Q1A Phase Offset[7:0] description.	0	R/W	Core clock	No
	5	Enable half divide		Q1A Half Integer Enable. This bit (default = 0) adds 0 or 0.5 to the integer portion of Q Divider Q1A.	0	R/W	Core clock	No
			0	QDIV1A = Q1A_int				
			1	QDIV1A = Q1A_int +0.5.				
	4	Enable pulse width control		Q1A Phase Offset or Pulse Width Mode Select. This bit (default = 0) selects between phase offset mode and pulse width mode with regard to the interpretation of the value of Phase Offset in Register 0x1504. The value of Phase Offset relates to the total division factor, QDIV1A, of the Q divider (QDIV1A includes the integer and half integer parts).	0	R/W	Core clock	No
			1	Pulse Width Mode. Pulse width mode controls the duty cycle of the output clock signal. Duty cycle resolution, DC_0, is a function of QDIV1A as DC_0 (%) = 50/QDIV1A. Duty cycle relates to Phase Offset as $DC_0 \times$ Phase Offset. For example, given QDIV1A = 101.5 and Phase Offset = 10, then DC_0 = 0.493% and duty cycle = 4.93%. Duty cycle constitutes a fraction of one Q divider output cycle from rising edge to falling edge. Subsequent phase offsets do not cause activation of the phase slew limiting function of the Q divider.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
			0	Phase Offset Mode (default). Phase resolution, θ_0, is a function of QDIV1A as θ_0 (degrees)= 180/QDIV1A. Phase, θ, is a function of Phase Offset as $\theta = \theta_0 \times$ Phase Offset. For example, given QDIV1A = 101.5 and Phase Offset = 10, then $\theta_0 = 1.773°$ and $\theta = 17.73°$. Subsequent phase offsets activate the phase slew limiting function of the Q divider.				
	3	Q1A phase slew mode		Q1A Phase Slew Mode. This bit (default = 0) selects between phase slewing modes.	0	R/W	Core clock	No
			0	Lag Mode (default). Phase slewing steps (Δθ) are always in the −Δθ/Δt direction. Thus, while phase slewing, the output frequency decreases in accordance with the sign of Δθ/Δt.				
			1	Minimum Steps Mode. Phase slewing steps (Δθ) are in the direction requiring the least number of steps to accomplish the specified phase offset. Thus, while phase slewing, the output frequency increases or decreases in accordance with the sign of Δθ/Δt necessary to satisfy the least number of steps requirement.				
	[2:0]	Maximum phase slew step		Q1A Maximum Phase Slew Step. This 3-bit value (default = 7) selects a maximum phase step size (θ_{MAX}) for phase slewing, where θ_{MAX} relates to the total division factor, QDIV1A, of the Q divider (QDIV1A includes the integer and half integer parts).	0x7	R/W	Core clock	No
			0	1 Q divider input half-cycle. θ_{MAX} = 180/QDIV1A (degrees).				
			1	1 Q divider input cycle. θ_{MAX} = 90/QDIV1A (degrees).				
			2	~1/32 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV1A/16)/QDIV1A. The user must ensure floor(QDIV1A/16) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			3	~1/16 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV1A/8)/QDIV1A. The user must ensure floor(QDIV1A/8) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			4	~1/8 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV1A/4)/QDIV1A. The user must ensure floor(QDIV1A/4) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			5	~1/4 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV1A/2)/QDIV1A. The user must ensure floor(QDIV1A/2) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			6	~1/2 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV1A)/QDIV1A. The user must ensure floor(QDIV1A) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			7	~1 Q divider output cycle (default). θ_{MAX} (degrees) = 180 × (2 × QDIV1A − 1)/QDIV1A. This setting results in the phase slewing function being effectively disabled and causes phase slewing to execute as though Bit 3 = 0 (even when Bit 3 = 1).				

DISTRIBUTION PARAMETERS: Q1AA—REGISTER 0x1509 TO REGISTER 0x1511

Table 75. Distribution Parameters: Q1AA Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1509	[7:0]	Q1AA Divide Ratio[7:0]		Q1AA Integer Divide Ratio. This 32-bit unsigned value, Q1AA_int (default = 0), is the integer portion of the divide factor (QDIV1AA) for Q Divider Q1AA. 0 and 1 are invalid values for Q1AA_int. Because the default value is 0, the user must program a valid value. When using the associated N shot generator or pulse width modulator, the following constraint applies: Q1AA_int ≥ 8.	0x00	R/W	Core clock	No
0x150A	[7:0]	Q1AA Divide Ratio[15:8]		Continuation of the Q1AA divide ratio bit field. See the Q1AA Divide Ratio[7:0] description.	0x00	R/W	Core clock	No
0x150B	[7:0]	Q1AA Divide Ratio[23:16]		Continuation of the Q1AA divide ratio bit field. See the Q1AA Divide Ratio[7:0] description.	0x00	R/W	Core clock	No
0x150C	[7:0]	Q1AA Divide Ratio[31:24]		Continuation of the Q1AA divide ratio bit field. See the Q1AA Divide Ratio[7:0] description.	0x00	R/W	Core clock	No
0x150D	[7:0]	Q1AA Phase Offset[7:0]		Q1AA Phase Offset or Pulse Width Magnitude. This 33-bit unsigned value, Phase Offset (default = 0), establishes either a phase offset or a pulse width for the Q1AA divider. The maximum usable value of Phase Offset ($OFST_{MAX}$) is as follows: $OFST_{MAX} = 2 \times QDIV1AA - 1$ where *QDIV1AA* is the total divide ratio of Q Divider Q1AA. The Q divider interprets the value of Phase Offset differently depending on whether phase offset or pulse width mode is in effect per Register 0x1511, Bit 4. Two categories of phase offset activation exist: initial and subsequent. An initial phase offset activates immediately following a device power-up or a reset, followed by completion of a distribution synchronization request. Subsequent phase offsets result from completed distribution synchronization requests that occur after completion of an initial phase offset.	0x00	R/W	Core clock	No
0x150E	[7:0]	Q1AA Phase Offset[15:8]		Continuation of the Q1AA phase offset bit field. See the Q1AA Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x150F	[7:0]	Q1AA Phase Offset[23:16]		Continuation of the Q1AA phase offset bit field. See the Q1AA Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x1510	[7:0]	Q1AA Phase Offset[31:24]		Continuation of the Q1AA phase offset bit field. See the Q1AA Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x1511	7	Reserved		Reserved.	0	R	Live	No
	6	Q1AA Phase Offset[32]		Continuation of the Q1AA phase offset bit field. See the Q1AA Phase Offset[7:0] description.	0	R/W	Core clock	No
	5	Enable half divide		Q1AA Half Integer Enable. This bit (default = 0) adds 0 or 0.5 to the integer portion of Q Divider Q1AA.	0	R/W	Core clock	No
			0	QDIV1AA = Q1AA_int.				
			1	QDIV1AA = Q1AA_int + 0.5.				
	4	Enable pulse width control		Q1AA Phase Offset or Pulse Width Mode Select. This bit (default = 0) selects between phase offset mode and pulse width mode with regard to the interpretation of the value of Phase Offset in Register 0x150D. The value of Phase Offset relates to the total division factor, QDIV1AA, of the Q divider (QDIV1AA includes the integer and half integer parts).	0	R/W	Core clock	No
			1	Pulse Width Mode. Pulse width mode controls the duty cycle of the output clock signal. Duty cycle resolution, DC_0, is a function of QDIV1AA as DC_0 (%) = 50/QDIV1AA. Duty cycle relates to Phase Offset as $DC_0 \times$ Phase Offset. For example, given QDIV1AA = 101.5 and Phase Offset = 10, then DC_0 = 0.493% and duty cycle = 4.93%. Duty cycle constitutes a fraction of one Q divider output cycle from rising edge to falling edge. Subsequent phase offsets do not cause activation of the phase slew limiting function of the Q divider.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
			0	Phase Offset Mode (default). Phase resolution, θ_0, is a function of QDIV1AA as θ_0 (degrees)= 180/QDIV1AA. Phase, θ, is a function of Phase Offset as $\theta = \theta_0 \times$ Phase Offset. For example, given QDIV1AA = 101.5 and Phase Offset = 10, then $\theta_0 = 1.773°$ and $\theta = 17.73°$. Subsequent phase offsets activate the phase slew limiting function of the Q divider.				
	3	Q1AA phase slew mode		Q1AA Phase Slew Mode. This bit (default = 0) selects between phase slewing modes.	0	R/W	Core clock	No
			0	Lag Mode (default). Phase slewing steps (Δθ) are always in the −Δθ/Δt direction. Thus, while phase slewing, the output frequency decreases in accordance with the sign of Δθ/Δt.				
			1	Minimum Steps Mode. Phase slewing steps (Δθ) are in the direction requiring the least number of steps to accomplish the specified phase offset. Thus, while phase slewing, the output frequency increases or decreases in accordance with the sign of Δθ/Δt necessary to satisfy the least number of steps requirement.				
	[2:0]	Maximum phase slew step		Q1AA Maximum Phase Slew Step. This 3-bit value (default = 7) selects a maximum phase step size (θ_{MAX}) for phase slewing, where θ_{MAX} relates to the total division factor, QDIV1AA, of the Q divider (QDIV1AA includes the integer and half integer parts).	0x7	R/W	Core clock	No
			0	1 Q divider input half-cycle. θ_{MAX} = 180/QDIV1AA (degrees).				
			1	1 Q divider input cycle. θ_{MAX} = 90/QDIV1AA (degrees).				
			2	~1/32 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV1AA/16)/QDIV1AA. The user must ensure floor(QDIV1AA/16) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			3	~1/16 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV1AA/8)/QDIV1AA. The user must ensure floor(QDIV1AA/8) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			4	~1/8 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV1AA/4)/QDIV1AA. The user must ensure floor(QDIV1AA/4) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			5	~1/4 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV1AA/2)/QDIV1AA. The user must ensure floor(QDIV1AA/2) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			6	~1/2 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV1AA)/QDIV1AA. The user must ensure floor(QDIV1AA) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			7	~1 Q divider output cycle (default). θ_{MAX} (degrees) = 180 × (2 × QDIV1AA − 1)/QDIV1AA. This setting results in the phase slewing function being effectively disabled and causes phase slewing to execute as though Bit 3 = 0 (even when Bit 3 = 1).				

DISTRIBUTION PARAMETERS: Q1B—REGISTER 0x1512 TO REGISTER 0x151A

Table 76. Distribution Parameters: Q1B Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1512	[7:0]	Q1B Divide Ratio[7:0]		Q1B Integer Divide Ratio. This 32-bit unsigned value, Q1B_int (default = 0), is the integer portion of the divide factor (QDIV1B) for Q Divider Q1B. 0 and 1 are invalid values for Q1B_int. Because the default value is 0, the user must program a valid value. When using the associated N shot generator or pulse width modulator, the following constraint applies: Q1B_int ≥ 8.	0x00	R/W	Core clock	No
0x1513	[7:0]	Q1B Divide Ratio[15:8]		Continuation of the Q1B divide ratio bit field. See the Q1B Divide Ratio[7:0] description.	0x00	R/W	Core clock	No
0x1514	[7:0]	Q1B Divide Ratio[23:16]		Continuation of the Q1B divide ratio bit field. See the Q1B Divide Ratio[7:0] description.	0x00	R/W	Core clock	No
0x1515	[7:0]	Q1B Divide Ratio[31:24]		Continuation of the Q1B divide ratio bit field. See the Q1B Divide Ratio[7:0] description.	0x00	R/W	Core clock	No
0x1516	[7:0]	Q1B Phase Offset[7:0]		Q1B Phase Offset or Pulse Width Magnitude. This 33-bit unsigned value, Phase Offset (default = 0), establishes either a phase offset or a pulse width for the Q1B divider. The maximum usable value of Phase Offset ($OFST_{MAX}$) is as follows: $OFST_{MAX} = 2 \times QDIV1B - 1$ where *QDIV1B* is the total divide ratio of Q Divider Q1B. The Q divider interprets the value of Phase Offset differently depending on whether phase offset or pulse width mode is in effect per Register 0x151A, Bit 4. Two categories of phase offset activation exist: initial and subsequent. An initial phase offset activates immediately following a device power-up or a reset, followed by completion of a distribution synchronization request. Subsequent phase offsets result from completed distribution synchronization requests that occur after completion of an initial phase offset.	0x00	R/W	Core clock	No
0x1517	[7:0]	Q1B Phase Offset[15:8]		Continuation of the Q1B phase offset bit field. See the Q1B Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x1518	[7:0]	Q1B Phase Offset[23:16]		Continuation of the Q1B phase offset bit field. See the Q1B Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x1519	[7:0]	Q1B Phase Offset[31:24]		Continuation of the Q1B phase offset bit field. See the Q1B Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x151A	7	Reserved		Reserved.	0	R	Live	No
	6	Q1B Phase Offset[32]		Continuation of the Q1B phase offset bit field. See the Q1B Phase Offset[7:0] description.	0	R/W	Core clock	No
	5	Enable half divide		Q1B Half Integer Enable. This bit (default = 0) adds 0 or 0.5 to the integer portion of Q Divider Q1B.	0	R/W	Core clock	No
			0	QDIV1B = Q1B_int.				
			1	QDIV1B = Q1B_int + 0.5.				
	4	Enable pulse width control		Q1B Phase Offset or Pulse Width Mode Select. This bit (default = 0) selects between phase offset mode and pulse width mode with regard to the interpretation of the value of Phase Offset in Register 0x1516. The value of Phase Offset relates to the total division factor, QDIV1B, of the Q divider (QDIV1B includes the integer and half integer parts).	0	R/W	Core clock	No
			1	Pulse Width Mode. Pulse width mode controls the duty cycle of the output clock signal. Duty cycle resolution, DC_0, is a function of QDIV1B as DC_0 (%) = 50/QDIV1B. Duty cycle relates to Phase Offset as $DC_0 \times$ Phase Offset. For example, given QDIV1B = 101.5 and Phase Offset = 10, then DC_0 = 0.493% and duty cycle = 4.93%. Duty cycle constitutes a fraction of one Q divider output cycle from rising edge to falling edge. Subsequent phase offsets do not cause activation of the phase slew limiting function of the Q divider.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
			0	Phase Offset Mode (default). Phase resolution, θ_0, is a function of QDIV1B as θ_0 (degrees)= 180/QDIV1B. Phase, θ, is a function of Phase Offset as $\theta = \theta_0 \times$ Phase Offset. For example, given QDIV1B = 101.5 and Phase Offset = 10, then $\theta_0 = 1.773°$ and $\theta = 17.73°$. Subsequent phase offsets activate the phase slew limiting function of the Q divider.				
	3	Q1B phase slew mode		Q1B Phase Slew Mode. This bit (default = 0) selects between phase slewing modes.	0	R/W	Core clock	No
			0	Lag Mode (default). Phase slewing steps (Δθ) are always in the −Δθ/Δt direction. Thus, while phase slewing, the output frequency decreases in accordance with the sign of Δθ/Δt.				
			1	Minimum Steps Mode. Phase slewing steps (Δθ) are in the direction requiring the least number of steps to accomplish the specified phase offset. Thus, while phase slewing, the output frequency increases or decreases in accordance with the sign of Δθ/Δt necessary to satisfy the least number of steps requirement.				
	[2:0]	Maximum phase slew step		Q1B Maximum Phase Slew Step. This 3-bit value (default = 7) selects a maximum phase step size (θ_{MAX}) for phase slewing, where θ_{MAX} relates to the total division factor, QDIV1B, of the Q divider (QDIV1B includes the integer and half integer parts).	0x7	R/W	Core clock	No
			0	1 Q divider input half-cycle. θ_{MAX} = 180/ QDIV1B (degrees).				
			1	1 Q divider input cycle. θ_{MAX} = 90/QDIV1B (degrees).				
			2	~1/32 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV1B/16)/QDIV1B. The user must ensure floor(QDIV1B/16) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			3	~1/16 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV1B/8)/QDIV1B. The user must ensure floor(QDIV1B/8) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			4	~1/8 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV1B/4)/QDIV1B. The user must ensure floor(QDIV1B/4) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			5	~1/4 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV1B/2)/QDIV1B. The user must ensure floor(QDIV1B/2) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			6	~1/2 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV1B)/QDIV1B. The user must ensure floor(QDIV1B) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			7	~1 Q divider output cycle (default). θ_{MAX} (degrees) = 180 × (2 × QDIV1B − 1)/QDIV1B. This setting results in the phase slewing function being effectively disabled and causes phase slewing to execute as though Bit 3 = 0 (even when Bit 3 = 1).				

DISTRIBUTION PARAMETERS: Q1BB—REGISTER 0x151B TO REGISTER 0x1523

Table 77. Distribution Parameters: Q1BB Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x151B	[7:0]	Q1BB Divide Ratio[7:0]		Q1BB Integer Divide Ratio. This 32-bit unsigned value, Q1BB_int (default = 0), is the integer portion of the divide factor (QDIV1BB) for Q Divider Q1BB. 0 and 1 are invalid values for Q1BB_int. Because the default value is 0, the user must program a valid value. when using the associated N shot generator or pulse width modulator, the following constraint applies: Q1BB_int ≥ 8.	0x00	R/W	Core clock	No
0x151C	[7:0]	Q1BB Divide Ratio[15:8]		Continuation of the Q1BB divide ratio bit field. See the Q1BB Divide Ratio[7:0] description.	0x00	R/W	Core clock	No
0x151D	[7:0]	Q1BB Divide Ratio[23:16]		Continuation of the Q1BB divide ratio bit field. See the Q1BB Divide Ratio[7:0] description.	0x00	R/W	Core clock	No
0x151E	[7:0]	Q1BB Divide Ratio[31:24]		Continuation of the Q1BB divide ratio bit field. See the Q1BB Divide Ratio[7:0] description.	0x00	R/W	Core clock	No
0x151F	[7:0]	Q1BB Phase Offset[7:0]		Q1BB Phase Offset or Pulse Width Magnitude. This 33-bit unsigned value, Phase Offset (default = 0), establishes either a phase offset or a pulse width for the Q1BB divider. The maximum usable value of Phase Offset ($OFST_{MAX}$) is as follows: $OFST_{MAX} = 2 \times QDIV1BB - 1$ where *QDIV1BB* is the total divide ratio of Q Divider Q1BB. The Q divider interprets the value of Phase Offset differently depending on whether phase offset or pulse width mode is in effect per Register 0x1523, Bit 4. Two categories of phase offset activation exist: initial and subsequent. An initial phase offset activates immediately following a device power-up or a reset, followed by completion of a distribution synchronization request. Subsequent phase offsets result from completed distribution synchronization requests that occur after completion of an initial phase offset.	0x00	R/W	Core clock	No
0x1520	[7:0]	Q1BB Phase Offset[15:8]		Continuation of the Q1BB phase offset bit field. See the Q1BB Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x1521	[7:0]	Q1BB Phase Offset[23:16]		Continuation of the Q1BB phase offset bit field. See the Q1BB Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x1522	[7:0]	Q1BB Phase Offset[31:24]		Continuation of the Q1BB phase offset bit field. See the Q1BB Phase Offset[7:0] description.	0x00	R/W	Core clock	No
0x1523	7	Reserved		Reserved.	0	R	Live	No
	6	Q1BB Phase Offset[32]		Continuation of the Q1BB phase offset bit field. See the Q1BB Phase Offset[7:0] description.	0	R/W	Core clock	No
	5	Enable half divide		Q1BB Half Integer Enable. This bit (default = 0) adds 0 or 0.5 to the integer portion of Q Divider Q1BB.	0	R/W	Core clock	No
			0	QDIV1BB = Q1BB_int.				
			1	QDIV1BB = Q1BB_int + 0.5.				
	4	Enable pulse width control		Q1BB Phase Offset or Pulse Width Mode Select. This bit (default = 0) selects between phase offset mode and pulse width mode with regard to the interpretation of the value of Phase Offset in Register 0x151F. The value of Phase Offset relates to the total division factor, QDIV1BB, of the Q divider (QDIV1BB includes the integer and half integer parts).	0	R/W	Core clock	No
			1	Pulse Width Mode. Pulse width mode controls the duty cycle of the output clock signal. Duty cycle resolution, DC_0, is a function of QDIV1BB as DC_0 (%) = 50/QDIV1BB. Duty cycle relates to Phase Offset as $DC_0 \times$ Phase Offset. For example, given QDIV1BB = 101.5 and Phase Offset = 10, then DC_0 = 0.493% and duty cycle = 4.93%. Duty cycle constitutes a fraction of one Q divider output cycle from rising edge to falling edge. Subsequent phase offsets do not cause activation of the phase slew limiting function of the Q divider.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
			0	Phase Offset Mode (default). Phase resolution, θ_0, is a function of QDIV1BB as θ_0 (degrees)= 180/QDIV1BB. Phase, θ, is a function of Phase Offset as $\theta = \theta_0 \times$ Phase Offset. For example, given QDIV1BB = 101.5 and Phase Offset = 10, then $\theta_0 = 1.773°$ and $\theta = 17.73°$. Subsequent phase offsets activate the phase slew limiting function of the Q divider.				
	3	Q1BB phase slew mode		Q1BB Phase Slew Mode. This bit (default = 0) selects between phase slewing modes.	0	R/W	Core clock	No
			0	Lag Mode (default). Phase slewing steps (Δθ) are always in the −Δθ/Δt direction. Thus, while phase slewing, the output frequency decreases in accordance with the sign of Δθ/Δt.				
			1	Minimum Steps Mode. Phase slewing steps (Δθ) are in the direction requiring the least number of steps to accomplish the specified phase offset. Thus, while phase slewing, the output frequency increases or decreases in accordance with the sign of Δθ/Δt necessary to satisfy the least number of steps requirement.				
	[2:0]	Maximum phase slew step		Q1BB Maximum Phase Slew Step. This 3-bit value (default = 7) selects a maximum phase step size (θ_{MAX}) for phase slewing, where θ_{MAX} relates to the total division factor, QDIV1BB, of the Q divider (QDIV1BB includes the integer and half integer parts).	0x7	R/W	Core clock	No
			0	1 Q divider input half-cycle. θ_{MAX} = 180/QDIV1BB (degrees).				
			1	1 Q divider input cycle. θ_{MAX} = 90/QDIV1BB (degrees).				
			2	~1/32 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV1BB/16)/QDIV1BB. The user must ensure floor(QDIV1BB/16) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			3	~1/16 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV1BB/8)/QDIV1BB. The user must ensure floor(QDIV1BB/8) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			4	~1/8 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV1BB/4)/QDIV1BB. The user must ensure floor(QDIV1BB/4) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			5	~1/4 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV1BB/2)/QDIV1BB. The user must ensure floor(QDIV1BB/2) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			6	~1/2 of a Q divider output cycle. θ_{MAX} (degrees) = 180 × floor(QDIV1BB)/QDIV1BB. The user must ensure floor(QDIV1BB) ≥ 1. floor(x) changes x only when x ≠ integer, in which case x becomes the nearest integer in the negative direction.				
			7	~1 Q divider output cycle (default). θ_{MAX} (degrees) = 180 × (2 × QDIV1BB − 1)/QDIV1BB. This setting results in the phase slewing function being effectively disabled and causes phase slewing to execute as though Bit 3 = 0 (even when Bit 3 = 1).				

TRANSLATION PROFILE 1.0 PARAMETERS—REGISTER 0x1600 TO REGISTER 0x1617

Table 78. Translation Profile 1.0 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1600	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	[5:1]	Translation Profile 1.0 selection priority		Translation Profile 1.0 Priority Value. This 5-bit unsigned value (default = 0) allows the user to assign a priority level to Translation Profile 1.0. Priority assignment (highest priority = 0, lowest priority = 31) allows DPLL1 to select one translation profile over another when reference switching.	0x00	R/W	Core clock	No
	0	Enable Translation Profile 1.0		Translation Profile 1.0 Enable. This bit enables Translation Profile 1.0 as a usable translation profile for DPLL1.	0	R/W	Core clock	No
			0	Disabled (default).				
			1	Enabled.				
0x1601	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:0]	Translation Profile 1.0 reference source selection		DPLL1 Reference Source Selection. This 5-bit unsigned value (default = 0) assigns a time stamp source as the input to DPLL1 when the DPLL activates Translation Profile 1.0.	0x00	R/W	Core clock	No
			0	REFA (default).				
			1	REFAA.				
			2	REFB.				
			3	REFBB.				
			4	Feedback from DPLL0.				
			6	Auxiliary REF0.				
			7	Auxiliary REF1.				
			8	Auxiliary NCO 0.				
			9	Auxiliary NCO 1.				
			11	Auxiliary REF2.				
			12	Auxiliary REF3.				
			13	Inverse User Time Stamper 0.				
			14	Inverse User Time Stamper 1.				
0x1602	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:0]	External zero-delay feedback path		DPLL1 External Zero-Delay Feedback Path. This 5-bit field (default = 0) selects a reference input as the feedback return path for DPLL1 when Translation Profile 1.0 is configured as a hitless external zero-delay profile. The selections of the reference input as the DPLL feedback are meaningless unless Register 0x1603, Bits[1:0] = 11 (binary).	0x00	R/W	Core clock	No
			0	REFA (default). When REFA is configured as a differential input, use this selection (not the REFAA selection).				
			1	REFAA.				
			2	REFB. When REFB is configured as a differential input, use this selection (not the REFBB selection).				
			3	REFBB.				
			4	Auxiliary REF0.				
			5	Auxiliary REF1.				
			6	Auxiliary REF2.				
			7	Auxiliary REF3.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[4:0]	Internal zero-delay feedback path		DPLL1 Internal Zero-Delay Feedback Path. This 5-bit field (default = 0) selects a Q divider output as the feedback return path for DPLL1 when Translation Profile 1.0 is configured as a hitless internal zero-delay profile. The selections of the Q divider output as the DPLL feedback return path are meaningless unless Register 0x1603, Bits[1:0] = 01 (binary).	0x00	R/W	Core clock	No
			0	Q1A Output as DPLL1 Feedback (default). When OUT1A is configured for differential mode, use this selection (not the Q1AA feedback selection).				
			1	Q1AA Output as DPLL1 Feedback.				
			2	Q1B Output as DPLL1 Feedback. When OUT1B is configured for differential mode, use this selection (not the Q1BB feedback selection).				
			3	Q1BB Output as DPLL1 Feedback.				
0x1603	7	Translation Profile 1.0 loop filter base		DPLL1 Loop Filter Base. This bit (default = 0) assigns one of the loop filter base coefficient sets (LFx) to DPLL1.	0	R/W	Core clock	No
			0	LF0 (default). Nominal 70° phase margin.				
			1	LF1. Nominal 88.5° phase margin (use this setting for applications requiring the response of the closed-loop transfer function of DPLL1 to have <0.1 dB peaking).				
	[6:5]	Reserved		Reserved.	0x0	R/W	Core clock	No
	[4:2]	Translation Profile 1.0 tag mode		DPLL1 Tag Modes. This 3-bit unsigned value (default = 0) selects the DPLL1 tag mode for Translation Profile 1.0.	0x0	R/W	Core clock	No
			0	No tagged time stamps in the reference or feedback path of DPLL1 (default).				
			1	Tagged time stamps only in the reference path of DPLL1.				
			2	Tagged time stamps only in the feedback path of DPLL1.				
			3	Tagged time stamps in the reference and feedback paths of DPLL1, but the untagged rates differ.				
			4	Tagged time stamps in the reference and feedback paths of DPLL1, but the untagged rates are equal.				
	[1:0]	Translation Profile 1.0 loop mode		DPLL1 Frequency Translation Mode. This 2-bit unsigned value (default = 0) establishes the frequency translation mode for DPLL1.	0x0	R/W	Core clock	No
			0	Phase buildout mode (default).				
			1	Hitless, internal zero delay mode.				
			3	Hitless, external zero delay mode.				
0x1604	[7:0]	Translation Profile 1.0 Loop Bandwidth[7:0]		DPLL1 Loop Bandwidth Scale Factor. This 32-bit unsigned value (default = 0) constitutes a scale factor (SF) applied to the base loop bandwidth (LBW_0) associated with the coefficients of Loop Filter LF0 or LF1. The resulting loop bandwidth (LBW) is LBW = SF × LBW_0. The default coefficients of LF0 and LF1 yield LBW_0 = 1 µHz (10^{-6} Hz). For example, given SF = 50,000,000, then LBW = 50 Hz for LF0 or LF1.	0x00	R/W	Core clock	No
0x1605	[7:0]	Translation Profile 1.0 Loop Bandwidth[15:8]		Continuation of the Translation Profile 1.0 loop bandwidth bit field. See the Translation Profile 1.0 Loop Bandwidth[7:0] description.	0x00	R/W	Core clock	No
0x1606	[7:0]	Translation Profile 1.0 Loop Bandwidth[23:16]		Continuation of the Translation Profile 1.0 loop bandwidth bit field. See the Translation Profile 1.0 Loop Bandwidth[7:0] description.	0x00	R/W	Core clock	No
0x1607	[7:0]	Translation Profile 1.0 Loop Bandwidth[31:24]		Continuation of the Translation Profile 1.0 loop bandwidth bit field. See the Translation Profile 1.0 Loop Bandwidth[7:0] description.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1608	[7:0]	Translation Profile 1.0 Hitless N Divider[7:0]		DPLL1 Feedback Divider (N): Hitless Zero-Delay Operation. This 32-bit unsigned value, N Hitless (default = 4000), sets the divide ratio, N, for the feedback divider of DPLL1 when the DPLL operates in internal hitless zero delay mode. $N = N\ Hitless + 1$ Thus, the default value yields N = 4001. A translation profile configured for external zero delay hitless DPLL operation uses Register 0x160F to Register 0x160C, Bits[31:0] instead of this register.	0x160	R/W	Core clock	No
0x1609	[7:0]	Translation Profile 1.0 Hitless N Divider[15:8]		Continuation of the Translation Profile 1.0 hitless N divider bit field. See the Translation Profile 1.0 Hitless N Divider[7:0] description.	0x15	R/W	Core clock	No
0x160A	[7:0]	Translation Profile 1.0 Hitless N Divider[23:16]		Continuation of the Translation Profile 1.0 hitless N divider bit field. See the Translation Profile 1.0 Hitless N Divider[7:0] description.	0x00	R/W	Core clock	No
0x160B	[7:0]	Translation Profile 1.0 Hitless N Divider[31:24]		Continuation of the Translation Profile 1.0 hitless N divider bit field. See the Translation Profile 1.0 Hitless N Divider[7:0] description.	0x00	R/W	Core clock	No
0x160C	[7:0]	Translation Profile 1.0 Buildout N Divider[7:0]		DPLL1 Feedback Divider (N_int): Phase Buildout Operation. This 32-bit unsigned value, $N\_int_{BUILDOUT}$ (default = 4000), sets the integer part of the divide ratio, N, for the feedback divider of DPLL1 when the DPLL operates in phase buildout mode. $N = N\_int_{BUILDOUT} + 1$ Thus, the default value yields N = 4001.	0x160	R/W	Core clock	No
0x160D	[7:0]	Translation Profile 1.0 Buildout N Divider[15:8]		Continuation of the Translation Profile 1.0 buildout N divider bit field. See the Translation Profile 1.0 Buildout N Divider[7:0] description.	0x15	R/W	Core clock	No
0x160E	[7:0]	Translation Profile 1.0 Buildout N Divider[23:16]		Continuation of the Translation Profile 1.0 buildout N divider bit field. See the Translation Profile 1.0 Buildout N Divider[7:0] description.	0x00	R/W	Core clock	No
0x160F	[7:0]	Translation Profile 1.0 Buildout N Divider[31:24]		Continuation of the Translation Profile 1.0 buildout N divider bit field. See the Translation Profile 1.0 Buildout N Divider[7:0] description.	0x00	R/W	Core clock	No
0x1610	[7:0]	Translation Profile 1.0 Buildout FRAC[7:0]		DPLL1 Feedback Divider (N_num): Phase Buildout Operation. This 24-bit unsigned value, $N\_num_{BUILDOUT}$ (default = 0), is the numerator of the fractional portion of the feedback divider of DPLL0 when the DPLL operates in phase buildout mode. The total divide ratio is as follows: $N\_total = (N\_int_{BUILDOUT} + 1) + (N\_num/N\_den)$ where: *N_den* is the denominator of the fractional portion of the feedback divider, which resides in Register 0x1615 to Register 0x1613, Bits[23:0]. $N\_num < N\_den$. To make N_total an integer, program N_num = 0 and N_den = 0.	0x00	R/W	Core clock	No
0x1611	[7:0]	Translation Profile 1.0 Buildout FRAC[15:8]		Continuation of the Translation Profile 1.0 buildout FRAC bit field. See the Translation Profile 1.0 Buildout FRAC[7:0] description.	0x00	R/W	Core clock	No
0x1612	[7:0]	Translation Profile 1.0 Buildout FRAC[23:16]		Continuation of the Translation Profile 1.0 buildout FRAC bit field. See the Translation Profile 1.0 Buildout FRAC[7:0] description.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1613	[7:0]	Translation Profile 1.0 Buildout MOD[7:0]		DPLL1 Feedback Divider (N_den): Phase Buildout Operation. This 24-bit unsigned value, $N\_den_{BUILDOUT}$ (default = 0), is the denominator of the fractional portion of the feedback divider of DPLL1 when the DPLL operates in phase buildout mode. The total divide ratio is as follows: $N\_total = (N\_int_{BUILDOUT} + 1) + (N\_num/N\_den)$ where *N_num* is the numerator of the fractional portion of the feedback divider, which resides in Register 0x1612 to Register 0x1610, Bits[23:0]. *N_num* < *N_den*. To make the N divider divide ratio an integer, program *N_num* = 0 and *N_den* = 0.	0x00	R/W	Core clock	No
0x1614	[7:0]	Translation Profile 1.0 Buildout MOD[15:8]		Continuation of the Translation Profile 1.0 buildout MOD bit field. See the Translation Profile 1.0 Buildout MOD[7:0] description.	0x00	R/W	Core clock	No
0x1615	[7:0]	Translation Profile 1.0 Buildout MOD[23:16]		Continuation of the Translation Profile 1.0 buildout MOD bit field. See the Translation Profile 1.0 Buildout MOD[7:0] description.	0x00	R/W	Core clock	No
0x1616	[7:4]	Reserved		Reserved.	0x0	R/W	Core clock	No
	[3:0]	Translation Profile 1.0 fast acquisition excess bandwidth		DPLL1 Fast Acquisition Excess Bandwidth Factor. This 3-bit unsigned value, ESF (default = 0), controls the behavior of the fast acquisition option for DPLL1, where ESF = 0 disables the fast acquisition feature. ESF constitutes an exponential scale factor applied to the nominal loop bandwidth of the DPLL (BW_0) to yield an excess bandwidth, EBW, as follows: $EBW = BW_0 \times 2^{ESF}$ The fast acquisition controller sets the loop bandwidth of the DPLL to EBW at the start of an acquisition sequence. When the DPLL indicates phase lock, the fast acquisition controller halves the loop bandwidth. The fast acquisition controller again waits for the DPLL to indicate phase lock. When the DPLL indicates phase lock, the fast acquisition controller again halves the loop bandwidth. The process repeats until the DPLL loop bandwidth reaches BW_0. The fast acquisition controller sets Register 0x3202, Bit 4 = 1 while sequencing through the loop bandwidth reduction steps to indicate its active status. 0 Fast acquisition controller disabled (default). 1 ESF = 1. 2 ESF = 2. 3 ESF = 3. 4 ESF = 4. 5 ESF = 5. 6 ESF = 6. 7 ESF = 7. 8 ESF = 8. 9 ESF = 9. 10 ESF = 10.	0x0	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1617	7	Reserved		Reserved.	0	R	Live	No
	[6:4]	Translation Profile 1.0 fast acquisition timeout		DPLL1 Fast Acquisition Timeout. This 3-bit unsigned value puts a time limit (t_{MAX}) on how long the fast acquisition controller waits for chatter free DPLL phase lock status to occur during each loop bandwidth reduction step. If the phase lock guard timer (see Bits[2:0]) fails to time out by t_{MAX}, the fast acquisition controller automatically moves on to the next loop bandwidth reduction step even though chatter free phase lock failed to occur. The fast acquisition controller indicates completion of the fast acquisition process by setting Register 0x3102, Bit 5 = 1 only when the fast acquisition controller is in its final bandwidth reduction step and the t_{MAX} timer fails to expire.	0x0	R/W	Core clock	No
			0	t_{MAX} = 10 ms (default).				
			1	t_{MAX} = 50 ms.				
			2	t_{MAX} = 100 ms.				
			3	t_{MAX} = 500 ms.				
			4	t_{MAX} = 1 sec.				
			5	t_{MAX} = 10 sec.				
			6	t_{MAX} = 50 sec.				
			7	t_{MAX} = 100 sec.				
	3	Reserved		Reserved.	0	R	Live	No
	[2:0]	Translation Profile 1.0 fast acquisition lock settle time		DPLL1 Fast Acquisition Phase Lock Guard Time. This 3-bit unsigned value, GUARD_TIME (default = 0), sets the period (t_{GUARD}) of a countdown timer used by the fast acquisition controller. The countdown timer starts when the DPLL indicates phase lock, but the fast acquisition controller reloads the countdown timer with a value per GUARD_TIME whenever the DPLL indicates phase unlock. It is only upon timeout of the countdown timer that the fast acquisition controller moves on to its next bandwidth reduction step. t_{GUARD} constitutes the minimum amount of time the fast acquisition controller must observe chatter free DPLL phase lock status during each loop bandwidth reduction step.	0x0	R/W	Core clock	No
			0	t_{GUARD} = 1 ms (default).				
			1	t_{GUARD} = 10 ms.				
			2	t_{GUARD} = 50 ms.				
			3	t_{GUARD} = 100 ms.				
			4	t_{GUARD} = 500 ms.				
			5	t_{GUARD} = 1 sec.				
			6	t_{GUARD} = 10 sec.				
			7	t_{GUARD} = 50 sec.				

TRANSLATION PROFILE 1.1 PARAMETERS—REGISTER 0x1620 TO REGISTER 0x1637

Table 79. Translation Profile 1.1 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1620	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	[5:1]	Translation Profile 1.1 selection priority		Translation Profile 1.1 Priority Value. This 5-bit unsigned value (default = 0) allows the user to assign a priority level to Translation Profile 1.1. Priority assignment (highest priority = 0, lowest priority = 31) allows DPLL1 to select one translation profile over another when reference switching.	0x00	R/W	Core clock	No
	0	Enable Translation Profile 1.1		Translation Profile 1.1 Enable. This bit enables Translation Profile 1.1 as a usable translation profile for DPLL1.	0	R/W	Core clock	No
			0	Disabled (default).				
			1	Enabled.				
0x1621	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:0]	Translation Profile 1.1 reference source selection		DPLL1 Reference Source Selection. This 5-bit unsigned value (default = 0) assigns a time stamp source as the input to DPLL1 when the DPLL activates Translation Profile 1.1.	0x00	R/W	Core clock	No
			0	REFA (default).				
			1	REFAA.				
			2	REFB.				
			3	REFBB.				
			4	Feedback from DPLL0.				
			6	Auxiliary REF0.				
			7	Auxiliary REF1.				
			8	Auxiliary NCO 0.				
			9	Auxiliary NCO 1.				
			11	Auxiliary REF2.				
			12	Auxiliary REF3.				
			13	Inverse User Time Stamper 0.				
			14	Inverse User Time Stamper 1.				
0x1622	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:0]	External zero-delay feedback path		DPLL1 External Zero-Delay Feedback Path. This 5-bit field (default = 0) selects a reference input as the feedback return path for DPLL1 when Translation Profile 1.1 is configured as a hitless external zero-delay profile. The selections of the reference input as the DPLL feedback are meaningless unless Register 0x1623, Bits[1:0] = 11 (binary).	0x00	R/W	Core clock	No
			0	REFA (default). When REFA is configured as a differential input, use this selection (not the REFAA selection).				
			1	REFAA.				
			2	REFB. When REFB is configured as a differential input, use this selection (not the REFBB selection).				
			3	REFBB.				
			4	Auxiliary REF0.				
			5	Auxiliary REF1.				
			6	Auxiliary REF2.				
			7	Auxiliary REF3.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[4:0]	Internal zero-delay feedback path		DPLL1 Internal Zero-Delay Feedback Path. This 5-bit field (default = 0) selects a Q divider output as the feedback return path for DPLL1 when Translation Profile 1.1 is configured as a hitless internal zero-delay profile. The selections of the Q divider output as the DPLL feedback return path are meaningless unless Register 0x1623, Bits[1:0] = 01 (binary).	0x00	R/W	Core clock	No
			0	Q1A Output as DPLL1 Feedback (default). When OUT1A is configured for differential mode, use this selection (not the Q1AA feedback selection).				
			1	Q1AA Output as DPLL1 Feedback.				
			2	Q1B Output as DPLL1 Feedback. When OUT1B is configured for differential mode, use this selection (not the Q1BB feedback selection).				
			3	Q1BB Output as DPLL1 Feedback.				
0x1623	7	Translation Profile 1.1 loop filter base		DPLL1 Loop Filter Base. This bit (default = 0) assigns one of the loop filter base coefficient sets (LFx) to DPLL1.	0	R/W	Core clock	No
			0	LF0 (default). Nominal 70° phase margin.				
			1	LF1. Nominal 88.5° phase margin (use this setting for applications requiring the response of the closed-loop transfer function of DPLL1 to have <0.1 dB peaking).				
	[6:5]	Reserved		Reserved.	0x0	R/W	Core clock	No
	[4:2]	Translation Profile 1.1 tag mode		DPLL1 Tag Modes. This 3-bit unsigned value (default = 0) selects the DPLL1 tag mode for Translation Profile 1.1.	0x0	R/W	Core clock	No
			0	No tagged time stamps in the reference or feedback path of DPLL1 (default).				
			1	Tagged time stamps only in the reference path of DPLL1.				
			2	Tagged time stamps only in the feedback path of DPLL1.				
			3	Tagged time stamps in the reference and feedback paths of DPLL1, but the untagged rates differ.				
			4	Tagged time stamps in the reference and feedback paths of DPLL1, but the untagged rates are equal.				
	[1:0]	Translation Profile 1.1 loop mode		DPLL1 Frequency Translation Mode. This 2-bit unsigned value (default = 0) establishes the frequency translation mode for DPLL1.	0x0	R/W	Core clock	No
			0	Phase buildout mode (default).				
			1	Hitless, internal zero delay mode.				
			3	Hitless, external zero delay mode.				
0x1624	[7:0]	Translation Profile 1.1 Loop Bandwidth[7:0]		DPLL1 Loop Bandwidth Scale Factor. This 32-bit unsigned value (default = 0) constitutes a scale factor (SF) applied to the base loop bandwidth (LBW_0) associated with the coefficients of Loop Filter LF0 or LF1. The resulting loop bandwidth (LBW) is LBW = SF × LBW_0. The default coefficients of LF0 and LF1 yield LBW_0 = 1 µHz (10^{-6} Hz). For example, given SF = 50,000,000, then LBW = 50 Hz for LF0 or LF1.	0x00	R/W	Core clock	No
0x1625	[7:0]	Translation Profile 1.1 Loop Bandwidth[15:8]		Continuation of the Translation Profile 1.1 loop bandwidth bit field. See the Translation Profile 1.1 Loop Bandwidth[7:0] description.	0x00	R/W	Core clock	No
0x1626	[7:0]	Translation Profile 1.1 Loop Bandwidth[23:16]		Continuation of the Translation Profile 1.1 loop bandwidth bit field. See the Translation Profile 1.1 Loop Bandwidth[7:0] description.	0x00	R/W	Core clock	No
0x1627	[7:0]	Translation Profile 1.1 Loop Bandwidth[31:24]		Continuation of the Translation Profile 1.1 loop bandwidth bit field. See the Translation Profile 1.1 Loop Bandwidth[7:0] description.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1628	[7:0]	Translation Profile 1.1 Hitless N Divider[7:0]		DPLL1 Feedback Divider (N): Hitless Zero-Delay Operation. This 32-bit unsigned value, N Hitless (default = 4000), sets the divide ratio, N, for the feedback divider of DPLL1 when the DPLL operates in internal hitless zero delay mode. $N = N\,Hitless + 1$ Thus, the default value yields N = 4001. A translation profile configured for external zero delay hitless DPLL operation uses Register 0x162F to Register 0x162C, Bits[31:0] instead of this register.	0x160	R/W	Core clock	No
0x1629	[7:0]	Translation Profile 1.1 Hitless N Divider[15:8]		Continuation of the Translation Profile 1.1 hitless N divider bit field. See the Translation Profile 1.1 Hitless N Divider[7:0] description.	0x15	R/W	Core clock	No
0x162A	[7:0]	Translation Profile 1.1 Hitless N Divider[23:16]		Continuation of the Translation Profile 1.1 hitless N divider bit field. See the Translation Profile 1.1 Hitless N Divider[7:0] description.	0x00	R/W	Core clock	No
0x162B	[7:0]	Translation Profile 1.1 Hitless N Divider[31:24]		Continuation of the Translation Profile 1.1 hitless N divider bit field. See the Translation Profile 1.1 Hitless N Divider[7:0] description.	0x00	R/W	Core clock	No
0x162C	[7:0]	Translation Profile 1.1 Buildout N Divider[7:0]		DPLL1 Feedback Divider (N_int): Phase Buildout Operation. This 32-bit unsigned value, $N\_int_{BUILDOUT}$ (default = 4000), sets the integer part of the divide ratio, N, for the feedback divider of DPLL1 when the DPLL operates in phase buildout mode. $N = N\_int_{BUILDOUT} + 1$ Thus, the default value yields N = 4001.	0x160	R/W	Core clock	No
0x162D	[7:0]	Translation Profile 1.1 Buildout N Divider[15:8]		Continuation of the Translation Profile 1.1 buildout N divider bit field. See the Translation Profile 1.1 Buildout N Divider[7:0] description.	0x15	R/W	Core clock	No
0x162E	[7:0]	Translation Profile 1.1 Buildout N Divider[23:16]		Continuation of the Translation Profile 1.1 buildout N divider bit field. See the Translation Profile 1.1 Buildout N Divider[7:0] description.	0x00	R/W	Core clock	No
0x162F	[7:0]	Translation Profile 1.1 Buildout N Divider[31:24]		Continuation of the Translation Profile 1.1 buildout N divider bit field. See the Translation Profile 1.1 Buildout N Divider[7:0] description.	0x00	R/W	Core clock	No
0x1630	[7:0]	Translation Profile 1.1 Buildout FRAC[7:0]		DPLL1 Feedback Divider (N_num): Phase Buildout Operation. This 24-bit unsigned value, $N\_num_{BUILDOUT}$ (default = 0), is the numerator of the fractional portion of the feedback divider of DPLL0 when the DPLL operates in phase buildout mode. The total divide ratio is as follows: $N\_total = (N\_int_{BUILDOUT} + 1) + (N\_num/N\_den)$ where: *N_den* is the denominator of the fractional portion of the feedback divider, which resides in Register 0x1635 to Register 0x1633, Bits[23:0]. $N\_num < N\_den$. To make N_total an integer, program N_num = 0 and N_den = 0.	0x00	R/W	Core clock	No
0x1631	[7:0]	Translation Profile 1.1 Buildout FRAC[15:8]		Continuation of the Translation Profile 1.1 buildout FRAC bit field. See the Translation Profile 1.1 Buildout FRAC[7:0] description.	0x00	R/W	Core clock	No
0x1632	[7:0]	Translation Profile 1.1 Buildout FRAC[23:16]		Continuation of the Translation Profile 1.1 buildout FRAC bit field. See the Translation Profile 1.1 Buildout FRAC[7:0] description.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1633	[7:0]	Translation Profile 1.1 Buildout MOD[7:0]		DPLL1 Feedback Divider (N_den): Phase Buildout Operation. This 24-bit unsigned value, $N\_den_{BUILDOUT}$ (default = 0), is the denominator of the fractional portion of the feedback divider of DPLL1 when the DPLL operates in phase buildout mode. The total divide ratio is as follows: $N\_total = (N\_int_{BUILDOUT} + 1) + (N\_num/N\_den)$ where *N_num* is the numerator of the fractional portion of the feedback divider, which resides in Register 0x1632 to Register 0x1630, Bits[23:0]. *N_num* < *N_den*. To make the N divider divide ratio an integer, program *N_num* = 0 and *N_den* = 0.	0x00	R/W	Core clock	No
0x1634	[7:0]	Translation Profile 1.1 Buildout MOD[15:8]		Continuation of the Translation Profile 1.1 buildout MOD bit field. See the Translation Profile 1.1 Buildout MOD[7:0] description.	0x00	R/W	Core clock	No
0x1635	[7:0]	Translation Profile 1.1 Buildout MOD[23:16]		Continuation of the Translation Profile 1.1 buildout MOD bit field. See the Translation Profile 1.1 Buildout MOD[7:0] description.	0x00	R/W	Core clock	No
0x1636	[7:4]	Reserved		Reserved.	0x0	R/W	Core clock	No
	[3:0]	Translation Profile 1.1 fast acquisition excess bandwidth		DPLL1 Fast Acquisition Excess Bandwidth Factor. This 3-bit unsigned value, ESF (default = 0), controls the behavior of the fast acquisition option for DPLL1, where ESF = 0 disables the fast acquisition feature. ESF constitutes an exponential scale factor applied to the nominal loop bandwidth of the DPLL (BW_0) to yield an excess bandwidth, EBW, as follows: $EBW = BW_0 \times 2^{ESF}$ The fast acquisition controller sets the loop bandwidth of the DPLL to EBW at the start of an acquisition sequence. When the DPLL indicates phase lock, the fast acquisition controller halves the loop bandwidth. The fast acquisition controller again waits for the DPLL to indicate phase lock. When the DPLL indicates phase lock, the fast acquisition controller again halves the loop bandwidth. The process repeats until the DPLL loop bandwidth reaches BW_0. The fast acquisition controller sets Register 0x3202, Bit 4 = 1 while sequencing through the loop bandwidth reduction steps to indicate its active status.	0x0	R/W	Core clock	No
			0	Fast acquisition controller disabled (default).				
			1	ESF = 1.				
			2	ESF = 2.				
			3	ESF = 3.				
			4	ESF = 4.				
			5	ESF = 5.				
			6	ESF = 6.				
			7	ESF = 7.				
			8	ESF = 8.				
			9	ESF = 9.				
			10	ESF = 10.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1637	7	Reserved		Reserved.	0	R	Live	No
	[6:4]	Translation Profile 1.1 fast acquisition timeout		DPLL1 Fast Acquisition Timeout. This 3-bit unsigned value puts a time limit (t_{MAX}) on how long the fast acquisition controller waits for chatter free DPLL phase lock status to occur during each loop bandwidth reduction step. If the phase lock guard timer (see Bits[2:0]) fails to time out by t_{MAX}, the fast acquisition controller automatically moves on to the next loop bandwidth reduction step even though chatter free phase lock failed to occur. The fast acquisition controller indicates completion of the fast acquisition process by setting Register 0x3102, Bit 5 = 1 only when the fast acquisition controller is in its final bandwidth reduction step and the t_{MAX} timer fails to expire.	0x0	R/W	Core clock	No
			0	t_{MAX} = 10 ms (default).				
			1	t_{MAX} = 50 ms.				
			2	t_{MAX} = 100 ms.				
			3	t_{MAX} = 500 ms.				
			4	t_{MAX} = 1 sec.				
			5	t_{MAX} = 10 sec.				
			6	t_{MAX} = 50 sec.				
			7	t_{MAX} = 100 sec.				
	3	Reserved		Reserved.	0	R	Live	No
	[2:0]	Translation Profile 1.1 fast acquisition lock settle time		DPLL1 Fast Acquisition Phase Lock Guard Time. This 3-bit unsigned value, GUARD_TIME (default = 0), sets the period (t_{GUARD}) of a countdown timer used by the fast acquisition controller. The countdown timer starts when the DPLL indicates phase lock, but the fast acquisition controller reloads the countdown timer with a value per GUARD_TIME whenever the DPLL indicates phase unlock. It is only upon timeout of the countdown timer that the fast acquisition controller moves on to its next bandwidth reduction step. t_{GUARD} constitutes the minimum amount of time the fast acquisition controller must observe chatter free DPLL phase lock status during each loop bandwidth reduction step.	0x0	R/W	Core clock	No
			0	t_{GUARD} = 1 ms (default).				
			1	t_{GUARD} = 10 ms.				
			2	t_{GUARD} = 50 ms.				
			3	t_{GUARD} = 100 ms.				
			4	t_{GUARD} = 500 ms.				
			5	t_{GUARD} = 1 sec.				
			6	t_{GUARD} = 10 sec.				
			7	t_{GUARD} = 50 sec.				

TRANSLATION PROFILE 1.2 PARAMETERS—REGISTER 0x1640 TO REGISTER 0x1657

Table 80. Translation Profile 1.2 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1640	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	[5:1]	Translation Profile 1.2 selection priority		Translation Profile 1.2 Priority Value. This 5-bit unsigned value (default = 0) allows the user to assign a priority level to Translation Profile 1.2. Priority assignment (highest priority = 0, lowest priority = 31) allows DPLL1 to select one translation profile over another when reference switching.	0x00	R/W	Core clock	No
	0	Enable Translation Profile 1.2		Translation Profile 1.2 Enable. This bit enables Translation Profile 1.2 as a usable translation profile for DPLL1.	0	R/W	Core clock	No
			0	Disabled (default).				
			1	Enabled.				
0x1641	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:0]	Translation Profile 1.2 reference source selection		DPLL1 Reference Source Selection. This 5-bit unsigned value (default = 0) assigns a time stamp source as the input to DPLL1 when the DPLL activates Translation Profile 1.2.	0x00	R/W	Core clock	No
			0	REFA (default).				
			1	REFAA.				
			2	REFB.				
			3	REFBB.				
			4	Feedback from DPLL0.				
			6	Auxiliary REF0.				
			7	Auxiliary REF1.				
			8	Auxiliary NCO 0.				
			9	Auxiliary NCO 1.				
			11	Auxiliary REF2.				
			12	Auxiliary REF3.				
			13	Inverse User Time Stamper 0.				
			14	Inverse User Time Stamper 1.				
0x1642	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:0]	External zero-delay feedback path		DPLL1 External Zero-Delay Feedback Path. This 5-bit field (default = 0) selects a reference input as the feedback return path for DPLL1 when Translation Profile 1.2 is configured as a hitless external zero-delay profile. The selections of the reference input as the DPLL feedback are meaningless unless Register 0x1643, Bits[1:0] = 11 (binary).	0x00	R/W	Core clock	No
			0	REFA (default). When REFA is configured as a differential input, use this selection (not the REFAA selection).				
			1	REFAA.				
			2	REFB. When REFB is configured as a differential input, use this selection (not the REFBB selection).				
			3	REFBB.				
			4	Auxiliary REF0.				
			5	Auxiliary REF1.				
			6	Auxiliary REF2.				
			7	Auxiliary REF3.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[4:0]	Internal zero-delay feedback path		DPLL1 Internal Zero-Delay Feedback Path. This 5-bit field (default = 0) selects a Q divider output as the feedback return path for DPLL1 when Translation Profile 1.2 is configured as a hitless internal zero-delay profile. The selections of the Q divider output as the DPLL feedback return path are meaningless unless Register 0x1643, Bits[1:0] = 01 (binary).	0x00	R/W	Core clock	No
			0	Q1A Output as DPLL1 Feedback (default). When OUT1A is configured for differential mode, use this selection (not the Q1AA feedback selection).				
			1	Q1AA Output as DPLL1 Feedback.				
			2	Q1B Output as DPLL1 Feedback. When OUT1B is configured for differential mode, use this selection (not the Q1BB feedback selection).				
			3	Q1BB Output as DPLL1 Feedback.				
0x1643	7	Translation Profile 1.2 loop filter base		DPLL1 Loop Filter Base. This bit (default = 0) assigns one of the loop filter base coefficient sets (LFx) to DPLL1.	0	R/W	Core clock	No
			0	LF0 (default). Nominal 70° phase margin.				
			1	LF1. Nominal 88.5° phase margin (use this setting for applications requiring the response of the closed-loop transfer function of DPLL1 to have <0.1 dB peaking).				
	[6:5]	Reserved		Reserved.	0x0	R/W	Core clock	No
	[4:2]	Translation Profile 1.2 tag mode		DPLL1 Tag Modes. This 3-bit unsigned value (default = 0) selects the DPLL1 tag mode for Translation Profile 1.2.	0x0	R/W	Core clock	No
			0	No tagged time stamps in the reference or feedback path of DPLL1 (default).				
			1	Tagged time stamps only in the reference path of DPLL1.				
			2	Tagged time stamps only in the feedback path of DPLL1.				
			3	Tagged time stamps in the reference and feedback paths of DPLL1, but the untagged rates differ.				
			4	Tagged time stamps in the reference and feedback paths of DPLL1, but the untagged rates are equal.				
	[1:0]	Translation Profile 1.2 loop mode		DPLL1 Frequency Translation Mode. This 2-bit unsigned value (default = 0) establishes the frequency translation mode for DPLL1.	0x0	R/W	Core clock	No
			0	Phase buildout mode (default).				
			1	Hitless, internal zero delay mode.				
			3	Hitless, external zero delay mode.				
0x1644	[7:0]	Translation Profile 1.2 Loop Bandwidth[7:0]		DPLL1 Loop Bandwidth Scale Factor. This 32-bit unsigned value (default = 0) constitutes a scale factor (SF) applied to the base loop bandwidth (LBW_0) associated with the coefficients of Loop Filter LF0 or LF1. The resulting loop bandwidth (LBW) is $LBW = SF \times LBW_0$. The default coefficients of LF0 and LF1 yield $LBW_0 = 1$ µHz (10^{-6} Hz). For example, given SF = 50,000,000, then LBW = 50 Hz for LF0 or LF1.	0x00	R/W	Core clock	No
0x1645	[7:0]	Translation Profile 1.2 Loop Bandwidth[15:8]		Continuation of the Translation Profile 1.2 loop bandwidth bit field. See the Translation Profile 1.2 Loop Bandwidth[7:0] description.	0x00	R/W	Core clock	No
0x1646	[7:0]	Translation Profile 1.2 Loop Bandwidth[23:16]		Continuation of the Translation Profile 1.2 loop bandwidth bit field. See the Translation Profile 1.2 Loop Bandwidth[7:0] description.	0x00	R/W	Core clock	No
0x1647	[7:0]	Translation Profile 1.2 Loop Bandwidth[31:24]		Continuation of the Translation Profile 1.2 loop bandwidth bit field. See the Translation Profile 1.2 Loop Bandwidth[7:0] description.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1648	[7:0]	Translation Profile 1.2 Hitless N Divider[7:0]		DPLL1 Feedback Divider (N): Hitless Zero-Delay Operation. This 32-bit unsigned value, N Hitless (default = 4000), sets the divide ratio, N, for the feedback divider of DPLL1 when the DPLL operates in internal hitless zero delay mode. $N = N\ Hitless + 1$ Thus, the default value yields N = 4001. A translation profile configured for external zero delay hitless DPLL operation uses Register 0x164F to Register 0x164C, Bits[31:0] instead of this register.	0x160	R/W	Core clock	No
0x1649	[7:0]	Translation Profile 1.2 Hitless N Divider[15:8]		Continuation of the Translation Profile 1.2 hitless N divider bit field. See the Translation Profile 1.2 Hitless N Divider[7:0] description.	0x15	R/W	Core clock	No
0x164A	[7:0]	Translation Profile 1.2 Hitless N Divider[23:16]		Continuation of the Translation Profile 1.2 hitless N divider bit field. See the Translation Profile 1.2 Hitless N Divider[7:0] description.	0x00	R/W	Core clock	No
0x164B	[7:0]	Translation Profile 1.2 Hitless N Divider[31:24]		Continuation of the Translation Profile 1.2 hitless N divider bit field. See the Translation Profile 1.2 Hitless N Divider[7:0] description.	0x00	R/W	Core clock	No
0x164C	[7:0]	Translation Profile 1.2 Buildout N Divider[7:0]		DPLL1 Feedback Divider (N_int): Phase Buildout Operation. This 32-bit unsigned value, $N\_int_{BUILDOUT}$ (default = 4000), sets the integer part of the divide ratio, N, for the feedback divider of DPLL1 when the DPLL operates in phase buildout mode. $N = N\_int_{BUILDOUT} + 1$ Thus, the default value yields N = 4001.	0x160	R/W	Core clock	No
0x164D	[7:0]	Translation Profile 1.2 Buildout N Divider[15:8]		Continuation of the Translation Profile 1.2 buildout N divider bit field. See the Translation Profile 1.2 Buildout N Divider[7:0] description.	0x15	R/W	Core clock	No
0x164E	[7:0]	Translation Profile 1.2 Buildout N Divider[23:16]		Continuation of the Translation Profile 1.2 buildout N divider bit field. See the Translation Profile 1.2 Buildout N Divider[7:0] description.	0x00	R/W	Core clock	No
0x164F	[7:0]	Translation Profile 1.2 Buildout N Divider[31:24]		Continuation of the Translation Profile 1.2 buildout N divider bit field. See the Translation Profile 1.2 Buildout N Divider[7:0] description.	0x00	R/W	Core clock	No
0x1650	[7:0]	Translation Profile 1.2 Buildout FRAC[7:0]		DPLL1 Feedback Divider (N_num): Phase Buildout Operation. This 24-bit unsigned value, $N\_num_{BUILDOUT}$ (default = 0), is the numerator of the fractional portion of the feedback divider of DPLL0 when the DPLL operates in phase buildout mode. The total divide ratio is as follows: $N\_total = (N\_int_{BUILDOUT} + 1) + (N\_num/N\_den)$ where: *N_den* is the denominator of the fractional portion of the feedback divider, which resides in Register 0x1655 to Register 0x1653, Bits[23:0]. $N\_num < N\_den$. To make N_total an integer, program N_num = 0 and N_den = 0.	0x00	R/W	Core clock	No
0x1651	[7:0]	Translation Profile 1.2 Buildout FRAC[15:8]		Continuation of the Translation Profile 1.2 buildout FRAC bit field. See the Translation Profile 1.2 Buildout FRAC[7:0] description.	0x00	R/W	Core clock	No
0x1652	[7:0]	Translation Profile 1.2 Buildout FRAC[23:16]		Continuation of the Translation Profile 1.2 buildout FRAC bit field. See the Translation Profile 1.2 Buildout FRAC[7:0] description.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1653	[7:0]	Translation Profile 1.2 Buildout MOD[7:0]		DPLL1 Feedback Divider (N_den): Phase Buildout Operation. This 24-bit unsigned value, $N\_den_{BUILDOUT}$ (default = 0), is the denominator of the fractional portion of the feedback divider of DPLL1 when the DPLL operates in phase buildout mode. The total divide ratio is as follows: $N\_total = (N\_int_{BUILDOUT} + 1) + (N\_num/N\_den)$ where *N_num* is the numerator of the fractional portion of the feedback divider, which resides in Register 0x1652 to Register 0x1650, Bits[23:0]. *N_num* < *N_den*. To make the N divider divide ratio an integer, program *N_num* = 0 and *N_den* = 0.	0x00	R/W	Core clock	No
0x1654	[7:0]	Translation Profile 1.2 Buildout MOD[15:8]		Continuation of the Translation Profile 1.2 buildout MOD bit field. See the Translation Profile 1.2 Buildout MOD[7:0] description.	0x00	R/W	Core clock	No
0x1655	[7:0]	Translation Profile 1.2 Buildout MOD[23:16]		Continuation of the Translation Profile 1.2 buildout MOD bit field. See the Translation Profile 1.2 Buildout MOD[7:0] description.	0x00	R/W	Core clock	No
0x1656	[7:4]	Reserved		Reserved.	0x0	R/W	Core clock	No
	[3:0]	Translation Profile 1.2 fast acquisition excess bandwidth		DPLL1 Fast Acquisition Excess Bandwidth Factor. This 3-bit unsigned value, ESF (default = 0), controls the behavior of the fast acquisition option for DPLL1, where ESF = 0 disables the fast acquisition feature. ESF constitutes an exponential scale factor applied to the nominal loop bandwidth of the DPLL (BW_0) to yield an excess bandwidth, EBW, as follows: $EBW = BW_0 \times 2^{ESF}$ The fast acquisition controller sets the loop bandwidth of the DPLL to EBW at the start of an acquisition sequence. When the DPLL indicates phase lock, the fast acquisition controller halves the loop bandwidth. The fast acquisition controller again waits for the DPLL to indicate phase lock. When the DPLL indicates phase lock, the fast acquisition controller again halves the loop bandwidth. The process repeats until the DPLL loop bandwidth reaches BW_0. The fast acquisition controller sets Register 0x3202, Bit 4 = 1 while sequencing through the loop bandwidth reduction steps to indicate its active status.	0x0	R/W	Core clock	No
			0	Fast acquisition controller disabled (default).				
			1	ESF = 1.				
			2	ESF = 2.				
			3	ESF = 3.				
			4	ESF = 4.				
			5	ESF = 5.				
			6	ESF = 6.				
			7	ESF = 7.				
			8	ESF = 8.				
			9	ESF = 9.				
			10	ESF = 10.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1657	7	Reserved		Reserved.	0	R	Live	No
	[6:4]	Translation Profile 1.2 fast acquisition timeout		DPLL1 Fast Acquisition Timeout. This 3-bit unsigned value puts a time limit (t_{MAX}) on how long the fast acquisition controller waits for chatter free DPLL phase lock status to occur during each loop bandwidth reduction step. If the phase lock guard timer (see Bits[2:0]) fails to time out by t_{MAX}, the fast acquisition controller automatically moves on to the next loop bandwidth reduction step even though chatter free phase lock failed to occur. The fast acquisition controller indicates completion of the fast acquisition process by setting Register 0x3102, Bit 5 = 1 only when the fast acquisition controller is in its final bandwidth reduction step and the t_{MAX} timer fails to expire.	0x0	R/W	Core clock	No
			0	t_{MAX} = 10 ms (default).				
			1	t_{MAX} = 50 ms.				
			2	t_{MAX} = 100 ms.				
			3	t_{MAX} = 500 ms.				
			4	t_{MAX} = 1 sec.				
			5	t_{MAX} = 10 sec.				
			6	t_{MAX} = 50 sec.				
			7	t_{MAX} = 100 sec.				
	3	Reserved		Reserved.	0	R	Live	No
	[2:0]	Translation Profile 1.2 fast acquisition lock settle time		DPLL1 Fast Acquisition Phase Lock Guard Time. This 3-bit unsigned value, GUARD_TIME (default = 0), sets the period (t_{GUARD}) of a countdown timer used by the fast acquisition controller. The countdown timer starts when the DPLL indicates phase lock, but the fast acquisition controller reloads the countdown timer with a value per GUARD_TIME whenever the DPLL indicates phase unlock. It is only upon timeout of the countdown timer that the fast acquisition controller moves on to its next bandwidth reduction step. t_{GUARD} constitutes the minimum amount of time the fast acquisition controller must observe chatter free DPLL phase lock status during each loop bandwidth reduction step.	0x0	R/W	Core clock	No
			0	t_{GUARD} = 1 ms (default).				
			1	t_{GUARD} = 10 ms.				
			2	t_{GUARD} = 50 ms.				
			3	t_{GUARD} = 100 ms.				
			4	t_{GUARD} = 500 ms.				
			5	t_{GUARD} = 1 sec.				
			6	t_{GUARD} = 10 sec.				
			7	t_{GUARD} = 50 sec.				

TRANSLATION PROFILE 1.3 PARAMETERS—REGISTER 0x1660 TO REGISTER 0x1677

Table 81. Translation Profile 1.3 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1660	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	[5:1]	Translation Profile 1.3 selection priority		Translation Profile 1.3 Priority Value. This 5-bit unsigned value (default = 0) allows the user to assign a priority level to Translation Profile 1.3. Priority assignment (highest priority = 0, lowest priority = 31) allows DPLL1 to select one translation profile over another when reference switching.	0x00	R/W	Core clock	No
	0	Enable Translation Profile 1.3		Translation Profile 1.3 Enable. This bit enables Translation Profile 1.3 as a usable translation profile for DPLL1.	0	R/W	Core clock	No
			0	Disabled (default).				
			1	Enabled.				
0x1661	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:0]	Translation Profile 1.3 reference source selection		DPLL1 Reference Source Selection. This 5-bit unsigned value (default = 0) assigns a time stamp source as the input to DPLL1 when the DPLL activates Translation Profile 1.3.	0x00	R/W	Core clock	No
			0	REFA (default).				
			1	REFAA.				
			2	REFB.				
			3	REFBB.				
			4	Feedback from DPLL0.				
			6	Auxiliary REF0.				
			7	Auxiliary REF1.				
			8	Auxiliary NCO 0.				
			9	Auxiliary NCO 1.				
			11	Auxiliary REF2.				
			12	Auxiliary REF3.				
			13	Inverse User Time Stamper 0.				
			14	Inverse User Time Stamper 1.				
0x1662	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:0]	External zero-delay feedback path		DPLL1 External Zero-Delay Feedback Path. This 5-bit field (default = 0) selects a reference input as the feedback return path for DPLL1 when Translation Profile 1.3 is configured as a hitless external zero-delay profile. The selections of the reference input as the DPLL feedback are meaningless unless Register 0x1633, Bits[1:0] = 11 (binary).	0x00	R/W	Core clock	No
			0	REFA (default). When REFA is configured as a differential input, use this selection (not the REFAA selection).				
			1	REFAA.				
			2	REFB. When REFB is configured as a differential input, use this selection (not the REFBB selection).				
			3	REFBB.				
			4	Auxiliary REF0.				
			5	Auxiliary REF1.				
			6	Auxiliary REF2.				
			7	Auxiliary REF3.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[4:0]	Internal zero-delay feedback path		DPLL1 Internal Zero-Delay Feedback Path. This 5-bit field (default = 0) selects a Q divider output as the feedback return path for DPLL1 when Translation Profile 1.3 is configured as a hitless internal zero-delay profile. The selections of the Q divider output as the DPLL feedback return path are meaningless unless Register 0x1663, Bits[1:0] = 01 (binary).	0x00	R/W	Core clock	No
			0	Q1A Output as DPLL1 Feedback (default). When OUT1A is configured for differential mode, use this selection (not the Q1AA feedback selection).				
			1	Q1AA Output as DPLL1 Feedback.				
			2	Q1B Output as DPLL1 Feedback. When OUT1B is configured for differential mode, use this selection (not the Q1BB feedback selection).				
			3	Q1BB Output as DPLL1 Feedback.				
0x1663	7	Translation Profile 1.3 loop filter base		DPLL1 Loop Filter Base. This bit (default = 0) assigns one of the loop filter base coefficient sets (LFx) to DPLL1.	0	R/W	Core clock	No
			0	LF0 (default). Nominal 70° phase margin.				
			1	LF1. Nominal 88.5° phase margin (use this setting for applications requiring the response of the closed-loop transfer function of DPLL1 to have <0.1 dB peaking).				
	[6:5]	Reserved		Reserved.	0x0	R/W	Core clock	No
	[4:2]	Translation Profile 1.3 tag mode		DPLL1 Tag Modes. This 3-bit unsigned value (default = 0) selects the DPLL1 tag mode for Translation Profile 1.3.	0x0	R/W	Core clock	No
			0	No tagged time stamps in the reference or feedback path of DPLL1 (default).				
			1	Tagged time stamps only in the reference path of DPLL1.				
			2	Tagged time stamps only in the feedback path of DPLL1.				
			3	Tagged time stamps in the reference and feedback paths of DPLL1, but the untagged rates differ.				
			4	Tagged time stamps in the reference and feedback paths of DPLL1, but the untagged rates are equal.				
	[1:0]	Translation Profile 1.3 loop mode		DPLL1 Frequency Translation Mode. This 2-bit unsigned value (default = 0) establishes the frequency translation mode for DPLL1.	0x0	R/W	Core clock	No
			0	Phase buildout mode (default).				
			1	Hitless, internal zero delay mode.				
			3	Hitless, external zero delay mode.				
0x1664	[7:0]	Translation Profile 1.3 Loop Bandwidth[7:0]		DPLL1 Loop Bandwidth Scale Factor. This 32-bit unsigned value (default = 0) constitutes a scale factor (SF) applied to the base loop bandwidth (LBW_0) associated with the coefficients of Loop Filter LF0 or LF1. The resulting loop bandwidth (LBW) is LBW = SF × LBW_0. The default coefficients of LF0 and LF1 yield LBW_0 = 1 µHz (10^{-6} Hz). For example, given SF = 50,000,000, then LBW = 50 Hz for LF0 or LF1.	0x00	R/W	Core clock	No
0x1665	[7:0]	Translation Profile 1.3 Loop Bandwidth[15:8]		Continuation of the Translation Profile 1.3 loop bandwidth bit field. See the Translation Profile 1.3 Loop Bandwidth[7:0] description.	0x00	R/W	Core clock	No
0x1666	[7:0]	Translation Profile 1.3 Loop Bandwidth[23:16]		Continuation of the Translation Profile 1.3 loop bandwidth bit field. See the Translation Profile 1.3 Loop Bandwidth[7:0] description.	0x00	R/W	Core clock	No
0x1667	[7:0]	Translation Profile 1.3 Loop Bandwidth[31:24]		Continuation of the Translation Profile 1.3 loop bandwidth bit field. See the Translation Profile 1.3 Loop Bandwidth[7:0] description.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1668	[7:0]	Translation Profile 1.3 Hitless N Divider[7:0]		DPLL1 Feedback Divider (N): Hitless Zero-Delay Operation. This 32-bit unsigned value, N Hitless (default = 4000), sets the divide ratio, N, for the feedback divider of DPLL1 when the DPLL operates in internal hitless zero delay mode. $N = N\,Hitless + 1$ Thus, the default value yields N = 4001. A translation profile configured for external zero delay hitless DPLL operation uses Register 0x166F to Register 0x166C, Bits[31:0] instead of this register.	0x160	R/W	Core clock	No
0x1669	[7:0]	Translation Profile 1.3 Hitless N Divider[15:8]		Continuation of the Translation Profile 1.3 hitless N divider bit field. See the Translation Profile 1.3 Hitless N Divider[7:0] description.	0x15	R/W	Core clock	No
0x166A	[7:0]	Translation Profile 1.3 Hitless N Divider[23:16]		Continuation of the Translation Profile 1.3 hitless N divider bit field. See the Translation Profile 1.3 Hitless N Divider[7:0] description.	0x00	R/W	Core clock	No
0x166B	[7:0]	Translation Profile 1.3 Hitless N Divider[31:24]		Continuation of the Translation Profile 1.3 hitless N divider bit field. See the Translation Profile 1.3 Hitless N Divider[7:0] description.	0x00	R/W	Core clock	No
0x166C	[7:0]	Translation Profile 1.3 Buildout N Divider[7:0]		DPLL1 Feedback Divider (N_int): Phase Buildout Operation. This 32-bit unsigned value, $N\_int_{BUILDOUT}$ (default = 4000), sets the integer part of the divide ratio, N, for the feedback divider of DPLL1 when the DPLL operates in phase buildout mode. $N = N\_int_{BUILDOUT} + 1$ Thus, the default value yields N = 4001.	0x160	R/W	Core clock	No
0x166D	[7:0]	Translation Profile 1.3 Buildout N Divider[15:8]		Continuation of the Translation Profile 1.3 buildout N divider bit field. See the Translation Profile 1.3 Buildout N Divider[7:0] description.	0x15	R/W	Core clock	No
0x166E	[7:0]	Translation Profile 1.3 Buildout N Divider[23:16]		Continuation of the Translation Profile 1.3 buildout N divider bit field. See the Translation Profile 1.3 Buildout N Divider[7:0] description.	0x00	R/W	Core clock	No
0x166F	[7:0]	Translation Profile 1.3 Buildout N Divider[31:24]		Continuation of the Translation Profile 1.3 buildout N divider bit field. See the Translation Profile 1.3 Buildout N Divider[7:0] description.	0x00	R/W	Core clock	No
0x1670	[7:0]	Translation Profile 1.3 Buildout FRAC[7:0]		DPLL1 Feedback Divider (N_num): Phase Buildout Operation. This 24-bit unsigned value, $N\_num_{BUILDOUT}$ (default = 0), is the numerator of the fractional portion of the feedback divider of DPLL0 when the DPLL operates in phase buildout mode. The total divide ratio is as follows: $N\_total = (N\_int_{BUILDOUT} + 1) + (N\_num/N\_den)$ where: *N_den* is the denominator of the fractional portion of the feedback divider, which resides in Register 0x1675 to Register 0x1673, Bits[23:0]. $N\_num < N\_den$. To make N_total an integer, program N_num = 0 and N_den = 0.	0x00	R/W	Core clock	No
0x1671	[7:0]	Translation Profile 1.3 Buildout FRAC[15:8]		Continuation of the Translation Profile 1.3 buildout FRAC bit field. See the Translation Profile 1.3 Buildout FRAC[7:0] description.	0x00	R/W	Core clock	No
0x1672	[7:0]	Translation Profile 1.3 Buildout FRAC[23:16]		Continuation of the Translation Profile 1.3 buildout FRAC bit field. See the Translation Profile 1.3 Buildout FRAC[7:0] description.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1673	[7:0]	Translation Profile 1.3 Buildout MOD[7:0]		DPLL1 Feedback Divider (N_den): Phase Buildout Operation. This 24-bit unsigned value, $N\_den_{BUILDOUT}$ (default = 0), is the denominator of the fractional portion of the feedback divider of DPLL1 when the DPLL operates in phase buildout mode. The total divide ratio is as follows: $N\_total = (N\_int_{BUILDOUT} + 1) + (N\_num/N\_den)$ where *N_num* is the numerator of the fractional portion of the feedback divider, which resides in Register 0x1672 to Register 0x1670, Bits[23:0]. *N_num* < *N_den*. To make the N divider divide ratio an integer, program *N_num* = 0 and *N_den* = 0.	0x00	R/W	Core clock	No
0x1674	[7:0]	Translation Profile 1.3 Buildout MOD[15:8]		Continuation of the Translation Profile 1.3 buildout MOD bit field. See the Translation Profile 1.3 Buildout MOD[7:0] description.	0x00	R/W	Core clock	No
0x1675	[7:0]	Translation Profile 1.3 Buildout MOD[23:16]		Continuation of the Translation Profile 1.3 buildout MOD bit field. See the Translation Profile 1.3 Buildout MOD[7:0] description.	0x00	R/W	Core clock	No
0x1676	[7:4]	Reserved		Reserved.	0x0	R/W	Core clock	No
	[3:0]	Translation Profile 1.3 fast acquisition excess bandwidth		DPLL1 Fast Acquisition Excess Bandwidth Factor. This 3-bit unsigned value, ESF (default = 0), controls the behavior of the fast acquisition option for DPLL1, where ESF = 0 disables the fast acquisition feature. ESF constitutes an exponential scale factor applied to the nominal loop bandwidth of the DPLL (BW_0) to yield an excess bandwidth, EBW, as follows: $EBW = BW_0 \times 2^{ESF}$ The fast acquisition controller sets the loop bandwidth of the DPLL to EBW at the start of an acquisition sequence. When the DPLL indicates phase lock, the fast acquisition controller halves the loop bandwidth. The fast acquisition controller again waits for the DPLL to indicate phase lock. When the DPLL indicates phase lock, the fast acquisition controller again halves the loop bandwidth. The process repeats until the DPLL loop bandwidth reaches BW_0. The fast acquisition controller sets Register 0x3202, Bit 4 = 1 while sequencing through the loop bandwidth reduction steps to indicate its active status.	0x0	R/W	Core clock	No
			0	Fast acquisition controller disabled (default).				
			1	ESF = 1.				
			2	ESF = 2.				
			3	ESF = 3.				
			4	ESF = 4.				
			5	ESF = 5.				
			6	ESF = 6.				
			7	ESF = 7.				
			8	ESF = 8.				
			9	ESF = 9.				
			10	ESF = 10.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1677	7	Reserved		Reserved.	0	R	Live	No
	[6:4]	Translation Profile 1.3 fast acquisition Timeout		DPLL1 Fast Acquisition Timeout. This 3-bit unsigned value puts a time limit (t_{MAX}) on how long the fast acquisition controller waits for chatter free DPLL phase lock status to occur during each loop bandwidth reduction step. If the phase lock guard timer (see Bits[2:0]) fails to time out by t_{MAX}, the fast acquisition controller automatically moves on to the next loop bandwidth reduction step even though chatter free phase lock failed to occur. The fast acquisition controller indicates completion of the fast acquisition process by setting Register 0x3102, Bit 5 = 1 only when the fast acquisition controller is in its final bandwidth reduction step and the t_{MAX} timer fails to expire.	0x0	R/W	Core clock	No
			0	t_{MAX} = 10 ms (default).				
			1	t_{MAX} = 50 ms.				
			2	t_{MAX} = 100 ms.				
			3	t_{MAX} = 500 ms.				
			4	t_{MAX} = 1 sec.				
			5	t_{MAX} = 10 sec.				
			6	t_{MAX} = 50 sec.				
			7	t_{MAX} = 100 sec.				
	3	Reserved		Reserved.	0	R	Live	No
	[2:0]	Translation Profile 1.3 fast acquisition lock settle time		DPLL1 Fast Acquisition Phase Lock Guard Time. This 3-bit unsigned value, GUARD_TIME (default = 0), sets the period (t_{GUARD}) of a countdown timer used by the fast acquisition controller. The countdown timer starts when the DPLL indicates phase lock, but the fast acquisition controller reloads the countdown timer with a value per GUARD_TIME whenever the DPLL indicates phase unlock. It is only upon timeout of the countdown timer that the fast acquisition controller moves on to its next bandwidth reduction step. t_{GUARD} constitutes the minimum amount of time the fast acquisition controller must observe chatter free DPLL phase lock status during each loop bandwidth reduction step.	0x0	R/W	Core clock	No
			0	t_{GUARD} = 1 ms (default).				
			1	t_{GUARD} = 10 ms.				
			2	t_{GUARD} = 50 ms.				
			3	t_{GUARD} = 100 ms.				
			4	t_{GUARD} = 500 ms.				
			5	t_{GUARD} = 1 sec.				
			6	t_{GUARD} = 10 sec.				
			7	t_{GUARD} = 50 sec.				

TRANSLATION PROFILE 1.4 PARAMETERS—REGISTER 0x1680 TO REGISTER 0x1697

Table 82. Translation Profile 1.4 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1680	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	[5:1]	Translation Profile 1.4 selection priority		Translation Profile 1.4 Priority Value. This 5-bit unsigned value (default = 0) allows the user to assign a priority level to Translation Profile 1.4. Priority assignment (highest priority = 0, lowest priority = 31) allows DPLL1 to select one translation profile over another when reference switching.	0x00	R/W	Core clock	No
	0	Enable Translation Profile 1.4		Translation Profile 1.4 Enable. This bit enables Translation Profile 1.4 as a usable translation profile for DPLL1.	0	R/W	Core clock	No
			0	Disabled (default).				
			1	Enabled.				
0x1681	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:0]	Translation Profile 1.4 reference source selection		DPLL1 Reference Source Selection. This 5-bit unsigned value (default = 0) assigns a time stamp source as the input to DPLL1 when the DPLL activates Translation Profile 1.4.	0x00	R/W	Core clock	No
			0	REFA (default).				
			1	REFAA.				
			2	REFB.				
			3	REFBB.				
			4	Feedback from DPLL0.				
			6	Auxiliary REF0.				
			7	Auxiliary REF1.				
			8	Auxiliary NCO 0.				
			9	Auxiliary NCO 1.				
			11	Auxiliary REF2.				
			12	Auxiliary REF3.				
			13	Inverse User Time Stamper 0.				
			14	Inverse User Time Stamper 1.				
0x1682	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:0]	External zero-delay feedback path		DPLL1 External Zero-Delay Feedback Path. This 5-bit field (default = 0) selects a reference input as the feedback return path for DPLL1 when Translation Profile 1.4 is configured as a hitless external zero-delay profile. The selections of the reference input as the DPLL feedback are meaningless unless Register 0x1683, Bits[1:0] = 11 (binary).	0x00	R/W	Core clock	No
			0	REFA (default). When REFA is configured as a differential input, use this selection (not the REFAA selection).				
			1	REFAA.				
			2	REFB. When REFB is configured as a differential input, use this selection (not the REFBB selection).				
			3	REFBB.				
			4	Auxiliary REF0.				
			5	Auxiliary REF1.				
			6	Auxiliary REF2.				
			7	Auxiliary REF3.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[4:0]	Internal zero-delay feedback path		DPLL1 Internal Zero-Delay Feedback Path. This 5-bit field (default = 0) selects a Q divider output as the feedback return path for DPLL1 when Translation Profile 1.4 is configured as a hitless internal zero-delay profile. The selections of the Q divider output as the DPLL feedback return path are meaningless unless Register 0x1683, Bits[1:0] = 01 (binary).	0x00	R/W	Core clock	No
			0	Q1A Output as DPLL1 Feedback (default). When OUT1A is configured for differential mode, use this selection (not the Q1AA feedback selection).				
			1	Q1AA Output as DPLL1 Feedback.				
			2	Q1B Output as DPLL1 Feedback. When OUT1B is configured for differential mode, use this selection (not the Q1BB feedback selection).				
			3	Q1BB Output as DPLL1 Feedback.				
0x1683	7	Translation Profile 1.4 loop filter base		DPLL1 Loop Filter Base. This bit (default = 0) assigns one of the loop filter base coefficient sets (LFx) to DPLL1.	0	R/W	Core clock	No
			0	LF0 (default). Nominal 70° phase margin.				
			1	LF1. Nominal 88.5° phase margin (use this setting for applications requiring the response of the closed-loop transfer function of DPLL1 to have <0.1 dB peaking).				
	[6:5]	Reserved		Reserved.	0x0	R/W	Core clock	No
	[4:2]	Translation Profile 1.4 tag mode		DPLL1 Tag Modes. This 3-bit unsigned value (default = 0) selects the DPLL1 tag mode for Translation Profile 1.4.	0x0	R/W	Core clock	No
			0	No tagged time stamps in the reference or feedback path of DPLL1 (default).				
			1	Tagged time stamps only in the reference path of DPLL1.				
			2	Tagged time stamps only in the feedback path of DPLL1.				
			3	Tagged time stamps in the reference and feedback paths of DPLL1, but the untagged rates differ.				
			4	Tagged time stamps in the reference and feedback paths of DPLL1, but the untagged rates are equal.				
	[1:0]	Translation Profile 1.4 loop mode		DPLL1 Frequency Translation Mode. This 2-bit unsigned value (default = 0) establishes the frequency translation mode for DPLL1.	0x0	R/W	Core clock	No
			0	Phase buildout mode (default).				
			1	Hitless, internal zero delay mode.				
			3	Hitless, external zero delay mode.				
0x1684	[7:0]	Translation Profile 1.4 Loop Bandwidth[7:0]		DPLL1 Loop Bandwidth Scale Factor. This 32-bit unsigned value (default = 0) constitutes a scale factor (SF) applied to the base loop bandwidth (LBW_0) associated with the coefficients of Loop Filter LF0 or LF1. The resulting loop bandwidth (LBW) is LBW = SF × LBW_0. The default coefficients of LF0 and LF1 yield LBW_0 = 1 µHz (10^{-6} Hz). For example, given SF = 50,000,000, then LBW = 50 Hz for LF0 or LF1.	0x00	R/W	Core clock	No
0x1685	[7:0]	Translation Profile 1.4 Loop Bandwidth[15:8]		Continuation of the Translation Profile 1.4 loop bandwidth bit field. See the Translation Profile 1.4 Loop Bandwidth[7:0] description.	0x00	R/W	Core clock	No
0x1686	[7:0]	Translation Profile 1.4 Loop Bandwidth[23:16]		Continuation of the Translation Profile 1.4 loop bandwidth bit field. See the Translation Profile 1.4 Loop Bandwidth[7:0] description.	0x00	R/W	Core clock	No
0x1687	[7:0]	Translation Profile 1.4 Loop Bandwidth[31:24]		Continuation of the Translation Profile 1.4 loop bandwidth bit field. See the Translation Profile 1.4 Loop Bandwidth[7:0] description.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1688	[7:0]	Translation Profile 1.4 Hitless N Divider[7:0]		DPLL1 Feedback Divider (N): Hitless Zero-Delay Operation. This 32-bit unsigned value, N Hitless (default = 4000), sets the divide ratio, N, for the feedback divider of DPLL1 when the DPLL operates in internal hitless zero delay mode. $N = N\ Hitless + 1$ Thus, the default value yields N = 4001. A translation profile configured for external zero delay hitless DPLL operation uses Register 0x168F to Register 0x168C, Bits[31:0] instead of this register.	0x160	R/W	Core clock	No
0x1689	[7:0]	Translation Profile 1.4 Hitless N Divider[15:8]		Continuation of the Translation Profile 1.4 hitless N divider bit field. See the Translation Profile 1.4 Hitless N Divider[7:0] description.	0x15	R/W	Core clock	No
0x168A	[7:0]	Translation Profile 1.4 Hitless N Divider[23:16]		Continuation of the Translation Profile 1.4 hitless N divider bit field. See the Translation Profile 1.4 Hitless N Divider[7:0] description.	0x00	R/W	Core clock	No
0x168B	[7:0]	Translation Profile 1.4 Hitless N Divider[31:24]		Continuation of the Translation Profile 1.4 hitless N divider bit field. See the Translation Profile 1.4 Hitless N Divider[7:0] description.	0x00	R/W	Core clock	No
0x168C	[7:0]	Translation Profile 1.4 Buildout N Divider[7:0]		DPLL1 Feedback Divider (N_int): Phase Buildout Operation. This 32-bit unsigned value, $N\_int_{BUILDOUT}$ (default = 4000), sets the integer part of the divide ratio, N, for the feedback divider of DPLL1 when the DPLL operates in phase buildout mode. $N = N\_int_{BUILDOUT} + 1$ Thus, the default value yields N = 4001.	0x160	R/W	Core clock	No
0x168D	[7:0]	Translation Profile 1.4 Buildout N Divider[15:8]		Continuation of the Translation Profile 1.4 buildout N divider bit field. See the Translation Profile 1.4 Buildout N Divider[7:0] description.	0x15	R/W	Core clock	No
0x168E	[7:0]	Translation Profile 1.4 Buildout N Divider[23:16]		Continuation of the Translation Profile 1.4 buildout N divider bit field. See the Translation Profile 1.4 Buildout N Divider[7:0] description.	0x00	R/W	Core clock	No
0x168F	[7:0]	Translation Profile 1.4 Buildout N Divider[31:24]		Continuation of the Translation Profile 1.4 buildout N divider bit field. See the Translation Profile 1.4 Buildout N Divider[7:0] description.	0x00	R/W	Core clock	No
0x1690	[7:0]	Translation Profile 1.4 Buildout FRAC[7:0]		DPLL1 Feedback Divider (N_num): Phase Buildout Operation. This 24-bit unsigned value, $N\_num_{BUILDOUT}$ (default = 0), is the numerator of the fractional portion of the feedback divider of DPLL0 when the DPLL operates in phase buildout mode. The total divide ratio is as follows: $N\_total = (N\_int_{BUILDOUT} + 1) + (N\_num/N\_den)$ where: *N_den* is the denominator of the fractional portion of the feedback divider, which resides in Register 0x1695 to Register 0x1693, Bits[23:0]. $N\_num < N\_den$. To make N_total an integer, program N_num = 0 and N_den = 0.	0x00	R/W	Core clock	No
0x1691	[7:0]	Translation Profile 1.4 Buildout FRAC[15:8]		Continuation of the Translation Profile 1.4 buildout FRAC bit field. See the Translation Profile 1.4 Buildout FRAC[7:0] description.	0x00	R/W	Core clock	No
0x1692	[7:0]	Translation Profile 1.4 Buildout FRAC[23:16]		Continuation of the Translation Profile 1.4 buildout FRAC bit field. See the Translation Profile 1.4 Buildout FRAC[7:0] description.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1693	[7:0]	Translation Profile 1.4 Buildout MOD[7:0]		DPLL1 Feedback Divider (N_den): Phase Buildout Operation. This 24-bit unsigned value, $N\_den_{BUILDOUT}$ (default = 0), is the denominator of the fractional portion of the feedback divider of DPLL1 when the DPLL operates in phase buildout mode. The total divide ratio is as follows: $N\_total = (N\_int_{BUILDOUT} + 1) + (N\_num/N\_den)$ where *N_num* is the numerator of the fractional portion of the feedback divider, which resides in Register 0x1692 to Register 0x1690, Bits[23:0]. *N_num* < *N_den*. To make the N divider divide ratio an integer, program *N_num* = 0 and *N_den* = 0.	0x00	R/W	Core clock	No
0x1694	[7:0]	Translation Profile 1.4 Buildout MOD[15:8]		Continuation of the Translation Profile 1.4 buildout MOD bit field. See the Translation Profile 1.4 Buildout MOD[7:0] description.	0x00	R/W	Core clock	No
0x1695	[7:0]	Translation Profile 1.4 Buildout MOD[23:16]		Continuation of the Translation Profile 1.4 buildout MOD bit field. See the Translation Profile 1.4 Buildout MOD[7:0] description.	0x00	R/W	Core clock	No
0x1696	[7:4]	Reserved		Reserved.	0x0	R/W	Core clock	No
	[3:0]	Translation Profile 1.4 fast acquisition excess bandwidth		DPLL1 Fast Acquisition Excess Bandwidth Factor. This 3-bit unsigned value, ESF (default = 0), controls the behavior of the fast acquisition option for DPLL1, where ESF = 0 disables the fast acquisition feature. ESF constitutes an exponential scale factor applied to the nominal loop bandwidth of the DPLL (BW_0) to yield an excess bandwidth, EBW, as follows: $EBW = BW_0 \times 2^{ESF}$ The fast acquisition controller sets the loop bandwidth of the DPLL to EBW at the start of an acquisition sequence. When the DPLL indicates phase lock, the fast acquisition controller halves the loop bandwidth. The fast acquisition controller again waits for the DPLL to indicate phase lock. When the DPLL indicates phase lock, the fast acquisition controller again halves the loop bandwidth. The process repeats until the DPLL loop bandwidth reaches BW_0. The fast acquisition controller sets Register 0x3202, Bit 4 = 1 while sequencing through the loop bandwidth reduction steps to indicate its active status.	0x0	R/W	Core clock	No
			0	Fast acquisition controller disabled (default).				
			1	ESF = 1.				
			2	ESF = 2.				
			3	ESF = 3.				
			4	ESF = 4.				
			5	ESF = 5.				
			6	ESF = 6.				
			7	ESF = 7.				
			8	ESF = 8.				
			9	ESF = 9.				
			10	ESF = 10.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x1697	7	Reserved		Reserved.	0	R	Live	No
	[6:4]	Translation Profile 1.4 fast acquisition timeout		DPLL1 Fast Acquisition Timeout. This 3-bit unsigned value puts a time limit (t_{MAX}) on how long the fast acquisition controller waits for chatter free DPLL phase lock status to occur during each loop bandwidth reduction step. If the phase lock guard timer (see Bits[2:0]) fails to time out by t_{MAX}, the fast acquisition controller automatically moves on to the next loop bandwidth reduction step even though chatter free phase lock failed to occur. The fast acquisition controller indicates completion of the fast acquisition process by setting Register 0x3102, Bit 5 = 1 only when the fast acquisition controller is in its final bandwidth reduction step and the t_{MAX} timer fails to expire.	0x0	R/W	Core clock	No
			0	t_{MAX} = 10 ms (default).				
			1	t_{MAX} = 50 ms.				
			2	t_{MAX} = 100 ms.				
			3	t_{MAX} = 500 ms.				
			4	t_{MAX} = 1 sec.				
			5	t_{MAX} = 10 sec.				
			6	t_{MAX} = 50 sec.				
			7	t_{MAX} = 100 sec.				
	3	Reserved		Reserved.	0	R	Live	No
	[2:0]	Translation Profile 1.4 fast acquisition lock settle time		DPLL1 Fast Acquisition Phase Lock Guard Time. This 3-bit unsigned value, GUARD_TIME (default = 0) sets the period (t_{GUARD}) of a countdown timer used by the fast acquisition controller. The countdown timer starts when the DPLL indicates phase lock, but the fast acquisition controller reloads the countdown timer with a value per GUARD_TIME whenever the DPLL indicates phase unlock. It is only upon timeout of the countdown timer that the fast acquisition controller moves on to its next bandwidth reduction step. t_{GUARD} constitutes the minimum amount of time the fast acquisition controller must observe chatter free DPLL phase lock status during each loop bandwidth reduction step.	0x0	R/W	Core clock	No
			0	t_{GUARD} = 1 ms (default).				
			1	t_{GUARD} = 10 ms.				
			2	t_{GUARD} = 50 ms.				
			3	t_{GUARD} = 100 ms.				
			4	t_{GUARD} = 500 ms.				
			5	t_{GUARD} = 1 sec.				
			6	t_{GUARD} = 10 sec.				
			7	t_{GUARD} = 50 sec.				

TRANSLATION PROFILE 1.5 PARAMETERS—REGISTER 0x16A0 TO REGISTER 0x16B7

Table 83. Translation Profile 1.5 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x16A0	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	[5:1]	Translation Profile 1.5 selection priority		Translation Profile 1.5 Priority Value. This 5-bit unsigned value (default = 0) allows the user to assign a priority level to Translation Profile 1.5. Priority assignment (highest priority = 0, lowest priority = 31) allows DPLL1 to select one translation profile over another when reference switching.	0x00	R/W	Core clock	No
	0	Enable Translation Profile 1.5		Translation Profile 1.5 Enable. This bit enables Translation Profile 1.5 as a usable translation profile for DPLL1.	0	R/W	Core clock	No
			0	Disabled (default).				
			1	Enabled.				
0x16A1	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:0]	Translation Profile 1.5 reference source selection		DPLL1 Reference Source Selection. This 5-bit unsigned value (default = 0) assigns a time stamp source as the input to DPLL1 when the DPLL activates Translation Profile 1.5.	0x00	R/W	Core clock	No
			0	REFA (default).				
			1	REFAA.				
			2	REFB.				
			3	REFBB.				
			4	Feedback from DPLL0.				
			6	Auxiliary REF0.				
			7	Auxiliary REF1.				
			8	Auxiliary NCO 0.				
			9	Auxiliary NCO 1.				
			11	Auxiliary REF2.				
			12	Auxiliary REF3.				
			13	Inverse User Time Stamper 0.				
			14	Inverse User Time Stamper 1.				
0x16A2	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	[4:0]	External zero-delay feedback path		DPLL1 External Zero-Delay Feedback Path. This 5-bit field (default = 0) selects a reference input as the feedback return path for DPLL1 when Translation Profile 1.5 is configured as a hitless external zero-delay profile. The selections of the reference input as the DPLL feedback are meaningless unless Register 0x16A3, Bits[1:0] = 11 (binary).	0x00	R/W	Core clock	No
			0	REFA (default). When REFA is configured as a differential input, use this selection (not the REFAA selection).				
			1	REFAA.				
			2	REFB. When REFB is configured as a differential input, use this selection (not the REFBB selection).				
			3	REFBB.				
			4	Auxiliary REF0.				
			5	Auxiliary REF1.				
			6	Auxiliary REF2.				
			7	Auxiliary REF3.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[4:0]	Internal zero-delay feedback path		DPLL1 Internal Zero-Delay Feedback Path. This 5-bit field (default = 0) selects a Q divider output as the feedback return path for DPLL1 when Translation Profile 1.5 is configured as a hitless internal zero-delay profile. The selections of the Q divider output as the DPLL feedback return path are meaningless unless Register 0x16A3, Bits[1:0] = 01 (binary).	0x00	R/W	Core clock	No
			0	Q1A Output as DPLL1 Feedback (default). When OUT1A is configured for differential mode, use this selection (not the Q1AA feedback selection).				
			1	Q1AA Output as DPLL1 Feedback.				
			2	Q1B Output as DPLL1 Feedback. When OUT1B is configured for differential mode, use this selection (not the Q1BB feedback selection).				
			3	Q1BB Output as DPLL1 Feedback.				
0x16A3	7	Translation Profile 1.5 loop filter base		DPLL1 Loop Filter Base. This bit (default = 0) assigns one of the loop filter base coefficient sets (LFx) to DPLL1.	0	R/W	Core clock	No
			0	LF0 (default). Nominal 70° phase margin.				
			1	LF1. Nominal 88.5° phase margin (use this setting for applications requiring the response of the closed-loop transfer function of DPLL1 to have <0.1 dB peaking).				
	[6:5]	Reserved		Reserved.	0x0	R/W	Core clock	No
	[4:2]	Translation Profile 1.5 tag mode		DPLL1 Tag Modes. This 3-bit unsigned value (default = 0) selects the DPLL1 tag mode for Translation Profile 1.5.	0x0	R/W	Core clock	No
			0	No tagged time stamps in the reference or feedback path of DPLL1 (default).				
			1	Tagged time stamps only in the reference path of DPLL1.				
			2	Tagged time stamps only in the feedback path of DPLL1.				
			3	Tagged time stamps in the reference and feedback paths of DPLL1, but the untagged rates differ.				
			4	Tagged time stamps in the reference and feedback paths of DPLL1, but the untagged rates are equal.				
	[1:0]	Translation Profile 1.5 loop mode		DPLL1 Frequency Translation Mode. This 2-bit unsigned value (default = 0) establishes the frequency translation mode for DPLL1.	0x0	R/W	Core clock	No
			0	Phase buildout mode (default).				
			1	Hitless, internal zero delay mode.				
			3	Hitless, external zero delay mode.				
0x16A4	[7:0]	Translation Profile 1.5 Loop Bandwidth[7:0]		DPLL1 Loop Bandwidth Scale Factor. This 32-bit unsigned value (default = 0) constitutes a scale factor (SF) applied to the base loop bandwidth (LBW_0) associated with the coefficients of Loop Filter LF0 or LF1. The resulting loop bandwidth (LBW) is LBW = SF × LBW_0. The default coefficients of LF0 and LF1 yield LBW_0 = 1 µHz (10^{-6} Hz). For example, given SF = 50,000,000, then LBW = 50 Hz for LF0 or LF1.	0x00	R/W	Core clock	No
0x16A5	[7:0]	Translation Profile 1.5 Loop Bandwidth[15:8]		Continuation of the Translation Profile 1.5 loop bandwidth bit field. See the Translation Profile 1.5 Loop Bandwidth[7:0] description.	0x00	R/W	Core clock	No
0x16A6	[7:0]	Translation Profile 1.5 Loop Bandwidth[23:16]		Continuation of the Translation Profile 1.5 loop bandwidth bit field. See the Translation Profile 1.5 Loop Bandwidth[7:0] description.	0x00	R/W	Core clock	No
0x16A7	[7:0]	Translation Profile 1.5 Loop Bandwidth[31:24]		Continuation of the Translation Profile 1.5 loop bandwidth bit field. See the Translation Profile 1.5 Loop Bandwidth[7:0] description.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x16A8	[7:0]	Translation Profile 1.5 Hitless N Divider[7:0]		DPLL1 Feedback Divider (N): Hitless Zero-Delay Operation. This 32-bit unsigned value, N Hitless (default = 4000), sets the divide ratio, N, for the feedback divider of DPLL1 when the DPLL operates in internal hitless zero delay mode. $N = N\,Hitless + 1$ Thus, the default value yields N = 4001. A translation profile configured for external zero delay hitless DPLL operation uses Register 0x16AF to Register 0x16AC, Bits[31:0] instead of this register.	0x160	R/W	Core clock	No
0x16A9	[7:0]	Translation Profile 1.5 Hitless N Divider[15:8]		Continuation of the Translation Profile 1.5 hitless N divider bit field. See the Translation Profile 1.5 Hitless N Divider[7:0] description.	0x15	R/W	Core clock	No
0x16AA	[7:0]	Translation Profile 1.5 Hitless N Divider[23:16]		Continuation of the Translation Profile 1.5 hitless N divider bit field. See the Translation Profile 1.5 Hitless N Divider[7:0] description.	0x00	R/W	Core clock	No
0x16AB	[7:0]	Translation Profile 1.5 Hitless N Divider[31:24]		Continuation of the Translation Profile 1.5 hitless N divider bit field. See the Translation Profile 1.5 Hitless N Divider[7:0] description.	0x00	R/W	Core clock	No
0x16AC	[7:0]	Translation Profile 1.5 Buildout N Divider[7:0]		DPLL1 Feedback Divider (N_int): Phase Buildout Operation. This 32-bit unsigned value, $N\_int_{BUILDOUT}$ (default = 4000), sets the integer part of the divide ratio, N, for the feedback divider of DPLL1 when the DPLL operates in phase buildout mode. $N = N\_int_{BUILDOUT} + 1$ Thus, the default value yields N = 4001.	0x160	R/W	Core clock	No
0x16AD	[7:0]	Translation Profile 1.5 Buildout N Divider[15:8]		Continuation of the Translation Profile 1.5 buildout N divider bit field. See the Translation Profile 1.5 Buildout N Divider[7:0] description.	0x15	R/W	Core clock	No
0x16AE	[7:0]	Translation Profile 1.5 Buildout N Divider[23:16]		Continuation of the Translation Profile 1.5 buildout N divider bit field. See the Translation Profile 1.5 Buildout N Divider[7:0] description.	0x00	R/W	Core clock	No
0x16AF	[7:0]	Translation Profile 1.5 Buildout N Divider[31:24]		Continuation of the Translation Profile 1.5 buildout N divider bit field. See the Translation Profile 1.5 Buildout N Divider[7:0] description.	0x00	R/W	Core clock	No
0x16B0	[7:0]	Translation Profile 1.5 Buildout FRAC[7:0]		DPLL1 Feedback Divider (N_num): Phase Buildout Operation. This 24-bit unsigned value, $N\_num_{BUILDOUT}$ (default = 0), is the numerator of the fractional portion of the feedback divider of DPLL0 when the DPLL operates in phase buildout mode. The total divide ratio is as follows: $N\_total = (N\_int_{BUILDOUT} + 1) + (N\_num/N\_den)$ where: *N_den* is the denominator of the fractional portion of the feedback divider, which resides in Register 0x16B5 to Register 0x16B3, Bits[23:0]. $N\_num < N\_den$. To make N_total an integer, program N_num = 0 and N_den = 0.	0x00	R/W	Core clock	No
0x16B1	[7:0]	Translation Profile 1.5 Buildout FRAC[15:8]		Continuation of the Translation Profile 1.5 buildout FRAC bit field. See the Translation Profile 1.5 Buildout FRAC[7:0] description.	0x00	R/W	Core clock	No
0x16B2	[7:0]	Translation Profile 1.5 Buildout FRAC[23:16]		Continuation of the Translation Profile 1.5 buildout FRAC bit field. See the Translation Profile 1.5 Buildout FRAC[7:0] description.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x16B3	[7:0]	Translation Profile 1.5 Buildout MOD[7:0]		DPLL1 Feedback Divider (N_den): Phase Buildout Operation. This 24-bit unsigned value, $N\_den_{BUILDOUT}$ (default = 0), is the denominator of the fractional portion of the feedback divider of DPLL1 when the DPLL operates in phase buildout mode. The total divide ratio is as follows: $N\_total = (N\_int_{BUILDOUT} + 1) + (N\_num/N\_den)$ where *N_num* is the numerator of the fractional portion of the feedback divider, which resides in Register 0x16B5 to Register 0x16B3, Bits[23:0]. *N_num* < *N_den*. To make the N divider divide ratio an integer, program *N_num* = 0 and *N_den* = 0.	0x00	R/W	Core clock	No
0x16B4	[7:0]	Translation Profile 1.5 Buildout MOD[15:8]		Continuation of the Translation Profile 1.5 buildout MOD bit field. See the Translation Profile 1.5 Buildout MOD[7:0] description.	0x00	R/W	Core clock	No
0x16B5	[7:0]	Translation Profile 1.5 Buildout MOD[23:16]		Continuation of the Translation Profile 1.5 buildout MOD bit field. See the Translation Profile 1.5 Buildout MOD[7:0] description.	0x00	R/W	Core clock	No
0x16B6	[7:4]	Reserved		Reserved.	0x0	R/W	Core clock	No
	[3:0]	Translation Profile 1.5 fast acquisition excess bandwidth		DPLL1 Fast Acquisition Excess Bandwidth Factor. This 3-bit unsigned value, ESF (default = 0), controls the behavior of the fast acquisition option for DPLL1, where ESF = 0 disables the fast acquisition feature. ESF constitutes an exponential scale factor applied to the nominal loop bandwidth of the DPLL (BW_0) to yield an excess bandwidth, EBW, as follows: $EBW = BW_0 \times 2^{ESF}$ The fast acquisition controller sets the loop bandwidth of the DPLL to EBW at the start of an acquisition sequence. When the DPLL indicates phase lock, the fast acquisition controller halves the loop bandwidth. The fast acquisition controller again waits for the DPLL to indicate phase lock. When the DPLL indicates phase lock, the fast acquisition controller again halves the loop bandwidth. The process repeats until the DPLL loop bandwidth reaches BW_0. The fast acquisition controller sets Register 0x3202, Bit 4 = 1 while sequencing through the loop bandwidth reduction steps to indicate its active status.	0x0	R/W	Core clock	No
			0	Fast acquisition controller disabled (default).				
			1	ESF = 1.				
			2	ESF = 2.				
			3	ESF = 3.				
			4	ESF = 4.				
			5	ESF = 5.				
			6	ESF = 6.				
			7	ESF = 7.				
			8	ESF = 8.				
			9	ESF = 9.				
			10	ESF = 10.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x16B7	7	Reserved		Reserved.	0	R	Live	No
	[6:4]	Translation Profile 1.5 fast acquisition timeout		DPLL1 Fast Acquisition Timeout. This 3-bit unsigned value puts a time limit (t_{MAX}) on how long the fast acquisition controller waits for chatter free DPLL phase lock status to occur during each loop bandwidth reduction step. If the phase lock guard timer (see Bits[2:0]) fails to time out by t_{MAX}, the fast acquisition controller automatically moves on to the next loop bandwidth reduction step even though chatter free phase lock failed to occur. The fast acquisition controller indicates completion of the fast acquisition process by setting Register 0x3102, Bit 5 = 1 only when the fast acquisition controller is in its final bandwidth reduction step and the t_{MAX} timer fails to expire.	0x0	R/W	Core clock	No
			0	t_{MAX} = 10 ms (default).				
			1	t_{MAX} = 50 ms.				
			2	t_{MAX} = 100 ms.				
			3	t_{MAX} = 500 ms.				
			4	t_{MAX} = 1 sec.				
			5	t_{MAX} = 10 sec.				
			6	t_{MAX} = 50 sec.				
			7	t_{MAX} = 100 sec.				
	3	Reserved		Reserved.	0	R	Live	No
	[2:0]	Translation Profile 1.5 fast acquisition lock settle time		DPLL1 Fast Acquisition Phase Lock Guard Time. This 3-bit unsigned value, GUARD_TIME (default = 0), sets the period (t_{GUARD}) of a countdown timer used by the fast acquisition controller. The countdown timer starts when the DPLL indicates phase lock, but the fast acquisition controller reloads the countdown timer with a value per GUARD_TIME whenever the DPLL indicates phase unlock. It is only upon timeout of the countdown timer that the fast acquisition controller moves on to its next bandwidth reduction step. t_{GUARD} constitutes the minimum amount of time the fast acquisition controller must observe chatter free DPLL phase lock status during each loop bandwidth reduction step.	0x0	R/W	Core clock	No
			0	t_{GUARD} = 1 ms (default).				
			1	t_{GUARD} = 10 ms.				
			2	t_{GUARD} = 50 ms.				
			3	t_{GUARD} = 100 ms.				
			4	t_{GUARD} = 500 ms.				
			5	t_{GUARD} = 1 sec.				
			6	t_{GUARD} = 10 sec.				
			7	t_{GUARD} = 50 sec.				

OPERATIONAL CONTROL: GENERAL—REGISTER 0x2000 TO REGISTER 0x2004

Table 84. Operational Controls: General Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x2000	[7:4]	Reserved		Reserved.	0x0	R/W	Serial port clock	No
	3	All sync		Synchronize All Distribution Dividers. Setting this bit to Logic 1 synchronizes all distribution dividers.	0	R/W	Serial port clock	No
	2	SYSCLK calibrate		Calibrate the System Clock PLL. Setting this bit to Logic 1 calibrates the system clock PLL.	0	R/W	Serial port clock	No
	1	All calibrate		Calibrate PLLs. Setting this bit to Logic 1 calibrates the system clock PLL and both APLLs.	0	R/W	Serial port clock	No
	0	All power-down		Device Power-Down. Setting this bit to Logic 1 powers down the system clock PLL, REFx, and Auxiliary REFx circuits (receivers, TDCs, dividers, demodulators), both DPLLs, both APLLs, and the temperature sensor.	0	R/W	Serial port clock	No
0x2001	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	3	Reference TDC REFBB power-down		REFBB Power-Down. Setting this bit to Logic 1 powers down the REFBB divider and TDC. Setting both this bit and Bit 2 to Logic 1 also powers down the input receivers and demodulator associated with REFB/REFBB.	0	R/W	Serial port clock	No
	2	Reference TDC REFB power-down		REFB Power-Down. Setting this bit to Logic 1 powers down the REFB divider and TDC. Setting both this bit and Bit 3 to Logic 1 also powers down the input receivers and demodulator associated with REFB/REFBB.	0	R/W	Serial port clock	No
	1	Reference TDC REFAA power-down		REFAA Power-Down. Setting this bit to Logic 1 powers down the REFAA divider and TDC. Setting both this bit and Bit 0 to Logic 1 also powers down the input receivers and demodulator associated with REFA/REFAA.	0	R/W	Serial port clock	No
	0	Reference TDC REFA power-down		REFA Power-Down. Setting this bit to Logic 1 powers down the REFA divider and TDC. Setting both this bit and Bit 1 to Logic 1 also powers down the input receivers and demodulator associated with REFA/REFAA.	0	R/W	Serial port clock	No
0x2002	7	Timeout Reference Monitor Auxiliary REF3		Force a Timeout of the Auxiliary REF3 Validation Timer. Setting this bit to Logic 1 forces the Auxiliary REF3 reference monitor validation timer to time out immediately.	0	R/W	Core clock	Yes
	6	Timeout Reference Monitor Auxiliary REF2		Force a Timeout of the Auxiliary REF2 Validation Timer. Setting this bit to Logic 1 forces the Auxiliary REF2 reference monitor validation timer to time out immediately.	0	R/W	Core clock	Yes
	5	Timeout Reference Monitor Auxiliary REF1		Force a Timeout of the Auxiliary REF1 Validation Timer. Setting this bit to Logic 1 forces the Auxiliary REF1 reference monitor validation timer to time out immediately.	0	R/W	Core clock	Yes
	4	Timeout Reference Monitor Auxiliary REF0		Force a Timeout of the Auxiliary REF0 Validation Timer. Setting this bit to Logic 1 forces the Auxiliary REF0 reference monitor validation timer to time out immediately.	0	R/W	Core clock	Yes
	3	Reference Monitor REFBB timeout		Force a Timeout of the REFBB Validation Timer. Setting this bit to Logic 1 forces the REFBB reference monitor validation timer to time out immediately.	0	R/W	Core clock	Yes

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	2	Reference Monitor REFB timeout		Force a Timeout of the REFB Validation Timer. Setting this bit to Logic 1 forces the REFB reference monitor validation timer to time out immediately.	0	R/W	Core clock	Yes
	1	Reference Monitor REFAA timeout		Force a Timeout of the REFAA Validation Timer. Setting this bit to Logic 1 forces the REFAA reference monitor validation timer to time out immediately.	0	R/W	Core clock	Yes
	0	Reference Monitor REFA timeout		Force a Timeout of the REFA Validation Timer. Setting this bit to Logic 1 forces the REFA reference monitor validation timer to time out immediately.	0	R/W	Core clock	Yes
0x2003	7	Invalidate Auxiliary REF3		Force Invalidation of Auxiliary REF3. Setting this bit to Logic 1 forces invalidation of Auxiliary REF3. The meaning of Logic 0 depends on the state of Register 0x2004, Bit 7.	0	R/W	Core clock	No
	6	Invalidate Auxiliary REF2		Force Invalidation of Auxiliary REF2. Setting this bit to Logic 1 forces invalidation of Auxiliary REF2. The meaning of Logic 0 depends on the state of Register 0x2004, Bit 6.	0	R/W	Core clock	No
	5	Invalidate Auxiliary REF1		Force Invalidation of Auxiliary REF1. Setting this bit to Logic 1 forces invalidation of Auxiliary REF1. The meaning of Logic 0 depends on the state of Register 0x2004, Bit 5.	0	R/W	Core clock	No
	4	Invalidate Auxiliary REF0		Force Invalidation of Auxiliary REF0. Setting this bit to Logic 1 forces invalidation of Auxiliary REF0. The meaning of Logic 0 depends on the state of Register 0x2004, Bit 4.	0	R/W	Core clock	No
	3	Invalidate REFBB		Force Invalidation of REFBB. Setting this bit to Logic 1 forces invalidation of REFBB. The meaning of Logic 0 depends on the state of Register 0x2004, Bit 3.	0	R/W	Core clock	No
	2	Invalidate REFB		Force Invalidation of REFB. Setting this bit to Logic 1 forces invalidation of REFB. The meaning of Logic 0 depends on the state of Register 0x2004, Bit 2.	0	R/W	Core clock	No
	1	Invalidate REFAA		Force Invalidation of REFAA. Setting this bit to Logic 1 forces invalidation of REFAA. The meaning of Logic 0 depends on the state of Register 0x2004, Bit 1.	0	R/W	Core clock	No
	0	Invalidate REFA		Force Invalidation of REFA. Setting this bit to Logic 1 forces invalidation of REFA. The meaning of Logic 0 depends on the state of Register 0x2004, Bit 0.	0	R/W	Core clock	No
0x2004	7	Bypass Reference Monitor Auxiliary REF3		Bypass Automatic Validation/Invalidation of Auxiliary REF3. This bit affects the behavior of the Auxiliary REF3 reference monitor valid/invalid indication mechanism.	0	R/W	Core clock	No
			0	Auxiliary REF3 invalidates manually when the user programs Register 0x2003, Bit 7 = 1 or invalidates automatically when Register 0x3022, Bit 3 = 1 (Auxiliary REF3 reference monitor fault indication). When Auxiliary REF3 is unfaulted (Register 0x3022, Bit 3 = 0), the user can fault Auxiliary REF3 by programming Register 0x2003, Bit 7 = 1. However, when Auxiliary REF3 is faulted (Register 0x3022, Bit 3 = 1), programming Register 0x2003, Bit 7 = 0 does not unfault Auxiliary REF3.				
			1	The Auxiliary REF3 reference monitor continues to indicate fault/unfault status via Register 0x3022, Bit 3, but the user manually validates Auxiliary REF3 by programming Register 0x2003, Bit 7 = 0 or invalidates Auxiliary REF3 by programming Register 0x2003, Bit 7 = 1.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	6	Bypass Reference Monitor Auxiliary REF2		Bypass Automatic Validation/Invalidation of Auxiliary REF2. This bit affects the behavior of the Auxiliary REF2 reference monitor valid/invalid indication mechanism.	0	R/W	Core clock	No
			0	Auxiliary REF2 invalidates manually when the user programs Register 0x2003, Bit 6 = 1 or invalidates automatically when Register 0x3021, Bit 3 = 1 (Auxiliary REF2 reference monitor fault indication). When Auxiliary REF2 is unfaulted (Register 0x3021, Bit 3 = 0), the user can fault Auxiliary REF2 by programming Register 0x2003, Bit 6 = 1. However, when Auxiliary REF2 is faulted (Register 0x3021, Bit 3 = 1), programming Register 0x2003, Bit 6 = 0 does not unfault Auxiliary REF2.				
			1	The Auxiliary REF2 reference monitor continues to indicate fault/unfault status via Register 0x3021, Bit 3, but the user manually validates Auxiliary REF2 by programming Register 0x2003, Bit 6 = 0 or invalidates Auxiliary REF2 by programming Register 0x2003, Bit 6 = 1.				
	5	Bypass Reference Monitor Auxiliary REF1		Bypass Automatic Validation/Invalidation of Auxiliary REF1. This bit affects the behavior of the Auxiliary REF1 reference monitor valid/invalid indication mechanism.	0	R/W	Core clock	No
			0	Auxiliary REF1 invalidates manually when the user programs Register 0x2003, Bit 5 = 1 or invalidates automatically when Register 0x3020, Bit 3 = 1 (Auxiliary REF1 reference monitor fault indication). When Auxiliary REF1 is unfaulted (Register 0x3020, Bit 3 = 0), the user can fault Auxiliary REF1 by programming Register 0x2003, Bit 5 = 1. However, when Auxiliary REF1 is faulted (Register 0x3020, Bit 3 = 1), programming Register 0x2003, Bit 5 = 0 does not unfault Auxiliary REF1.				
			1	The Auxiliary REF1 reference monitor continues to indicate fault/unfault status via Register 0x3020, Bit 3, but the user manually validates Auxiliary REF1 by programming Register 0x2003, Bit 5 = 0 or invalidates Auxiliary REF1 by programming Register 0x2003, Bit 5 = 1.				
	4	Bypass Reference Monitor Auxiliary REF0		Bypass Automatic Validation/Invalidation of Auxiliary REF0. This bit affects the behavior of the Auxiliary REF0 reference monitor valid/invalid indication mechanism.	0	R/W	Core clock	No
			0	Auxiliary REF0 invalidates manually when the user programs Register 0x2003, Bit 4 = 1 or invalidates automatically when Register 0x301F, Bit 3 = 1 (Auxiliary REF0 reference monitor fault indication). When Auxiliary REF0 is unfaulted (Register 0x301F, Bit 3 = 0), the user can fault Auxiliary REF0 by programming Register 0x2003, Bit 4 = 1. However, when Auxiliary REF0 is faulted (Register 0x301F, Bit 3 = 1), programming Register 0x2003, Bit 4 = 0 does not unfault Auxiliary REF0.				
			1	The Auxiliary REF0 reference monitor continues to indicate fault/unfault status via Register 0x301F, Bit 3, but the user manually validates Auxiliary REF0 by programming Register 0x2003, Bit 4 = 0 or invalidates Auxiliary REF0 by programming Register 0x2003, Bit 4 = 1.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	3	Reference Monitor REFBB bypass		Bypass Automatic Validation/Invalidation of REFBB. This bit affects the behavior of the REFBB reference monitor valid/invalid indication mechanism.	0	R/W	Core clock	No
			0	REFBB invalidates manually when the user programs Register 0x2003, Bit 3 = 1 or invalidates automatically when Register 0x3008, Bit 3 = 1 (REFBB reference monitor fault indication). When REFBB is unfaulted (Register 0x3008, Bit 3 = 0), the user can fault REFBB by programming Register 0x2003, Bit 3 = 1. However, when REFBB is faulted (Register 0x3008, Bit 3 = 1), programming Register 0x2003, Bit 3 = 0 does not unfault REFBB.				
			1	The REFBB reference monitor continues to indicate fault/unfault status via Register 0x3008, Bit 3, but the user manually validates REFBB by programming Register 0x2003, Bit 3 = 0 or invalidates REFBB by programming Register 0x2003, Bit 3 = 1.				
	2	Reference Monitor REFB bypass		Bypass Automatic Validation/Invalidation of REFB. This bit affects the behavior of the REFB reference monitor valid/invalid indication mechanism.	0	R/W	Core clock	No
			0	REFB invalidates manually when the user programs Register 0x2003, Bit 2 = 1 or invalidates automatically when Register 0x3007, Bit 3 = 1 (REFB reference monitor fault indication). When REFB is unfaulted (Register 0x3007, Bit 3 = 0), the user can fault REFB by programming Register 0x2003, Bit 2 = 1. However, when REFB is faulted (Register 0x3007, Bit 3 = 1), programming Register 0x2003, Bit 2 = 0 does not unfault REFB.				
			1	The REFB reference monitor continues to indicate fault/unfault status via Register 0x3007, Bit 3, but the user manually validates REFB by programming Register 0x2003, Bit 2 = 0 or invalidates REFB by programming Register 0x2003, Bit 2 = 1.				
	1	Reference Monitor REFAA bypass		Bypass Automatic Validation/Invalidation of REFAA. This bit affects the behavior of the REFAA reference monitor valid/invalid indication mechanism.	0	R/W	Core clock	No
			0	REFAA invalidates manually when the user programs Register 0x2003, Bit 1 = 1 or invalidates automatically when Register 0x3006, Bit 3 = 1 (REFAA reference monitor fault indication). When REFAA is unfaulted (Register 0x3006, Bit 3 = 0), the user can fault REFAA by programming Register 0x2003, Bit 1 = 1. However, when REFAA is faulted (Register 0x3006, Bit 3 = 1), programming Register 0x2003, Bit 1 = 0 does not unfault REFAA.				
			1	The REFAA reference monitor continues to indicate fault/unfault status via Register 0x3006, Bit 3, but the user manually validates REFAA by programming Register 0x2003, Bit 1 = 0 or invalidates REFAA by programming Register 0x2003, Bit 1 = 1.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	0	Reference Monitor REFA bypass		Bypass Automatic Validation/Invalidation of REFA. This bit affects the behavior of the REFA reference monitor valid/invalid indication mechanism.	0	R/W	Core clock	No
			0	REFA invalidates manually when the user programs Register 0x2003, Bit 0 = 1 or invalidates automatically when Register 0x3005, Bit 3 = 1 (REFA reference monitor fault indication). When REFA is unfaulted (Register 0x3005, Bit 3 = 0), the user can fault REFA by programming Register 0x2003, Bit 0 = 1. However, when REFA is faulted (Register 0x3005, Bit 3 = 1), programming Register 0x2003, Bit 0 = 0 does not unfault REFA.				
			1	The REFA reference monitor continues to indicate fault/unfault status via Register 0x3005, Bit 3, but the user manually validates REFA by programming Register 0x2003, Bit 0 = 0 or invalidates REFA by programming Register 0x2003, Bit 0 = 1.				

IRQ CLEAR—REGISTER 0x2005 TO REGISTER 0x2019

Table 85. IRQ Clear Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x2005	7	Reset watchdog timer		Reset Watchdog Timer. Setting this bit to Logic 1 resets the watchdog timer. A timeout of the watchdog timer causes a watchdog IRQ (assuming Register 0x010C, Bit 2 = 1) or strobe pulse on an appropriately configured Mx status pin. Regularly resetting the watchdog timer before it times out prevents the occurrence of a watchdog IRQ or a watchdog strobe pulse.	0	R/W	Core clock	Yes
	[6:4]	Reserved		Reserved.	0x0	R	Live	No
	3	Clear all IRQ status bits in the IRQ PLL1 group		Clear All IRQ Status Bits in the IRQ PLL1 Group. Setting this bit to Logic 1 clears all IRQ status bits associated with DPLL1 and APLL1.	0	R/W	Core clock	Yes
	2	Clear all IRQ status bits in the IRQ PLL0 group		Clear All IRQ Status Bits in the IRQ PLL0 Group. Setting this bit to Logic 1 clears all IRQ status bits associated with DPLL0 and APLL0.	0	R/W	Core clock	Yes
	1	Clear all IRQ status bits in the IRQ common group		Clear All IRQ Status Bits in the IRQ Common Group. Setting this bit to Logic 1 clears all IRQ status bits in the IRQ common group, which comprises all IRQ status bits not belonging to the IRQ PLL0 group or the IRQ PLL1 group.	0	R/W	Core clock	Yes
	0	Clear all IRQ status bits		Clear All IRQ Status Bits. Setting this bit to Logic 1 clears all IRQ status bits.	0	R/W	Core clock	Yes
0x2006	7	SYSCLK unlock IRQ clear		System Clock PLL Unlocked IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of a system clock PLL has phase unlocked event.	0	R/W	Core clock	Yes
	6	SYSCLK stable IRQ clear		System Clock PLL Stable IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of a system clock PLL is phase locked and the stability period has been met event.	0	R/W	Core clock	Yes
	5	SYSCLK lock IRQ clear		System Clock PLL Locked IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of a system clock PLL has phase locked event.	0	R/W	Core clock	Yes
	4	SYSCLK calibration end IRQ clear		System Clock PLL Calibration Ended IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of a calibration of the system clock PLL has ended event.	0	R/W	Core clock	Yes

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	3	SYSCLK calibration start IRQ clear		System Clock PLL Calibration Started IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of a calibration of the system clock PLL has started event.	0	R/W	Core clock	Yes
	2	Watchdog timeout IRQ clear		Watchdog Timeout IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of a watchdog timer expired event.	0	R/W	Core clock	Yes
	1	EEPROM fault IRQ clear		EEPROM Upload Fault IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of an EEPROM upload fault event.	0	R/W	Core clock	Yes
	0	EEPROM complete IRQ clear		EEPROM Action Complete IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of the EEPROM controller completed an invoked action event (for example, an upload sequence).	0	R/W	Core clock	Yes
0x2007	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	Skew limit exceeded IRQ clear		Skew Limit Exceeded IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of the time skew measurement processor reported drift beyond its 1/16th UI drift limit event.	0	R/W	Core clock	Yes
	4	Temperature warning IRQ clear		Temperature Range Warning IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of a temperature sensor output violated the user programmed threshold limits event.	0	R/W	Core clock	Yes
	3	Auxiliary DPLL unfault IRQ clear		Auxiliary DPLL Unfaulted IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of the auxiliary DPLL reference monitor unfaulted event.	0	R/W	Core clock	Yes
	2	Auxiliary DPLL fault IRQ clear		Auxiliary DPLL Faulted IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of the auxiliary DPLL reference monitor faulted event.	0	R/W	Core clock	Yes
	1	Auxiliary DPLL unlock IRQ clear		Auxiliary DPLL Unlocked IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of the auxiliary DPLL phase unlocked event.	0	R/W	Core clock	Yes
	0	Auxiliary DPLL lock IRQ clear		Auxiliary DPLL Locked IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of the auxiliary DPLL phase locked event.	0	R/W	Core clock	Yes
0x2008	7	REFAA R divider resynchronization IRQ clear		REFAA Divider Resynchronization IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of a REFAA reference divider was resynchronized event.	0	R/W	Core clock	Yes
	6	REFAA valid IRQ clear		REFAA Validated IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of a REFAA reference monitor validated event.	0	R/W	Core clock	Yes
	5	REFAA unfault IRQ clear		REFAA Unfaulted IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of a REFAA reference monitor unfaulted event.	0	R/W	Core clock	Yes
	4	REFAA fault IRQ clear		REFAA Faulted IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of a REFAA reference monitor faulted event.	0	R/W	Core clock	Yes
	3	REFA R divider resynchronization IRQ clear		REFA Divider Resynchronization IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of a REFA reference divider was resynchronized event.	0	R/W	Core clock	Yes
	2	REFA valid IRQ clear		REFA Validated IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of a REFA reference monitor validated event.	0	R/W	Core clock	Yes

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	1	REFA unfault IRQ clear		REFA Unfaulted IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of a REFA reference monitor unfaulted event.	0	R/W	Core clock	Yes
	0	REFA fault IRQ clear		REFA Faulted IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of a REFA reference monitor faulted event.	0	R/W	Core clock	Yes
0x2009	7	REFBB R divider resynchronization IRQ clear		REFBB Divider Resynchronization IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of a REFBB reference divider was resynchronized event.	0	R/W	Core clock	Yes
	6	REFBB valid IRQ clear		REFBB Validated IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of a REFBB reference monitor validated event.	0	R/W	Core clock	Yes
	5	REFBB unfault IRQ clear		REFBB Unfaulted IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of a REFBB reference monitor unfaulted event.	0	R/W	Core clock	Yes
	4	REFBB fault IRQ clear		REFBB Faulted IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of a REFBB reference monitor faulted event.	0	R/W	Core clock	Yes
	3	REFB R divider resynchronization IRQ clear		REFB Divider Resynchronization IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of a REFB reference divider was resynchronized event.	0	R/W	Core clock	Yes
	2	REFB valid IRQ clear		REFB Validated IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of a REFB reference monitor validated event.	0	R/W	Core clock	Yes
	1	REFB unfault IRQ clear		REFB Unfaulted IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of a REFB reference monitor unfaulted event.	0	R/W	Core clock	Yes
	0	REFB fault IRQ clear		REFB Faulted IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of a REFB reference monitor faulted event.	0	R/W	Core clock	Yes
0x200A	[7:5]	Reserved		Reserved.	0x0	R/W	Core clock	Yes
	4	Skew measurement updated IRQ clear		Skew Measurement Updated IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of the time skew measurement processor completed a time skew measurement event.	0	R/W	Core clock	Yes
	3	UTSP1 update IRQ clear		UTSP1 Update IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of a User Time Stamp Processor 1 completed a time stamp conversion event.	0	R/W	Core clock	Yes
	2	UTSP0 update IRQ clear		UTSP0 Update IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of a User Time Stamp Processor 0 completed a time stamp conversion event.	0	R/W	Core clock	Yes
	1	Auxiliary NCO 1 event IRQ clear		Auxiliary NCO 1 Event IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of an Auxiliary NCO 1 accumulator rollover occurred event.	0	R/W	Core clock	Yes
	0	Auxiliary NCO 0 event IRQ clear		Auxiliary NCO 0 Event IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of an Auxiliary NCO 0 accumulator rollover occurred event.	0	R/W	Core clock	Yes

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x200B	7	DPLL0 frequency unclamped IRQ clear		DPLL0 Frequency Unclamped IRQ Clear (PLL0 Group). Program Logic 1 to clear IRQ status of a DPLL0 frequency clamp became unclamped event.	0	R/W	Core clock	Yes
	6	DPLL0 frequency clamped IRQ clear		DPLL0 Frequency Clamped IRQ Clear (PLL0 Group). Program Logic 1 to clear IRQ status of a DPLL0 frequency clamp started actively clamping event.	0	R/W	Core clock	Yes
	5	DPLL0 phase slew limiter inactive IRQ clear		DPLL0 Phase Slew Limiter Inactive IRQ Clear (PLL0 Group). Program Logic 1 to clear IRQ status of a DPLL0 phase slew limiter became inactive event.	0	R/W	Core clock	Yes
	4	DPLL0 phase slew limiter active IRQ clear		DPLL0 Phase Slew Limiter Active IRQ Clear (PLL0 Group). Program Logic 1 to clear IRQ status of a DPLL0 phase slew limiter became active event.	0	R/W	Core clock	Yes
	3	DPLL0 frequency unlocked IRQ clear		DPLL0 Frequency Unlocked IRQ Clear (PLL0 Group). Program Logic 1 to clear IRQ status of a DPLL0 frequency lock to unlock transition event.	0	R/W	Core clock	Yes
	2	DPLL0 frequency locked IRQ clear		DPLL0 Frequency Locked IRQ Clear (PLL0 Group). Program Logic 1 to clear IRQ status of a DPLL0 frequency unlock to lock transition event.	0	R/W	Core clock	Yes
	1	DPLL0 phase unlocked IRQ clear		DPLL0 Phase Unlocked IRQ Clear (PLL0 Group). Program Logic 1 to clear IRQ status of a DPLL0 phase lock to unlock transition event.	0	R/W	Core clock	Yes
	0	DPLL0 phase-locked IRQ clear		DPLL0 Phase-Locked IRQ Clear (PLL0 Group). Program Logic 1 to clear IRQ status of a DPLL0 phase unlock to lock transition event.	0	R/W	Core clock	Yes
0x200C	7	DPLL0 reference switch IRQ clear		DPLL0 Reference Switch IRQ Clear (PLL0 Group). Program Logic 1 to clear IRQ status of a DPLL0 initiated a reference switchover event.	0	R/W	Core clock	Yes
	6	DPLL0 entered freerun mode IRQ clear		DPLL0 Entered Freerun Mode IRQ Clear (PLL0 Group). Program Logic 1 to clear IRQ status of a DPLL0 entered freerun mode event.	0	R/W	Core clock	Yes
	5	DPLL0 entered holdover mode IRQ clear		DPLL0 Entered Holdover Mode IRQ Clear (PLL0 Group). Program Logic 1 to clear IRQ status of a DPLL0 entered holdover mode event.	0	R/W	Core clock	Yes
	4	DPLL0 hitless mode Entered IRQ clear		DPLL0 Hitless Mode Entered IRQ Clear (PLL0 Group). Program Logic 1 to clear IRQ status of a DPLL0 entered hitless mode event.	0	R/W	Core clock	Yes
	3	DPLL0 hitless mode exited IRQ clear		DPLL0 Hitless Mode Exited IRQ Clear (PLL0 Group). Program Logic 1 to clear IRQ status of a DPLL0 exited hitless mode event.	0	R/W	Core clock	Yes
	2	DPLL0 holdover FTW history updated IRQ clear		DPLL0 Holdover FTW History Updated IRQ Clear (PLL0 Group). Program Logic 1 to clear IRQ status of a DPLL0 holdover frequency tuning word history updated event.	0	R/W	Core clock	Yes
	1	Reserved		Reserved.	0	R/W	Core clock	Yes
	0	DPLL0 phase step detected IRQ clear		DPLL0 Phase Step Detected IRQ Clear (PLL0 Group). Program Logic 1 to clear IRQ status of a DPLL0 reference input phase step detected event.	0	R/W	Core clock	Yes

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x200D	[7:5]	Reserved		Reserved.	0x0	R/W	Core clock	Yes
	4	DPLL0 N divider resynchronized IRQ clear		DPLL0 N Divider Resynchronized IRQ Clear (PLL0 Group). Program Logic 1 to clear IRQ status of a DPLL0 feedback divider resynchronized event.	0	R/W	Core clock	Yes
	3	DPLL0 fast acquisition completed IRQ clear		DPLL0 Fast Acquisition Completed IRQ Clear (PLL0 Group). Program Logic 1 to clear IRQ status of a DPLL0 completed a fast acquisition sequence event.	0	R/W	Core clock	Yes
	2	DPLL0 fast acquisition started IRQ clear		DPLL0 Fast Acquisition Started IRQ Clear (PLL0 Group). Program Logic 1 to clear IRQ status of a DPLL0 started a fast acquisition sequence event.	0	R/W	Core clock	Yes
	[1:0]	Reserved		Reserved.	0x0	R/W	Core clock	Yes
0x200E	[7:6]	Reserved		Reserved.	0x0	R/W	Core clock	Yes
	5	DPLL0 Translation Profile 0.5 activated IRQ clear		DPLL0 Translation Profile 0.5 Activated IRQ Clear (PLL0 Group). Program Logic 1 to clear IRQ status of a DPLL0 Translation Profile 0.5 activated event.	0	R/W	Core clock	Yes
	4	DPLL0 Translation Profile 0.4 activated IRQ clear		DPLL0 Translation Profile 0.4 Activated IRQ Clear (PLL0 Group). Program Logic 1 to clear IRQ status of a DPLL0 Translation Profile 0.4 activated event.	0	R/W	Core clock	Yes
	3	DPLL0 Translation Profile 0.3 activated IRQ clear		DPLL0 Translation Profile 0.3 Activated IRQ Clear (PLL0 Group). Program Logic 1 to clear IRQ status of a DPLL0 Translation Profile 0.3 activated event.	0	R/W	Core clock	Yes
	2	DPLL0 Translation Profile 0.2 activated IRQ clear		DPLL0 Translation Profile 0.2 Activated IRQ Clear (PLL0 Group). Program Logic 1 to clear IRQ status of a DPLL0 Translation Profile 0.2 activated event.	0	R/W	Core clock	Yes
	1	DPLL0 Translation Profile 0.1 activated IRQ clear		DPLL0 Translation Profile 0.1 Activated IRQ Clear (PLL0 Group). Program Logic 1 to clear IRQ status of a DPLL0 Translation Profile 0.1 activated event.	0	R/W	Core clock	Yes
	0	DPLL0 Translation Profile 0.0 activated IRQ clear		DPLL0 Translation Profile 0.0 Activated IRQ Clear (PLL0 Group). Program Logic 1 to clear IRQ status of a DPLL0 Translation Profile 0.0 activated event.	0	R/W	Core clock	Yes
0x200F	[7:5]	Reserved		Reserved.	0x0	R/W	Core clock	Yes
	4	PLL0 clock outputs synchronized IRQ clear		PLL0 Clock Outputs Synchronized IRQ Clear (PLL0 Group). Program Logic 1 to clear IRQ status of a PLL0 clock distribution outputs synchronized event.	0	R/W	Core clock	Yes
	3	APLL0 phase unlocked IRQ clear		APLL0 Phase Unlocked IRQ Clear (PLL0 Group). Program Logic 1 to clear IRQ status of an APLL0 phase lock to unlock transition event.	0	R/W	Core clock	Yes
	2	APLL0 phase-locked IRQ clear		APLL0 Phase-Locked IRQ Clear (PLL0 Group). Program Logic 1 to clear IRQ status of an APLL0 phase unlock to lock transition event.	0	R/W	Core clock	Yes
	1	APLL0 calibration completed IRQ clear		APLL0 Calibration Completed IRQ Clear (PLL0 Group). Program Logic 1 to clear IRQ status of an APLL0 calibration completed event.	0	R/W	Core clock	Yes
	0	APLL0 calibration started IRQ clear		APLL0 Calibration Started IRQ Clear (PLL0 Group). Program Logic 1 to clear IRQ status of an APLL0 calibration started event.	0	R/W	Core clock	Yes

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x2010	7	DPLL1 frequency unclamped IRQ clear		DPLL1 Frequency Unclamped IRQ Clear (PLL1 Group). Program Logic 1 to clear IRQ status of a DPLL1 frequency clamp became unclamped event.	0	R/W	Core clock	Yes
	6	DPLL1 frequency clamped IRQ clear		DPLL1 Frequency Clamped IRQ Clear (PLL1 Group). Program Logic 1 to clear IRQ status of a DPLL1 frequency clamp started actively clamping event.	0	R/W	Core clock	Yes
	5	DPLL1 phase slew limiter inactive IRQ clear		DPLL1 Phase Slew Limiter Inactive IRQ Clear (PLL1 Group). Program Logic 1 to clear IRQ status of a DPLL1 phase slew limiter became inactive event.	0	R/W	Core clock	Yes
	4	DPLL1 phase slew limiter active IRQ clear		DPLL1 Phase Slew Limiter Active IRQ Clear (PLL1 Group). Program Logic 1 to clear IRQ status of a DPLL1 phase slew limiter became active event.	0	R/W	Core clock	Yes
	3	DPLL1 frequency unlocked IRQ clear		DPLL1 Frequency Unlocked IRQ Clear (PLL1 Group). Program Logic 1 to clear IRQ status of a DPLL1 frequency lock to unlock transition event.	0	R/W	Core clock	Yes
	2	DPLL1 frequency locked IRQ clear		DPLL1 Frequency Locked IRQ Clear (PLL1 Group). Program Logic 1 to clear IRQ status of a DPLL1 frequency unlock to lock transition event.	0	R/W	Core clock	Yes
	1	DPLL1 phase unlocked IRQ clear		DPLL1 Phase Unlocked IRQ Clear (PLL1 Group). Program Logic 1 to clear IRQ status of a DPLL1 phase lock to unlock transition event.	0	R/W	Core clock	Yes
	0	DPLL1 phase-locked IRQ clear		DPLL1 Phase-Locked IRQ Clear (PLL1 Group). Program Logic 1 to clear IRQ status of a DPLL1 phase unlock to lock transition event.	0	R/W	Core clock	Yes
0x2011	7	DPLL1 reference switch IRQ clear		DPLL1 Reference Switch IRQ Clear (PLL1 Group). Program Logic 1 to clear IRQ status of a DPLL1 initiated a reference switchover event.	0	R/W	Core clock	Yes
	6	DPLL1 entered freerun mode IRQ clear		DPLL1 Entered Freerun Mode IRQ Clear (PLL1 Group). Program Logic 1 to clear IRQ status of a DPLL1 entered freerun mode event.	0	R/W	Core clock	Yes
	5	DPLL1 entered holdover mode IRQ clear		DPLL1 Entered Holdover Mode IRQ Clear (PLL1 Group). Program Logic 1 to clear IRQ status of a DPLL1 entered holdover mode event.	0	R/W	Core clock	Yes
	4	DPLL1 hitless mode entered IRQ clear		DPLL1 Hitless Mode Entered IRQ Clear (PLL1 Group). Program Logic 1 to clear IRQ status of a DPLL1 entered hitless mode event.	0	R/W	Core clock	Yes
	3	DPLL1 hitless mode exited IRQ clear		DPLL1 Hitless Mode Exited IRQ Clear (PLL1 Group). Program Logic 1 to clear IRQ status of a DPLL1 exited hitless mode event.	0	R/W	Core clock	Yes
	2	DPLL1 holdover FTW History updated IRQ clear		DPLL1 Holdover FTW History Updated IRQ Clear (PLL1 Group). Program Logic 1 to clear IRQ status of a DPLL1 holdover frequency tuning word history updated event.	0	R/W	Core clock	Yes
	1	Reserved		Reserved.	0	R/W	Core clock	Yes
	0	DPLL1 phase step detected IRQ clear		DPLL1 Phase Step Detected IRQ Clear (PLL1 Group). Program Logic 1 to clear IRQ status of a DPLL1 reference input phase step detected event.	0	R/W	Core clock	Yes

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x2012	[7:5]	Reserved		Reserved.	0x0	R/W	Core clock	Yes
	4	DPLL1 N divider resynchronized IRQ clear		DPLL1 N Divider Resynchronized IRQ Clear (PLL1 Group). Program Logic 1 to clear IRQ status of a DPLL1 feedback divider resynchronized event.	0	R/W	Core clock	Yes
	3	DPLL1 fast acquisition completed IRQ clear		DPLL1 Fast Acquisition Completed IRQ Clear (PLL1 Group). Program Logic 1 to clear IRQ status of a DPLL1 completed a fast acquisition sequence event.	0	R/W	Core clock	Yes
	2	DPLL1 fast acquisition started IRQ clear		DPLL1 Fast Acquisition Started IRQ Clear (PLL1 Group). Program Logic 1 to clear IRQ status of a DPLL1 started a fast acquisition sequence event.	0	R/W	Core clock	Yes
	[1:0]	Reserved		Reserved.	0x0	R/W	Core clock	Yes
0x2013	[7:6]	Reserved		Reserved.	0x0	R/W	Core clock	Yes
	5	DPLL1 Translation Profile 1.5 activated IRQ clear		DPLL1 Translation Profile 1.5 Activated IRQ Clear (PLL1 Group). Program Logic 1 to clear IRQ status of a DPLL1 Translation Profile 1.5 activated event.	0	R/W	Core clock	Yes
	4	DPLL1 Translation Profile 1.4 activated IRQ clear		DPLL1 Translation Profile 1.4 Activated IRQ Clear (PLL1 Group). Program Logic 1 to clear IRQ status of a DPLL1 Translation Profile 1.4 activated event.	0	R/W	Core clock	Yes
	3	DPLL1 Translation Profile 1.3 activated IRQ clear		DPLL1 Translation Profile 1.3 Activated IRQ Clear (PLL1 Group). Program Logic 1 to clear IRQ status of a DPLL1 Translation Profile 1.3 activated event.	0	R/W	Core clock	Yes
	2	DPLL1 Translation Profile 1.2 activated IRQ clear		DPLL1 Translation Profile 1.2 Activated IRQ Clear (PLL1 Group). Program Logic 1 to clear IRQ status of a DPLL1 Translation Profile 1.2 activated event.	0	R/W	Core clock	Yes
	1	DPLL1 Translation Profile 1.1 activated IRQ clear		DPLL1 Translation Profile 1.1 Activated IRQ Clear (PLL1 Group). Program Logic 1 to clear IRQ status of a DPLL1 Translation Profile 1.1 activated event.	0	R/W	Core clock	Yes
	0	DPLL1 Translation Profile 1.0 activated IRQ clear		DPLL1 Translation Profile 1.0 Activated IRQ Clear (PLL1 Group). Program Logic 1 to clear IRQ status of a DPLL1 Translation Profile 1.0 activated event.	0	R/W	Core clock	Yes
0x2014	[7:5]	Reserved		Reserved.	0x0	R/W	Core clock	Yes
	4	PLL1 clock outputs synchronized IRQ clear		PLL1 Clock Outputs Synchronized IRQ Clear (PLL1 Group). Program Logic 1 to clear IRQ status of a PLL1 clock distribution outputs synchronized event.	0	R/W	Core clock	Yes
	3	APLL1 phase unlocked IRQ clear		APLL1 Phase Unlocked IRQ Clear (PLL1 Group). Program Logic 1 to clear IRQ status of an APLL1 phase lock to unlock transition event.	0	R/W	Core clock	Yes
	2	APLL1 phase-locked IRQ clear		APLL1 Phase-Locked IRQ Clear (PLL1 Group). Program Logic 1 to clear IRQ status of an APLL1 phase unlock to lock transition event.	0	R/W	Core clock	Yes
	1	APLL1 calibration completed IRQ clear		APLL1 Calibration Completed IRQ Clear (PLL1 Group). Program Logic 1 to clear IRQ status of an APLL1 calibration completed event.	0	R/W	Core clock	Yes
	0	APLL1 calibration started IRQ clear		APLL1 Calibration Started IRQ Clear (PLL1 Group). Program Logic 1 to clear IRQ status of an APLL1 calibration started event.	0	R/W	Core clock	Yes

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x2015	7	Auxiliary REF1 R divider resynchronization IRQ clear		Auxiliary REF1 Divider Resynchronization IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of an Auxiliary REF1 reference divider was resynchronized event.	0	R/W	Core clock	Yes
	6	Auxiliary REF1 valid IRQ clear		Auxiliary REF1 Validated IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of an Auxiliary REF1 reference monitor validated event.	0	R/W	Core clock	Yes
	5	Auxiliary REF1 unfault IRQ clear		Auxiliary REF1 Unfaulted IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of an Auxiliary REF1 reference monitor unfaulted event.	0	R/W	Core clock	Yes
	4	Auxiliary REF1 Fault IRQ Clear		Auxiliary REF1 Faulted IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of an Auxiliary REF1 reference monitor faulted event.	0	R/W	Core clock	Yes
	3	Auxiliary REF0 R divider resynchronization IRQ clear		Auxiliary REF0 Divider Resynchronization IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of an Auxiliary REF0 reference divider was resynchronized event.	0	R/W	Core clock	Yes
	2	Auxiliary REF0 valid IRQ clear		Auxiliary REF0 Validated IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of an Auxiliary REF0 reference monitor validated event.	0	R/W	Core clock	Yes
	1	Auxiliary REF0 unfault IRQ clear		Auxiliary REF0 Unfaulted IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of an Auxiliary REF0 reference monitor unfaulted event.	0	R/W	Core clock	Yes
	0	Auxiliary REF0 fault IRQ clear		Auxiliary REF0 Faulted IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of an Auxiliary REF0 reference monitor faulted event.	0	R/W	Core clock	Yes
0x2016	7	Auxiliary REF3 R divider resynchronization IRQ clear		Auxiliary REF3 Divider Resynchronization IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of an Auxiliary REF3 reference divider was resynchronized event.	0	R/W	Core clock	Yes
	6	Auxiliary REF3 valid IRQ clear		Auxiliary REF3 Validated IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of an Auxiliary REF3 reference monitor validated event.	0	R/W	Core clock	Yes
	5	Auxiliary REF3 unfault IRQ clear		Auxiliary REF3 Unfaulted IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of an Auxiliary REF3 reference monitor unfaulted event.	0	R/W	Core clock	Yes
	4	Auxiliary REF3 fault IRQ clear		Auxiliary REF3 Faulted IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of an Auxiliary REF3 reference monitor faulted event.	0	R/W	Core clock	Yes
	3	Auxiliary REF2 R divider resynchronization IRQ clear		Auxiliary REF2 Divider Resynchronization IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of an Auxiliary REF2 reference divider was resynchronized event.	0	R/W	Core clock	Yes
	2	Auxiliary REF2 valid IRQ clear		Auxiliary REF2 Validated IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of an Auxiliary REF2 reference monitor validated event.	0	R/W	Core clock	Yes
	1	Auxiliary REF2 unfault IRQ clear		Auxiliary REF2 Unfaulted IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of an Auxiliary REF2 reference monitor unfaulted event.	0	R/W	Core clock	Yes
	0	Auxiliary REF2 fault IRQ clear		Auxiliary REF2 Faulted IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of an Auxiliary REF2 reference monitor faulted event.	0	R/W	Core clock	Yes

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x2017	7	UTS FIFO overflowed IRQ clear		UTS FIFO Overflowed IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of a User Time Stamper FIFO overflowed (data lost) event.	0	R/W	Core clock	Yes
	6	UTS FIFO new sample arrived IRQ clear		UTS FIFO New Sample Arrived IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of a User Time Stamper FIFO received a sample from a UTS event.	0	R/W	Core clock	Yes
	5	UTS FIFO became not empty IRQ clear		UTS FIFO Became Not Empty IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of a User Time Stamper FIFO transitioned from empty to not empty event.	0	R/W	Core clock	Yes
	4	Common clock DPLL switched to holdover IRQ clear		Common Clock DPLL Switched to Holdover IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of the CCDPLL switched to holdover (no reference available).	0	R/W	Core clock	Yes
	3	Common clock DPLL selected secondary reference IRQ clear		Common Clock DPLL Selected Secondary Reference IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of the CCDPLL selected CCR1 event.	0	R/W	Core clock	Yes
	2	Common clock DPLL selected primary reference IRQ clear		Common Clock DPLL Selected Primary Reference IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of the CCDPLL selected CCR0 event.	0	R/W	Core clock	Yes
	1	Common clock DPLL unlock IRQ clear		Common Clock DPLL Unlocked IRQ Clear (Common Group). Program Logic 1 to clear IRQ status for of CCDPLL phase unlocked event.	0	R/W	Core clock	Yes
	0	Common clock DPLL lock IRQ clear		Common Clock DPLL Locked IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of the CCDPLL phase-locked event.	0	R/W	Core clock	Yes
0x2018	7	Common clock DPLL secondary reference invalid IRQ clear		Common Clock DPLL Secondary Reference Invalidated IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of a CCDPLL CCR1 reference monitor invalidated event.	0	R/W	Core clock	Yes
	6	Common clock DPLL secondary reference valid IRQ clear		Common Clock DPLL Secondary Reference Validated IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of a CCDPLL CCR1 reference monitor validated event.	0	R/W	Core clock	Yes
	5	Common clock DPLL primary reference invalid IRQ clear		Common Clock DPLL Primary Reference Invalidated IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of a CCDPLL CCR0 reference monitor invalidated event.	0	R/W	Core clock	Yes
	4	Common clock DPLL primary reference valid IRQ clear		Common Clock DPLL Primary Reference Validated IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of a CCDPLL CCR0 reference monitor validated event.	0	R/W	Core clock	Yes
	3	Common clock synchronizer slew limiter stopped slewing IRQ clear		Common Clock Synchronizer Slew Limiter Stopped Slewing IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of a CCS slew limiter stopped slewing event.	0	R/W	Core clock	Yes
	2	common clock synchronizer slew limiter started slewing IRQ clear		Common Clock Synchronizer Slew Limiter Started Slewing IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of a CCS slew limiter started slewing event.	0	R/W	Core clock	Yes
	1	Common clock synchronizer sync guard activated IRQ clear		Common Clock Synchronizer Synchronization Guard Activated IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of a CCS synchronization guard was activated event.	0	R/W	Core clock	Yes
	0	Common clock synchronizer ready IRQ clear		Common Clock Synchronizer Ready IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of a CCS is ready to support Digitized Clocking resources event.	0	R/W	Core clock	Yes

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x2019	[7:4]	Reserved		Reserved.	0x0	R/W	Core clock	Yes
	3	IUTS 1 invalid IRQ clear		IUTS 1 Became Invalid IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of an IUTS 1 became invalid event.	0	R/W	Core clock	Yes
	2	IUTS 1 valid IRQ clear		IUTS 1 Became Valid IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of an IUTS 1 became valid event.	0	R/W	Core clock	Yes
	1	IUTS 0 invalid IRQ clear		IUTS 0 Became Invalid IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of an IUTS 0 became invalid event.	0	R/W	Core clock	Yes
	0	IUTS 0 valid IRQ clear		IUTS 0 Became Valid IRQ Clear (Common Group). Program Logic 1 to clear IRQ status of an IUTS 0 became valid event.	0	R/W	Core clock	Yes

OPERATIONAL CONTROL: PLL CHANNEL 0—REGISTER 0x2100 TO REGISTER 0x2107

Table 86. Operational Controls: PLL Channel 0 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x2100	[7:2]	Reserved		Reserved.	0x00	R/W	Serial port clock	No
	1	APLL0 calibrate		APLL0 Calibrate. Logic 0 (default) is normal operation. Logic 1 initiates the APLL0 calibration sequence.	0	R/W	Serial port clock	No
	0	PLL0 power-down		PLL0 Power-Down. Logic 0 (default) is normal operation. Logic 1 powers down PLL0.	0	R/W	Serial port clock	No
0x2101	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	3	Channel 0 synchronize Q dividers		Channel 0 Synchronize Q dividers. Logic 0 (default) is normal operation. Logic 1 initiates a synchronization sequence for the Channel 0 Q dividers.	0	R/W	Serial port clock	No
	2	Channel 0 reset all drivers		Channel 0 Reset All Drivers. Logic 0 (default) is normal operation. Logic 1 resets all Channel 0 output drivers.	0	R/W	Serial port clock	No
	1	Channel 0 mute all drivers		Channel 0 Mute All Drivers. Logic 0 (default) is normal operation. Logic 1 mutes all Channel 0 output drivers.	0	R/W	Serial port clock	No
	0	Channel 0 N shot request		Channel 0 N shot Request. Logic 0 (default) is normal operation. Logic 1 initiates an N shot request to Channel 0.	0	R/W	Serial port clock	No
0x2102	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	OUT0AP/OUT0AN driver reset		OUT0AP/OUT0AN Driver Reset.	0	R/W	Serial port clock	No
			0	Logic 0 (default) is normal operation.				
			1	Logic 1 resets the OUT0AP/OUT0AN drivers, making the P and N outputs static Logic 0. For a differential configuration, the N output is static Logic 1.				
				The two drivers reset asynchronously (the result of runt pulse mitigation) but come out of reset synchronously.				
	4	OUT0AP/OUT0AN driver power-down		OUT0AP/OUT0AN Driver Power-Down.	0	R/W	Serial port clock	No
			0	Logic 0 (default) is normal operation.				
			1	Logic 1 powers down the OUT0AP/OUT0AN drivers (tristate outputs).				
	3	OUT0AN driver mute		OUT0AN Driver Mute. This bit is only meaningful for a single-ended output configuration.	0	R/W	Serial port clock	No
			0	Logic 0 (default) is normal operation.				
			1	Logic 1 mutes the OUT0AN driver, making the output static Logic 0.				
	2	OUT0AP driver mute		OUT0AP Driver Mute.	0	R/W	Serial port clock	No
			0	Logic 0 (default) is normal operation.				
			1	Logic 1 mutes the OUT0AP driver, making the output static Logic 0 and, for a differential output configuration, the OUT0AN driver output static Logic 1.				
	1	Q0AA reset		Q0AA Reset. Logic 0 (default) is normal operation. Logic 1 resets the Q0AA divider.	0	R/W	Serial port clock	No
	0	Q0A reset		Q0A Reset. Logic 0 (default) is normal operation. Logic 1 resets the Q0A divider.	0	R/W	Serial port clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x2103	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	OUT0BP/OUT0BN driver reset		OUT0BP/OUT0BN Driver Reset.	0	R/W	Serial port clock	No
			0	Logic 0 (default) is normal operation.				
			1	Logic 1 resets the OUT0BP/OUT0BN drivers, making the P and N outputs static Logic 0. For a differential configuration, the N output is static Logic 1.				
				The two drivers reset asynchronously (the result of runt pulse mitigation) but come out of reset synchronously.				
	4	OUT0BP/OUT0BN driver power-down		OUT0BP/OUT0BN Driver Power-Down.	0	R/W	Serial port clock	No
			0	Logic 0 (default) is normal operation.				
			1	Logic 1 powers down the OUT0BP/OUT0BN drivers (tristate outputs).				
	3	OUT0BN driver mute		OUT0BN Driver Mute. This bit is only meaningful for a single-ended output configuration.	0	R/W	Serial port clock	No
			0	Logic 0 (default) is normal operation.				
			1	Logic 1 mutes the OUT0BN driver, making the output static Logic 0.				
	2	OUT0BP driver mute		OUT0BP Driver Mute.	0	R/W	Serial port clock	No
			0	Logic 0 (default) is normal operation.				
			1	Logic 1 mutes the OUT0BP driver, making the output static Logic 0 and, for a differential output configuration, the OUT0BN driver output static Logic 1.				
	1	Q0BB Reset		Q0BB Reset. Logic 0 (default) is normal operation. Logic 1 resets the Q0BB divider.	0	R/W	Serial port clock	No
	0	Q0B Reset		Q0B Reset. Logic 0 (default) is normal operation. Logic 1 resets the Q0B divider.	0	R/W	Serial port clock	No
0x2104	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	OUT0CP/OUT0CN driver reset		OUT0CP/OUT0CN Driver Reset.	0	R/W	Serial port clock	No
			0	Logic 0 (default) is normal operation.				
			1	Logic 1 resets the OUT0CP/OUT0CN drivers making the P and N outputs static Logic 0. For a differential configuration, the N output is static Logic 1.				
				The two drivers reset asynchronously (the result of runt pulse mitigation) but come out of reset synchronously.				
	4	OUT0CP/OUT0CN driver power-down		OUT0CP/OUT0CN Driver Power-Down.	0	R/W	Serial port clock	No
			0	Logic 0 (default) is normal operation.				
			1	Logic 1 powers down the OUT0CP/OUT0CN drivers (tristate outputs).				
	3	OUT0CN driver mute		OUT0CN Driver Mute. This bit is only meaningful for a single-ended output configuration.	0	R/W	Serial port clock	No
			0	Logic 0 (default) is normal operation.				
			1	Logic 1 mutes the OUT0CN driver making the output static Logic 0.				
	2	OUT0CP driver mute		OUT0CP Driver Mute.	0	R/W	Serial port clock	No
			0	Logic 0 (default) is normal operation.				
			1	Logic 1 mutes the OUT0CP driver making the output static Logic 0 and, for a differential output configuration, the OUT0CN driver output static Logic 1.				
	1	Q0CC Reset		Q0CC Reset. Logic 0 (default) is normal operation. Logic 1 resets the Q0CC divider.	0	R/W	Serial port clock	No
	0	Q0C Reset		Q0C Reset. Logic 0 (default) is normal operation. Logic 1 resets the Q0C divider.	0	R/W	Serial port clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x2105	7	DPLL0 phase step detection resets reference monitor enable		DPLL0 Phase Step Detection Resets Reference Monitor Enable. This bit (default = 0) controls how DPLL0 responds when it detects a large (user defined) phase step.	0	R/W	Core clock	No
			0	Phase step detection initiates a new DPLL0 acquisition sequence (default).				
			1	Phase step detection resets the reference monitor and initiates a new DPLL0 acquisition sequence.				
	[6:4]	DPLL0 manual translation profile		DPLL0 Manual Translation Profile. This 3-bit unsigned value (default = 0) assigns the translation profile that is in effect when DPLL0 is in one of the manual translation profile selection modes.	0x0	R/W	Core clock	No
			0	Translation Profile 0.0 (default).				
			1	Translation Profile 0.1.				
			2	Translation Profile 0.2.				
			3	Translation Profile 0.3.				
			4	Translation Profile 0.4.				
			5	Translation Profile 0.5.				
			6	Not valid (do not use).				
			7	Not valid (do not use).				
	[3:2]	DPLL0 translation profile selection mode		DPLL0 Translation Profile Selection Mode. This 2-bit unsigned value (default = 0) determines how DPLL0 selects a translation profile (protocol for reference switching).	0x0	R/W	Core clock	No
			0	Automatic, priority-based translation profile selection (default). DPLL0 selects a translation profile automatically based on the priority of the translation profiles as programmed by the user.				
			1	Manual translation profile selection, but with fall back to automatic. DPLL0 uses the translation profile defined by Bits[6:4]. However, if the specified translation profile invalidates, the DPLL uses automatic translation profile selection (based on the priority of the translation profiles as programmed by the user).				
			2	Manual translation profile selection, but with fall back to holdover. DPLL0 uses the translation profile defined by Bits[6:4]. However, if the specified translation profile invalidates, the DPLL switches to holdover mode.				
			3	Manual translation profile selection. DPLL0 uses the translation profile defined by Bits[6:4]. The recommendation is to avoid this mode because of operational caveats. For example, if the translation profile invalidates, the DPLL remains attached to an invalid reference source, resulting in unpredictable DPLL operation.				
	1	DPLL0 force holdover mode		DPLL0 Force Holdover Mode. Logic 0 (default) is normal DPLL0 operation. Logic 1 forces the DPLL0 into holdover mode (the DPLL uses the frequency tuning word result from the tuning word history processor, if available).	0	R/W	Core clock	No
	0	DPLL0 force freerun mode		DPLL0 Force Freerun Mode. Logic 0 (default) is normal DPLL0 operation. Logic 1 forces the DPLL0 into freerun mode (the DPLL uses the freerun frequency tuning word).	0	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x2106	[7:4]	Reserved		Reserved.	0x0	R/W	Core clock	No
	3	DPLL0 restrict fast acquisition: no Channel 0 outputs toggling		DPLL0 Restrict Fast Acquisition: No Channel 0 Outputs Toggling. This bit (default = 0) places a restriction on DPLL0 initiating a fast acquisition sequence. When Register 0x2106, Bits[3:0] > 0, all enabled restrictions apply. When Register 0x2106, Bits[3:0] = 0, there are no restrictions on initiation of a fast acquisition sequence. That is, every acquisition is a fast acquisition (provided the fast acquisition excess bandwidth value, Bits[3:0] in the active Translation Profile 0.x register, is nonzero).	0	R/W	Core clock	No
			0	No fast acquisition restriction on an acquisition when no outputs are toggling (default).				
			1	fast acquisition restricted to an acquisition for which no outputs are toggling. For example, when all Channel 0 outputs are muted.				
	2	DPLL0 restrict fast acquisition: first fast acquisition		DPLL0 Restrict Fast Acquisition: First Fast Acquisition. This bit (default = 0) places a restriction on DPLL0 initiating a fast acquisition sequence. When Register 0x2106, Bits[3:0] > 0, all enabled restrictions apply. When Register 0x2106, Bits[3:0] = 0, there are no restrictions on initiation of a fast acquisition sequence. That is, every acquisition is a fast acquisition (provided the fast acquisition excess bandwidth value, Bits[3:0] in the active Translation Profile 0.x register, is nonzero).	0	R/W	Core clock	No
			0	No fast acquisition restriction to only the first fast acquisition (default).				
			1	fast acquisition restricted to first fast acquisition. That is, initiate fast acquisition only if Register 0x3102, Bit 5 = 0.				
	1	DPLL0 restrict fast acquisition: acquisition post holdover		DPLL0 Restrict Fast Acquisition: Acquisition Post Holdover. This bit (default = 0) places a restriction on DPLL0 initiating a fast acquisition sequence. When Register 0x2106, Bits[3:0] > 0, all enabled restrictions apply. When Register 0x2106, Bits[3:0] = 0, there are no restrictions on initiation of a fast acquisition sequence. That is, every acquisition is a fast acquisition (provided the fast acquisition excess bandwidth value, Bits[3:0] in the active Translation Profile 0.x register, is nonzero).	0	R/W	Core clock	No
			0	No fast acquisition restriction on an acquisition from holdover (default).				
			1	fast acquisition restricted to an acquisition from holdover.				
	0	DPLL0 restrict fast acquisition: acquisition post freerun		DPLL0 Restrict Fast Acquisition: Acquisition Post Freerun. This bit (default = 0) places a restriction on DPLL0 initiating a fast acquisition sequence. When Register 0x2106, Bits[3:0] > 0, all enabled restrictions apply. When Register 0x2106, Bits[3:0] = 0, there are no restrictions on initiation of a fast acquisition sequence. That is, every acquisition is a fast acquisition (provided the fast acquisition excess bandwidth value, Bits[3:0] in the active Translation Profile 0.x register, is nonzero).	0	R/W	Core clock	No
			0	No fast acquisition restriction on an acquisition from freerun (default).				
			1	fast acquisition restricted to an acquisition from freerun.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x2107	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	4	Channel 0 automute clear		Channel 0 Automute Clear. Program Logic 1 to clear the automute state of Channel 0.	0	R/W	Core clock	Yes
	3	DPLL0 fast acquisition state clear		DPLL0 Fast Acquisition State Clear. Program Logic 1 to clear the state of the DPLL0 fast acquisition controller. Asserting this bit allows subsequent fast acquisition sequences when Register 0x2106, Bit 2 = 1.	0	R/W	Core clock	Yes
	2	Reserved		Reserved.	0	R/W	Core clock	Yes
	1	DPLL0 tuning word history process reset		DPLL0 Tuning Word History Process Reset. Program Logic 1 to reset the tuning word history averaging process. Asserting this bit causes the tuning word processor to set Register 0x3102, Bit 0 = 0, but does not clear the previously computed tuning word history in Register 0x3108 to Register 0x3103, Bits[45:0].	0	R/W	Core clock	Yes
	0	Channel 0 autosync clear		Channel 0 Autosynchronization Clear. Program Logic 1 to clear the autosynchronization state of Channel 0. The completion of an autosynchronization sequence on Channel 0 prevents the occurrence of a subsequent autosynchronization sequence unless the user clears the autosynchronization state via this bit or updates the autosynchronization mode via Register 0x10DB, Bits[1:0].	0	R/W	Core clock	Yes

OPERATIONAL CONTROL: PLL CHANNEL 1—REGISTER 0x2200 TO REGISTER 0x2207

Table 87. Operational Controls: PLL Channel 1 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x2200	[7:2]	Reserved		Reserved.	0x00	R/W	Serial port clock	No
	1	APLL1 calibrate		APLL1 Calibrate. Logic 0 (default) is normal operation. Logic 1 initiates the APLL1 calibration sequence.	0	R/W	Serial port clock	No
	0	PLL1 power-down		PLL1 Power-Down. Logic 0 (default) is normal operation. Logic 1 powers down PLL1.	0	R/W	Serial port clock	No
0x2201	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	3	Channel 1 synchronize Q dividers		Channel 1 Synchronize Q dividers. Logic 0 (default) is normal operation. Logic 1 initiates a synchronization sequence for the Channel 1 Q dividers.	0	R/W	Serial port clock	No
	2	Channel 1 reset all drivers		Channel 1 Reset All Drivers. Logic 0 (default) is normal operation. Logic 1 resets all Channel 1 output drivers.	0	R/W	Serial port clock	No
	1	Channel 1 mute all drivers		Channel 1 Mute All Drivers. Logic 0 (default) is normal operation. Logic 1 mutes all Channel 1 output drivers.	0	R/W	Serial port clock	No
	0	Channel 1 N shot request		Channel 1 N shot Request. Logic 0 (default) is normal operation. Logic 1 initiates an N shot request to Channel 1.	0	R/W	Serial port clock	No
0x2202	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	OUT1AP/OUT1AN driver reset		OUT1AP/OUT1AN Driver Reset.	0	R/W	Serial port clock	No
			0	Logic 0 (default) is normal operation.				
			1	Logic 1 resets the OUT0AP/OUT0AN drivers, making the P and N outputs static Logic 0. For a differential configuration, the N output is static Logic 1.				
				The two drivers reset asynchronously (the result of runt pulse mitigation) but come out of reset synchronously.				
	4	OUT1AP/OUT1AN driver power-down		OUT1AP/OUT1AN Driver Power-Down.	0	R/W	Serial port clock	No
			0	Logic 0 (default) is normal operation.				
			1	Logic 1 powers down the OUT1AP/OUT1AN drivers (tristate outputs).				
	3	OUT1AN driver mute		OUT1AN Driver Mute. This bit is only meaningful for a single-ended output configuration.	0	R/W	Serial port clock	No
			0	Logic 0 (default) is normal operation.				
			1	Logic 1 mutes the OUT1AN driver, making the output static Logic 0.				
	2	OUT1AP driver mute		OUT1AP Driver Mute.	0	R/W	Serial port clock	No
			0	Logic 0 (default) is normal operation.				
			1	Logic 1 mutes the OUT1AP driver, making the output static Logic 0 and, for a differential output configuration, the OUT1AN driver output static Logic 1.				
	1	Q1AA Reset		Q1AA Reset. Logic 0 (default) is normal operation. Logic 1 resets the Q1AA divider.	0	R/W	Serial port clock	No
	0	Q1A Reset		Q1A Reset. Logic 0 (default) is normal operation. Logic 1 resets the Q1A divider.	0	R/W	Serial port clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x2203	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	OUT1BP/OUT1BN driver reset		OUT1BP/OUT1BN Driver Reset.	0	R/W	Serial port clock	No
			0	Logic 0 (default) is normal operation.				
			1	Logic 1 resets the OUT1BP/OUT1BN drivers, making the P and N outputs static Logic 0. For a differential configuration, the N output is static Logic 1.				
				The two drivers reset asynchronously (the result of runt pulse mitigation) but come out of reset synchronously.				
	4	OUT1BP/OUT1BN driver power-down		OUT1BP/OUT1BN Driver Power-Down.	0	R/W	Serial port clock	No
			0	Logic 0 (default) is normal operation.				
			1	Logic 1 powers down the OUT1BP/OUT1BN drivers (tristate outputs).				
	3	OUT1BN driver mute		OUT1BN Driver Mute. This bit is only meaningful for a single-ended output configuration.	0	R/W	Serial port clock	No
			0	Logic 0 (default) is normal operation.				
			1	Logic 1 mutes the OUT1BN driver, making the output static Logic 0.				
	2	OUT1BP driver mute		OUT1BP Driver Mute.	0	R/W	Serial port clock	No
			0	Logic 0 (default) is normal operation.				
			1	Logic 1 mutes the OUT1BP driver, making the output static Logic 0 and, for a differential output configuration, the OUT1BN driver output static Logic 1.				
	1	Q1BB Reset		Q1BB Reset. Logic 0 (default) is normal operation. Logic 1 resets the Q1BB divider.	0	R/W	Serial port clock	No
	0	Q1B Reset		Q1B Reset. Logic 0 (default) is normal operation. Logic 1 resets the Q1B divider.	0	R/W	Serial port clock	No
0x2205	7	DPLL1 phase step detection resets reference monitor enable		DPLL1 Phase Step Detection Resets Reference Monitor Enable. This bit (default = 0) controls how DPLL1 responds when it detects a large (user defined) phase step.	0	R/W	Core clock	No
			0	Phase step detection initiates a new DPLL1 acquisition sequence (default).				
			1	Phase step detection resets the reference monitor and initiates a new DPLL1 acquisition sequence.				
	[6:4]	DPLL1 manual translation profile		DPLL1 Manual Translation Profile. This 3-bit unsigned value (default = 0) assigns the translation profile that is in effect when DPLL1 is in one of the manual translation profile selection modes.	0x0	R/W	Core clock	No
			0	Translation Profile 1.0 (default).				
			1	Translation Profile 1.1.				
			2	Translation Profile 1.2.				
			3	Translation Profile 1.3.				
			4	Translation Profile 1.4.				
			5	Translation Profile 1.5.				
			6	Not valid (do not use).				
			7	Not valid (do not use).				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[3:2]	DPLL1 translation profile selection mode		DPLL1 Translation Profile Selection Mode. This 2-bit unsigned value (default = 0) determines how DPLL1 selects a translation profile (protocol for reference switching).	0x0	R/W	Core clock	No
			0	Automatic, priority-based translation profile selection (default). DPLL1 selects a translation profile automatically based on the priority of the translation profiles as programmed by the user.				
			1	Manual translation profile selection, but with fall back to automatic. DPLL1 uses the translation profile defined by Bits[6:4]. However, if the specified translation profile invalidates, the DPLL uses automatic translation profile selection (based on the priority of the translation profiles as programmed by the user).				
			2	Manual translation profile selection, but with fall back to holdover. DPLL1 uses the translation profile defined by Bits[6:4]. However, if the specified translation profile invalidates, the DPLL switches to holdover mode.				
			3	Manual translation profile selection. DPLL1 uses the translation profile defined by Bits[6:4]. The recommendation is to avoid this mode because of operational caveats. For example, should the translation profile invalidate, the DPLL remains attached to an invalid reference source, resulting in unpredictable DPLL operation.				
	1	DPLL1 force holdover mode		DPLL1 Force Holdover Mode. Logic 0 (default) is normal DPLL1 operation. Logic 1 forces the DPLL1 into holdover mode (the DPLL uses the frequency tuning word result from the tuning word history processor, if available).	0	R/W	Core clock	No
	0	DPLL1 force freerun mode		DPLL1 Force Freerun Mode. Logic 0 (default) is normal DPLL1 operation. Logic 1 forces the DPLL1 into freerun mode (the DPLL uses the freerun frequency tuning word).	0	R/W	Core clock	No
0x2206	[7:4]	Reserved		Reserved.	0x0	R/W	Core clock	No
	3	DPLL1 restrict fast acquisition: no Channel 1 outputs toggling		DPLL1 Restrict Fast Acquisition: No Channel 1 Outputs Toggling. This bit (default = 0) places a restriction on DPLL1 initiating a fast acquisition sequence. When Register 0x2206, Bits[3:0] > 0, all enabled restrictions apply. When Register 0x2206, Bits[3:0] = 0, there are no restrictions on initiation of a fast acquisition sequence. That is, every acquisition is a fast acquisition (provided the fast acquisition excess bandwidth value, Bits[3:0] in the active Translation Profile 1.x register, is nonzero).	0	R/W	Core clock	No
			0	No fast acquisition restriction on an acquisition when no outputs are toggling (default).				
			1	fast acquisition restricted to an acquisition for which no outputs are toggling. For example, when all Channel 1 outputs are muted.				
	2	DPLL1 restrict fast acquisition: first fast acquisition		DPLL1 Restrict Fast Acquisition: First Fast Acquisition. This bit (default = 0) places a restriction on DPLL1 initiating a fast acquisition sequence. When Register 0x2206, Bits[3:0] > 0, all enabled restrictions apply. When Register 0x2206, Bits[3:0] = 0, there are no restrictions on initiation of a fast acquisition sequence. That is, every acquisition is a fast acquisition (provided the fast acquisition excess bandwidth value, Bits[3:0] in the active Translation Profile 1.x register, is nonzero).	0	R/W	Core clock	No
			0	No fast acquisition restriction to only the first fast acquisition (default).				
			1	fast acquisition restricted to first fast acquisition. That is, initiate fast acquisition only if Register 0x3202, Bit 5 = 0.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	1	DPLL1 restrict fast acquisition: acquisition post holdover		DPLL1 Restrict Fast Acquisition: Acquisition Post Holdover. This bit (default = 0) places a restriction on DPLL1 initiating a fast acquisition sequence. When Register 0x2206, Bits[3:0] > 0, all enabled restrictions apply. When Register 0x2206, Bits[3:0] = 0, there are no restrictions on initiation of a fast acquisition sequence. That is, every acquisition is a fast acquisition (provided the fast acquisition excess bandwidth value, Bits[3:0] in the active Translation Profile 1.x register, is nonzero).	0	R/W	Core clock	No
			0	No fast acquisition restriction on an acquisition from holdover (default).				
			1	fast acquisition restricted to an acquisition from holdover.				
	0	DPLL1 restrict fast acquisition: acquisition post freerun		DPLL1 Restrict Fast Acquisition: Acquisition Post Freerun. This bit (default = 0) places a restriction on DPLL1 initiating a fast acquisition sequence. When Register 0x2206, Bits[3:0] > 0, all enabled restrictions apply. When Register 0x2206, Bits[3:0] = 0, there are no restrictions on initiation of a fast acquisition sequence. That is, every acquisition is a fast acquisition (provided the fast acquisition excess bandwidth value, Bits[3:0] in the active Translation Profile 1.x register, is nonzero).	0	R/W	Core clock	No
			0	No fast acquisition restriction on an acquisition from freerun (default).				
			1	fast acquisition restricted to an acquisition from freerun.				
0x2207	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	4	Channel 1 automute clear		Channel 1 Automute Clear. Program Logic 1 to clear the automute state of Channel 1.	0	R/W	Core clock	Yes
	3	DPLL1 fast acquisition state clear		DPLL1 Fast Acquisition State Clear. Program Logic 1 to clear the state of the DPLL1 fast acquisition controller. Asserting this bit allows subsequent fast acquisition sequences when Register 0x2206, Bit 2 = 1.	0	R/W	Core clock	Yes
	2	Reserved		Reserved.	0	R/W	Core clock	Yes
	1	DPLL1 tuning word history process reset		DPLL1 Tuning Word History Process Reset. Program Logic 1 to reset the tuning word history averaging process. Asserting this bit causes the tuning word processor to set Register 0x3202, Bit 0 = 0, but does not clear the previously computed tuning word history in Register 0x3208 to Register 0x3203, Bits[45:0].	0	R/W	Core clock	Yes
	0	Channel 1 autosync clear		Channel 1 Autosynchronization Clear. Program Logic 1 to clear the autosynchronization state of Channel 1. The successful completion of an autosynchronization sequence on Channel 1 prevents the occurrence of a subsequent autosynchronization sequence unless the user clears the autosynchronization state via this bit or updates the autosynchronization mode via Register 0x14DB, Bits[1:0].	0	R/W	Core clock	Yes

AUXILIARY NCO 0 PARAMETERS—REGISTER 0x2800 TO REGISTER 0x281E

Table 88. Auxiliary NCO 0 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x2800	[7:0]	Auxiliary NCO 0 Center Frequency[7:0]		Auxiliary NCO 0 Center Frequency. This 56-bit unsigned value, Center Frequency in units of 2^{-40} Hz (default = 0), establishes the center frequency (f_{CENTER}) of Auxiliary NCO 0. Center Frequency (rounded to the nearest integer) relates to f_{CENTER} as follows: *Center Frequency* = $f_{CENTER} \times 2^{40}$ Hz For example, let f_{CENTER} = 10 kHz, then Center Frequency = 10,995,116,277,760,000 (0x 27 1000 0000 0000). The maximum f_{CENTER} is ~65.5 kHz.	0x00	R/W	Core clock	No
0x2801	[7:0]	Auxiliary NCO 0 Center Frequency[15:8]		Continuation of the Auxiliary NCO 0 center frequency bit field. See the Auxiliary NCO 0 Center Frequency[7:0] description.	0x00	R/W	Core clock	No
0x2802	[7:0]	Auxiliary NCO 0 Center Frequency[23:16]		Continuation of the Auxiliary NCO 0 center frequency bit field. See the Auxiliary NCO 0 Center Frequency[7:0] description.	0x00	R/W	Core clock	No
0x2803	[7:0]	Auxiliary NCO 0 Center Frequency[31:24]		Continuation of the Auxiliary NCO 0 center frequency bit field. See the Auxiliary NCO 0 Center Frequency[7:0] description.	0x00	R/W	Core clock	No
0x2804	[7:0]	Auxiliary NCO 0 Center Frequency[39:32]		Continuation of the Auxiliary NCO 0 center frequency bit field. See the Auxiliary NCO 0 Center Frequency[7:0] description.	0x00	R/W	Core clock	No
0x2805	[7:0]	Auxiliary NCO 0 Center Frequency[47:40]		Continuation of the Auxiliary NCO 0 center frequency bit field. See the Auxiliary NCO 0 Center Frequency[7:0] description.	0x00	R/W	Core clock	No
0x2806	[7:0]	Auxiliary NCO 0 Center Frequency[55:48]		Continuation of the Auxiliary NCO 0 center frequency bit field. See the Auxiliary NCO 0 Center Frequency[7:0] description.	0x00	R/W	Core clock	No
0x2807	[7:0]	Auxiliary NCO 0 Offset Frequency[7:0]		Auxiliary NCO 0 Offset Frequency. This 32-bit unsigned value, Offset Frequency in units of 2^{-24} Hz (default = 0), sets an offset frequency (f_{OFFSET}) for Auxiliary NCO 0. Offset Frequency (rounded to the nearest integer) relates to f_{OFFSET} as follows: *Offset Frequency* = $f_{OFFSET} \times 2^{24}$ Hz For example, let f_{OFFSET} = 100 Hz, then Offset Frequency = 1,677,721,600 (0x 6400 0000). The maximum f_{OFFSET} is ~256 Hz.	0x00	R/W	Core clock	No
0x2808	[7:0]	Auxiliary NCO 0 Offset Frequency[15:8]		Continuation of the Auxiliary NCO 0 offset frequency bit field. See the Auxiliary NCO 0 Offset Frequency[7:0] description.	0x00	R/W	Core clock	No
0x2809	[7:0]	Auxiliary NCO 0 Offset Frequency[23:16]		Continuation of the Auxiliary NCO 0 offset frequency bit field. See the Auxiliary NCO 0 Offset Frequency[7:0] description.	0x00	R/W	Core clock	No
0x280A	[7:0]	Auxiliary NCO 0 Offset Frequency[31:24]		Continuation of the Auxiliary NCO 0 offset frequency bit field. See the Auxiliary NCO 0 Offset Frequency[7:0] description.	0x00	R/W	Core clock	No
0x280B	[7:0]	Auxiliary NCO 0 Tag Ratio[7:0]		Auxiliary NCO 0 Tag Ratio. This 16-bit unsigned value, N, designates every N^{th} time stamp generated by Auxiliary NCO 0 as a tagged time stamp. N = 0 (default) disables the time stamp tagging feature.	0x00	R/W	Core clock	No
0x280C	[7:0]	Auxiliary NCO 0 Tag Ratio[15:8]		Continuation of the Auxiliary NCO 0 tag ratio bit field. See the Auxiliary NCO 0 Tag Ratio[7:0] description.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x280D	[7:0]	Auxiliary NCO 0 Tag Shift[7:0]		Auxiliary NCO 0 Tag Shift. This 16-bit signed value, K, shifts the tagged time stamps (if enabled) generated by Auxiliary NCO 0 by K × $t_{AuxNCO0}$. K < N (see Register 0x280C to Register 0x280B for N). $t_{AuxNCO0} = 1/(f_{CENTER} + f_{OFFSET})$ where: f_{CENTER} is the frequency associated with the value in Register 0x2806 to Register 0x2800. f_{OFFSET} is the frequency associated with the value in Register 0x280A to Register 0x2807.	0x00	R/W	Core clock	Yes
0x280E	[7:0]	Auxiliary NCO 0 Tag Shift[15:8]		Continuation of the Auxiliary NCO 0 tag shift bit field. See the Auxiliary NCO 0 Tag Shift[7:0] description.	0x00	R/W	Core clock	Yes
0x280F	[7:2]	Reserved		Reserved.	0x00	R	Live	No
	1	Auxiliary NCO 0 elapsed UI type		Auxiliary NCO 0 Elapsed UI Type. This bit (default = 0) controls how Auxiliary NCO 0 adjusts the integer part of its time output (Register 0x3A09 to Register 0x3A05, Bits[79:40]) resulting from user updates of UI Adjust in Register 0x281D to Register 0x2819, Bits[39:0].	0	R/W	Core clock	No
			0	Absolute UI Adjust (default). Causes UI Adjust (unsigned) to apply as a direct replacement of the integer part of the time output of Auxiliary NCO 0 in Register 0x3A09 to Register 0x3A05, Bits[79:40] upon assertion of IO update.				
			1	Relative UI Adjust. Causes UI Adjust (signed) to apply as an offset to the current value of the integer part of the time output of Auxiliary NCO 0 in Register 0x3A09 to Register 0x3A05, Bits[79:40] upon assertion of IO update. For example, when UI Adjust = 100, the value of Register 0x3A09 to Register 0x3A05, Bits[79:40] increments by 100 (a negative value of UI Adjust decrements Register 0x3A09 to Register 0x3A05, Bits[79:40]).				
	0	Auxiliary NCO 0 phase offset type		Auxiliary NCO 0 Phase Offset Type. This bit (default = 0) controls how Auxiliary NCO 0 interprets the phase value, Phase Offset, in Register 0x2818 to Register 0x2814, Bits[39:0]. Applying an out of range value for Phase Offset causes an error (Register 0x3002, Bit 5 = 1).	0	R/W	Core clock	No
			0	Absolute Phase Offset (default). Causes Phase Offset to be interpreted as a time offset, Δt, in units of picoseconds, where Δt = Phase Offset × 10^{-12}. Constraint: $\|\Delta t\| < 1/(f_{CENTER} + f_{OFFSET})$ (see Register 0x2806 to Register 0x2800 for f_{CENTER} and Register 0x280A to Register 0x2807 for f_{OFFSET}). For example, to shift the phase by −4 µs, Phase Offset = -4,000,000 (0x FF FFC2 F700).				
			1	Relative Phase Offset. Causes Phase Offset to be interpreted as a fractional offset, η, relative to one period (1 UI) of Auxiliary NCO 0 covering a range of ±1/2 UI in units of 2^{-40} UI. Phase Offset relates to η as: η = (Phase Offset + 2^{39})/(2^{40} − 1) − 1/2. For example, given η = −0.04 (a phase shift of −0.04 UI or −14.4°), Phase Offset = −43,980,465,112 (0x F5 C28F 5C28) rounded to the nearest integer.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x2810	[7:0]	Auxiliary NCO 0 Phase Slew Limit[7:0]		Auxiliary NCO 0 Phase Slew Limit. This 32-bit unsigned value, Phase Slew Limit (default = 0) in units of 2^{-36}, establishes a maximum rate of change of phase by Auxiliary NCO 0 when the user calls for a phase change via Register 0x2818 to Register 0x2814, Bits[39:0]. The maximum desired phase slew rate limit ($PSRL_{MAX}$) (rounded to the nearest integer) relates to Phase Slew Limit as follows: $Phase\ Slew\ Limit = PSRL_{MAX} \times 2^{36}$ For example, given $PSRL_{MAX} = 10^{-6}$ (that is 1 µs/sec), then Phase Slew Limit = 68,719 (0x 0001 0C6F) rounded to the nearest integer. Phase Slew Limit = 0 disables the phase slew limit feature. Therefore, Auxiliary NCO 0 applies a requested phase change as a step function.	0x00	R/W	Core clock	No
0x2811	[7:0]	Auxiliary NCO 0 Phase Slew Limit[15:8]		Continuation of the Auxiliary NCO 0 phase slew limit bit field. See the Auxiliary NCO 0 Phase Slew Limit[7:0] description.	0x00	R/W	Core clock	No
0x2812	[7:0]	Auxiliary NCO 0 Phase Slew Limit[23:16]		Continuation of the Auxiliary NCO 0 phase slew limit bit field. See the Auxiliary NCO 0 Phase Slew Limit[7:0] description.	0x00	R/W	Core clock	No
0x2813	[7:0]	Auxiliary NCO 0 Phase Slew Limit[31:24]		Continuation of the Auxiliary NCO 0 phase slew limit bit field. See the Auxiliary NCO 0 Phase Slew Limit[7:0] description.	0x00	R/W	Core clock	No
0x2814	[7:0]	Auxiliary NCO 0 Phase Offset[7:0]		Auxiliary NCO 0 Phase Offset. This 40-bit signed value, Phase Offset (default = 0), assigns a phase offset to the frequency produced by Auxiliary NCO 0. The value of Phase Offset has different meaning depending on Register 0x280F, Bit 0 (see that bit for details).	0x00	R/W	Core clock	Yes
0x2815	[7:0]	Auxiliary NCO 0 Phase Offset[15:8]		Continuation of the Auxiliary NCO 0 phase offset bit field. See the Auxiliary NCO 0 Phase Offset[7:0] description.	0x00	R/W	Core clock	Yes
0x2816	[7:0]	Auxiliary NCO 0 Phase Offset[23:16]		Continuation of the Auxiliary NCO 0 phase offset bit field. See the Auxiliary NCO 0 Phase Offset[7:0] description.	0x00	R/W	Core clock	Yes
0x2817	[7:0]	Auxiliary NCO 0 Phase Offset[31:24]		Continuation of the Auxiliary NCO 0 phase offset bit field. See the Auxiliary NCO 0 Phase Offset[7:0] description.	0x00	R/W	Core clock	Yes
0x2818	[7:0]	Auxiliary NCO 0 Phase Offset[39:32]		Continuation of the Auxiliary NCO 0 phase offset bit field. See the Auxiliary NCO 0 Phase Offset[7:0] description.	0x00	R/W	Core clock	Yes
0x2819	[7:0]	Auxiliary NCO 0 UI Adjust[7:0]		Auxiliary NCO 0 UI Adjust. This 40-bit value, UI Adjust (default = 0), constitutes a whole number of Auxiliary NCO 0 periods. UI Adjust has different meaning depending on Register 0x280F, Bit 1 (see that bit for details).	0x00	R/W	Core clock	No
0x281A	[7:0]	Auxiliary NCO 0 UI Adjust[15:8]		Continuation of the Auxiliary NCO 0 UI adjust bit field. See the Auxiliary NCO 0 UI Adjust[7:0] description.	0x00	R/W	Core clock	No
0x281B	[7:0]	Auxiliary NCO 0 UI Adjust[23:16]		Continuation of the Auxiliary NCO 0 UI adjust bit field. See the Auxiliary NCO 0 UI Adjust[7:0] description.	0x00	R/W	Core clock	No
0x281C	[7:0]	Auxiliary NCO 0 UI Adjust[31:24]		Continuation of the Auxiliary NCO 0 UI adjust bit field. See the Auxiliary NCO 0 UI Adjust[7:0] description.	0x00	R/W	Core clock	No
0x281D	[7:0]	Auxiliary NCO 0 UI Adjust[39:32]		Continuation of the Auxiliary NCO 0 UI adjust bit field. See the Auxiliary NCO 0 UI Adjust[7:0] description.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x281E	[7:4]	Auxiliary NCO 0 pulse width exponent		Auxiliary NCO 0 Pulse Width Exponent. This 4-bit unsigned value, E, constitutes the exponent portion of an expression for the duration of an output pulse (t_{PULSE}) by Auxiliary NCO 0 on an appropriately configured Mx status pin. E relates to t_{PULSE} as follows: $K = (f_S \times t_{PULSE}/96 - 1)/32$ where f_S is the frequency of the system clock PLL VCO. $E = \text{ceil}(\log(K/15)/\log(2))$ where: $0 \le E \le 15$. $E = \text{ceil}(x)$ means $E = x$ if x is an integer. Otherwise, E is the nearest integer to x in the positive direction.	0x0	R/W	Core clock	No
	[3:0]	Auxiliary NCO 0 pulse width significand		Auxiliary NCO 0 Pulse Width Significand. This 4-bit unsigned value, S, constitutes the significand portion of an expression for the duration of an output pulse (t_{PULSE}) by Auxiliary NCO 0 on an appropriately configured Mx status pin. S relates to t_{PULSE} as follows: $K = (f_S \times t_{PULSE}/96 - 1)/32$ where f_S is the frequency of the system clock PLL VCO. $S = \text{round}(K/2^E)$ where: $0 \le S \le 15$. Round(x) means round x to the nearest integer. See Bits[7:4] to determine the value of E. S and E result in a quantization of t_{PULSE} as follows: $t_{PULSE} = (96/f_S) \times (1 + S \times 2^{E+5})$. where $t_{PULSE} \le 1/(f_{CENTER} + f_{OFFSET})$. See Register 0x2806 to Register 0x2800 for f_{CENTER} and Register 0x280A to Register 0x2807 for f_{OFFSET}.	0x0	R/W	Core clock	No

AUXILIARY NCO 1 PARAMETERS—REGISTER 0x2840 TO REGISTER 0x285E

Table 89. Auxiliary NCO 1 Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x2840	[7:0]	Auxiliary NCO 1 Center Frequency[7:0]		Auxiliary NCO 1 Center Frequency. This 56-bit unsigned value, Center Frequency in units of 2^{-40} Hz (default = 0), establishes the center frequency (f_{CENTER}) of Auxiliary NCO 1. Center Frequency (rounded to the nearest integer) relates to f_{CENTER} as follows: *Center Frequency* = $f_{CENTER} \times 2^{40}$ Hz For example, let f_{CENTER} = 10 kHz, then Center Frequency = 10,995,116,277,760,000 (0x 27 1000 0000 0000). The maximum f_{CENTER} is ~65.5 kHz.	0x00	R/W	Core clock	No
0x2841	[7:0]	Auxiliary NCO 1 Center Frequency[15:8]		Continuation of the Auxiliary NCO 1 center frequency bit field. See the Auxiliary NCO 1 Center Frequency[7:0] description.	0x00	R/W	Core clock	No
0x2842	[7:0]	Auxiliary NCO 1 Center Frequency[23:16]		Continuation of the Auxiliary NCO 1 center frequency bit field. See the Auxiliary NCO 1 Center Frequency[7:0] description.	0x00	R/W	Core clock	No
0x2843	[7:0]	Auxiliary NCO 1 Center Frequency[31:24]		Continuation of the Auxiliary NCO 1 center frequency bit field. See the Auxiliary NCO 1 Center Frequency[7:0] description.	0x00	R/W	Core clock	No
0x2844	[7:0]	Auxiliary NCO 1 Center Frequency[39:32]		Continuation of the Auxiliary NCO 1 center frequency bit field. See the Auxiliary NCO 1 Center Frequency[7:0] description.	0x00	R/W	Core clock	No
0x2845	[7:0]	Auxiliary NCO 1 Center Frequency[47:40]		Continuation of the Auxiliary NCO 1 center frequency bit field. See the Auxiliary NCO 1 Center Frequency[7:0] description.	0x00	R/W	Core clock	No
0x2846	[7:0]	Auxiliary NCO 1 Center Frequency[55:48]		Continuation of the Auxiliary NCO 1 center frequency bit field. See the Auxiliary NCO 1 Center Frequency[7:0] description.	0x00	R/W	Core clock	No
0x2847	[7:0]	Auxiliary NCO 1 Offset Frequency[7:0]		Auxiliary NCO 1 Offset Frequency. This 32-bit unsigned value, Offset Frequency in units of 2^{-24} Hz (default = 0), sets an offset frequency (f_{OFFSET}) for Auxiliary NCO 1. Offset Frequency (rounded to the nearest integer) relates to f_{OFFSET} as follows: *Offset Frequency* = $f_{OFFSET} \times 2^{24}$ Hz For example, let f_{OFFSET} = 100 Hz, then Offset Frequency = 1,677,721,600 (0x 6400 0000). The maximum f_{OFFSET} is ~256 Hz.	0x00	R/W	Core clock	No
0x2848	[7:0]	Auxiliary NCO 1 Offset Frequency[15:8]		Continuation of the Auxiliary NCO 1 offset frequency bit field. See the Auxiliary NCO 1 Offset Frequency[7:0] description.	0x00	R/W	Core clock	No
0x2849	[7:0]	Auxiliary NCO 1 Offset Frequency[23:16]		Continuation of the Auxiliary NCO 1 offset frequency bit field. See the Auxiliary NCO 1 Offset Frequency[7:0] description.	0x00	R/W	Core clock	No
0x284A	[7:0]	Auxiliary NCO 1 Offset Frequency[31:24]		Continuation of the Auxiliary NCO 1 offset frequency bit field. See the Auxiliary NCO 1 Offset Frequency[7:0] description.	0x00	R/W	Core clock	No
0x284B	[7:0]	Auxiliary NCO 1 Tag Ratio[7:0]		Auxiliary NCO 1 Tag Ratio. This 16-bit unsigned value, N, designates every N^{th} time stamp generated by Auxiliary NCO 1 as a tagged time stamp. N = 0 (default) disables the time stamp tagging feature.	0x00	R/W	Core clock	No
0x284C	[7:0]	Auxiliary NCO 1 Tag Ratio[15:8]		Continuation of the Auxiliary NCO 1 tag ratio bit field. See the Auxiliary NCO 1 Tag Ratio[7:0] description.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x284D	[7:0]	Auxiliary NCO 1 Tag Shift[7:0]		Auxiliary NCO 1 Tag Shift. This 16-bit signed value, K, shifts the tagged time stamps (if enabled) generated by Auxiliary NCO 1 by K × $t_{AuxNCO1}$. K < N (see Register 0x284C to Register 0x284B for N). $t_{AuxNCO1} = 1/(f_{CENTER} + f_{OFFSET})$ where: f_{CENTER} is the frequency associated with the value in Register 0x2846 to Register 0x2840. f_{OFFSET} is the frequency associated with the value in Register 0x284A to Register 0x2847.	0x00	R/W	Core clock	Yes
0x284E	[7:0]	Auxiliary NCO 1 Tag Shift[15:8]		Continuation of the Auxiliary NCO 1 tag shift bit field. See the Auxiliary NCO 1 Tag Shift[7:0] description.	0x00	R/W	Core clock	Yes
0x284F	[7:2]	Reserved		Reserved.	0x00	R	Live	No
	1	Auxiliary NCO 1 elapsed UI type		Auxiliary NCO 1 Elapsed UI Type. This bit (default = 0) controls how Auxiliary NCO 1 adjusts the integer part of its time output (Register 0x3A13 to Register 0x3A0F, Bits[79:40]) resulting from user updates of UI Adjust, in Register 0x285D to Register 0x2859, Bits[39:0].	0	R/W	Core clock	No
			0	Absolute UI Adjust (default). Causes UI Adjust (unsigned) to apply as a direct replacement of the integer part of the time output of Auxiliary NCO 1 in Register 0x3A13 to Register 0x3A0F, Bits[79:40] upon assertion of IO update.				
			1	Relative UI Adjust. Causes UI Adjust (signed) to apply as an offset to the current value of the integer part of the time output of Auxiliary NCO 1 in Register 0x3A13 to Register 0x3A0F, Bits[79:40] upon assertion of IO update. For example, when UI Adjust = 100, the value of Register 0x3A13 to Register 0x3A0F, Bits[79:40] increments by 100 (a negative value of UI Adjust decrements Register 0x3A13 to Register 0x3A0F, Bits[79:40]).				
	0	Auxiliary NCO 1 phase offset type		Auxiliary NCO 1 Phase Offset Type. This bit (default = 0) controls how Auxiliary NCO 1 interprets the phase value, Phase Offset, in Register 0x2858 to Register 0x2854, Bits[39:0]. Applying an out of range value for Phase Offset causes an error (Register 0x3002, Bit 7 = 1).	0	R/W	Core clock	No
			0	Absolute Phase Offset (default). Causes Phase Offset to be interpreted as a time offset, Δt, in units of picoseconds, where Δt = Phase Offset × 10^{-12}. Constraint: $\|\Delta t\| < 1/(f_{CENTER} + f_{OFFSET})$ (see Register 0x2846 to Register 0x2840 for f_{CENTER} and Register 0x284A to Register 0x2847 for f_{OFFSET}). For example, to shift the phase by −4 µs, Phase Offset = -4,000,000 (0x FF FFC2 F700).				
			1	Relative Phase Offset. Causes Phase Offset to be interpreted as a fractional offset, η, relative to one period (1 UI) of Auxiliary NCO 1 covering a range of ±1/2 UI in units of 2^{-40} UI. Phase Offset relates to η as: η = (Phase Offset + 2^{39})/(2^{40} − 1) − 1/2. For example, given η = −0.04 (a phase shift of −0.04 UI or −14.4°), Phase Offset = −43,980,465,112 (0x F5 C28F 5C28) rounded to the nearest integer.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x2850	[7:0]	Auxiliary NCO 1 Phase Slew Limit[7:0]		Auxiliary NCO 1 Phase Slew Limit. This 32-bit unsigned value, Phase Slew Limit (default = 0) in units of 2^{-36}, establishes a maximum rate of change of phase by Auxiliary NCO 1 when the user calls for a phase change via Register 0x2858 to Register 0x2854, Bits[39:0]. The maximum desired phase slew rate limit ($PSRL_{MAX}$) (rounded to the nearest integer) relates to Phase Slew Limit as follows: $Phase\ Slew\ Limit = PSRL_{MAX} \times 2^{36}$ For example, given $PSRL_{MAX} = 10^{-6}$ (that is 1 µs/sec), then Phase Slew Limit = 68,719 (0x 0001 0C6F) rounded to the nearest integer. Phase Slew Limit = 0 disables the phase slew limit feature. Therefore, Auxiliary NCO 0 applies a requested phase change as a step function.	0x00	R/W	Core clock	No
0x2851	[7:0]	Auxiliary NCO 1 Phase Slew Limit[15:8]		Continuation of the Auxiliary NCO 1 phase slew limit bit field. See the Auxiliary NCO 1 Phase Slew Limit[7:0] description.	0x00	R/W	Core clock	No
0x2852	[7:0]	Auxiliary NCO 1 Phase Slew Limit[23:16]		Continuation of the Auxiliary NCO 1 phase slew limit bit field. See the Auxiliary NCO 1 Phase Slew Limit[7:0] description.	0x00	R/W	Core clock	No
0x2853	[7:0]	Auxiliary NCO 1 Phase Slew Limit[31:24]		Continuation of the Auxiliary NCO 1 phase slew limit bit field. See the Auxiliary NCO 1 Phase Slew Limit[7:0] description.	0x00	R/W	Core clock	No
0x2854	[7:0]	Auxiliary NCO 1 Phase Offset[7:0]		Auxiliary NCO 1 Phase Offset. This 40-bit signed value, Phase Offset (default = 0), assigns a phase offset to the frequency produced by Auxiliary NCO 1. The value of Phase Offset has different meaning depending on Register 0x284F, Bit 0 (see that bit for details).	0x00	R/W	Core clock	Yes
0x2855	[7:0]	Auxiliary NCO 1 Phase Offset[15:8]		Continuation of the Auxiliary NCO 1 phase offset bit field. See the Auxiliary NCO 1 Phase Offset[7:0] description.	0x00	R/W	Core clock	Yes
0x2856	[7:0]	Auxiliary NCO 1 Phase Offset[23:16]		Continuation of the Auxiliary NCO 1 phase offset bit field. See the Auxiliary NCO 1 Phase Offset[7:0] description.	0x00	R/W	Core clock	Yes
0x2857	[7:0]	Auxiliary NCO 1 Phase Offset[31:24]		Continuation of the Auxiliary NCO 1 phase offset bit field. See the Auxiliary NCO 1 Phase Offset[7:0] description.	0x00	R/W	Core clock	Yes
0x2858	[7:0]	Auxiliary NCO 1 Phase Offset[39:32]		Continuation of the Auxiliary NCO 1 phase offset bit field. See the Auxiliary NCO 1 Phase Offset[7:0] description.	0x00	R/W	Core clock	Yes
0x2859	[7:0]	Auxiliary NCO 1 UI Adjust[7:0]		Auxiliary NCO 1 UI Adjust. This 40-bit value, UI Adjust (default = 0), constitutes a whole number of Auxiliary NCO 1 periods. UI Adjust has different meaning depending on Register 0x284F, Bit 1 (see that bit for details).	0x00	R/W	Core clock	No
0x285A	[7:0]	Auxiliary NCO 1 UI Adjust[15:8]		Continuation of the Auxiliary NCO 1 UI adjust bit field. See the Auxiliary NCO 1 UI Adjust[7:0] description.	0x00	R/W	Core clock	No
0x285B	[7:0]	Auxiliary NCO 1 UI Adjust[23:16]		Continuation of the Auxiliary NCO 1 UI adjust bit field. See the Auxiliary NCO 1 UI Adjust[7:0] description.	0x00	R/W	Core clock	No
0x285C	[7:0]	Auxiliary NCO 1 UI Adjust[31:24]		Continuation of the Auxiliary NCO 1 UI adjust bit field. See the Auxiliary NCO 1 UI Adjust[7:0] description.	0x00	R/W	Core clock	No
0x285D	[7:0]	Auxiliary NCO 1 UI Adjust[39:32]		Continuation of the Auxiliary NCO 1 UI adjust bit field. See the Auxiliary NCO 1 UI Adjust[7:0] description.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x285E	[7:4]	Auxiliary NCO 1 pulse width exponent		Auxiliary NCO 1 Pulse Width Exponent. This 4-bit unsigned value, E, constitutes the exponent portion of an expression for the duration of an output pulse (t_{PULSE}) by Auxiliary NCO 1 on an appropriately configured Mx status pin. E relates to t_{PULSE} as follows: $K = (f_S \times t_{PULSE}/96 - 1)/32$ where f_S is the frequency of the system clock PLL VCO. $E = \text{ceil}(\log(K/15)/\log(2))$ where: $0 \le E \le 15$. $E = \text{ceil}(x)$ means $E = x$ if x is an integer. Otherwise, E is the nearest integer to x in the positive direction.	0x0	R/W	Core clock	No
	[3:0]	Auxiliary NCO 1 pulse width significand		Auxiliary NCO 1 Pulse Width Significand. This 4-bit unsigned value, S, constitutes the significand portion of an expression for the duration of an output pulse (t_{PULSE}) by Auxiliary NCO 1 on an appropriately configured Mx status pin. S relates to t_{PULSE} as follows: $K = (f_S \times t_{PULSE}/96 - 1)/32$ where f_S is the frequency of the system clock PLL VCO. $S = \text{round}(K/2^E)$ where: $0 \le S \le 15$. Round(x) means round x to the nearest integer. See Bits[7:4] to determine the value of E. S and E result in a quantization of t_{PULSE} as follows: $t_{PULSE} = (96/f_S) \times (1 + S \times 2^{E+5})$. where $t_{PULSE} \le 1/(f_{CENTER} + f_{OFFSET})$. See Register 0x2846 to Register 0x2840 for f_{CENTER} and Register 0x284A to Register 0x2847 for f_{OFFSET}.	0x0	R/W	Core clock	No

TEMPERATURE SENSOR PARAMETERS—REGISTER 0x2900 TO REGISTER 0x2906

Table 90. Temperature Sensor Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x2900	[7:0]	External Temperature[7:0]		External Temperature. This 16-bit signed value, External Temperature (default = 0) in units of 2^{-7}°C, constitutes a user programmed temperature value (T_{EXT}) (in lieu of the internal temperature sensor). External Temperature (rounded to the nearest integer) relates to T_{EXT} as follows: *External Temperature* = $T_{EXT} \times 2^7$ For example, given T_{EXT} = 95°C, then *External Temperature* = 12,160 (0x 2F80).	0x00	R/W	Core clock	No
0x2901	[7:0]	External Temperature[15:8]		Continuation of the External Temperature bit field. See the External Temperature[7:0] description.	0x00	R/W	Core clock	No
0x2902	[7:3]	Reserved		Reserved.	0x00	R	Live	No
	2	Temperature source select for DPLL1 delay compensation		Temperature Source Select for DPLL1 Delay Compensation. This bit (default = 0) selects either the internal temperature sensor or a user programmed temperature (Register 0x2901 to Register 0x2900, Bits[15:0]) as the temperature source for temperature dependent delay compensation of DPLL1.	0	R/W	Core clock	No
			0	Internal Temperature Sensor (default).				
			1	User Programmed Temperature.				
	1	Temperature source select for DPLL0 delay compensation		Temperature Source Select for DPLL0 Delay Compensation. This bit (default = 0) selects either the internal temperature sensor or a user programmed temperature (Register 0x2901 to Register 0x2900, Bits[15:0]) as the temperature source for temperature dependent delay compensation of DPLL0.	0	R/W	Core clock	No
			0	Internal Temperature Sensor (default).				
			1	User Programmed Temperature.				
	0	Temperature source select for SYSCLK compensation Method 1		Temperature Source Select for SYSCLK Compensation Method 1. This bit (default = 0) selects either the internal temperature sensor or a user programmed temperature (Register 0x2901 to Register 0x2900, Bits[15:0]) as the temperature source for temperature dependent delay compensation of the system clock (Method 1 compensation).	0	R/W	Core clock	No
			0	Internal Temperature Sensor (default).				
			1	User Programmed Temperature.				
0x2903	[7:0]	Temperature Alarm Threshold Low[7:0]		Temperature Alarm Threshold Low. This 16-bit signed value, Low Temperature Threshold (default = 0) in units of 2^{-7}°C, constitutes a lower temperature threshold (T_{LOW}) below which triggers a temperature alarm (Register 0x3002, Bit 0 = 1). Low Temperature Threshold (rounded to the nearest integer) relates to T_{LOW} as follows: *Low Temperature Threshold* = $T_{LOW} \times 2^7$ For example, given T_{LOW} = −35°C, then Low Temperature Threshold = −4,480 (0x EE80).	0x00	R/W	Core clock	No
0x2904	[7:0]	Temperature Alarm Threshold Low[15:8]		Continuation of the temperature alarm threshold low bit field. See the Temperature Alarm Threshold Low[7:0] description.	0x00	R/W	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x2905	[7:0]	Temperature Alarm Threshold High[7:0]		Temperature Alarm Threshold High. This 16-bit signed value, High Temperature Threshold (default = 0) in units of 2^{-7}°C, constitutes an upper temperature threshold (T_{HIGH}) above which triggers a temperature alarm (Register 0x3002, Bit 0 = 1). High Temperature Threshold relates to T_{HIGH} as follows: *High Temperature Threshold* = $T_{HIGH} \times 2^7$ For example, given T_{HIGH} = 50°C, then High Temperature Threshold = 6,400 (0x 1900).	0x00	R/W	Core clock	No
0x2906	[7:0]	Temperature Alarm Threshold High[15:8]		Continuation of the temperature alarm threshold high bit field. See the Temperature Alarm Threshold High[7:0] description.	0x00	R/W	Core clock	No

USER TIME STAMP PROCESSOR (UTSP) CONTROL PARAMETERS—REGISTER 0x2A12 TO REGISTER 0x2A13

Table 91. UTSP Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x2A12	[7:6]	UTSP0 Time scale source		UTSP0 Time Scale Source. This 2-bit value (default = 0) selects the time scale UTSP0 uses for time stamp conversion.	0x0	R/W	Core clock	No
			0	Auxiliary NCO 0 time scale (default). The time scale generated by Auxiliary NCO 0.				
			1	Common time scale. The time scale generated by the CCS.				
			2	Auxiliary NCO 1 time scale. The time scale generated by Auxiliary NCO 1.				
	5	Use Tagged UTSP0 source time stamps		Use Tagged UTSP0 Source Time Stamps.	0	R/W	Core clock	No
			0	Use all time stamps from source (default).				
			1	Use only tagged time stamps from source.				
	[4:0]	UTSP0 time stamp source		User Time Stamp Processor 0 Time Stamp Source. This 5-bit value (default = 6) selects the time stamp source that UTSP0 converts to user time stamps, which appear in Register 0x3A1D to Register 0x3A14, Bits[79:0].	0x06	R/W	Core clock	No
			0	REFA TDC.				
			1	REFAA TDC.				
			2	REFB TDC.				
			3	REFBB TDC.				
			4	DPLL0 feedback TDC.				
			5	DPLL1 feedback TDC.				
			6	Auxiliary REF0 TDC (default).				
			7	Auxiliary REF1 TDC.				
			8	Auxiliary NCO 0.				
			9	Auxiliary NCO 1.				
			10	Auxiliary REF0 TDC (redundant).				
			11	Auxiliary REF2 TDC.				
			12	Auxiliary REF3 TDC.				
			13	IUTS 0.				
			14	IUTS 1.				
0x2A13	[7:6]	UTSP1 time scale source		UTSP1 Time Scale Source. This 2-bit value (default = 0) selects the time scale UTSP1 uses for time stamp conversion.	0x0	R/W	Core clock	No
			0	Auxiliary NCO 0 time scale (default). The time scale generated by Auxiliary NCO 0.				
			1	Common time scale. The time scale generated by the CCS.				
			2	Auxiliary NCO 1 time scale. The time scale generated by Auxiliary NCO 1.				
	5	Use Tagged UTSP1 source time stamps		Use Tagged UTSP1 Source Time Stamps.	0	R/W	Core clock	No
			0	Use all time stamps from source (default).				
			1	Use only tagged time stamps from source.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	[4:0]	UTSP1 time stamp source		User Time Stamp Processor 1 Time Stamp Source. This 5-bit value (default = 6) selects the time stamp source that UTSP1 converts to user time stamps, which appear in Register 0x3A29 to Register 0x3A20, Bits[79:0].	0x07	R/W	Core clock	No
			0	REFA TDC.				
			1	REFAA TDC.				
			2	REFB TDC.				
			3	REFBB TDC.				
			4	DPLL0 feedback TDC.				
			5	DPLL1 feedback TDC.				
			6	Auxiliary REF0 TDC.				
			7	Auxiliary REF1 TDC (default).				
			8	Auxiliary NCO 0.				
			9	Auxiliary NCO 1.				
			10	Auxiliary REF0 TDC (redundant).				
			11	Auxiliary REF2 TDC.				
			12	Auxiliary REF3 TDC.				
			13	IUTS 0.				
			14	IUTS 1.				

SKEW MEASUREMENT PROCESSOR CONTROL PARAMETERS—REGISTER 0x2A14 TO REGISTER 0x2A16

Table 92. Skew Measurement Processor Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x2A14	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	[3:0]	Skew sample averaging size		Skew Sample Averaging Size. This 4-bit value (default = 0) selects the number of time stamps the skew measurement processor uses for calculating a moving average. The selection determines the number, S and D, of moving average samples for skew (offset) measurements and skew drift measurements, respectively. The occurrence of the S^{th} time stamp average triggers an IRQ via Register 0x300F, Bit 4.	0x0	R/W	Core clock	No
			0	S = 2, D = 2 (default).				
			1	S = 4, D = 4.				
			2	S = 8, D = 8.				
			3	S = 16, D = 16.				
			4	S = 32, D = 16.				
			5	S = 64, D = 16.				
			6	S = 128, D = 16.				
			7	S = 256, D = 16.				
			8	S = 512, D = 16.				
			9	S = 1024, D = 16.				
			10	S = 2048, D = 16.				
			11	S = 4096, D = 16.				
			12	S = 8192, D = 16.				
			13	S = 16384, D = 16.				
			14	S = 32768, D = 16.				
0x2A15	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	Use tagged skew reference source time stamps		Use Tagged Skew Reference Source Time Stamps.	0	R/W	Core clock	No
			0	Use all time stamps from reference source (default).				
			1	Use only tagged time stamps from reference source.				
	[4:0]	Skew reference time stamp source		Skew Measurement Processor Reference Time Stamp Source. This 5-bit value (default = 0) selects the time stamp source that the skew measurement processor uses as its reference. Skew measurements comprise the difference between time stamps from the target source (see Register 0x2A16, Bits[4:0]) relative to the reference source. The skew measurement processor yields two results: skew offset and skew drift. Skew offset results appear in Register 0x3A33 to Register 0x3A2C, Bits[61:0]. Skew drift results appear in Register 0x3A3B to Register 0x3A34, Bits[61:0].	0x00	R/W	Core clock	No
			0	REFA TDC (default).				
			1	REFAA TDC.				
			2	REFB TDC.				
			3	REFBB TDC.				
			4	DPLL0 feedback TDC.				
			5	DPLL1 feedback TDC.				
			6	Auxiliary REF0 TDC.				
			7	Auxiliary REF1 TDC.				
			8	Auxiliary NCO 0.				
			9	Auxiliary NCO 1.				
			10	Auxiliary REF0 TDC.				
			11	Auxiliary REF2 TDC.				
			12	Auxiliary REF3 TDC.				
			13	IUTS 0.				
			14	IUTS 1.				

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x2A16	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	Use tagged skew target source time stamps		Use Tagged Skew Target Source Time Stamps.	0	R/W	Core clock	No
			0	Use all time stamps from target source (default).				
			1	Use only tagged time stamps from target source.				
	[4:0]	Skew target time stamp source		Skew Measurement Processor Target Time Stamp Source. This 5-bit value (default = 0) selects the time stamp source that the skew measurement processor uses as its target. Skew measurements comprise the difference between time stamps from the target source relative to the reference source (see Register 0x2A15, Bits[4:0]). The skew measurement processor yields two results: skew offset and skew drift. Skew offset results appear in Register 0x3A33 to Register 0x3A2C, Bits[61:0]. Skew drift results appear in Register 0x3A3B to Register 0x3A34, Bits[61:0].	0x00	R/W	Core clock	No
			0	REFA TDC (default).				
			1	REFAA TDC.				
			2	REFB TDC.				
			3	REFBB TDC.				
			4	DPLL0 feedback TDC.				
			5	DPLL1 feedback TDC.				
			6	Auxiliary REF0 TDC.				
			7	Auxiliary REF1 TDC.				
			8	Auxiliary NCO 0.				
			9	Auxiliary NCO 1.				
			10	Auxiliary REF0 TDC.				
			11	Auxiliary REF2 TDC.				
			12	Auxiliary REF3 TDC.				
			13	IUTS 0.				
			14	IUTS 1.				

ANALOG LOOPBACK CONTROL PARAMETERS—REGISTER 0x2D02

Table 93. Analog Loopback Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x2D02	[7:3]	Reserved		Reserved.	0x00	R/W	Core clock	No
	[2:0]	Loopback path		Select Analog Loopback Path to M4 Pin. This 3-bit unsigned value (default = 0) selects tap points within the REFB and REFBB input blocks that route to the M4 pin. The analog loopback path allows the user to route a clock signal arriving at the REFB pin or the REFBB pin and send it back out through the M4 pin, but at selectable tap locations within the REFB and REFBB blocks. The goal is to route the M4 pin signal back to its point of origin to accommodate the measurement of round trip delay. See the AD9546 data sheet for details. To complete the analog loopback path, the user must enable the M4 pin output driver by programming Register 0x0106, Bit 7 = 1.	0x0	R/W	Core clock	No
			0	Analog loopback disabled (default).				
			1	Tap the output of the REFB receiver.				
			2	Tap the output of the REFBB receiver.				
			3	Tap the output of the REFB divider.				
			4	Tap the output of the REFBB divider.				
			5	Tap the synchronization output of the REFB demodulator.				
			6	Tap the synchronization output of the REFBB demodulator.				

EEPROM CONTROL PARAMETERS—REGISTER 0x2E00 TO REGISTER 0x2E03

Table 94. EEPROM Control Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x2E00	[7:3]	Reserved		Reserved.	0x00	R	Live	No
	2	CRC verify		CRC Verify. Programming this bit to Logic 1 tells the EEPROM controller to initiate an EEPROM download sequence (but without transferring data to the AD9546 registers), calculate a checksum via a cyclic redundancy check (CRC), and compare the calculated checksum with the checksum stored in the EEPROM. See Register 0x3000, Bit 3 for the pass or fail status of the CRC verification.	0	R/W	Live	No
	1	I²C speed		I²C Speed.	0	R/W	Live	No
			0	Standard mode: 100 kHz (default).				
			1	Fast mode: 400 kHz.				
	0	EEPROM write enable		EEPROM Write Enable.	0	R/W	Live	No
			0	EEPROM write protect (default).				
			1	EEPROM write enable. Allows the EEPROM controller to write to the EEPROM during an upload sequence (see Register 0x2E02, Bit 0).				
0x2E01	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	[3:0]	EEPROM condition value		EEPROM Condition Value. This 4-bit value (default = 0) allows conditional processing of EEPROM instructions stored in Register 0x2E10 to Register 0x2E1E. Conditional processing makes it possible for the user to store specific configurations in the EEPROM and select those configurations when downloading from the EEPROM. Issuing an EEPROM upload command with a condition value of 0 (default) causes the EEPROM controller to upload unconditionally (that is, all instructions execute sequentially without conditional processing). Refer to the AD9546 data sheet for details on conditional EEPROM instructions.	0x0	R/W	Live	No
0x2E02	[7:1]	Reserved		Reserved.	0x00	R	Live	No
	0	EEPROM upload command		EEPROM Upload Command. Programming this bit to Logic 1 initiates an EEPROM upload sequence, which causes the EEPROM controller to store the AD9546 register contents (and other information) to an external EEPROM. The user must program Register 0x2E00, Bit 0 = 1 to give the EEPROM controller permission to write to the EEPROM. Initiating an EEPROM upload sequence with Register 0x2E00, Bit 0 = 0 results in a EEPROM fault (Register 0x3000, Bit 2 = 1). The EEPROM controller reads a sequence of up to 15 upload instruction bytes residing in Register 0x2E10 to Register 0x2E1E, which the user must program prior to executing the EEPROM upload command.	0	R/W	Live	Yes
0x2E03	[7:1]	Reserved		Reserved.	0x00	R	Live	No
	0	EEPROM download command		EEPROM Download Command. Programming this bit to Logic 1 initiates an EEPROM download sequence, which causes the EEPROM controller to transfer data from an external EEPROM to the AD9546 registers.	0	R/W	Live	Yes

EEPROM UPLOAD INSTRUCTION SPACE—REGISTER 0x2E10 TO REGISTER 0x2E1E

Table 95. EEPROM Upload Instruction Space Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x2E10 to 0x2E1E	[7:0]	EEPROM instruction sequence space		EEPROM Instruction Sequence Space. Register 0x2E10 to Register 0x2E1E constitute 15 consecutive address locations for storing up to 15 EEPROM instruction bytes.	0xFF	R/W	Live	No

EEPROM STATUS—REGISTER 0x3000

Table 96. EEPROM Status Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x3000	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	3	EEPROM CRC fault		EEPROM CRC Fault. The EEPROM controller sets this bit when a checksum error occurs during a download sequence.	0	R	Live	No
	2	EEPROM fault		EEPROM Fault. The EEPROM controller sets this bit when it encounters an error other than a CRC fault. Issuing an upload command (Register 0x2E02, Bit 0 = 1) while write protected (Register 0x2E00, Bit 0 = 0) results in an EEPROM fault indication.	0	R	Live	No
	1	EEPROM busy downloading		EEPROM Busy Downloading. The EEPROM controller sets this bit while it is in the process of downloading data from the external EEPROM to the AD9546.	0	R	Live	No
	0	EEPROM busy uploading		EEPROM Busy Uploading. The EEPROM controller sets this bit while it is in the process of uploading AD9546 data to the external EEPROM.	0	R	Live	No

PLL STATUS—REGISTER 0x3001

Table 97. PLL Status Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x3001	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	PLL1 locked status		PLL1 Locked Status.	0	R	Live	No
			0	DPLL1 or APLL1 unlocked.				
			1	DPLL1 and APLL1 locked.				
	4	PLL0 locked status		PLL0 Locked Status.	0	R	Live	No
			0	DPLL0 or APLL0 unlocked.				
			1	DPLL0 and APLL0 locked.				
	3	Reserved		Reserved.	0	R	Live	No
	2	System clock PLL busy calibrating		System Clock PLL Busy Calibrating. Logic 1 indicates the system clock PLL is in the process of a VCO calibration.	0	R	Live	No
	1	System clock PLL stable		System Clock PLL Stable. Logic 1 indicates the system clock PLL is locked and the stability timer has expired.	0	R	Live	No
	0	System clock PLL lock status		System Clock PLL Locked Status.	0	R	Live	No
			0	Unlocked.				
			1	Locked.				

MISCELLANEOUS STATUS—REGISTER 0x3002

Table 98. Miscellaneous Status Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x3002	7	Auxiliary NCO 1 phase offset error		Auxiliary NCO 1 Phase Offset Error. This bit indicates an attempt to invoke an out of limits phase offset (see Register 0x284F, Bit 1). Assertion of IO update populates this bit with the current status.	0	R	Core clock	No
			0	Normal operation.				
			1	Error.				
	6	Auxiliary NCO 1 phase slewing		Auxiliary NCO 1 Phase Slewing. This bit indicates the status of the Auxiliary NCO 1 phase slew rate limiter. Assertion of IO update populates this bit with the current status.	0	R	Core clock	No
			0	Normal operation.				
			1	Phase slewing.				
	5	Auxiliary NCO 0 phase offset error		Auxiliary NCO 0 Phase Offset Error. This bit indicates an attempt to invoke an out of limits phase offset (see Register 0x280F, Bit 1). Assertion of IO update populates this bit with the current status.	0	R	Core clock	No
			0	Normal operation.				
			1	Error.				
	4	Auxiliary NCO 0 phase slewing		Auxiliary NCO 0 Phase Slewing. This bit indicates the status of the Auxiliary NCO 0 phase slew rate limiter. Assertion of IO update populates this bit with the current status.	0	R	Core clock	No
			0	Normal operation.				
			1	Phase slewing.				
	3	Reserved		Reserved.	0	R	Live	No
	2	Auxiliary DPLL reference status		Auxiliary DPLL Reference Status. Reference status of the Auxiliary DPLL (or CCDPLL CCR0 (see Register 0x0D40, Bit 4)).	1	R	Core clock	No
			0	Auxiliary DPLL reference not faulted (or CCDPLL CCR0 valid).				
			1	Auxiliary DPLL reference faulted (or CCDPLL CCR0 invalid).				
	1	Auxiliary DPLL lock status		Auxiliary DPLL Lock Status. Phase lock status of the auxiliary DPLL or CCDPLL.	0	R	Core clock	No
			0	Unlocked.				
			1	Locked.				
	0	Temperature alarm		Temperature Alarm. Logic 1 indicates the temperature source (internal temperature sensor or Register 0x2901 to Register 0x2900, Bits[15:0]) exceeds the limits of the temperature threshold settings in Register 0x2904 to Register 0x2903, Bits[15:0] and Register 0x2906 to Register 0x2905, Bits[15:0].	0	R	Core clock	No

TEMPERATURE SENSOR OUTPUT—REGISTER 0x3003 TO REGISTER 0x3004

Table 99. Temperature Sensor Output Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x3003	[7:0]	Temperature Sensor Output[7:0]		Temperature Sensor Output. This 16-bit signed value, T_{SENSE} in units of 2^{-7}°C, constitutes the output of the internal temperature sensor as of the most recent assertion of an IO update. T_{SENSE} relates to the temperature of the die (T_{DIE}) as follows: $T_{DIE} = T_{SENSE} \times 2^{-7}$ For example, for T_{SENSE} = 0xF833 (−1997 decimal), T_{DIE} = −15.6015625°C.	0x00	R	Core clock	No
0x3004	[7:0]	Temperature Sensor Output[15:8]		Continuation of the temperature sensor output bit field. See the Temperature Sensor Output[7:0] description.	0x00	R	Core clock	No

REFx STATUS—REGISTER 0x3005 TO REGISTER 0x3008

Table 100. REFx Status Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x3005	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	REFA: LOS		REFA: Loss of Signal (LOS). Logic 1 indicates the REFA reference monitor detected a loss of signal or a phase discontinuity (see the AD9546 data sheet for details).	0	R	Core clock	No
	4	REFA: valid		REFA: Valid. Logic 1 indicates the REFA reference monitor declares REFA as valid. That is, REFA has been unfaulted (Bit 3 = 0) for at least as long as the user specified validation period (Register 0x0412 to Register 0x0410, Bits[19:0]). The user can force this bit to Logic 1 by programming Register 0x2004, Bit 0 = 1 and Register 0x2003, Bit 0 = 0.	0	R	Core clock	No
	3	REFA: fault		REFA: Fault. Logic 1 indicates the REFA reference monitor detected a fault (logical OR of Bit 5, and Bits[2:0]).	0	R	Core clock	No
	2	REFA: excess jitter		REFA: Excess Jitter. Logic 1 indicates the REFA reference monitor detects jitter exceeding the user specified limits (see Register 0x0414 to Register 0x0413). When Register 0x0414 to Register 0x0413, Bits[15:0] = 0, this bit is Logic 0.	0	R	Core clock	No
	1	REFA: fast		REFA: Fast. Logic 1 indicates the REFA reference monitor declares the period of the input signal as less than the user specified limits (see Register 0x0400 to Register 0x040F).	0	R	Core clock	No
	0	REFA: slow		REFA: Slow. Logic 1 indicates the REFA reference monitor declares the period of the input signal as greater than the user specified limits (see Register 0x0400 to Register 0x040F).	0	R	Core clock	No
0x3006	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	REFAA: LOS		REFAA: Loss of Signal (LOS). Logic 1 indicates the REFAA reference monitor detected a loss of signal or a phase discontinuity (see the AD9546 data sheet for details).	0	R	Core clock	No
	4	REFAA: valid		REFAA: Valid. Logic 1 indicates the REFAA reference monitor declares REFAA as valid. That is, REFAA has been unfaulted (Bit 3 = 0) for at least as long as the user specified validation period (Register 0x0432 to Register 0x0430, Bits[19:0]). The user can force this bit to Logic 1 by programming Register 0x2004, Bit 1 = 1 and Register 0x2003, Bit 1 = 0.	0	R	Core clock	No
	3	REFAA: fault		REFAA: Fault. Logic 1 indicates the REFAA reference monitor detected a fault (logical OR of Bit 5 and Bits[2:0]).	0	R	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	2	REFAA: excess jitter		REFAA: Excess Jitter. Logic 1 indicates the REFAA reference monitor detects jitter exceeding the user specified limits (see Register 0x0434 to Register 0x0433). When Register 0x0434 to Register 0x0433, Bits[15:0] = 0, this bit is Logic 0.	0	R	Core clock	No
	1	REFAA: fast		REFAA: Fast. Logic 1 indicates the REFAA reference monitor declares the period of the input signal as less than the user specified limits (see Register 0x0420 to Register 0x042F).	0	R	Core clock	No
	0	REFAA: slow		REFAA: Slow. Logic 1 indicates the REFAA reference monitor declares the period of the input signal as greater than the user specified limits (see Register 0x0420 to Register 0x042F).	0	R	Core clock	No
0x3007	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	REFB: LOS		REFB: Loss of Signal (LOS). Logic 1 indicates the REFB reference monitor detected a loss of signal or a phase discontinuity (see the AD9546 data sheet for details).	0	R	Core clock	No
	4	REFB: valid		REFB: Valid. Logic 1 indicates the REFB reference monitor declares REFB as valid. That is, REFB has been unfaulted (Bit 3 = 0) for at least as long as the user specified validation period (Register 0x0452 to Register 0x0450, Bits[19:0]). The user can force this bit to Logic 1 by programming Register 0x2004, Bit 2 = 1 and Register 0x2003, Bit 2 = 0.	0	R	Core clock	No
	3	REFB: fault		REFB: Fault. Logic 1 indicates the REFB reference monitor detected a fault (logical OR of Bit 5 and Bits[2:0]).	0	R	Core clock	No
	2	REFB: excess jitter		REFB: Excess Jitter. Logic 1 indicates the REFB reference monitor detects jitter exceeding the user specified limits (see Register 0x0454 to Register 0x0453). When Register 0x0454 to Register 0x0453, Bits[15:0] = 0, this bit is Logic 0.	0	R	Core clock	No
	1	REFB: fast		REFB: Fast. Logic 1 indicates the REFB reference monitor declares the period of the input signal as less than the user specified limits (see Register 0x0440 to Register 0x044F).	0	R	Core clock	No
	0	REFB: slow		REFB: Slow. Logic 1 indicates the REFB reference monitor declares the period of the input signal as greater than the user specified limits (see Register 0x0440 to Register 0x044F).	0	R	Core clock	No
0x3008	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	REFBB: LOS		REFBB: Loss of Signal (LOS). Logic 1 indicates the REFBB reference monitor detected a loss of signal or a phase discontinuity (see the AD9546 data sheet for details).	0	R	Core clock	No
	4	REFBB: valid		REFBB: Valid. Logic 1 indicates the REFBB reference monitor declares REFBB as valid. That is, REFBB has been unfaulted (Bit 3 = 0) for at least as long as the user specified validation period (Register 0x0472 to Register 0x0470, Bits[19:0]). The user can force this bit to Logic 1 by programming Register 0x2004, Bit 3 = 1 and Register 0x2003, Bit 3 = 0.	0	R	Core clock	No
	3	REFBB: fault		REFBB: Fault. Logic 1 indicates the REFBB reference monitor detected a fault (logical OR of Bit 5 and Bits[2:0]).	0	R	Core clock	No
	2	REFBB: excess jitter		REFBB: Excess Jitter. Logic 1 indicates the REFBB reference monitor detects jitter exceeding the user specified limits (see Register 0x0474 to Register 0x0473). When Register 0x0474 to Register 0x0473, Bits[15:0] = 0, this bit is Logic 0.	0	R	Core clock	No
	1	REFBB: fast		REFBB: Fast. Logic 1 indicates the REFBB reference monitor declares the period of the input signal as less than the user specified limits (see Register 0x0460 to Register 0x046F).	0	R	Core clock	No
	0	REFBB: slow		REFBB: Slow. Logic 1 indicates the REFBB reference monitor declares the period of the input signal as greater than the user specified limits (see Register 0x0460 to Register 0x046F).	0	R	Core clock	No

DPLL PROFILE STATUS—REGISTER 0x3009 TO REGISTER 0x300A

Table 101. DPLL Profile Status Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x3009	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	DPLL0 Active Translation Profile 0.5		DPLL0 Active Translation Profile 0.5. Logic 1 indicates DPLL0 is using Translation Profile 0.5.	0	R	Core clock	No
	4	DPLL0 Active Translation Profile 0.4		DPLL0 Active Translation Profile 0.4. Logic 1 indicates DPLL0 is using Translation Profile 0.4.	0	R	Core clock	No
	3	DPLL0 Active Translation Profile 0.3		DPLL0 Active Translation Profile 0.3. Logic 1 indicates DPLL0 is using Translation Profile 0.3.	0	R	Core clock	No
	2	DPLL0 Active Translation Profile 0.2		DPLL0 Active Translation Profile 0.2. Logic 1 indicates DPLL0 is using Translation Profile 0.2.	0	R	Core clock	No
	1	DPLL0 Active Translation Profile 0.1		DPLL0 Active Translation Profile 0.1. Logic 1 indicates DPLL0 is using Translation Profile 0.1.	0	R	Core clock	No
	0	DPLL0 Active Translation Profile 0.0		DPLL0 Active Translation Profile 0.0. Logic 1 indicates DPLL0 is using Translation Profile 0.0.	0	R	Core clock	No
0x300A	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	DPLL1 Active Translation Profile 1.5		DPLL1 Active Translation Profile 1.5. Logic 1 indicates DPLL1 is using Translation Profile 1.5.	0	R	Core clock	No
	4	DPLL1 Active Translation Profile 1.4		DPLL1 Active Translation Profile 1.4. Logic 1 indicates DPLL1 is using Translation Profile 1.4.	0	R	Core clock	No
	3	DPLL1 Active Translation Profile 1.3		DPLL1 Active Translation Profile 1.3. Logic 1 indicates DPLL1 is using Translation Profile 1.3.	0	R	Core clock	No
	2	DPLL1 Active Translation Profile 1.2		DPLL1 Active Translation Profile 1.2. Logic 1 indicates DPLL1 is using Translation Profile 1.2.	0	R	Core clock	No
	1	DPLL1 Active Translation Profile 1.1		DPLL1 Active Translation Profile 1.1. Logic 1 indicates DPLL1 is using Translation Profile 1.1.	0	R	Core clock	No
	0	DPLL1 Active Translation Profile 1.0		DPLL1 Active Translation Profile 1.0. Logic 1 indicates DPLL1 is using Translation Profile 1.0.	0	R	Core clock	No

IRQ STATUS—REGISTER 0x300B TO REGISTER 0x301E

Table 102. IRQ Status Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x300B	7	SYSCLK unlock IRQ status		System Clock PLL Unlocked IRQ Status (Common Group). The system clock PLL has phase unlocked.	0	R	Live	No
	6	SYSCLK stable IRQ status		System Clock PLL Stable IRQ Status (Common Group). The system clock PLL is phase-locked and the stability period has been met.	0	R	Live	No
	5	SYSCLK lock IRQ status		System Clock PLL Locked IRQ Status (Common Group). The system clock PLL has phase-locked.	0	R	Live	No
	4	SYSCLK calibration end IRQ status		System Clock PLL Calibration Ended IRQ Status (Common Group). Calibration of the system clock PLL has ended.	0	R	Live	No
	3	SYSCLK calibration start IRQ status		System Clock PLL Calibration Started IRQ Status (Common Group). Calibration of the system clock PLL has started.	0	R	Live	No
	2	Watchdog timeout IRQ status		Watchdog Timeout IRQ Status (Common Group). The watchdog timer expired.	0	R	Live	No
	1	EEPROM fault IRQ status		EEPROM Upload Fault IRQ Status (Common Group). EEPROM upload fault.	0	R	Live	No
	0	EEPROM complete IRQ status		EEPROM Action Complete IRQ Status (Common Group). The EEPROM controller completed an invoked action (for example, an upload sequence).	0	R	Live	No
0x300C	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	Skew limit exceeded IRQ status		Skew Limit Exceeded IRQ Status (Common Group). The time skew measurement processor reported drift beyond its 1/16th UI drift limit.	0	R	Live	No
	4	Temperature warning IRQ status		Temperature Range Warning IRQ Status (Common Group). The temperature sensor output violated the user programmed threshold limits.	0	R	Live	No
	3	Auxiliary DPLL unfault IRQ status		Auxiliary DPLL Unfaulted IRQ Status (Common Group). The auxiliary DPLL reference monitor unfaulted.	0	R	Live	No
	2	Auxiliary DPLL fault IRQ status		Auxiliary DPLL Faulted IRQ Status (Common Group). The auxiliary DPLL reference monitor faulted.	0	R	Live	No
	1	Auxiliary DPLL unlock IRQ status		Auxiliary DPLL Unlocked IRQ Status (Common Group). The auxiliary DPLL phase unlocked.	0	R	Live	No
	0	Auxiliary DPLL lock IRQ status		Auxiliary DPLL Locked IRQ Status (Common Group). The auxiliary DPLL phase-locked.	0	R	Live	No
0x300D	7	REFAA R divider resynchronization IRQ status		REFAA R Divider Resynchronization IRQ Status (Common Group). The REFAA reference divider was resynchronized.	0	R	Live	No
	6	REFAA valid IRQ status		REFAA Validated IRQ Status (Common Group). The REFAA reference monitor validated.	0	R	Live	No
	5	REFAA unfault IRQ status		REFAA Unfaulted IRQ Status (Common Group). The REFAA reference monitor unfaulted.	0	R	Live	No
	4	REFAA fault IRQ status		REFAA Faulted IRQ Status (Common Group). The REFAA reference monitor faulted.	0	R	Live	No
	3	REFA R divider resynchronization IRQ status		REFA R Divider Resynchronization IRQ Status (Common Group). The REFA reference divider was resynchronized.	0	R	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	2	REFA valid IRQ status		REFA Validated IRQ Status (Common Group). The REFA reference monitor validated.	0	R	Live	No
	1	REFA unfault IRQ status		REFA Unfaulted IRQ Status (Common Group). The REFA reference monitor unfaulted.	0	R	Live	No
	0	REFA fault IRQ status		REFA Faulted IRQ Status (Common Group). The REFA reference monitor faulted.	0	R	Live	No
0x300E	7	REFBB R divider resynchronization IRQ status		REFBB R Divider Resynchronization IRQ Status (Common Group). The REFBB reference divider was resynchronized.	0	R	Live	No
	6	REFBB valid IRQ status		REFBB Validated IRQ Status (Common Group). The REFBB reference monitor validated.	0	R	Live	No
	5	REFBB unfault IRQ status		REFBB Unfaulted IRQ Status (Common Group). The REFBB reference monitor unfaulted.	0	R	Live	No
	4	REFBB fault IRQ status		REFBB Faulted IRQ Status (Common Group). The REFBB reference monitor faulted.	0	R	Live	No
	3	REFB R divider resynchronization IRQ status		REFB R Divider Resynchronization IRQ Status (Common Group). The REFB reference divider was resynchronized.	0	R	Live	No
	2	REFB valid IRQ status		REFB Validated IRQ Status (Common Group). The REFB reference monitor validated.	0	R	Live	No
	1	REFB unfault IRQ status		REFB Unfaulted IRQ Status (Common Group). The REFB reference monitor unfaulted.	0	R	Live	No
	0	REFB fault IRQ status		REFB Faulted IRQ Status (Common Group). The REFB reference monitor faulted.	0	R	Live	No
0x300F	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	4	Skew measurement updated IRQ status		Skew Measurement Updated IRQ Status (Common Group). The time skew measurement processor completed a time skew measurement.	0	R	Live	No
	3	UTSP1 update IRQ status		UTSP1 Update IRQ Status (Common Group). User Time Stamp Processor 1 completed a time stamp conversion.	0	R	Live	No
	2	UTSP0 update IRQ status		UTSP0 Update IRQ Status (Common Group). User Time Stamp Processor 0 completed a time stamp conversion.	0	R	Live	No
	1	Auxiliary NCO 1 event IRQ status		Auxiliary NCO 1 Event IRQ Status (Common Group). An Auxiliary NCO 1 accumulator rollover event occurred.	0	R	Live	No
	0	Auxiliary NCO 0 event IRQ status		Auxiliary NCO 0 Event IRQ Status (Common Group). An Auxiliary NCO 0 accumulator rollover event occurred.	0	R	Live	No
0x3010	7	DPLL0 frequency unclamped IRQ status		DPLL0 Frequency Unclamped IRQ Status (PLL0 Group). DPLL0 frequency clamp became unclamped.	0	R	Live	No
	6	DPLL0 frequency clamped IRQ status		DPLL0 Frequency Clamped IRQ Status (PLL0 Group). DPLL0 frequency clamp started actively clamping.	0	R	Live	No
	5	DPLL0 phase slew limiter inactive IRQ status		DPLL0 Phase Slew Limiter Inactive IRQ Status (PLL0 Group). DPLL0 phase slew limiter became inactive.	0	R	Live	No
	4	DPLL0 phase slew limiter active IRQ status		DPLL0 Phase Slew Limiter Active IRQ Status (PLL0 Group). DPLL0 phase slew limiter became active.	0	R	Live	No
	3	DPLL0 frequency unlocked IRQ status		DPLL0 Frequency Unlocked IRQ Status (PLL0 Group). DPLL0 frequency lock to unlock transition.	0	R	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	2	DPLL0 frequency locked IRQ status		DPLL0 Frequency Locked IRQ Status (PLL0 Group). DPLL0 frequency unlock to lock transition.	0	R	Live	No
	1	DPLL0 phase unlocked IRQ status		DPLL0 Phase Unlocked IRQ Status (PLL0 Group). DPLL0 phase lock to unlock transition.	0	R	Live	No
	0	DPLL0 phase-locked IRQ status		DPLL0 Phase-Locked IRQ Status (PLL0 Group). DPLL0 phase unlock to lock transition.	0	R	Live	No
0x3011	7	DPLL0 reference switch IRQ status		DPLL0 Reference Switch IRQ Status (PLL0 Group). DPLL0 initiated a reference switchover.	0	R	Live	No
	6	DPLL0 entered freerun mode IRQ status		DPLL0 Entered Freerun Mode IRQ Status (PLL0 Group). DPLL0 entered freerun mode.	0	R	Live	No
	5	DPLL0 entered holdover mode IRQ status		DPLL0 Entered Holdover Mode IRQ Status (PLL0 Group). DPLL0 entered holdover mode.	0	R	Live	No
	4	DPLL0 hitless mode entered IRQ status		DPLL0 Hitless Mode Entered IRQ Status (PLL0 Group). DPLL0 entered hitless mode.	0	R	Live	No
	3	DPLL0 hitless mode exited IRQ status		DPLL0 Hitless Mode Exited IRQ Status (PLL0 Group). DPLL0 exited hitless mode.	0	R	Live	No
	2	DPLL0 holdover FTW history updated IRQ status		DPLL0 Holdover FTW History Updated IRQ Status (PLL0 Group). DPLL0 holdover frequency tuning word history updated.	0	R	Live	No
	1	Reserved		Reserved.	0	R	Live	No
	0	DPLL0 phase step detected IRQ status		DPLL0 Phase Step Detected IRQ Status (PLL0 Group). DPLL0 reference input phase step detected.	0	R	Live	No
0x3012	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	4	DPLL0 N divider resynchronized IRQ status		DPLL0 N Divider Resynchronized IRQ Status (PLL0 Group). DPLL0 feedback divider resynchronized.	0	R	Live	No
	3	DPLL0 fast acquisition completed IRQ status		DPLL0 Fast Acquisition Completed IRQ Status (PLL0 Group). DPLL0 completed a fast acquisition sequence.	0	R	Live	No
	2	DPLL0 fast acquisition started IRQ status		DPLL0 Fast Acquisition Started IRQ Status (PLL0 Group). DPLL0 started a fast acquisition sequence.	0	R	Live	No
	[1:0]	Reserved		Reserved.	0x0	R	Live	No
0x3013	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	DPLL0 Translation Profile 0.5 activated IRQ status		DPLL0 Translation Profile 0.5 Activated IRQ Status (PLL0 Group). DPLL0 Translation Profile 0.5 activated.	0	R	Live	No
	4	DPLL0 Translation Profile 0.4 activated IRQ status		DPLL0 Translation Profile 0.4 Activated IRQ Status (PLL0 Group). DPLL0 activated Translation Profile 0.4 activated.	0	R	Live	No
	3	DPLL0 Translation Profile 0.3 activated IRQ status		DPLL0 Translation Profile 0.3 Activated IRQ Status (PLL0 Group). DPLL0 Translation Profile 0.3 activated.	0	R	Live	No
	2	DPLL0 Translation Profile 0.2 activated IRQ status		DPLL0 Translation Profile 0.2 Activated IRQ Status (PLL0 Group). DPLL0 Translation Profile 0.2 activated.	0	R	Live	No
	1	DPLL0 Translation Profile 0.1 activated IRQ status		DPLL0 Translation Profile 0.1 Activated IRQ Status (PLL0 Group). DPLL0 Translation Profile 0.1 activated.	0	R	Live	No
	0	DPLL0 Translation Profile 0.0 activated IRQ status		DPLL0 Translation Profile 0.0 Activated IRQ Status (PLL0 Group). DPLL0 Translation Profile 0.0 activated.	0	R	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x3014	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	4	PLL0 clock outputs synchronized IRQ status		PLL0 Clock Outputs Synchronized IRQ Status (PLL0 Group). PLL0 clock distribution outputs synchronized.	0	R	Live	No
	3	APLL0 phase unlocked IRQ status		APLL0 Phase Unlocked IRQ Status (PLL0 Group). APLL0 phase lock to unlock transition.	0	R	Live	No
	2	APLL0 phase-locked IRQ status		APLL0 Phase-Locked IRQ Status (PLL0 Group). APLL0 phase unlock to lock transition.	0	R	Live	No
	1	APLL0 calibration completed IRQ status		APLL0 Calibration Completed IRQ Status (PLL0 Group). APLL0 calibration completed.	0	R	Live	No
	0	APLL0 calibration started IRQ status		APLL0 Calibration Started IRQ Status (PLL0 Group). APLL0 calibration started.	0	R	Live	No
0x3015	7	DPLL1 frequency unclamped IRQ status		DPLL1 Frequency Unclamped IRQ Status (PLL1 Group). DPLL1 frequency clamp became unclamped.	0	R	Live	No
	6	DPLL1 frequency clamped IRQ status		DPLL1 Frequency Clamped IRQ Status (PLL1 Group). DPLL1 frequency clamp started actively clamping.	0	R	Live	No
	5	DPLL1 phase slew limiter inactive IRQ status		DPLL1 Phase Slew Limiter Inactive IRQ Status (PLL1 Group). DPLL1 phase slew limiter became inactive.	0	R	Live	No
	4	DPLL1 phase slew limiter active IRQ status		DPLL1 Phase Slew Limiter Active IRQ Status (PLL1 Group). DPLL1 phase slew limiter became active.	0	R	Live	No
	3	DPLL1 frequency unlocked IRQ status		DPLL1 Frequency Unlocked IRQ Status (PLL1 Group). DPLL1 frequency lock to unlock transition.	0	R	Live	No
	2	DPLL1 Frequency Locked IRQ status		DPLL1 Frequency Locked IRQ Status (PLL1 Group). DPLL1 frequency unlock to lock transition.	0	R	Live	No
	1	DPLL1 phase unlocked IRQ status		DPLL1 Phase Unlocked IRQ Status (PLL1 Group). DPLL1 phase lock to unlock transition.	0	R	Live	No
	0	DPLL1 phase-locked IRQ status		DPLL1 Phase-Locked IRQ Status (PLL1 Group). DPLL1 phase unlock to lock transition.	0	R	Live	No
0x3016	7	DPLL1 reference switch IRQ status		DPLL1 Reference Switch IRQ Status (PLL1 Group). DPLL1 initiated a reference switchover.	0	R	Live	No
	6	DPLL1 entered freerun mode IRQ status		DPLL1 Entered Freerun Mode IRQ Status (PLL1 Group). DPLL1 entered freerun mode.	0	R	Live	No
	5	DPLL1 entered holdover mode IRQ status		DPLL1 Entered Holdover Mode IRQ Status (PLL1 Group). DPLL1 entered holdover mode.	0	R	Live	No
	4	DPLL1 hitless mode entered IRQ status		DPLL1 Hitless Mode Entered IRQ Status (PLL1 Group). DPLL1 entered hitless mode.	0	R	Live	No
	3	DPLL1 hitless mode exited IRQ status		DPLL1 Hitless Mode Exited IRQ Status (PLL1 Group). DPLL1 exited hitless mode.	0	R	Live	No
	2	DPLL1 holdover FTW history updated IRQ status		DPLL1 Holdover FTW History Updated IRQ Status (PLL1 Group). DPLL1 holdover frequency tuning word history updated.	0	R	Live	No
	1	Reserved		Reserved.	0	R	Live	No
	0	DPLL1 phase step detected IRQ status		DPLL1 Phase Step Detected IRQ Status (PLL1 Group). DPLL1 reference input phase step detected.	0	R	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x3017	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	4	DPLL1 N divider resynchronized IRQ status		DPLL1 N Divider Resynchronized IRQ Status (PLL1 Group). DPLL1 feedback divider resynchronized.	0	R	Live	No
	3	DPLL1 fast acquisition completed IRQ status		DPLL1 Fast Acquisition Completed IRQ Status (PLL1 Group). DPLL1 completed a fast acquisition sequence.	0	R	Live	No
	2	DPLL1 fast acquisition started IRQ status		DPLL1 Fast Acquisition Started IRQ Status (PLL1 Group). DPLL1 started a fast acquisition sequence.	0	R	Live	No
	[1:0]	Reserved		Reserved.	0x0	R	Live	No
0x3018	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	DPLL1 Translation Profile 1.5 activated IRQ status		DPLL1 Translation Profile 1.5 Activated IRQ Status (PLL1 Group). DPLL1 translation profile 1.5 activated.	0	R	Live	No
	4	DPLL1 Translation Profile 1.4 activated IRQ status		DPLL1 Translation Profile 1.4 Activated IRQ Status (PLL1 Group). DPLL1 Translation Profile 1.4 activated.	0	R	Live	No
	3	DPLL1 Translation Profile 1.3 activated IRQ status		DPLL1 Translation Profile 1.3 Activated IRQ Status (PLL1 Group). DPLL1 Translation Profile 1.3 activated.	0	R	Live	No
	2	DPLL1 Translation Profile 1.2 activated IRQ status		DPLL1 Translation Profile 1.2 Activated IRQ Status (PLL1 Group). DPLL1 Translation Profile 1.2 activated.	0	R	Live	No
	1	DPLL1 Translation Profile 1.1 activated IRQ status		DPLL1 Translation Profile 1.1 Activated IRQ Status (PLL1 Group). DPLL1 Translation Profile 1.1 activated.	0	R	Live	No
	0	DPLL1 Translation Profile 1.0 activated IRQ status		DPLL1 Translation Profile 1.0 Activated IRQ Status (PLL1 Group). DPLL1 Translation Profile 1.0 activated.	0	R	Live	No
0x3019	[7:5]	Reserved		Reserved.	0x0	R	Live	No
	4	PLL1 clock outputs synchronized IRQ status		PLL1 Clock Outputs Synchronized IRQ Status (PLL1 Group). PLL1 clock distribution outputs synchronized.	0	R	Live	No
	3	APLL1 phase unlocked IRQ status		APLL1 Phase Unlocked IRQ Status (PLL1 Group). APLL1 phase lock to unlock transition.	0	R	Live	No
	2	APLL1 phase-locked IRQ status		APLL1 Phase-Locked IRQ Status (PLL1 Group). APLL1 phase unlock to lock transition.	0	R	Live	No
	1	APLL1 calibration completed IRQ status		APLL1 Calibration Completed IRQ Status (PLL1 Group). APLL1 calibration completed.	0	R	Live	No
	0	APLL1 calibration started IRQ status		APLL1 Calibration Started IRQ Status (PLL1 Group). APLL1 calibration started.	0	R	Live	No
0x301A	7	Auxiliary REF1 R divider resynchronization IRQ status		Auxiliary REF1 R Divider Resynchronization IRQ Status (Common Group). The Auxiliary REF1 reference divider was resynchronized.	0	R	Live	No
	6	Auxiliary REF1 valid IRQ status		Auxiliary REF1 Validated IRQ Status (Common Group). The Auxiliary REF1 reference monitor validated.	0	R	Live	No
	5	Auxiliary REF1 unfault IRQ status		Auxiliary REF1 Unfaulted IRQ Status (Common Group). The Auxiliary REF1 reference monitor unfaulted.	0	R	Live	No
	4	Auxiliary REF1 fault IRQ status		Auxiliary REF1 Faulted IRQ Status (Common Group). The Auxiliary REF1 reference monitor faulted.	0	R	Live	No
	3	Auxiliary REF0 R divider resynchronization IRQ status		Auxiliary REF0 R Divider Resynchronization IRQ Status (Common Group). The Auxiliary REF0 reference divider was resynchronized.	0	R	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	2	Auxiliary REF0 valid IRQ status		Auxiliary REF0 Validated IRQ Status (Common Group). The Auxiliary REF0 reference monitor validated.	0	R	Live	No
	1	Auxiliary REF0 unfault IRQ status		Auxiliary REF0 Unfaulted IRQ Status (Common Group). The Auxiliary REF0 reference monitor unfaulted.	0	R	Live	No
	0	Auxiliary REF0 fault IRQ status		Auxiliary REF0 Faulted IRQ Status (Common Group). The Auxiliary REF0 reference monitor faulted.	0	R	Live	No
0x301B	7	Auxiliary REF3 R divider resynchronization IRQ status		Auxiliary REF3 R Divider Resynchronization IRQ Status (Common Group). The Auxiliary REF3 reference divider was resynchronized.	0	R	Live	No
	6	Auxiliary REF3 valid IRQ status		Auxiliary REF3 Validated IRQ Status (Common Group). The Auxiliary REF3 reference monitor validated.	0	R	Live	No
	5	Auxiliary REF3 unfault IRQ status		Auxiliary REF3 Unfaulted IRQ Status (Common Group). The Auxiliary REF3 reference monitor unfaulted.	0	R	Live	No
	4	Auxiliary REF3 fault IRQ status		Auxiliary REF3 Faulted IRQ Status (Common Group). The Auxiliary REF3 reference monitor faulted.	0	R	Live	No
	3	Auxiliary REF2 R divider resynchronization IRQ status		Auxiliary REF2 R Divider Resynchronization IRQ Status (Common Group). The Auxiliary REF2 reference divider was resynchronized.	0	R	Live	No
	2	Auxiliary REF2 valid IRQ status		Auxiliary REF2 Validated IRQ Status (Common Group). The Auxiliary REF2 reference monitor validated.	0	R	Live	No
	1	Auxiliary REF2 unfault IRQ status		Auxiliary REF2 Unfaulted IRQ Status (Common Group). The Auxiliary REF2 reference monitor unfaulted.	0	R	Live	No
	0	Auxiliary REF2 fault IRQ status		Auxiliary REF2 Faulted IRQ Status (Common Group). The Auxiliary REF2 reference monitor faulted.	0	R	Live	No
0x301C	7	UTS FIFO overflowed IRQ status		UTS FIFO Overflowed IRQ Status (Common Group). The UTS FIFO overflowed (data lost).	0	R	Live	No
	6	UTS FIFO new sample arrived IRQ status		UTS FIFO New Sample Arrived IRQ Status (Common Group). The UTS FIFO received a sample from a UTS.	0	R	Live	No
	5	UTS FIFO became not empty IRQ status		UTS FIFO Became Not Empty IRQ Status (Common Group). The UTS FIFO transitioned from empty to not empty.	0	R	Live	No
	4	Common clock DPLL switched to holdover IRQ status		Common Clock DPLL Switched to Holdover IRQ Status (Common Group). The CCDPLL switched to holdover (no reference available).	0	R	Live	No
	3	Common clock DPLL selected secondary reference IRQ status		Common Clock DPLL Selected Secondary Reference IRQ Status (Common Group). The CCDPLL selected CCR1.	0	R	Live	No
	2	Common clock DPLL selected primary reference IRQ status		Common Clock DPLL Selected Primary Reference IRQ Status (Common Group). The CCDPLL selected CCR0.	0	R	Live	No
	1	Common clock DPLL unlock IRQ status		Common Clock DPLL Unlocked IRQ Status (Common Group). The CCDPLL phase unlocked.	0	R	Live	No
	0	Common clock DPLL lock IRQ status		Common Clock DPLL Locked IRQ Status (Common Group). The CCDPLL phase-locked.	0	R	Live	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x301D	7	CCDPLL secondary reference invalid IRQ status		Common Clock DPLL Secondary Reference Invalidated IRQ Status (Common Group). The CCDPLL CCR1 reference monitor invalidated.	0	R	Live	No
	6	CCDPLL secondary reference valid IRQ status		Common Clock DPLL Secondary Reference Validated IRQ Status (Common Group). The CCDPLL CCR1 reference monitor validated.	0	R	Live	No
	5	CCDPLL Primary Reference Invalid IRQ Status		Common Clock DPLL Primary Reference Invalidated IRQ Status (Common Group). The CCDPLL CCR0 reference monitor invalidated.	0	R	Live	No
	4	CCDPLL Primary Reference Valid IRQ Status		Common Clock DPLL Primary Reference Validated IRQ Status (Common Group). The CCDPLL CCR0 reference monitor validated.	0	R	Live	No
	3	CCS slew limiter stopped slewing IRQ status		Common Clock Synchronizer Slew Limiter Stopped Slewing IRQ Status (Common Group). The CCS slew limiter stopped slewing.	0	R	Live	No
	2	CCS slew limiter started slewing IRQ status		Common Clock Synchronizer Slew Limiter Started Slewing IRQ Status (Common Group). The CCS slew limiter started slewing.	0	R	Live	No
	1	CCS sync guard activated IRQ status		Common Clock Synchronizer Synchronization Guard Activated IRQ Status (Common Group). The CCS synchronization guard was activated.	0	R	Live	No
	0	CCS ready IRQ status		Common Clock Synchronizer Ready IRQ Status (Common Group). The CCS is ready to support digitized clocking resources.	0	R	Live	No
0x301E	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	3	IUTS 1 invalid IRQ status		IUTS 1 Became Invalid IRQ Status (Common Group). IUTS 1 became invalid.	0	R	Live	No
	2	IUTS 1 valid IRQ status		IUTS 1 Became Valid IRQ Status (Common Group). IUTS 1 became valid.	0	R	Live	No
	1	IUTS 0 invalid IRQ status		IUTS 0 Became Invalid IRQ Status (Common Group). IUTS 0 became invalid.	0	R	Live	No
	0	IUTS 0 valid IRQ status		IUTS 0 Became Valid IRQ Status (Common Group). IUTS 0 became valid.	0	R	Live	No

AUXILIARY REFx STATUS—REGISTER 0x301F TO REGISTER 0x3022

Table 103. Auxiliary REFx Status Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x301F	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	Auxiliary REF0: LOS		Auxiliary REF0: Loss of Signal (LOS). Logic 1 indicates the Auxiliary REF0 reference monitor detected a loss of signal or a phase discontinuity (see the AD9546 data sheet for details).	0	R	Core clock	No
	4	Auxiliary REF0: valid		Auxiliary REF0: Valid. Logic 1 indicates the Auxiliary REF0 reference monitor declares Auxiliary REF0 as valid. That is, Auxiliary REF0 has been unfaulted (Bit 3 = 0) for at least as long as the user specified validation period (Register 0x0492 to Register 0x0490, Bits[19:0]). The user can force this bit to Logic 1 by programming Register 0x2004, Bit 4 = 1 and Register 0x2003, Bit 4 = 0.	0	R	Core clock	No
	3	Auxiliary REF0: fault		Auxiliary REF0: Fault. Logic 1 indicates the Auxiliary REF0 reference monitor detected a fault (logical OR of Bit 5 and Bits[2:0]).	0	R	Core clock	No
	2	Auxiliary REF0: excess jitter		Auxiliary REF0: Excess Jitter. Logic 1 indicates the Auxiliary REF0 reference monitor detects jitter exceeding the user specified limits (see Register 0x0494 to Register 0x0493). When Register 0x0494 to Register 0x0493, Bits[15:0] = 0, this bit is Logic 0.	0	R	Core clock	No
	1	Auxiliary REF0: fast		Auxiliary REF0: Fast. Logic 1 indicates the Auxiliary REF0 reference monitor declares the period of the input signal as less than the user specified limits (see Register 0x0480 to Register 0x048F).	0	R	Core clock	No
	0	Auxiliary REF0: slow		Auxiliary REF0: Slow. Logic 1 indicates the Auxiliary REF0 reference monitor declares the period of the input signal as greater than the user specified limits (see Register 0x0480 to Register 0x048F).	0	R	Core clock	No
0x3020	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	Auxiliary REF1: LOS		Auxiliary REF1: Loss of Signal (LOS). Logic 1 indicates the Auxiliary REF1 reference monitor detected a loss of signal or a phase discontinuity (see the AD9546 data sheet for details).	0	R	Core clock	No
	4	Auxiliary REF1: valid		Auxiliary REF1: Valid. Logic 1 indicates the Auxiliary REF1 reference monitor declares Auxiliary REF1 as valid. That is, Auxiliary REF1 has been unfaulted (Bit 3 = 0) for at least as long as the user specified validation period (Register 0x04B2 to Register 0x04B0, Bits[19:0]). The user can force this bit to Logic 1 by programming Register 0x2004, Bit 5 = 1 and Register 0x2003, Bit 5 = 0.	0	R	Core clock	No
	3	Auxiliary REF1: fault		Auxiliary REF1: Fault. Logic 1 indicates the Auxiliary REF1 reference monitor detected a fault (logical OR of Bit 5 and Bits[2:0]).	0	R	Core clock	No
	2	Auxiliary REF1: excess jitter		Auxiliary REF1: Excess Jitter. Logic 1 indicates the Auxiliary REF1 reference monitor detects jitter exceeding the user specified limits (see Register 0x04B4 to Register 0x04B3). When Register 0x04B4 to Register 0x04B3, Bits[15:0] = 0, this bit is Logic 0.	0	R	Core clock	No
	1	Auxiliary REF1: fast		Auxiliary REF1: Fast. Logic 1 indicates the Auxiliary REF1 reference monitor declares the period of the input signal as less than the user specified limits (see Register 0x04A0 to Register 0x04AF).	0	R	Core clock	No
	0	Auxiliary REF1: slow		Auxiliary REF1: Slow. Logic 1 indicates the Auxiliary REF1 reference monitor declares the period of the input signal as greater than the user specified limits (see Register 0x04A0 to Register 0x04AF).	0	R	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x3021	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	Auxiliary REF2: LOS		Auxiliary REF2: Loss of Signal (LOS). Logic 1 indicates the Auxiliary REF2 reference monitor detected a loss of signal or a phase discontinuity (see the AD9546 data sheet for details).	0	R	Core clock	No
	4	Auxiliary REF2: valid		Auxiliary REF2: Valid. Logic 1 indicates the Auxiliary REF2 reference monitor declares Auxiliary REF2 as valid. That is, Auxiliary REF2 has been unfaulted (Bit 3 = 0) for at least as long as the user specified validation period (Register 0x04D2 to Register 0x04D0, Bits[19:0]). The user can force this bit to Logic 1 by programming Register 0x2004, Bit 6 = 1 and Register 0x2003, Bit 6 = 0.	0	R	Core clock	No
	3	Auxiliary REF2: fault		Auxiliary REF2: Fault. Logic 1 indicates the Auxiliary REF2 reference monitor detected a fault (logical OR of Bit 5 and Bits[2:0]).	0	R	Core clock	No
	2	Auxiliary REF2: excess jitter		Auxiliary REF2: Excess Jitter. Logic 1 indicates the Auxiliary REF2 reference monitor detects jitter exceeding the user specified limits (see Register 0x04D4 to Register 0x04D3). When Register 0x04D4 to Register 0x04D3, Bits[15:0] = 0, this bit is Logic 0.	0	R	Core clock	No
	1	Auxiliary REF2: fast		Auxiliary REF2: Fast. Logic 1 indicates the Auxiliary REF2 reference monitor declares the period of the input signal as less than the user specified limits (see Register 0x04C0 to Register 0x04CF).	0	R	Core clock	No
	0	Auxiliary REF2: slow		Auxiliary REF2: Slow. Logic 1 indicates the Auxiliary REF2 reference monitor declares the period of the input signal as greater than the user specified limits (see Register 0x04C0 to Register 0x04CF).	0	R	Core clock	No
0x3022	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	Auxiliary REF3: LOS		Auxiliary REF3: Loss of Signal (LOS). Logic 1 indicates the Auxiliary REF3 reference monitor detected a loss of signal or a phase discontinuity (see the AD9546 data sheet for details).	0	R	Core clock	No
	4	Auxiliary REF3: valid		Auxiliary REF3: Valid. Logic 1 indicates the Auxiliary REF3 reference monitor declares Auxiliary REF3 as valid. That is, Auxiliary REF3 has been unfaulted (Bit 3 = 0) for at least as long as the user specified validation period (Register 0x04F2 to Register 0x04F0, Bits[19:0]). The user can force this bit to Logic 1 by programming Register 0x2004, Bit 7 = 1 and Register 0x2003, Bit 7 = 0.	0	R	Core clock	No
	3	Auxiliary REF3: fault		Auxiliary REF3: Fault. Logic 1 indicates the Auxiliary REF3 reference monitor detected a fault (logical OR of Bit 5 and Bits[2:0]).	0	R	Core clock	No
	2	Auxiliary REF3: excess jitter		Auxiliary REF3: Excess Jitter. Logic 1 indicates the Auxiliary REF3 reference monitor detects jitter exceeding the user specified limits (see Register 0x04F4 to Register 0x04F3). When Register 0x04F4 to Register 0x04F3, Bits[15:0] = 0, this bit is Logic 0.	0	R	Core clock	No
	1	Auxiliary REF3: fast		Auxiliary REF3: Fast. Logic 1 indicates the Auxiliary REF3 reference monitor declares the period of the input signal as less than the user specified limits (see Register 0x04E0 to Register 0x04EF).	0	R	Core clock	No
	0	Auxiliary REF3: slow		Auxiliary REF3: Slow. Logic 1 indicates the Auxiliary REF3 reference monitor declares the period of the input signal as greater than the user specified limits (see Register 0x04E0 to Register 0x04EF).	0	R	Core clock	No

IUTS STATUS—REGISTER 0x3023

Table 104. IUTS Status Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x3023	[7:2]	Reserved		Reserved.	0x00	R	Live	No
	1	IUTS 1 valid status		IUTS 1 Valid Status. Logic 1 indicates IUTS 1 can be used as a valid time stamp source to internal time stamp destinations (for example, as a reference input to a DPLL). The user can invalidate an otherwise valid IUTS 1 by programming Register 0x0F04, Bit 0 = 1.	0	R	Core clock	No
	0	IUTS 0 valid status		IUTS 0 Valid Status. Logic 1 indicates IUTS 0 can be used as a valid time stamp source to internal time stamp destinations (for example, as a reference input to a DPLL). The user can invalidate an otherwise valid IUTS 0 by programming Register 0x0F00, Bit 0 = 1.	0	R	Core clock	No

PLL CHANNEL 0 STATUS—REGISTER 0x3100 TO REGISTER 0x310E

Table 105. PLL Channel 0 Status Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x3100	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	APLL0 done calibrating		APLL0 Done Calibrating. Logic 1 indicates APLL0 has completed its calibration process.	0	R	Live	No
	4	APLL0 busy calibrating		APLL0 Busy Calibrating. Logic 1 indicates APLL0 is in the process of calibrating.	0	R	Live	No
	3	APLL0 phase-locked		APLL0 Phase-Locked. Logic 1 indicates APLL0 is phase-locked.	0	R	Live	No
	2	DPLL0 frequency locked		DPLL0 Frequency Locked. Logic 1 indicates DPLL0 is frequency locked.	0	R	Live	No
	1	DPLL0 phase-locked		DPLL0 Phase-Locked. Logic 1 indicates DPLL0 is phase-locked.	0	R	Live	No
	0	PLL0 locked		PLL0 Locked. Logic 1 indicates DPLL0 and APLL0 are both phase-locked.	0	R	Live	No
0x3101	7	Reserved		Reserved.	0	R	Live	No
	[6:4]	DPLL0 current profile		DPLL0 Current Profile. This 3-bit value, x, indicates the number of the currently active DPLL0 translation profile (for example, Translation Profile 0.x). When all DPLL0 translation profiles are inactive, x indicates the most recently active DPLL0 translation profile.	0x0	R	Core clock	No
	3	DPLL0 active		DPLL0 Active. Logic 1 indicates DPLL0 is attached to an active translation profile.	0	R	Core clock	No
	2	DPLL0 switching translation profiles		DPLL0 Switching Translation Profiles. Logic 1 indicates DPLL0 is in the process of switching to a new translation profile.	0	R	Core clock	No
	1	DPLL0 holdover mode		DPLL0 Holdover Mode. Logic 1 indicates DPLL0 is in holdover mode.	0	R	Core clock	No
	0	DPLL0 freerun mode		DPLL0 Freerun Mode. Logic 1 indicates DPLL0 is in freerun mode.	0	R	Core clock	No
0x3102	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	DPLL0 fast acquisition complete		DPLL0 Fast Acquisition Complete. Logic 1 indicates the DPLL0 completed a fast acquisition sequence.	0	R	Core clock	No
	4	DPLL0 performing fast acquisition		DPLL0 Performing Fast Acquisition. Logic 1 indicates the DPLL0 is in the process of a fast acquisition sequence.	0	R	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	3	Reserved		Reserved.	0	R	Live	No
	2	DPLL0 actively phase slew limiting		DPLL0 Actively Slewing Phase. Logic 1 indicates the DPLL0 phase slew limiter is actively phase slew limiting.	0	R	Core clock	No
	1	DPLL0 actively frequency clamping		DPLL0 Actively Frequency Clamping. Logic 1 indicates the DPLL0 frequency clamp is actively clamping the DPLL output frequency.	0	R	Core clock	No
	0	DPLL0 tuning word history available		DPLL0 Tuning Word History Available. Logic 1 indicates frequency tuning word history is available from the history tuning word processor of DPLL0 (see Register 0x3108 to Register 0x3103, Bits[45:0]).	0	R	Core clock	No
0x3103	[7:0]	DPLL0 FTW History Value[7:0]		DPLL0 Frequency Tuning Word History Value. This 46-bit value ($FTW_{HISTORY}$) constitutes the output of the frequency tuning word history processor of DPLL0. This tuning word value (when available) is the input to the NCO of DPLL0 in holdover mode.	0x00	R	Core clock	No
0x3104	[7:0]	DPLL0 FTW History Value[15:8]		Continuation of the DPLL0 FTW history value bit field. See the DPLL0 FTW History Value[7:0] description.	0x00	R	Core clock	No
0x3105	[7:0]	DPLL0 FTW History Value[23:16]		Continuation of the DPLL0 FTW history value bit field. See the DPLL0 FTW History Value[7:0] description.	0x00	R	Core clock	No
0x3106	[7:0]	DPLL0 FTW History Value[31:24]		Continuation of the DPLL0 FTW history value bit field. See the DPLL0 FTW History Value[7:0] description.	0x00	R	Core clock	No
0x3107	[7:0]	DPLL0 FTW History Value[39:32]		Continuation of the DPLL0 FTW history value bit field. See the DPLL0 FTW History Value[7:0] description.	0x00	R	Core clock	No
0x3108	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	[5:0]	DPLL0 FTW History Value[45:40]		Continuation of the DPLL0 FTW history value bit field. See the DPLL0 FTW History Value[7:0] description.	0x00	R	Core clock	No
0x3109	[7:0]	DPLL0 Phase Lock Detector Tub Level[7:0]		DPLL0 Phase Lock Detector Tub Level. This 12-bit value constitutes the instantaneous level in the phase lock detector tub of DPLL0.	0x00	R	Core clock	No
0x310A	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	[3:0]	DPLL0 Phase Lock Detector Tub Level[11:8]		Continuation of the DPLL0 phase lock detector tub level bit field. See the DPLL0 Phase Lock Detector Tub Level[7:0] description.	0x0	R	Core clock	No
0x310B	[7:0]	DPLL0 Frequency Lock Detector Tub Level[7:0]		DPLL0 Frequency Lock Detector Tub Level. This 12-bit value constitutes the instantaneous level in the frequency lock detector tub of DPLL0.	0x00	R	Core clock	No
0x310C	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	[3:0]	DPLL0 Frequency Lock Detector Tub Level[11:8]		Continuation of the DPLL0 Frequency Lock Detector Tub Level bit field. See the DPLL0 Frequency Lock Detector Tub Level[7:0] description.	0x0	R	Core clock	No
0x310D	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	Q0CC phase slew active		Q0CC Phase Slew Active. Logic 1 indicates the Q0CC divider is actively phase slewing.	0	R	Core clock	No
	4	Q0C phase slew active		Q0C Phase Slew Active. Logic 1 indicates the Q0C divider is actively phase slewing.	0	R	Core clock	No
	3	Q0BB phase slew active		Q0BB Phase Slew Active. Logic 1 indicates the Q0BB divider is actively phase slewing.	0	R	Core clock	No
	2	Q0B phase slew active		Q0B Phase Slew Active. Logic 1 indicates the Q0B divider is actively phase slewing.	0	R	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
	1	Q0AA phase slew active		Q0AA Phase Slew Active. Logic 1 indicates the Q0AA divider is actively phase slewing.	0	R	Core clock	No
	0	Q0A phase slew active		Q0A Phase Slew Active. Logic 1 indicates the Q0A divider is actively phase slewing.	0	R	Core clock	No
0x310E	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	Q0CC phase control error		Q0CC Phase Control Error. Logic 1 indicates an error by the phase controller for the Q0CC divider. This error generally results from the user programming an out of limits phase offset value.	0	R	Core clock	No
	4	Q0C phase control error		Q0C Phase Control Error. Logic 1 indicates an error by the phase controller for the Q0C divider. This error generally results from the user programming an out of limits phase offset value.	0	R	Core clock	No
	3	Q0BB phase control error		Q0BB Phase Control Error. Logic 1 indicates an error by the phase controller for the Q0BB divider. This error generally results from the user programming an out of limits phase offset value.	0	R	Core clock	No
	2	Q0B phase control error		Q0B Phase Control Error. Logic 1 indicates an error by the phase controller for the Q0B divider. This error generally results from the user programming an out of limits phase offset value.	0	R	Core clock	No
	1	Q0AA phase control error		Q0AA Phase Control Error. Logic 1 indicates an error by the phase controller for the Q0AA divider. This error generally results from the user programming an out of limits phase offset value.	0	R	Core clock	No
	0	Q0A phase control error		Q0A Phase Control Error. Logic 1 indicates an error by the phase controller for the Q0A divider. This error generally results from the user programming an out of limits phase offset value.	0	R	Core clock	No

PLL CHANNEL 1 STATUS—REGISTER 0x3200 TO REGISTER 0x320E

Table 106. PLL Channel 1 Status Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x3200	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	APLL1 done calibrating		APLL1 Done Calibrating. Logic 1 indicates APLL1 has completed its calibration process.	0	R	Live	No
	4	APLL1 busy calibrating		APLL1 Busy Calibrating. Logic 1 indicates APLL1 is in the process of calibrating.	0	R	Live	No
	3	APLL1 phase-locked		APLL1 Phase-Locked. Logic 1 indicates APLL1 is phase-locked.	0	R	Live	No
	2	DPLL1 frequency locked		DPLL1 Frequency Locked. Logic 1 indicates DPLL1 is frequency locked.	0	R	Live	No
	1	DPLL1 phase-locked		DPLL1 Phase-Locked. Logic 1 indicates DPLL1 is phase-locked.	0	R	Live	No
	0	PLL1 locked		PLL1 Locked. Logic 1 indicates DPLL1 and APLL1 are both phase-locked.	0	R	Live	No
0x3201	7	Reserved		Reserved.	0	R	Live	No
	[6:4]	DPLL1 current profile		DPLL1 Current Profile. This 3-bit value, x, indicates the number of the currently active DPLL1 translation profile (for example, Translation Profile 1.x). When all DPLL1 translation profiles are inactive, x indicates the most recently active DPLL1 translation profile.	0x0	R	Core clock	No
	3	DPLL1 active		DPLL1 Active. Logic 1 indicates DPLL1 is attached to an active translation profile.	0	R	Core clock	No
	2	DPLL1 switching translation profiles		DPLL1 Switching Translation Profiles. Logic 1 indicates DPLL1 is in the process of switching to a new translation profile.	0	R	Core clock	No
	1	DPLL1 holdover mode		DPLL1 Holdover Mode. Logic 1 indicates DPLL1 is in holdover mode.	0	R	Core clock	No
	0	DPLL1 freerun mode		DPLL1 Freerun Mode. Logic 1 indicates DPLL1 is in freerun mode.	0	R	Core clock	No
0x3202	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	5	DPLL1 fast acquisition complete		DPLL1 Fast Acquisition Complete. Logic 1 indicates the DPLL1 completed a fast acquisition sequence.	0	R	Core clock	No
	4	DPLL1 performing fast acquisition		DPLL1 Performing Fast Acquisition. Logic 1 indicates the DPLL1 is in the process of a fast acquisition sequence.	0	R	Core clock	No
	3	Reserved		Reserved.	0	R	Live	No
	2	DPLL1 actively phase slew limiting		DPLL1 Actively Slewing Phase. Logic 1 indicates the DPLL1 phase slew limiter is actively phase slew limiting.	0	R	Core clock	No
	1	DPLL1 actively frequency clamping		DPLL1 Actively Frequency Clamping. Logic 1 indicates the DPLL1 frequency clamp is actively clamping the DPLL output frequency.	0	R	Core clock	No
	0	DPLL1 tuning word history available		DPLL1 Tuning Word History Available. Logic 1 indicates frequency tuning word history is available from the history tuning word processor of DPLL1 (see Register 0x3208 to Register 0x3203, Bits[45:0]).	0	R	Core clock	No
0x3203	[7:0]	DPLL1 FTW History Value[7:0]		DPLL1 Frequency Tuning Word History Value. This 46-bit value ($FTW_{HISTORY}$) constitutes the output of the frequency tuning word history processor of DPLL1. This tuning word value (when available) is the input to the NCO of DPLL1 in holdover mode.	0x00	R	Core clock	No
0x3204	[7:0]	DPLL1 FTW History Value[15:8]		Continuation of the DPLL1 FTW history value bit field. See the DPLL1 FTW History Value[7:0] description.	0x00	R	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x3205	[7:0]	DPLL1 FTW History Value[23:16]		Continuation of the DPLL1 FTW history value bit field. See the DPLL1 FTW History Value[7:0] description.	0x00	R	Core clock	No
0x3206	[7:0]	DPLL1 FTW History Value[31:24]		Continuation of the DPLL1 FTW history value bit field. See the DPLL1 FTW History Value[7:0] description.	0x00	R	Core clock	No
0x3207	[7:0]	DPLL1 FTW History Value[39:32]		Continuation of the DPLL1 FTW history value bit field. See the DPLL1 FTW History Value[7:0] description.	0x00	R	Core clock	No
0x3208	[7:6]	Reserved		Reserved.	0x0	R	Live	No
	[5:0]	DPLL1 FTW History Value[45:40]		Continuation of the DPLL1 FTW history value bit field. See the DPLL1 FTW History Value[7:0] description.	0x00	R	Core clock	No
0x3209	[7:0]	DPLL1 Phase Lock Detector Tub Level[7:0]		DPLL1 Phase Lock Detector Tub Level. This 12-bit value constitutes the instantaneous level in the phase lock detector tub of DPLL1.	0x00	R	Core clock	No
0x320A	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	[3:0]	DPLL1 Phase Lock Detector Tub Level[11:8]		Continuation of the DPLL1 phase lock detector tub level bit field. See the DPLL1 Phase Lock Detector Tub Level[7:0] description.	0x0	R	Core clock	No
0x320B	[7:0]	DPLL1 Frequency Lock Detector Tub Level[7:0]		DPLL1 Frequency Lock Detector Tub Level. This 12-bit value constitutes the instantaneous level in the frequency lock detector tub of DPLL1.	0x00	R	Core clock	No
0x320C	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	[3:0]	DPLL1 Frequency Lock Detector Tub Level[11:8]		Continuation of the DPLL1 Frequency Lock Detector Tub Level bit field. See the DPLL1 Frequency Lock Detector Tub Level[7:0] description.	0x0	R	Core clock	No
0x320D	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	3	Q1BB phase slew active		Q1BB Phase Slew Active. Logic 1 indicates the Q1BB divider is actively phase slewing.	0	R	Core clock	No
	2	Q1B phase slew active		Q1B Phase Slew Active. Logic 1 indicates the Q1B divider is actively phase slewing.	0	R	Core clock	No
	1	Q1AA phase slew active		Q1AA Phase Slew Active. Logic 1 indicates the Q1AA divider is actively phase slewing.	0	R	Core clock	No
	0	Q1A phase slew active		Q1A Phase Slew Active. Logic 1 indicates the Q1A divider is actively phase slewing.	0	R	Core clock	No
0x320E	[7:4]	Reserved		Reserved.	0x0	R	Live	No
	3	Q1BB phase control error		Q1BB Phase Control Error. Logic 1 indicates an error by the phase controller for the Q1BB divider. This error generally results from the user programming an out of limits phase offset value.	0	R	Core clock	No
	2	Q1B phase control error		Q1B Phase Control Error. Logic 1 indicates an error by the phase controller for the Q1B divider. This error generally results from the user programming an out of limits phase offset value.	0	R	Core clock	No
	1	Q1AA phase control error		Q1AA Phase Control Error. Logic 1 indicates an error by the phase controller for the Q1AA divider. This error generally results from the user programming an out of limits phase offset value.	0	R	Core clock	No
	0	Q1A phase control error		Q1A Phase Control Error. Logic 1 indicates an error by the phase controller for the Q1A divider. This error generally results from the user programming an out of limits phase offset value.	0	R	Core clock	No

AUXILIARY NCO 0 TIME SCALE OUTPUT—REGISTER 0x3A00 TO REGISTER 0x3A09

Table 107. Auxiliary NCO 0 Time Scale Output Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x3A00	[7:0]	Auxiliary NCO 0 Time Scale[7:0]		Auxiliary NCO 0 Time Scale. This 80-bit register provides access to the time scale of Auxiliary NCO 0 (as of the most recent assertion of IO update). Bits[39:0] constitute the state of the 40-bit accumulator at the heart of Auxiliary NCO 0. The 40-bit value represents a fraction of one cycle (or unit interval, UI) of the programmed frequency of Auxiliary NCO 0 (that is, the LSB equals 2^{-40} UI). Bits[79:40] represent increments of each rollover of the Auxiliary NCO 0 accumulator (that is, whole cycles or integer UI). The user can adjust the value that appears in Bits[79:40] (see Register 0x281D to Register 0x2819, Bits[39:0]).	0x00	R	Core clock	No
0x3A01	[7:0]	Auxiliary NCO 0 Time Scale[15:8]		Continuation of the Auxiliary NCO 0 time scale bit field. See the Auxiliary NCO 0 Time Scale[7:0] description.	0x00	R	Core clock	No
0x3A02	[7:0]	Auxiliary NCO 0 Time Scale[23:16]		Continuation of the Auxiliary NCO 0 time scale bit field. See the Auxiliary NCO 0 Time Scale[7:0] description.	0x00	R	Core clock	No
0x3A03	[7:0]	Auxiliary NCO 0 Time Scale[31:24]		Continuation of the Auxiliary NCO 0 time scale bit field. See the Auxiliary NCO 0 Time Scale[7:0] description.	0x00	R	Core clock	No
0x3A04	[7:0]	Auxiliary NCO 0 Time Scale[39:32]		Continuation of the Auxiliary NCO 0 time scale bit field. See the Auxiliary NCO 0 Time Scale[7:0] description.	0x00	R	Core clock	No
0x3A05	[7:0]	Auxiliary NCO 0 Time Scale[47:40]		Continuation of the Auxiliary NCO 0 time scale bit field. See the Auxiliary NCO 0 Time Scale[7:0] description.	0x00	R	Core clock	No
0x3A06	[7:0]	Auxiliary NCO 0 Time Scale[55:48]		Continuation of the Auxiliary NCO 0 time scale bit field. See the Auxiliary NCO 0 Time Scale[7:0] description.	0x00	R	Core clock	No
0x3A07	[7:0]	Auxiliary NCO 0 Time Scale[63:56]		Continuation of the Auxiliary NCO 0 time scale bit field. See the Auxiliary NCO 0 Time Scale[7:0] description.	0x00	R	Core clock	No
0x3A08	[7:0]	Auxiliary NCO 0 Time Scale[71:64]		Continuation of the Auxiliary NCO 0 time scale bit field. See the Auxiliary NCO 0 Time Scale[7:0] description.	0x00	R	Core clock	No
0x3A09	[7:0]	Auxiliary NCO 0 Time Scale[79:72]		Continuation of the Auxiliary NCO 0 time scale bit field. See the Auxiliary NCO 0 Time Scale[7:0] description.	0x00	R	Core clock	No

AUXILIARY NCO 1 TIME SCALE OUTPUT—REGISTER 0x3A0A TO REGISTER 0x3A13

Table 108. Auxiliary NCO 1 Time Scale Output Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x3A0A	[7:0]	Auxiliary NCO 1 Time Scale[7:0]		Auxiliary NCO 1 Time Scale. This 80-bit register provides access to the time scale of Auxiliary NCO 1 (as of the most recent assertion of IO update). Bits[39:0] constitute the state of the 40-bit accumulator at the heart of Auxiliary NCO 1. The 40-bit value represents a fraction of one cycle (or unit interval, UI) of the programmed frequency of Auxiliary NCO 1 (that is, the LSB equals 2^{-40} UI). Bits[79:40] represent increments of each rollover of the Auxiliary NCO 1 accumulator (that is, whole cycles or integer UI). The user can adjust the value that appears in Bits[79:40] (see Register 0x281D to Register 0x2819, Bits[39:0]).	0x00	R	Core clock	No
0x3A0B	[7:0]	Auxiliary NCO 1 Time Scale[15:8]		Continuation of the Auxiliary NCO 1 time scale bit field. See the Auxiliary NCO 1 Time Scale[7:0] description.	0x00	R	Core clock	No
0x3A0C	[7:0]	Auxiliary NCO 1 Time Scale[23:16]		Continuation of the Auxiliary NCO 1 time scale bit field. See the Auxiliary NCO 1 Time Scale[7:0] description.	0x00	R	Core clock	No
0x3A0D	[7:0]	Auxiliary NCO 1 Time Scale[31:24]		Continuation of the Auxiliary NCO 1 time scale bit field. See the Auxiliary NCO 1 Time Scale[7:0] description.	0x00	R	Core clock	No
0x3A0E	[7:0]	Auxiliary NCO 1 Time Scale[39:32]		Continuation of the Auxiliary NCO 1 time scale bit field. See the Auxiliary NCO 1 Time Scale[7:0] description.	0x00	R	Core clock	No
0x3A0F	[7:0]	Auxiliary NCO 1 Time Scale[47:40]		Continuation of the Auxiliary NCO 1 time scale bit field. See the Auxiliary NCO 1 Time Scale[7:0] description.	0x00	R	Core clock	No
0x3A10	[7:0]	Auxiliary NCO 1 Time Scale[55:48]		Continuation of the Auxiliary NCO 1 time scale bit field. See the Auxiliary NCO 1 Time Scale[7:0] description.	0x00	R	Core clock	No
0x3A11	[7:0]	Auxiliary NCO 1 Time Scale[63:56]		Continuation of the Auxiliary NCO 1 time scale bit field. See the Auxiliary NCO 1 Time Scale[7:0] description.	0x00	R	Core clock	No
0x3A12	[7:0]	Auxiliary NCO 1 Time Scale[71:64]		Continuation of the Auxiliary NCO 1 time scale bit field. See the Auxiliary NCO 1 Time Scale[7:0] description.	0x00	R	Core clock	No
0x3A13	[7:0]	Auxiliary NCO 1 Time Scale[79:72]		Continuation of the Auxiliary NCO 1 time scale bit field. See the Auxiliary NCO 1 Time Scale[7:0] description.	0x00	R	Core clock	No

USER TIME STAMP PROCESSOR OUTPUT: UTSP0—REGISTER 0x3A14 TO REGISTER 0x3A1F

Table 109. UTSP0 Output Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x3A14	[7:0]	UTSP0 Output[7:0]		UTSP0 Output. This 80-bit unsigned value, TS_CONV, is the result of a time stamp conversion by UTSP0. However, the user must assert an IO update to transfer the current time stamp conversion to this register. The reference period, t_0, for the time stamp conversion depends on the selected time scale per Register 0x2A12, Bits[7:6]. The value of TS_CONV and t_0 yield a time stamp value, TS, as follows: $TS = TS\_CONV \times 2^{-40} \times t_0$ For example, given a 1 kHz time scale (t_0 = 0.001 sec) and TS_CONV = 0x 0000 0000 B10E 04F0 07C1 (194,673,770,497,985), then TS = 0.1770547628421 sec. The user can independently access the integer part of TS_CONV (TS_INT) via Bits[79:40] and the fractional part of TS_CONV (TS_FRAC) via Bits[39:0] yielding the following relationships: $t_{TS\_INT} = TS\_INT \times t_0$ $t_{TS\_FRAC} = TS\_FRAC \times 2^{-40} \times t_0$ Using this example, TS_INT = 0x 00 0000 00B1 (177 decimal) leading to t_{TS_INT} = 177 ms and TS_FRAC = 0x 0E 04F0 07C1 (60,212,381,633) leading to t_{TS_FRAC} = 54.7628421 µs.	0x00	R	Core clock	No
0x3A15	[7:0]	UTSP0 Output[15:8]		Continuation of the UTSP0 output bit field. See the UTSP0 Output[7:0] description.	0x00	R	Core clock	No
0x3A16	[7:0]	UTSP0 Output[23:16]		Continuation of the UTSP0 output bit field. See the UTSP0 Output[7:0] description.	0x00	R	Core clock	No
0x3A17	[7:0]	UTSP0 Output[31:24]		Continuation of the UTSP0 output bit field. See the UTSP0 Output[7:0] description.	0x00	R	Core clock	No
0x3A18	[7:0]	UTSP0 Output[39:32]		Continuation of the UTSP0 output bit field. See the UTSP0 Output[7:0] description.	0x00	R	Core clock	No
0x3A19	[7:0]	UTSP0 Output[47:40]		Continuation of the UTSP0 output bit field. See the UTSP0 Output[7:0] description.	0x00	R	Core clock	No
0x3A1A	[7:0]	UTSP0 Output[55:48]		Continuation of the UTSP0 output bit field. See the UTSP0 Output[7:0] description.	0x00	R	Core clock	No
0x3A1B	[7:0]	UTSP0 Output[63:56]		Continuation of the UTSP0 output bit field. See the UTSP0 Output[7:0] description.	0x00	R	Core clock	No
0x3A1C	[7:0]	UTSP0 Output[71:64]		Continuation of the UTSP0 output bit field. See the UTSP0 Output[7:0] description.	0x00	R	Core clock	No
0x3A1D	[7:0]	UTSP0 Output[79:72]		Continuation of the UTSP0 output bit field. See the UTSP0 Output[7:0] description.	0x00	R	Core clock	No
0x3A1E	[7:0]	UTSP0 time stamps missed count		UTSP0 Time Stamps Missed Count. This 8-bit unsigned value, CNT, indicates the number of UTSP0 time stamp conversions not read by the user via Register 0x3A1D to Register 0x3A14, Bits[79:0]. Thus, CNT > 0 indicates the count of loss of time stamp conversions and CNT = 255 indicates the loss of at least 255 time stamp conversions.	0x00	R	Core clock	No
0x3A1F	[7:1]	Reserved		Reserved.	0x00	R	Live	No
	0	UTSP0 overdue time stamp		UTSP0 Overdue Time Stamp. Logic 1 indicates the last time stamp received from the user designated time stamp source to UTSP0 occurred well beyond the user specified period for the time stamp source. Such an occurrence can degrade the precision of the converted time stamp. Thus, when this bit is Logic 1, the accuracy of the time stamp conversion is uncertain.	0	R	Core clock	No

USER TIME STAMP PROCESSOR OUTPUT: UTSP1—REGISTER 0x3A20 TO REGISTER 0x3A2B

Table 110. UTSP1 Output Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x3A20	[7:0]	UTSP1 Output[7:0]		UTSP1 Output. This 80-bit unsigned value, TS_CONV, is the result of a time stamp conversion by UTSP1. However, the user must assert an IO update to transfer the current time stamp conversion to this register. The reference period, t_0, for the time stamp conversion depends on the selected time scale per Register 0x2A12, Bits[7:6]. The value of TS_CONV and t_0 yield a time stamp value, TS, as follows: $TS = TS\_CONV \times 2^{-40} \times t_0$ For example, given a 1 kHz time scale (t_0 = 0.001 sec) and TS_CONV = 0x 0000 0000 B10E 04F0 07C1 (194,673,770,497,985), then TS = 0.1770547628421 sec. The user can independently access the integer part of TS_CONV (TS_INT) via Bits[79:40] and the fractional part of TS_CONV (TS_FRAC) via Bits[39:0] yielding the following relationships: $t_{TS\_INT} = TS\_INT \times t_0$ $t_{TS\_FRAC} = TS\_FRAC \times 2^{-40} \times t_0$ Using this example, TS_INT = 0x 00 0000 00B1 (177 decimal) leading to t_{TS_INT} = 177 ms and TS_FRAC = 0x 0E 04F0 07C1 (60,212,381,633) leading to t_{TS_FRAC} = 54.7628421 µs.	0x00	R	Core clock	No
0x3A21	[7:0]	UTSP1 Output[15:8]		Continuation of the UTSP1 output bit field. See the UTSP1 Output[7:0] description.	0x00	R	Core clock	No
0x3A22	[7:0]	UTSP1 Output[23:16]		Continuation of the UTSP1 output bit field. See the UTSP1 Output[7:0] description.	0x00	R	Core clock	No
0x3A23	[7:0]	UTSP1 Output[31:24]		Continuation of the UTSP1 output bit field. See the UTSP1 Output[7:0] description.	0x00	R	Core clock	No
0x3A24	[7:0]	UTSP1 Output[39:32]		Continuation of the UTSP1 output bit field. See the UTSP1 Output[7:0] description.	0x00	R	Core clock	No
0x3A25	[7:0]	UTSP1 Output[47:40]		Continuation of the UTSP1 output bit field. See the UTSP1 Output[7:0] description.	0x00	R	Core clock	No
0x3A26	[7:0]	UTSP1 Output[55:48]		Continuation of the UTSP1 output bit field. See the UTSP1 Output[7:0] description.	0x00	R	Core clock	No
0x3A27	[7:0]	UTSP1 Output[63:56]		Continuation of the UTSP1 output bit field. See the UTSP1 Output[7:0] description.	0x00	R	Core clock	No
0x3A28	[7:0]	UTSP1 Output[71:64]		Continuation of the UTSP1 output bit field. See the UTSP1 Output[7:0] description.	0x00	R	Core clock	No
0x3A29	[7:0]	UTSP1 Output[79:72]		Continuation of the UTSP1 output bit field. See the UTSP1 Output[7:0] description.	0x00	R	Core clock	No
0x3A2A	[7:0]	UTSP1 time stamps missed count		UTSP1 Time Stamps Missed Count. This 8-bit unsigned value, CNT, indicates the number of UTSP1 time stamp conversions not read by the user via Register 0x3A29 to Register 0x3A20, Bits[79:0]. Thus, CNT > 0 indicates the count of loss of time stamp conversions and CNT = 255 indicates the loss of at least 255 time stamp conversions.	0x00	R	Core clock	No
0x3A2B	[7:1]	Reserved		Reserved.	0x00	R	Live	No
	0	UTSP1 overdue time stamp		UTSP1 Overdue Time Stamp. Logic 1 indicates the last time stamp received from the user designated time stamp source to UTSP1 occurred well beyond the user specified period for the time stamp source. Such an occurrence can degrade the precision of the converted time stamp. Thus, when this bit is Logic 1, the accuracy of the time stamp conversion is uncertain.	0	R	Core clock	No

SKEW MEASUREMENT PROCESSOR OUTPUT—REGISTER 0x3A2C TO REGISTER 0x3A3B

Table 111. Skew Measurement Processor Output Details

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
0x3A2C	[7:0]	Skew Offset Result[7:0]		Skew Offset Result. This 62-bit signed value, SKEW_OFST in units of 2^{-16} ps, constitutes the average measured time difference, t_{SKEW}, between time stamps from the reference source (per Register 0x2A15, Bits[4:0]) and time stamps from the target source (per Register 0x2A16, Bits[4:0]). The value of SKEW_OFST relates to t_{SKEW} as follows: $t_{SKEW} = SKEW\_OFST \times 2^{-16}$ ps For example, given SKEW_OFST = 0x 3FFF FFF8 A673 24B5 (−31,567,174,475), then t_{SKEW} = −481,676.8566131591796875 ps. A negative SKEW_OFST value means the target source leads the reference source. SKEW_OFST is averaged (see Register 0x2A14, Bits[3:0]). Skew measurements expect the reference and target sources to be of the same frequency. Otherwise, successive skew measurements drift over time. See Register 0x3A3A to Register 0x3A34, Bits[61:0] regarding skew drift.	0x00	R	Core clock	No
0x3A2D	[7:0]	Skew Offset Result[15:8]		Continuation of the skew offset result bit field. See the Skew Offset Result[7:0] description.	0x00	R	Core clock	No
0x3A2E	[7:0]	Skew Offset Result[23:16]		Continuation of the skew offset result bit field. See the Skew Offset Result[7:0] description.	0x00	R	Core clock	No
0x3A2F	[7:0]	Skew Offset Result[31:24]		Continuation of the skew offset result bit field. See the Skew Offset Result[7:0] description.	0x00	R	Core clock	No
0x3A30	[7:0]	Skew Offset Result[39:32]		Continuation of the skew offset result bit field. See the Skew Offset Result[7:0] description.	0x00	R	Core clock	No
0x3A31	[7:0]	Skew Offset Result[47:40]		Continuation of the skew offset result bit field. See the Skew Offset Result[7:0] description.	0x00	R	Core clock	No
0x3A32	[7:0]	Skew Offset Result[55:48]		Continuation of the skew offset result bit field. See the Skew Offset Result[7:0] description.	0x00	R	Core clock	No
0x3A33	7	Skew measurement average complete		Skew Measurement Average Complete. Logic 1 indicates that the skew measurement processor has averaged at least as many skew samples as specified by Register 0x2A14, Bits[3:0], which triggers an IRQ via Register 0x300F, Bit 4. Logic 0 indicates an under averaged result, which exhibits greater variance relative to a fully averaged result.	0	R	Core clock	No
	6	Reserved		Reserved.	0	R	Live	No
	[5:0]	Skew Offset Result[61:56]		Skew Offset Result. These six bits constitute the 6 MSBs of the 62-bit signed SKEW_OFST value (see Register 0x3A2C).	0x00	R	Core clock	No
0x3A34	[7:0]	Skew Drift Result[7:0]		Skew Drift Result. This 62-bit signed value, SKEW_DRIFT in units of 2^{-16} ps/UI, constitutes the average drift rate of successive time skew measurement samples. SKEW_DRIFT represents the fractional period error, FPE, of the target source (per Register 0x2A16, Bits[4:0]) relative to the reference source (per Register 0x2A15, Bits[4:0]). UI is the measured period of the reference source, t_{REFSRC}. FPE relates to SKEW_DRIFT as follows: $FPE = 2^{-16} \times 10^{-12} \times SKEW\_DRIFT/t_{REFSRC}$ For example, given t_{REFSRC} = 0.01 (100 Hz) and SKEW_DRIFT = 0x 3FFF FFF8 A673 24B5 (−31,567,174,475), then FPE = $-48.16768566131591796875 \times 10^{-6}$.	0x00	R	Core clock	No

Address	Bits	Bit Name	Settings	Description	Reset	R/W	IO Update	Auto-clear
				FPE relates to fractional frequency error, FFE as follows: $FFE = -FPE/(1 + FPE)$ Yielding FFE = 48.17000589901836561886401370494 4 × 10^{-6}. Thus, given a source frequency of 100 Hz, the target frequency is 100 × (1 + FFE) ≈ 100.004817 Hz. Skew drift measurements have a limit of UI/16, which, if exceeded, causes the skew measurement processor to flag an error that triggers an IRQ via Register 0x300C, Bit 5.				
0x3A35	[7:0]	Skew Drift Result[15:8]		Continuation of the skew drift result bit field. See the Skew Drift Result[7:0] description.	0x00	R	Core clock	No
0x3A36	[7:0]	Skew Drift Result[23:16]		Continuation of the skew drift result bit field. See the Skew Drift Result[7:0] description.	0x00	R	Core clock	No
0x3A37	[7:0]	Skew Drift Result[31:24]		Continuation of the skew drift result bit field. See the Skew Drift Result[7:0] description.	0x00	R	Core clock	No
0x3A38	[7:0]	Skew Drift Result[39:32]		Continuation of the skew drift result bit field. See the Skew Drift Result[7:0] description.	0x00	R	Core clock	No
0x3A39	[7:0]	Skew Drift Result[47:40]		Continuation of the skew drift result bit field. See the Skew Drift Result[7:0] description.	0x00	R	Core clock	No
0x3A3A	[7:0]	Skew Drift Result[55:48]		Continuation of the skew drift result bit field. See the Skew Drift Result[7:0] description.	0x00	R	Core clock	No
0x3A3B	7	Skew Drift Average Complete		Skew Drift Average Complete. Logic 1 indicates that the skew measurement processor has averaged at least as many skew drift samples as specified by Register 0x2A14, Bits[3:0]. Logic 0 indicates an under averaged result, which exhibits greater variance relative to a fully averaged result.	0	R	Core clock	No
	6	Reserved		Reserved.	0	R	Live	No
	[5:0]	Skew Drift Result[61:56]		Skew Drift Result. These six bits constitute the 6 MSBs of the 62-bit signed SKEW_DRIFT value (see Register 0x3A34).	0x00	R	Core clock	No

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).