ANALOG DEVICES

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Evaluating the AD9547 and AD9548 Digital PLL Clock Synthesizers

FEATURES

Simple power connection using 6 V wall adapter and on-board switching and LDO voltage regulators
Regulators easily bypassed for power measurements
8 ac-coupled SMA connectors for output
SMA connectors for
    2 differential or 4 single-ended reference input
    System clock input
On-board provisions for OCXO, crystal oscillator, or crystal
USB connection to PC
32-bit or 64-bit Windows-based evaluation software with simple graphical user interface
On-board PLL loop filter
Easy access to digital I/O and diagnostic signals via I/O header
Status LEDs for diagnostic signals

APPLICATIONS

GPS 1 pps applications (AD9548 only)
Networking and communications line cards and synchronous equipment timing source (SETS) devices
Test and measurement equipment
Wireless base stations, controllers
Clock cleanup/jitter attenuation

GENERAL DESCRIPTION

This user guide applies to the evaluation boards for the AD9547 and AD9548, although only the AD9548 is discussed within. The two devices differ primarily in the number of inputs and outputs. The only other difference is the maximum size of the feedback divider. The AD9548 accepts input reference frequencies as low as 1 Hz. The minimum input reference frequency of the AD9547 is 1 kHz.

The AD9548 is a very low noise DDS-based digital PLL clock synthesizer with up to eight reference inputs and up to eight outputs. The AD9548 features reference clock validation, automatic holdover, and hitless reference clock switching. The AD9548 is also capable of accepting a 1 pulse per second (pps) reference input clock.

The AD9548 Revision E evaluation board is a compact, easy-to-use platform for evaluating all features of the AD9548.
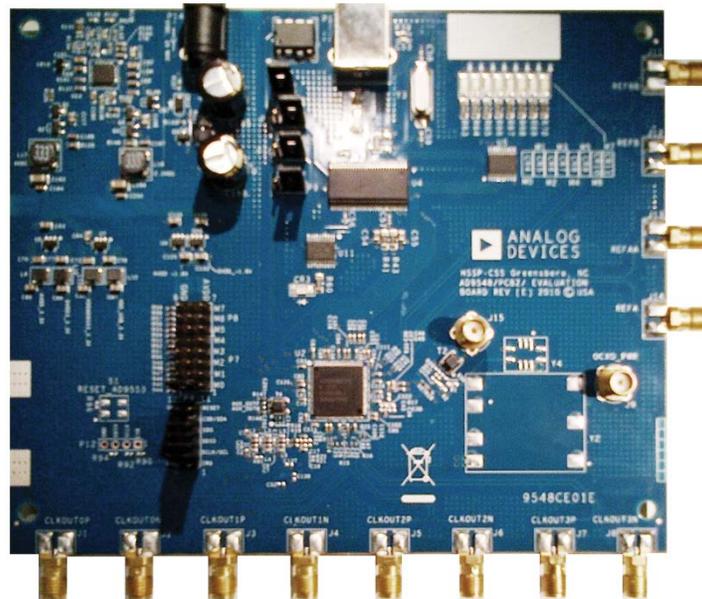
Figure 1. AD9548 Evaluation Board, Revision E

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REVISION HISTORY

4/14—Revision 0: Initial Version

CONSIDERATIONS FOR 1 PPS OPERATION

The AD9548 1 pps operation requires special components as well as modifications to the evaluation board.

The crystal on the evaluation board is stable enough to allow loop bandwidths down to approximately 50 Hz. Use an OCXO, TCXO, or external signal generator as the system clock source to go lower. The maximum loop bandwidth for 1 pps operation is 50 mHz.

In addition, the reference inputs need to be dc-coupled.

DC-COUPLING THE REFERENCE INPUTS

Most 1 pps signals are single-ended CMOS, and these instructions assume that this is the case. Though these instructions reference REFA and REFAA, the same instructions apply to REFB and REFBB.

1. Remove R24.
2. Change C41 and C42 to a 33 Ω resistor.
3. Many single-ended signals experience significant loss travelling from the 1 pps source to the AD9548 evaluation board. Probe the REFA (or REFAA) input to determine the V_{IH} of the signal, and set that amplitude on the REF input screen. See the Reference Input Configuration section for more details.
4. Ensure there is no ringing on the 1 pps signal. Ringing on the AD9548 could cause the device to interpret the 1 pps signal as a 2 pps or 3 pps signal rendering the reference input invalid. Some experimentation of the optimal value of the resistor used in the C42/C43 position may be needed to reduce ringing.

USING A TCXO AS THE SYSTEM CLOCK SOURCE

The system clock input is a self-biased 1.8 V receiver, thus V_{IH} must never exceed 1.8 V. The best type of TCXO is one with a 1.8 V or 3.3 V CMOS output. These instructions assume that a Vectron TX-700 (or compatible) TCXO is soldered to location Y4 on the evaluation board. The lowest output phase noise is achieved with a TCXO with a high frequency, such as 27 MHz.

1. Remove R27 and R28 to disconnect the 50 MHz crystal.
2. Install the TCXO at position Y4.
3. Install R1 = 300 Ω and R2 = 150 Ω. The goal of the voltage divider is to convert a 3.3 V CMOS inputs to a 1 V p-p ac-coupled signal. However, the suggested resistor values may not be optimal because some CMOS drivers may have difficulty driving a low impedance load. Verify that the waveform is not distorted. The AD9548 evaluation board schematic has alternate resistor values that may work better if you want to dc-couple a 1.8 V CMOS signal into the SYSCLKP pin, but doing so may make it more difficult to maintain a 50% duty cycle.
4. Install C50 = 0.1 μF. This is a bypass capacitor for the (unused) complimentary system clock input.
5. Install R29 = 0 Ω.

USING AN OCXO AS THE SYSTEM CLOCK SOURCE

The system clock input is a self-biased 1.8 V receiver, so V_{IH} must never exceed 1.8 V. The best type of OCXO is one with a 1.8 V or 3.3 V CMOS output. These instructions assume that a Vectron OX-221 (or compatible) OCXO is soldered to location Y2 on the evaluation board. The lowest output phase noise is achieved with an OCXO with a high frequency, such as 27 MHz. Another popular choice is 19.2 MHz.

1. Remove R27 and R28 to disconnect the 50 MHz crystal.
2. Install the OCXO at position Y2.
3. Install R1 = 300 Ω and R2 = 150 Ω. The goal of the voltage divider is to convert a 3.3 V CMOS inputs to a 1 V p-p ac-coupled signal. However, the suggested resistor values may not be optimal because some CMOS drivers may have difficulty driving a low impedance load. Verify that the waveform is not distorted. The AD9548 evaluation board schematic has alternate resistor values that may work better if you want to dc-couple a 1.8 V signal CMOS signal into the SYSCLKP pin, but doing so may make it more difficult to maintain a 50% duty cycle.
4. Install C50 = 0.1 μF. This is a bypass capacitor for the (unused) complimentary system clock input.
5. Install R29 = 0 Ω.
6. Supply power to the OCXO using Connector J9.

USING THE SYSTEM CLOCK DOUBLER WITH AN OCXO OR A TCXO

The system clock doubler can significantly reduce the amount of in-band jitter of the AD9548. However, it relies on a nearly 50% duty cycle of the system clock input. If you have difficulty getting a system clock stable indication when using the doubler, disable it, multiply the system clock feedback divider by 2, and recalibrate the system clock VCO. See the System Clock Configuration section for more details.

SETTING UP THE EVALUATION BOARD

The following instructions are for setting up the physical connections to the AD9548 evaluation board.

It is important to install the evaluation software prior to connecting the evaluation board.

POWER AND PC CONNECTIONS

1. Install the evaluation software. Note that administrative privileges are required for installation.

2. Connect the wall power supply to the main power connector labeled P11. The green CR3 LED should be on.

3. Connect the USB cable to the evaluation board and the computer. The red LED labeled CR2 on the AD9548 evaluation board should illuminate and the green CR3 LED should start blinking.

4. Select **Install the software automatically** and click **Next** if the **Found New Hardware Wizard** automatically appears when the evaluation board is connected. The **Found New Hardware Wizard** may appear twice, and a system restart may be required.

5. Run the evaluation software as described in the Running the Software section.

If the green CR3 LED is not blinking, ensure that:

- Jumpers are installed on Position P2 and on either the I²C or the SPI position of P3 and P10.

- The jumper on P9 lies across the center pin and the PC symbol.

- The USB port on the PC is operational and that the USB cable is not damaged.

SIGNAL CONNECTIONS

1. Connect a signal generator to any one of the SMA connectors (J11 to J14). By default, the reference inputs on this evaluation board are ac-coupled and terminated 50 Ω across the differential pair.

    - If connecting a 1 pps GPS signal (or other low frequency CMOS signal to a reference input), see the Considerations for 1 PPS Operation section for more details.

    - If connecting a signal generator with single-ended output to a reference input, remove the termination resistor (R23 or R24) across the differential pair. An amplitude setting of 0 to +6 dBm is fine.

2. Connect an oscilloscope, spectrum analyzer, or other lab equipment to any of the J2, or J4-J10 SMA connectors on the right hand side of the board.

BYPASSING THE WALL POWER SUPPLY

1. Remove the L7 and L13 ferrite beads as well as the R75 and R76 resistors.

2. Connect a bench power supply to J17 (2.2 V) and J16 (4 V).

The 4 V supply is routed to the LDOs labeled U6 and U7 where U6 supplies the 3.3 V analog power pins while U7 powers the 3.3 V digital power pins.

The 2.2 V supply is routed to the LDOs labeled U9 and U10 where U9 supplies the 3.3 V analog power pins while U10 powers the 3.3 V digital power pins.

BYPASSING THE SYSTEM CLOCK PLL

By default, the evaluation board is configured for a 50 MHz crystal installed on the back of the board at position Y1.

To bypass the crystal and supply a system clock signal on SMA connector J15,

1. Remove R27 and R28.

2. Place 0.1 μF capacitors on C50 and C51.

3. Place a 50 Ω resistor on R33.

R29 and R30 are provided as an alternative to R33 for equipment that prefers termination to ground instead of across the differential pair.

USING THE I²C SERIAL PORT MODE

1. Move the P3 and P10 jumpers from SPI to I²C.

2. Select the desired I²C address using Jumpers M0, M1, and M2 in jumper block P7. See the SPI/I²C port selection information in the AD9548 data sheet for I²C address selection.

3. On the evaluation software, select **Configure Serial Port** from the **I/O** menu.

4. Click on **Reset Serial Port** and then click **Detect Current Configuration**. A dialog box should open and acknowledge the I²C mode and address.

SETTING UP THE SOFTWARE

The following instructions are for setting up the AD9548 evaluation board software. Starting with Version 2.0.0, the evaluation software and USB drivers are compatible with 32-bit and 64-bit versions of Microsoft® Windows®.

However, the USB identity of the evaluation board has changed in the process of adding 64-bit support. Older evaluation boards must have their USB EEPROM updated. See the Flashing the Evaluation Board USB EEPROM section for instructions.

CHECKING FOR SOFTWARE COMPATIBILITY AND INSTALLATING THE SOFTWARE

Do not connect the evaluation board until the software installation is complete.

1. Verify that you are installing Version 2.0.0 (or later) of the AD9548 evaluation software to ensure compatibility with 32-bit and 64-bit versions of Windows.
2. Download and run the evaluation software.
3. Check for any updates to the evaluation software on the same page.

RUNNING THE SOFTWARE

1. Apply power and connect the evaluation board to the PC. Alternatively, use the software in standalone mode and specify which version of the AD9548 will be used. Standalone mode is useful for verifying register settings for a given PLL setup.
2. Load the evaluation software. If the evaluation board is connected while the evaluation software is running, the evaluation software may not automatically detect it.

If the evaluation board was not automatically detected when it was connected, then you can

1. Select **Select Evaluation Board** from the **I/O** menu.
2. Select **Cyusb-1**, **Cyusb-2**, or **Cyusb-3**.

Note that if the computer connected to the evaluation board enters suspend or hibernation mode, you may need to restart the evaluation software to reestablish the connection between the software and the evaluation board.
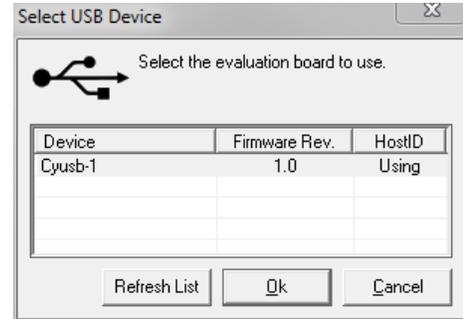

Figure 2. Evaluation Board Selection Window

This user guide assumes that status polling is enabled. If **Status**, located left of center at the bottom of the main window of the software (see Figure 4), is not flashing, enable status polling by clicking on **File>Options**, and ensuring that **Enable Status Polling** is checked.

See the Evaluation Software Components section for a description of the evaluation software features, and/or the Quick Start Guide to the AD9548 PLL section for details on the individual blocks of the AD9548.

FLASHING THE EVALUATION BOARD USB EEPROM
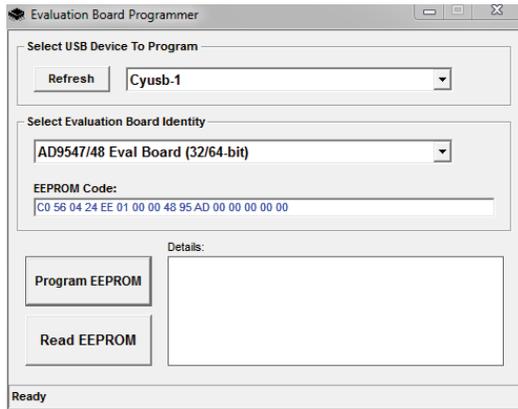
Figure 3. Evaluation Board USB Programmer

The following steps reflash AD9547/AD9548 EEPROM for the USB controller to make it compatible with 64-bit USB drivers. This utility is also useful if the CR3 LED fails to blink when the evaluation board is connected to the computer.

1. Download and install the evaluation board USB EEPROM programmer file from the evaluation board page.

2. Before applying power, pull the P2 jumper. On older evaluation boards, this may be labeled **EEPROM ENABLE**.

3. Apply power to the board. (This puts the USB controller chip from Cypress Semiconductor in default mode.)

4. Replace the jumper. This reestablishes the connection between EEPROM and the Cypress chip.

5. Connect the USB cable. The LED next to the USB connector will not blink.

6. Run the software. It should find the evaluation board and allow you to flash it. If the USB programmer software does not find the evaluation board, locate a file called DriverGuide.mht, which is located in the same directory as the USB programmer software, that is, C:\Program Files (x86)\Analog Devices\USB Eval Board Programmer\DriverGuide.mht.

   This file contains step-by-step instructions for using the Windows Device Manager in the event that the evaluation board is identified by Windows as an unknown USB device.

7. Select AD9547/**48 Eval Board (32/64-bit)**. The software should indicate successful programming.

8. Disconnect the USB cable and power cycle the board.

9. Connect the USB cable to the 64-bit machine. The USB status LED (CR3) should blink after Windows completes loading the USB drivers. If Windows prompts for the location of the USB drivers, select **Install from the default location**.

PLL QUICK START

Once the evaluation software is installed, the evaluation board is connected, and the software is loaded, follow the steps in this section to configure and lock the PLL. These steps assume that the input signal is present, the evaluation board has not been modified, and that the digital PLL loop filter is suitable for the application.

This quick start guide covers only simple PLL operation to get the PLL up and running. See the AD9548 data sheet and the Evaluation Software Components section of this user guide for a detailed explanation of the various AD9548 features including

- 1 GHz system clock: 50 MHz crystal with doubler and feedback divider = 10 (÷ N)
- Input frequency: differential 19.44 MHz on REFA
- Output frequency: 161.1328125 MHz
- Loop bandwidth: 10 kHz
- 3rd pole location: 200 kHz
- Phase margin: 88°
- DPLL reference divider: 27
- DPLL feedback divider: 223 + 611/768

CONFIGURATION

Configuring the device consists of configuring the

- System clock
- Digital PLL (DPLL)
- DPLL reference inputs
- Output drivers
- Status pins (optional)

The configuration steps are detailed in the subsections that follow.

Configure the System Clock

1. Click **Click for Details** in the **DPLL Configuration** portion of the AD9548 **Blocks** window and select the **System Clock** tab.
2. Select **Xtal Input**.
3. Enter 50 (**MHz**) for the **External Clock**.
4. Check **Clock Doubler**.
5. Enter 10 as the **Feedback Divide ÷ N** ratio.
6. Click **LOAD** and then click **Calibrate System Clock**.
7. To ensure that the system clock is running, click **Refresh** on the AD9548 **Blocks** window. When the status window appears, green boxes labeled **Locked** and **Stable** should appear in the **System Clock** portion of the window.

Configure the Digital PLL

1. Select the **DPLL** tab on the **DPLL Configuration** window (see Figure 9).
2. Click **Free Running** in the **Frequency** section of the window. Enter the desired free running frequency (161.1328125 MHz in this case) and click **LOAD**.
3. Select the **Profiles** tab on the **DPLL Configuration** screen and click **Design a New Profile**. Microsoft Excel® loads the profile designer worksheet.
4. Ensure that macros are enabled.
5. Enter the following values in Cells C14, C15, C16, and C17: R = 27, S = 223, U = 611, and V = 768. These are the feedforward and feedback divider ratios for the example.
6. Enter a loop bandwidth of 1 kHz, a phase margin of 88°, and a 3rd pole offset of 200 kHz.
7. Click on the **Save** tab, and click on **Save Profile File**.
8. Return to the AD9548 Evaluation Software Profile Summary screen and click **Load Profile Setup**.
9. Select **FDProfile0.psu** and click **Open**.

Configure the Reference Inputs

1. Click the **Reference Inputs** tab under **DPLL Configuration** window.
2. Select **Profile 0** for Reference A under **Manual Profile Assignment**.
3. The default value of differential is already selected for this application. Note that you can connect a 0 dBm signal generator or a single-ended LVPECL input to the J14 connector and leave J13 open, if desired.
4. Click **LOAD** to have the register values take effect.

Configure the Output Drivers

1. Click **Click for Details** in the **Clock Distribution** portion of the AD9548 **Blocks** window.
2. Click **Enable Output** on Output 0 and Output 1, and select **LVPECL** for Output 0 and **+CMOS/−CMOS** for Output 1.
3. Click **LOAD** and then click **Synchronize Distribution**. You should now see the free running frequency at the output, or a 161 MHz output that is phase locked to the 19.44 MHz input if a valid reference input signal is present.
4. To check to make sure the DPLL is locked, click **Refresh** on the Status portion of the on the AD9548 **Blocks** window. The DPLL mode will be locked if the DPLL is locked.

# EVALUATION SOFTWARE COMPONENTS

MAIN SCREEN
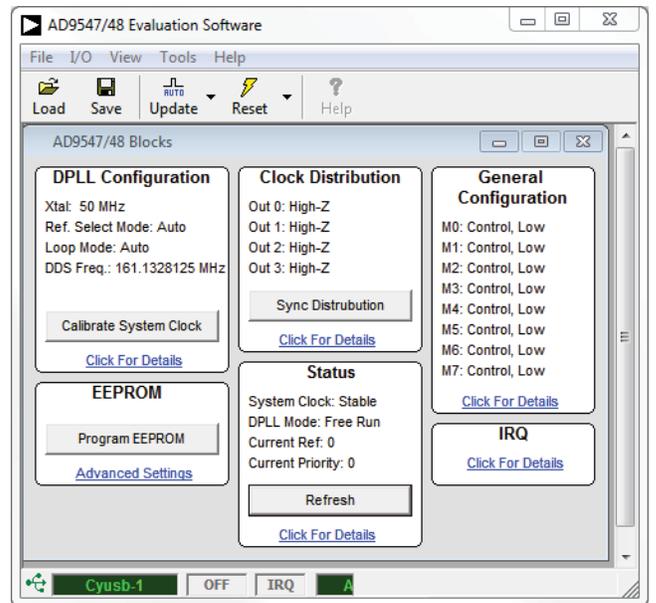
Figure 4. AD9548 Evaluation Software Main Window
(Also Referred to as the AD9548 Blocks Window)

The AD9548 evaluation software is comprised of subsections that correspond to the AD9548 major functional blocks. These subsections are described within this section of the user guide, and each subsection has its own window. From the main window, each functional block can be accessed by clicking on the appropriate block.

If an evaluation board is not communicating with the evaluation software, **Cyusb-1** (in the lower left corner of the window) changes to **Not Connected**. To have the evaluation software search for an evaluation board that was just connected, select the evaluation board from the **I/O** menu.

If status polling is enabled, **Status** (left of center, bottom) blinks. Status polling allows the AD9548 software to continuously monitor the status of the AD9548 evaluation board.

If an interrupt request (IRQ) occurs, **IRQ** (center bottom) turns orange until the IRQ is cleared.

To reset the AD9548 evaluation board, click **Reset** on the tool bar.

DPLL CONFIGURATION WINDOW

The AD9548 DPLL configuration has five main components: the DAC system clock (also referred to as the sysclk), the operational controls, profile management, DPLL free-run and holdover control, and reference input configuration.

System Clock Configuration
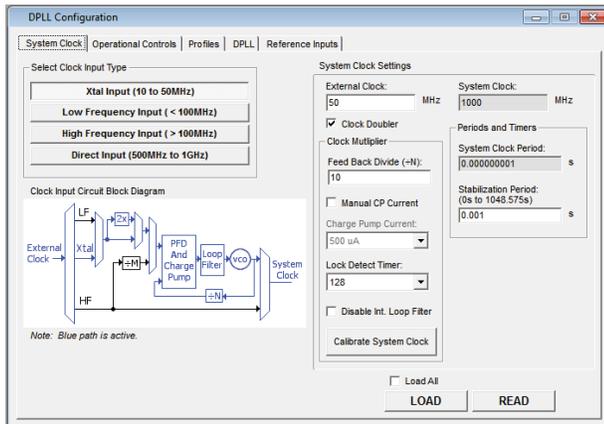
Figure 5. DPLL System Clock Configuration Window

The window shown in Figure 5 is accessed by clicking the **System Clock** tab. This window is used to configure the system clock PLL which accepts a low frequency input signal and multiplies it to 900 MHz to 1000 MHz.

Select **XTAL Input (20 to 50 MHz)** if you intend to connect a crystal to the reference input. The default configuration is a 50 MHz crystal, but you can use a crystal in the 10 MHz to 50 MHz range.

Low Frequency Input is intended for input less than 100 MHz.

High Frequency Input is intended for input greater than 100 MHz. If the system clock input frequency is 100 MHz, you are encouraged to experiment with both the low and high frequency setting to determine optimal performance.

Direct Input bypasses the system clock PLL and is intended for input greater than 500 MHz.

The system clock PLL doubler (**Clock Doubler**) can be used to reduce the phase noise in the 100 kHz offset region. However, make sure the input duty cycle is as close to 50% as possible, and the frequency going into the doubler is not be more than 75 MHz.

The **Feedback Divider (÷N)** is the clock multiplication ratio; this value should be chosen such that the resulting system clock frequency is 900 MHz to 1000 MHz.

Disable the internal loop filter (**Disable Int. Loop Filter)** by checking the appropriate box in cases when you design an external analog loop filter for the DAC system clock PLL.

The system clock PLL lock detect timer is for cases where you want to increase the number of consecutive phase detector edges within a threshold before declaring that the system clock

PLL locked. It is typically changed only in cases where a very precise, low frequency oscillator (like an OCXO) requires additional time to stabilize.

In most cases, the remainder of the system clock PLL settings can be left at their default values.

To enable the system clock PLL, initiate the system clock PLL calibration after configuring it. System clock PLL calibration only needs to be run once, unless you change the system clock PLL configuration or system clock input.

Operational Controls
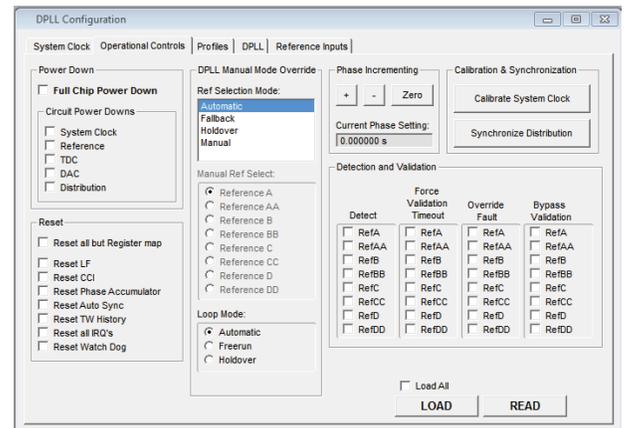
Figure 6. Operational Control Window

The **Operational Controls** window shown in Figure 6 has seven sections. It is opened by clicking the **Operational Controls** tab on the **DPLL Configuration** window. The loop mode section of this window is used frequently to select the mode of the digital PLL.

This window allows the user to control power down, reset, automatic reference selection, DPLL operating mode, closed-loop phase offset, and forced validation of reference inputs.

The DPLL **Ref. Selection Mode** has four settings: **Automatic**, **Fallback**, **Holdover**, and **Manual**. These modes are described in the Reference Switchover section of the AD9548 data sheet.

In automatic mode, the PLL is in free run mode until there is a valid reference, at which point it will lock to that reference. In cases where more than one reference is valid, it obeys the priority scheme defined in the profile setup.

In fallback mode, the PLL locks to the reference input selected by the user if that reference is valid. If the selected reference is invalid, it obeys the priority scheme defined in the profile setup.

The manual mode of the DPLL reference selection is useful in cases where the user wants to force the DPLL to use a given reference input regardless of its priority and validity.

A slight variation on this is holdover mode, in which the DPLL uses a given reference if it is valid, and uses holdover if it is not valid.

The AD9548 has three settings for its loop mode: **Automatic**, **Freerun**, and **Holdover**. In automatic mode, the PLL locks to a valid reference input if one is present. In free run mode, the PLL behaves like a DDS synthesizer and outputs the frequency programmed into the free running frequency (see the DPLL Free Run and Holdover Control (DPLL) section). Holdover mode forces the AD9548 to behave as though all reference inputs are invalid.

The **Phase Incrementing** section allows you to vary the static phase offset of the DPLL while the loop is locked. This is in contrast to the free running phase control (in the **DPLL** tab) which controls the phase offset in free run mode.

The **Calibration & Synchronization** buttons allow you to calibrate the system clock VCO and synchronize the clock distribution block, respectively. The system clock PLL must be calibrated after its configuration. Output synchronization must be performed once, and only after there is a signal present at the input to the clock distribution section.

Profile Manager (Profiles)
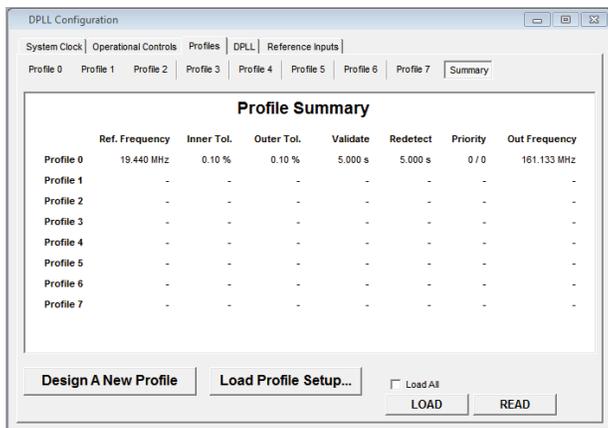
Figure 7. DPLL Profile Summary Window

The DPLL **Profile Summary** window shown in Figure 7 has nine tabs. It is opened by clicking the **Profiles** tab on the **DPLL Configuration** window.

The nine tabs correspond to the eight DPLL profiles, as well as a **Summary** tab. The easiest way to enter information in the DPLL profile is to follow the instructions in the Digital PLL Profile Designer Spreadsheet section.
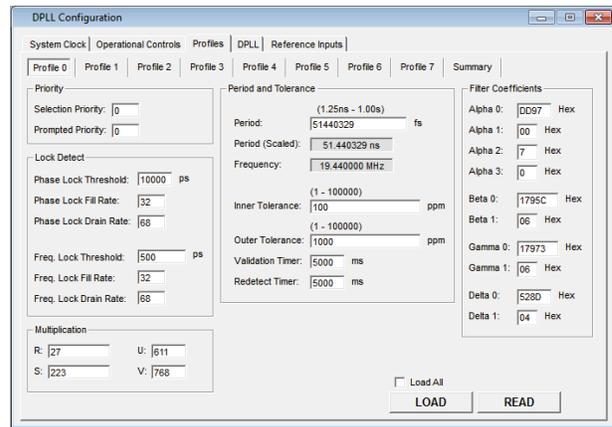
Figure 8. Individual Profile Configuration Window

Click on an individual profile to display the **Individual Profile Configuration** window (see Figure 8) for editing profile settings manually.

Changing values in this window does not update the corresponding partial setup (.psu) files generated by the profile designer spreadsheet. Therefore, Analog Devices, Inc., recommends that you make the corresponding changes in the profile designer spreadsheet. This avoids differences between the psu files and the actual setup. In addition, the profile designer has internal checking to avoid invalid settings.

DPLL Free Run and Holdover Control (DPLL)
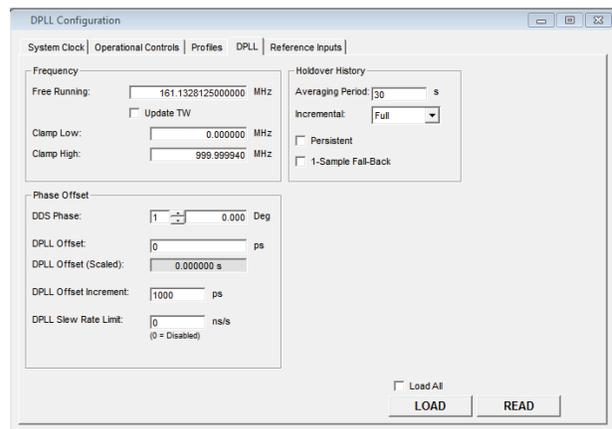
Figure 9. DPLL Configuration Window

The **DPLL Free Run and Holdover Control** window shown in Figure 9 is opened by clicking the **DPLL** tab on the **DPLL Configuration** window. Set the free run frequency, the phase offset, and holdover history using this window.

The **Frequency** section allows you to enter the free running frequency. Double-click within the **Frequency** section to open the window shown in Figure 10.
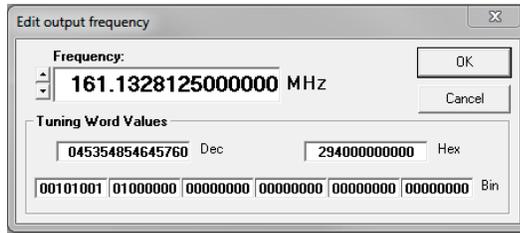
Figure 10. Edit Output Frequency Window

After entering the frequency and clicking **OK**, the **Phase Offset** section of the **Edit Phase Offset** window allows you to vary the phase of the DDS output. There are five items in this menu: DDS Phase, DPLL Offset, Scaled DPLL Offset, DPLL Offset Increment, and DPLL Slew Rate Limit. These are described in detail in the AD9548 data sheet.

DDS Phase controls the output phase in free running mode. Double-clicking on the box holding the value of the **DDS Phase** setting box opens the window shown in Figure 11.
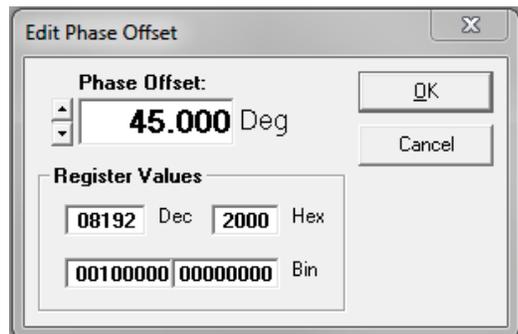
Figure 11. Edit Phase Offset Window

Three other settings (DPLL offset, scaled DPLL offset, and DPLL offset increment) apply when the DPLL is active and tracking the reference input.

The DPLL slew rate limit applies when the DPLL is switching references.

Reference Input Configuration
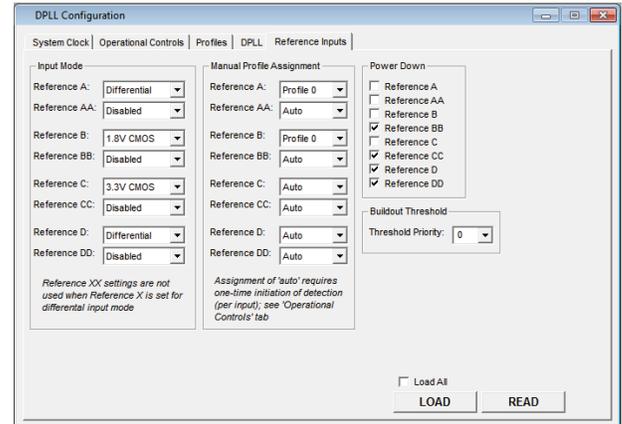
Figure 12. Reference Input Configuration Window

Open the **Reference Input Configuration** window shown in Figure 12 by clicking on the **Reference Inputs** tab on the **DPLL Configuration** window. It is used to configure the input references.

The input mode allows you to set the logic type for a given reference input. When using single-ended inputs, remove R24 for Reference A/Reference AA (or R23 for Reference B/Reference BB). R23 and R24 are 100 Ω resistors intended for differential environments. It is important to note that the decoupling capacitors labeled C39, C40, C41, and C42 should be removed for reference inputs frequencies that are < 10 MHz and be replaced with zero Ω resistors.

The manual profile assignment bypasses the automatic frequency detection and automatic profile assignment by the DPLL logic. This can be a handy way to eliminate possible setup errors during debugging.

The phase master threshold priority value is set by changing the **Threshold Priority** in the **Buildout Threshold** section of this window. This feature allows you to set up a phase master, and is described in detail in the Phase Build-Out Reference Switching section of the AD9548 data sheet.

CLOCK DISTRIBUTION MENU
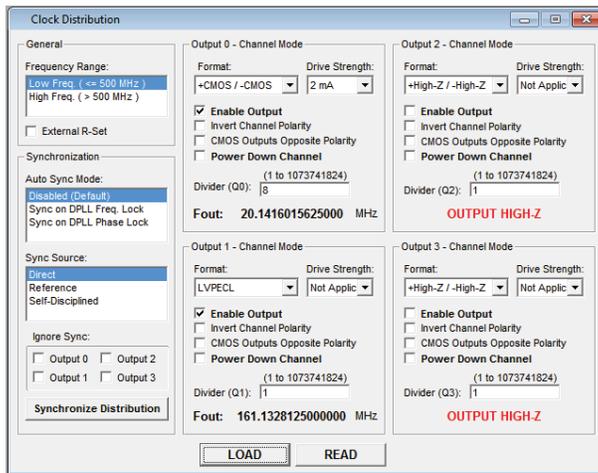
Figure 13. Clock Distribution Window

The **Clock Distribution** window shown in Figure 13 is accessed by clicking on the **Clock Distribution** box on the AD9548 **Blocks** window, or by clicking on **Clock Distribution** on the **View** menu. This window allow you to configure the output drivers and post dividers.

It is important to leave unused outputs disabled on the evaluation board because they can be a major source of unwanted spurs.

The AD9548 evaluation board output driver terminations are configured for differential (LVPECL and LVDS) configuration. If an output is configured as single-ended CMOS, remove R12 (for OUT0), R15 (for OUT1), R16 (for OUT2), or R25 (for OUT3). In addition, remove the decoupling capacitors for output frequencies < 10 MHz.

It is important to note that you must click on **Synchronize Distribution** after a valid clock is sent to the distribution section or no clock output will be toggling. **Auto Sync Mode** can be set to perform this synchronization automatically.

Sync Source controls the source of the synchronization. This feature is described in the Clock Distribution Synchronization section of the data sheet.

GENERAL CONFIGURATION
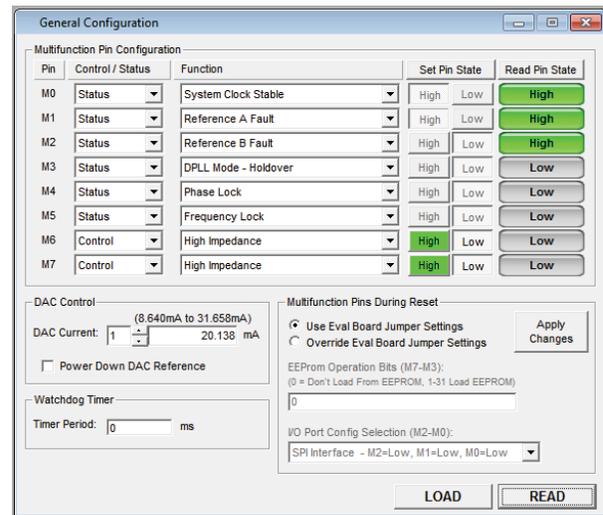
Figure 14. AD9548 General Configuration Window

The **General Configuration** window shown in Figure 14 is accessed by clicking on the **General Configuration** box on the AD9548 **Blocks** window, or by clicking **General Configuration** on the **View** menu. It allows you to configure the multifunction pins and serial port configuration.

The upper left portion of this window allows you to configure the multifunction pins **M0** to **M7**. You can choose whether these pins are a control (input) or a status (output), and which function the pin is to perform. After setting the desired function, click **LOAD** at the bottom of the window.

You can now click on **Set Pin State** or **Read Pin State** to set or read the state of the M0 to M7 pins, respectively. The LEDs next to the USB connector can be used to monitor the status of the M0 to M7 pins. If the M0 to M7 LEDs are not working, ensure that R61, adjacent to the USB connector, is removed. You may need to remove the M0 to M7 jumpers to the left of the AD9548 device because early versions of the evaluation board have 1 kΩ pull-down resistors in positions R45 to R58, which draw too much current for the AD9548 to drive high.

The **DAC Control** section of this window allows you to control the amount of current flowing out of the DDS DAC output. It is normally left at 20.1 mA. However, it can be increased if you require greater output amplitude.

The watchdog **Timer Period** setting (if used) can be entered in the **Watchdog Timer** section of this window. The watchdog timer is a user programmable timer that can be set to generate an interrupt (or activate a multifunction pin) on a regular interval. Its operation does not affect the rest of the AD9548 operation.

The **Multifunction Pins During Reset** section of this window is used to control the serial port selection and multifunction pin operation of the AD9548.

EEPROM CONTROL WINDOW

There are two tabs on the **EEPROM Control** window: **Simple** and **Advanced**.

Simple EEPROM Programming Mode
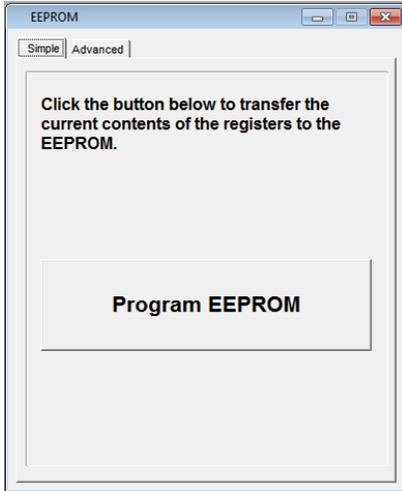
Figure 15. *AD9548* EEPROM Control Window

The **EEPROM Control** window, shown in Figure 15, is accessed by clicking the **EEPROM** box on the AD9548 **Blocks** window, or by clicking on the **EEPROM** window on the **View** menu.

To store the current register settings of the AD9548 to the EEPROM, click **Program EEPROM**.

To load the values stored in the EEPROM, ensure that the appropriate M0 to M7 pin is pulled high and reset the AD9548. See the AD9548 data sheet for more details on EEPROM programming

Advanced EEPROM Programming Mode
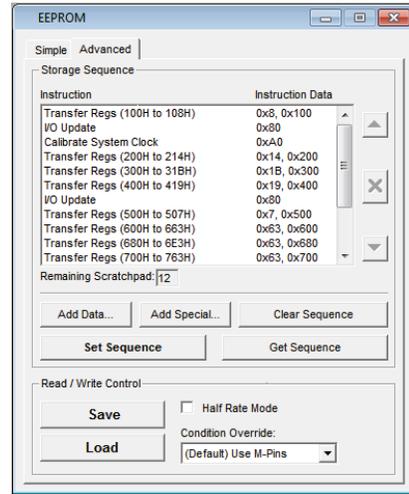
Figure 16. *AD9548* EEPROM Control Window

The **Advanced EEPROM Control** window shown in Figure 16 is accessed by clicking the **EEPROM** box on the AD9548 **Blocks** window and then selecting the **Advanced** tab.

STATUS WINDOW
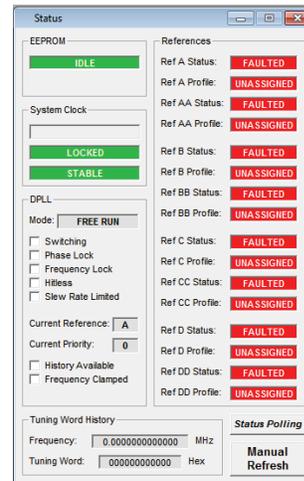
Figure 17. Status Window

The **Status** window, shown Figure 17, is accessed by clicking on the **Status** box on the AD9548 **Blocks** window, or by clicking on the **Status** window on the **View** menu.

INTERRUPT REQUEST (IRQ) WINDOW
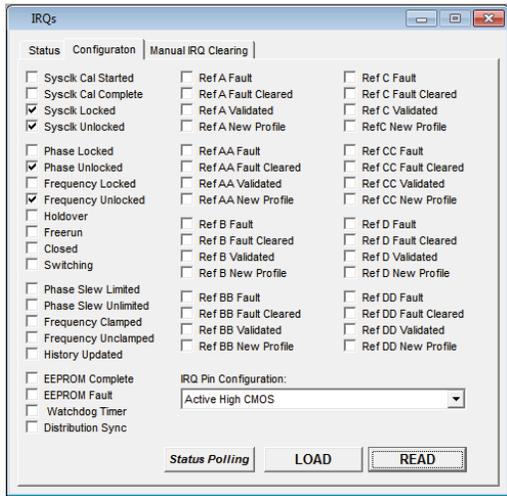
Figure 18. IRQ Window

The **IRQ** window, shown in Figure 18, is accessed by clicking on the **IRQ** box on the AD9548 **Blocks** window, or by clicking on **IRQ Window…** on the **View** menu.

To use the IRQ function on the evaluation board, change the **IRQ Pin Configuration** to **Active High CMOS** mode. The IRQ indicator at the bottom of the AD9548 evaluation software main window turns orange when an IRQ has occurred.

TUNING WORD LOGGER WINDOW
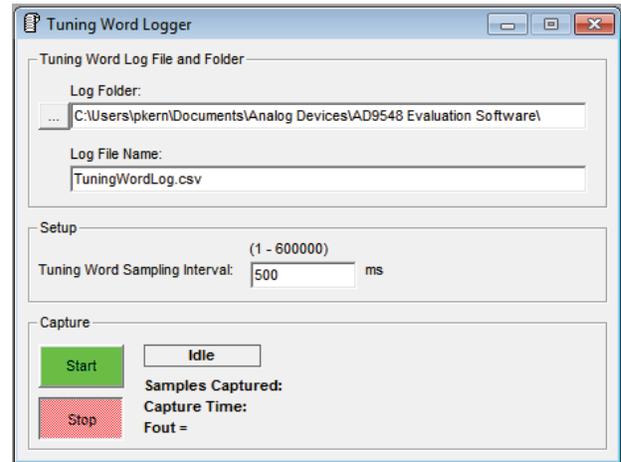
Figure 19. AD9548 Channel Divider Window

The **Tuning Word Logger** window, shown in Figure 19, is accessed by clicking **Tuning Word Logger…** on the **Tools** menu.

The tuning word logger records the DDS tuning words (which directly correspond to the AD9548 DDS output frequency) at a user-defined interval.

EVALUATION SOFTWARE MENU ITEMS

MENU BAR

File

Load Setup

Selecting **Load Setup** loads a previously saved AD9548 setup file (.stp). A setup file is a text file that contains the AD9548 register setup file, plus any evaluation board settings.

Save Setup

Selecting **Save Setup** saves an AD9548 setup file (.stp). A setup file is a text file that contains the AD9548 register setup file, plus any evaluation board settings.

Options

Select **Options** to bring up the windows shown in Figure 20 and Figure 21. These options are seldom changed. Status polling can occasionally cause problems on older systems; it should be disabled in these cases.
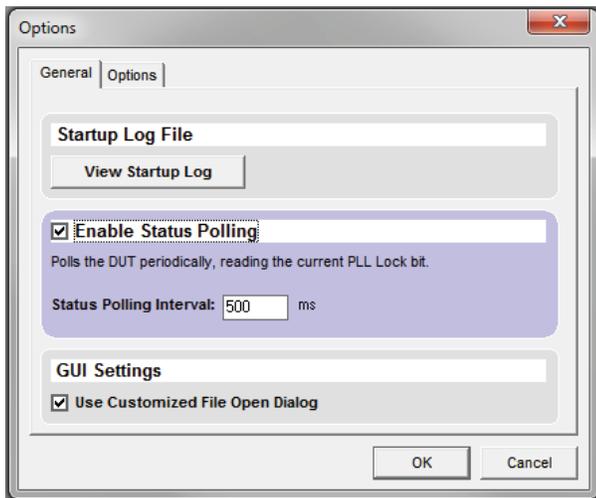
Figure 20. Evaluation Software, General Options
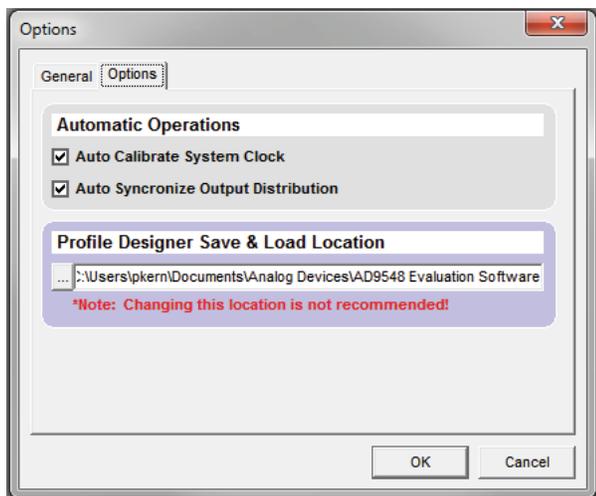
Figure 21. Evaluation Software, Other Options

Exit

Exits the evaluation software.

Note that no checking is done to ensure that the existing setup is saved.

I/O

Select Evaluation Board

The AD9548 evaluation system allows one PC to control multiple evaluation boards. This window allows the user to select which evaluation board the software is controlling. Click **Refresh List** to have the software detect a recently connected evaluation board.
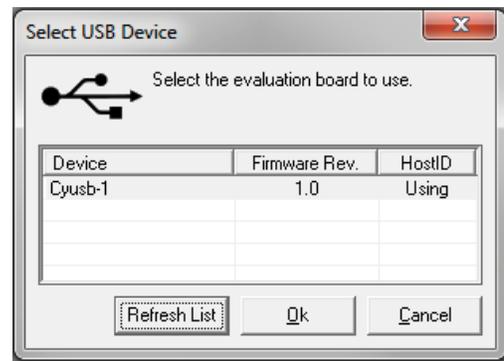
Figure 22. USB Device Selection

Configure Serial Port

This window allows the user to control how the USB controller interacts with the AD9548 serial port.
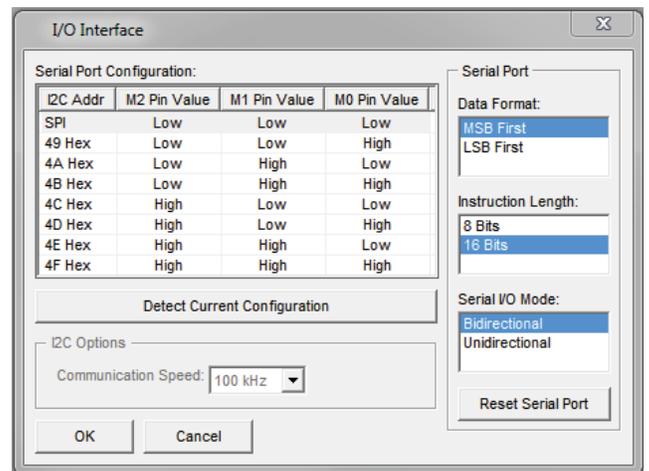
Figure 23. USB Device Selection

If you are using I²C mode, this window allows you to select which address to use. Note that the address should correspond to the jumper settings M0, M1, and M2 on the evaluation board. You can also click on **Detect Current Configuration** to have the evaluation software discover which I²C address is active.

However, if you are attempting to program an AD9548 on a remote board via a header cable from Connector P1, then the I²C address of the on-board AD9548 must not match the I²C address of the remote AD9548 that you are attempting to program.

View

Debug

This window allows you to write and read registers directly as well as force the various configuration pins high and low.
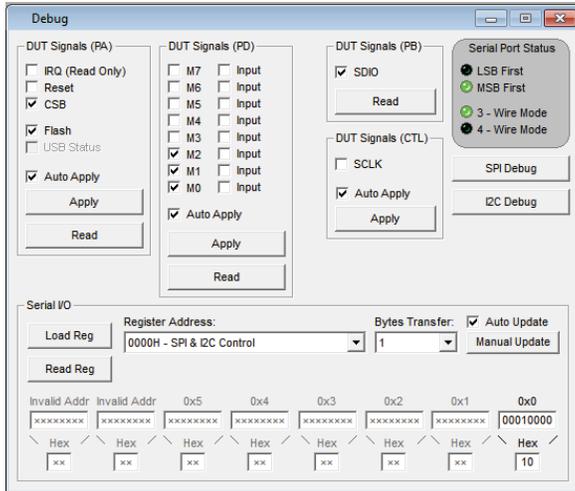
Figure 24. Debug Window

The **Debug** window shown in Figure 24 is accessed by clicking **Debug** from the **View** menu.

Register Map Values Menu
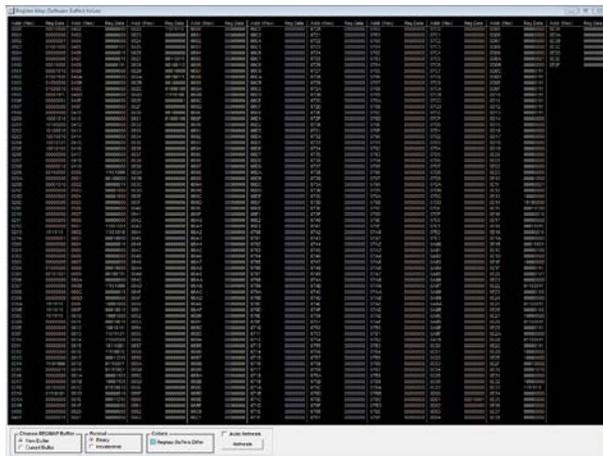
Figure 25. Register Map Values Window

This window is a handy way to view all AD9548 registers in a tabular format.

Choose either **New Buffer** or **Current Buffer** in the **Choose REGMAP Buffer** box at the bottom of the window. **Current Buffer** allows you to see the values currently active in the chip. **New Buffer** allows you to see the values that will take effect when the next register update occurs.

Format allows you to choose either binary or hexadecimal format for the register values.

Register Map Debug Menu
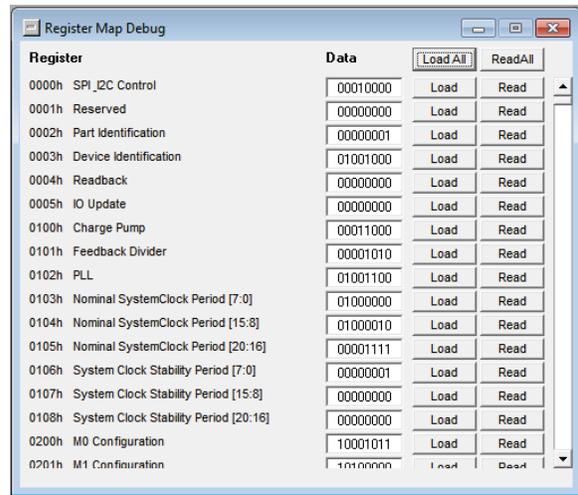
Figure 26. Register Map Debug Window

The **Register Map Debug** window shown in Figure 26 is accessed by clicking on the **View/Register Debug** window from the menu bar. This screen allows you to easily modify individual registers.

Tools

Selecting **Tools** opens the menu for opening the **Tuning Word Logger.**

Help

Selecting **Help** opens the **About** AD9548 splash screen. This screen contains information such as revision number, region information, contact information, and so on.

DIGITAL PLL PROFILE DESIGNER SPREADSHEET

The AD9548 evaluation software relies on an Excel worksheet for calculating loop filter coefficients. Clicking **Design A New Profile** opens the digital loop filter design spreadsheet.

Macros must be enabled when using FilterDesign.xls. However, the evaluation board does not need to be connected to the PC to access this worksheet. In addition, you must enable the **Analysis ToolPak** and **Analysis ToolPak VBA** add-ins. These are enabled by selecting **Add-Ins** from the Excel **Tools** menu.

There are four tabs in the worksheet: the **Profile** tab is where you enter the desired loop filter parameters. The **Transfer Plot** tab allows you to see a graph of the DPLL transfer function. The **Registers** tab allows you to easily see the register values calculated by the software. The **Save** tab is for exporting the design to the evaluation software.

The AD9548 supports up to eight digital PLL profiles. Each profile is a set of PLL parameters.

This spreadsheet calculates the digital loop filter coefficients from the following ten inputs:

- Profile priority
- System clock
- Reference (input) frequency
- R-divider (reference input divider)
- S-divider (feedback divider)
- Fractional division ratio (if necessary)
- Location of loop filter 3rd pole
- Loop bandwidth
- Desired phase margin
- Validation timers

Input the desired values in the outlined boxes (Cell C3 to Cell C38) on the **Profile Sheet** tab. Cell G3 to Cell H38 contain the allowed minimum and maximum for each value, and these are updated as values are entered. If an input cell is out of range, the offending cell displays a red outline. If that happens, refer to the G and H columns for the allowable range for that parameter.

Once the desired values are chosen, you can switch to the **Save** worksheet tab. If you like, enter an optional comment. Then, choose one of eight profiles and click on **Save Profile File**. This writes a .psu (partial setup file) called FDProfileX.psu (where X is 0 to 7 corresponding to Profile 0 through Profile 7) to the same directory where the evaluation software is located. You can then switch back to the AD9548 evaluation software and click **Load Profile Setup** at the bottom of the **Profile Summary** window.

In the example in the Quick Start Guide to the AD9548 PLL section, a deliberately difficult case was chosen to illustrate the internal checking of the profile designer. Typically, the entry of new values is very straightforward.

Refer to the AD9548 data sheet for details on each of these parameters, as well as the formula used to calculate the loop filter coefficients. The remainder of this section covers some of the less obvious parameters in more detail and, where necessary, uses the following configuration as an example:

System clock:	1 GHz
Input frequency:	Differential 19.44 MHz on REF1
Output frequency:	161.1328125 MHz
Loop bandwidth:	10 kHz
3rd pole location:	200 kHz
Phase margin:	88°
Reference divider:	27
Feedback divider:	223 + 611/768

CALCULATING FRACTIONAL-N DIVIDE RATIOS

The AD9548 fractional divide capability is governed by the equation

$$N = S + U / V$$

In this equation, N is the overall feedback divide ratio. Therefore, when using this formula, express the desired feedback ratio as a mixed number. This is easily accomplished in Excel.

The first requirement in frequency planning is to make the phase detector frequency < 10 MHz. Therefore, the R divider must be at least 2. In the 19.44 MHz to 161.1328125 MHz example, using an R divider of 27 allows the AD9548 to generate 161.1328125 with zero PPM error.

To verify this, you can divide 161.1328125/19.44 × 27 to get 223.795. Then, format this cell in Excel as a 3-digit fraction (223 611/768). You can then crosscheck that this ratio is perfect and results in zero ppm error. Some experimentation may be necessary to determine which R divider (if any) will allow you to generate a given frequency with zero PPM error.

The AD9548 can use very large R divider ratios with the only limitation that the loop bandwidth must not be larger than the phase detector frequency divided by 20. In this example, the maximum loop bandwidth is 36 kHz because the phase detector frequency is 720 kHz.

DIGITAL FILTER 3RD POLE LOCATION

The AD9548 profile designer allows you to specify the location of the 3rd pole in the digital PLL transfer function. In general, the 3rd pole location depends on any phase margin or peaking requirements of the digital PLL. In most cases, the 3rd pole location is at least a factor of 10 above the loop bandwidth, and may need to be a factor of 20 or greater for cases where a very flat transfer function is required. The profile designer alerts you (by turning a cell red) if you placed the 3rd pole too close for the specified phase margin requirement to be met.

In the example above, in order to have 88° of phase margin, the 3rd pole must be placed at its maximum of 720 kHz.

CHOOSING THE PHASE MARGIN

In many communication applications, a PLL transfer function with < 0.1 dB of peaking is required. To achieve this, enter at least 88° of phase margin. If you want to have a loop with less damping, a phase margin of 50° to 60° works well. Phase margins of < 40° should generally be avoided, to minimize the occurrence of stability issues.

AD9548 FREQUENCY PLANNING

The AD9548 has tremendous flexibility thanks to its programming of DAC system clock frequency, phase detector frequency, and output frequency. Certain frequency combinations result in better performance than others.

In general, the best performance is achieved when the DAC system clock is not running at an integer multiple of F_{OUT}. This is an easy situation to avoid when using the system clock PLL, because the system clock can be easily adjusted within the 850 MHz to 1000 MHz region by adjusting the system clock PLL, and carefully choosing the frequency of the oscillator driving the system clock PLL.

The second situation to avoid (in non-GPS cases) is having the system clock frequency as a multiple of DPLL phase detector frequency. Once again, this is an easy situation to avoid because the AD9548 offers tremendous flexibility in its feedback divider (including fractional-N modes) as well as the ability to run the phase detector as low as 1 Hz. The reason that the 1 PPS GPS case is excluded is that it is difficult to avoid having the system clock run at an integer multiple of 1 Hz.

RECONSTRUCTION FILTER

The [AD9548](#) evaluation board has a 240 MHz differential low-pass reconstruction filter as shown in Figure 26. The DPLL output frequency can be up to 250 MHz using this filter. Contact Analog Devices if a higher output frequency configuration is needed. This filter has a transformer on both sides to maximize common-mode rejection. The transformer used is a Mini Circuits ADTT-1 with a −3 dB bandwidth of approximately 0.3 MHz to 300 MHz.

In many applications, a single-ended, 5th-order filter is acceptable, especially if the output frequency is < 200 MHz.

DIFFERENTIAL FILTER DESIGN

Differential filters offer higher performance and better common-mode rejection than single-ended filters. The 100 Ω

differential source impedance is internal to the IOUT/IOUTB driver. In addition, the ac-coupling between IOUT differential pair and FDBK_IN differential pair is critical. Component matching between the corresponding LC sections is important in this design.

The 240 MHz 7th-order elliptical differential low pass filter offers

- Pass-band frequency of 240 MHz
- Pass-band ripple of 1.0 dB
- Stop-band ratio of 1.3
- Stop-band frequency of 312 MHz
- Stop-band attenuation of 70 dB
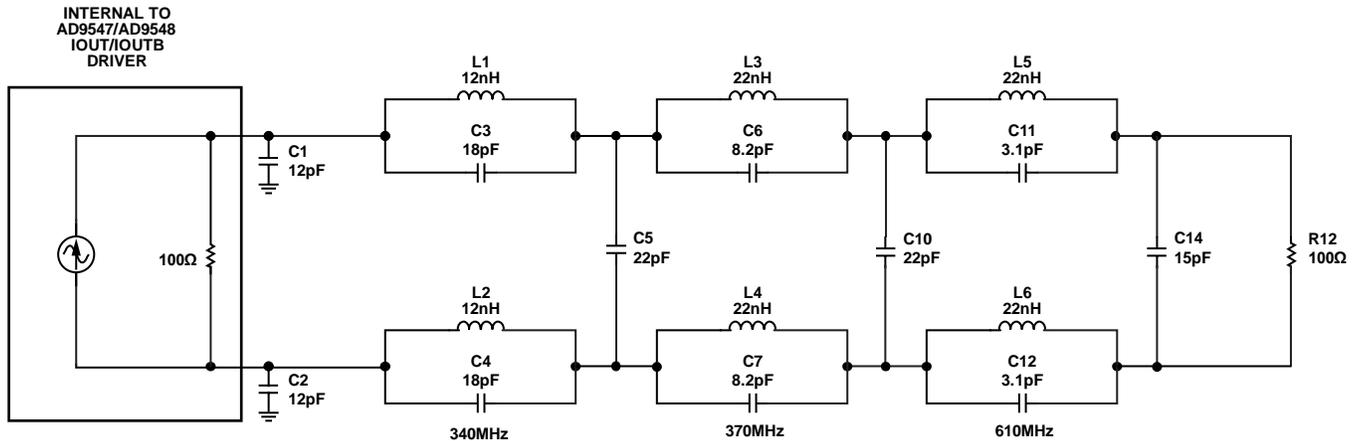
Figure 27. Default 240 MHz Differential Low-Pass Reconstruction Filter
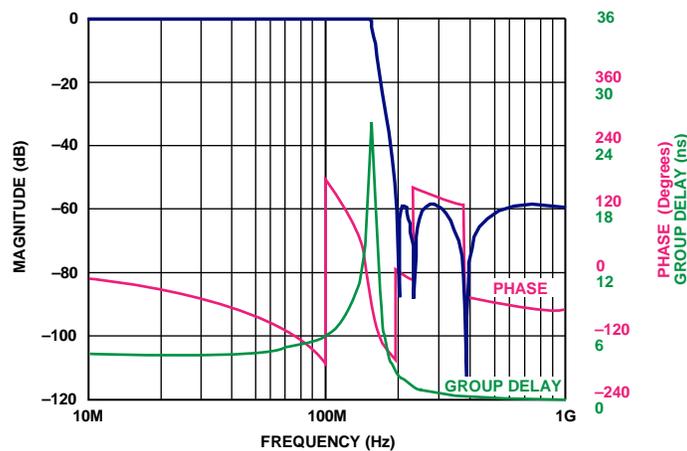
Figure 28. Frequency Response of Differential Reconstruction Filter Shown in Figure 25

SINGLE-ENDED FILTER DESIGN

The single-ended design with transformers used fewer components than the differential design. Contact Analog Devices for information regarding the best choice for your application.

The 5th-order single-ended low-pass elliptical filter offers

- Pass-band frequency of 150 MHz
- Pass-band ripple of 0.1 dB
- Stop-band ratio of 1.3
- Stop-band frequency of 195 MHz
- Stop-band attenuation of 45 dB
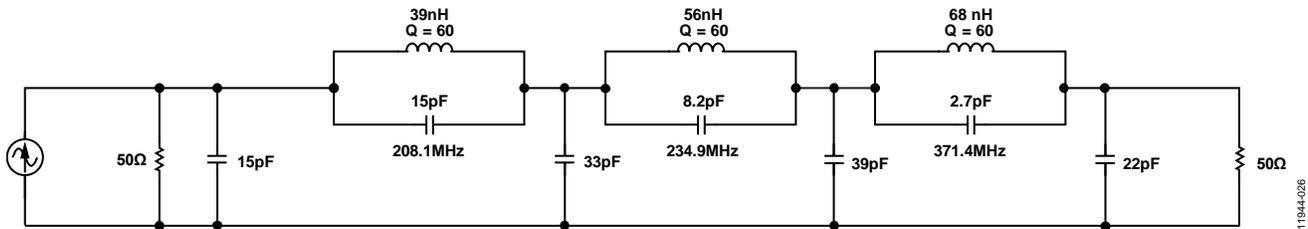
Figure 29. Evaluation Board Default Single-Ended Reconstruction Filter
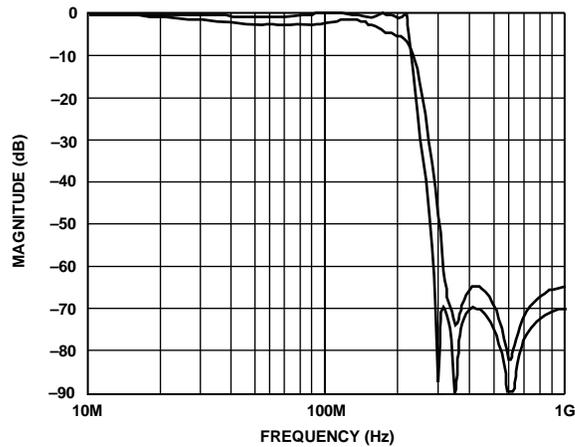
Figure 30. Frequency Response of Single-Ended Reconstruction Filter Shown in Figure 26

PROGRAMMING AN AD9548 ON A CUSTOMER BOARD

This user guide describes how to use an AD9548 evaluation board to program an AD9548 on a customer board using the I²C interface. It assumes you have access to the I²C pins via a header on the target board, and that you know the assigned address of the target I²C device.

1. On Jumper P3, place a jumper block such that it straddles the center and left pins.

2. Move Jumper P10 to the center and left (I²C) pins.

3. Select the desired I²C address for the AD9548 evaluation board using the jumpers labeled M2 to M0.

   - M0 = M1 = M2 = Low is reserved for SPI mode.
   - This I²C address should not conflict with the I²C address of the target AD9548.

4. Attach a jumper cable from CSB/SDA pin of Header P6 of the evaluation board to the SDA pin on the target board.

5. Repeat Step 4 for both the SERIALCLK and ground pins on Header P6 of the AD9548 evaluation board to the SCL pin and ground pin of the target board, respectively. On the evaluation software, select **Configure Serial Port** from the **I/O** menu. This window is shown in Figure 31.
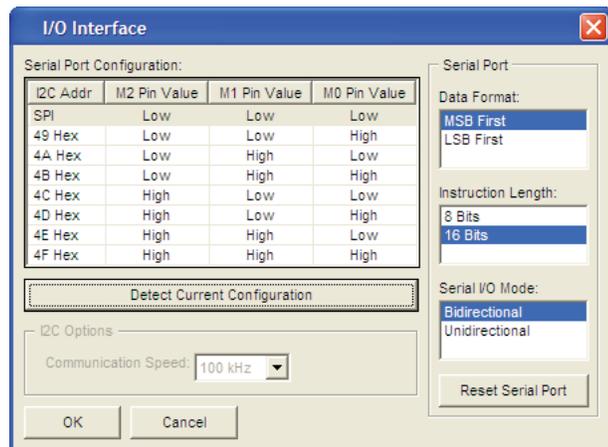
Figure 31. Serial Port Configuration

6. Click **Reset Serial Port** and then click **Detect Current Configuration**. A dialog box opens and acknowledges the I²C mode and address. The evaluation software starts at I²C Address 0x058 and stops at the first valid I²C address found. If the target I²C address is different from the one automatically selected, select the I²C address of the target AD9548 from the list, and click **OK**.

7. Click on the **View** menu, and select the **Debug** window. Then, click on **I²C Debug**. The window shown in Figure 32 opens.
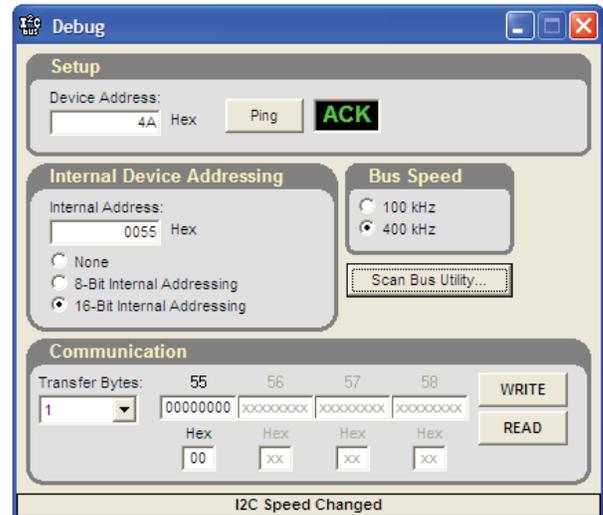
Figure 32. I²C Debug Window

8. Enter the I²C address set by Jumpers M2 to M0 on the AD9548 evaluation board, and click **Ping**. You should see a green **ACK** message as shown in Figure 32. Repeat this step for the I²C address of the target AD9548. If **ACK** is returned for both addresses, the remote AD9548 is ready to be programmed.

   If the ping test fails, double-check the cabling between the boards, as well as the I²C address of the target AD9548. Ensure that the I²C address of the AD9548 on the evaluation board is different from the target AD9548. Disconnect the jumper cable, and make sure that I²C mode is working properly on the AD9548 evaluation board.

9. Proceed to program the target AD9548 with the desired settings. When finished, you can access the EEPROM window by clicking **EEPROM**, and then clicking on **Program EEPROM** to write the settings to the EEPROM.

NOTES

NOTES

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ANALOG DEVICES

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