

The AD9552: A Programmable Crystal Oscillator for Network Clocking Applications

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The ubiquitous quartz crystal oscillator has been the workhorse of timekeeping applications for decades. Low cost, coupled with relatively high stability, is the driving force behind the success of the quartz crystal oscillator in a broad range of applications.

The high resonant Q factor makes the quartz crystal oscillator an attractive candidate for the resonant element in fixed frequency oscillators. However, an ever-increasing number of network clock applications require a stable, single frequency oscillator as a source for synthesizing different network frequencies. The AD9552 is a low cost, integrated solution for such applications.

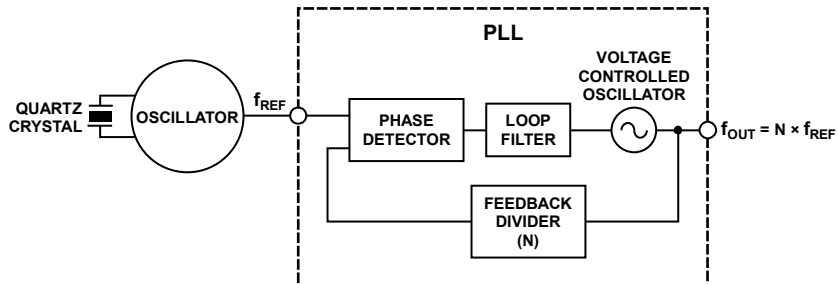


Figure 1. PLL-Based Frequency Upconverter

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FREQUENCY UPCONVERSION

The relatively low resonant frequency of a quartz crystal resonator (typically less than 50 MHz for fundamental mode resonance) is a shortcoming for network applications requiring an output frequency in excess of 100 MHz. The higher output frequency requirement of these applications implies the need for translating the relatively low output frequency of the basic crystal oscillator to a higher frequency, a process often referred to as upconversion. One of the most common upconversion methods involves the use of a phase-locked loop (PLL) with a frequency divider in its feedback path (see Figure 1). The output frequency (f_o) is given by

$$f_o = N \times f_{REF}$$

where:

N is the frequency divider value.

f_{REF} is the input frequency.

Generally, the bandwidth of the loop filter is relatively narrow in order to minimize spurious artifacts in the output spectrum. Furthermore, by making N programmable, the PLL upconverter solves the problem of producing different output frequencies from a single frequency source, namely a quartz crystal oscillator. This architecture is relatively easy to implement, especially if the feedback divider is only required to provide integer division factors.

The drawback to the architecture shown in Figure 1 is that the output frequency must be the same as or greater than f_{REF} .

To resolve this restriction, simply place a second programmable frequency divider at the output, as shown in Figure 2.

With the additional divider the output frequency is given by

$$f_o = (N/P) \times f_{REF}$$

where P is the output frequency divider value.

The architecture shown in Figure 2 allows for rational f_{OUT}/f_{REF} ratios (that is, one integer divided by another). Furthermore, for $P > N$, f_{OUT} is less than f_{REF} , which overcomes the aforementioned drawback. Note that in the previous architecture (Figure 1) there is a necessary harmonic relationship between f_{OUT} and f_{REF} because N is an integer. An unintentional benefit of the new architecture (Figure 2) is the elimination of this harmonic restriction. The same result is possible by placing the second divider at the output of the crystal oscillator instead of at the output of the PLL. Such an arrangement, however, means that the PLL design must accommodate a range of input frequencies rather than the single crystal oscillator frequency.

The architecture of Figure 2 satisfies any application for which the ratio, N/P , meets the required output/input frequency ratio. The amount of flexibility provided by this architecture depends on the range of N and P , that is, the larger the range of N and P , the more flexible the solution. There is a practical limit, however, to the range of N because the range of N determines the required frequency range of the voltage controlled oscillator (VCO). The wider the VCO range, the more difficult it is to design the VCO without sacrificing performance.

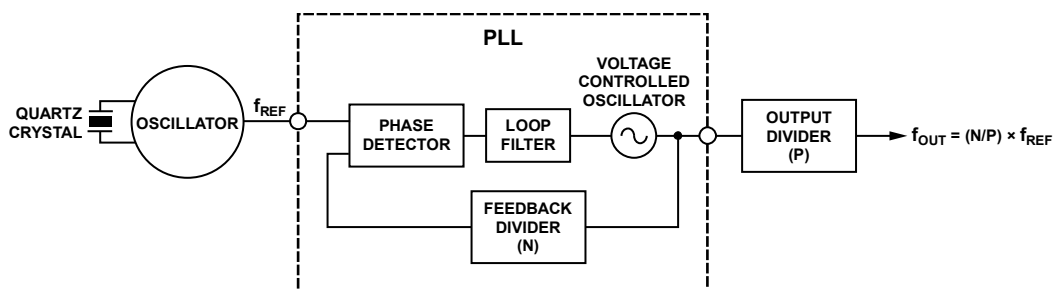


Figure 2. PLL-Based Frequency Upconverter with Output Divider

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THE AD9552 ARCHITECTURE

The AD9552 incorporates the basic architecture of Figure 2, but has a feedback divider capable of fractional divide values. A simplified block diagram of the AD9552 appears in Figure 3.

The AD9552 offers two programming methods. One is via a serial communication port that provides full control of the device settings. The other is via configuration selection pins that allow the user to select one of a predefined set of common network clock frequencies simply by pin strapping

the device (potentially eliminating the need for serial communication).

The AD9552 has nine configuration pins partitioned into a group of three (Pin A0 to Pin A2) and a group of six (Pin Y0 to Pin Y5). The A pins select 1 of 8 predefined reference frequencies (see Table 1), while the Y pins select 1 of 64 output frequencies (see Table 2). The configuration pins automatically set the appropriate internal divider values for generating the frequency at OUT1, as indicated in Table 2.

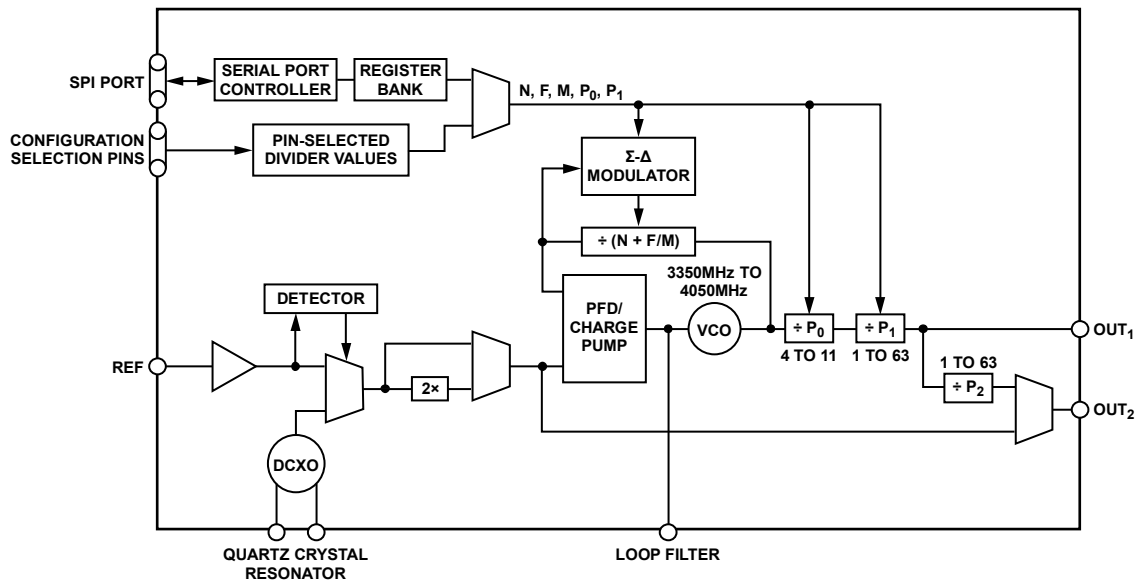


Figure 3. The AD9552 Crystal Oscillator and Frequency Up-Converter

Table 1. Pin Strapped Reference Frequency

A2	A1	A0	Reference Frequency (MHz)
0	0	0	10.00
0	0	1	12.00
0	1	0	12.80
0	1	1	16.00
1	0	0	19.20
1	0	1	19.44
1	1	0	20.00
1	1	1	26.00

Table 2. Pin Strapped Output Frequency

Y5	Y4	Y3	Y2	Y1	Y0	Output (MHz)	Y5	Y4	Y3	Y2	Y1	Y0	Output (MHz)
0	0	0	0	0	0	51.84	1	0	0	0	0	0	569.1964
0	0	0	0	0	1	54	1	0	0	0	0	1	622.08
0	0	0	0	1	0	60	1	0	0	0	1	0	624.7048
0	0	0	0	1	1	61.44	1	0	0	0	1	1	625
0	0	0	1	0	0	62.5	1	0	0	1	0	0	622.08(239/237)
0	0	0	1	0	1	66.666	1	0	0	1	0	1	629.9878
0	0	0	1	1	0	74.17582	1	0	0	1	1	0	640
0	0	0	1	1	1	74.25	1	0	0	1	1	1	641.52
0	0	1	0	0	0	77.76	1	0	1	0	0	0	625(66/64)
0	0	1	0	0	1	98.304	1	0	1	0	0	1	657.421875
0	0	1	0	1	0	100	1	0	1	0	1	0	657.421875(239/238)
0	0	1	0	1	1	106.25	1	0	1	0	1	1	622.08(15/14)
0	0	1	1	0	0	120	1	0	1	1	0	0	669.1281
0	0	1	1	0	1	125	1	0	1	1	0	1	622.08(255/237)
0	0	1	1	1	0	133	1	0	1	1	1	0	625(15/14)
0	0	1	1	1	1	155.52	1	0	1	1	1	1	670.8386
0	1	0	0	0	0	156.25	1	1	0	0	0	0	622.08(255/236)
0	1	0	0	0	1	159.375	1	1	0	0	0	1	625(66/64)(15/14)
0	1	0	0	1	0	161.1328125	1	1	0	0	1	0	625(255/237)(66/64)
0	1	0	0	1	1	10518.75/64	1	1	0	0	1	1	693.75
0	1	0	1	0	0	155.52(15/14)	1	1	0	1	0	0	622.08(253/226)
0	1	0	1	0	1	155.52(255/237)	1	1	0	1	0	1	657.421875(255/238)
0	1	0	1	1	0	167.6616	1	1	0	1	1	0	657.421875(255/237)
0	1	0	1	1	1	177.7371	1	1	0	1	1	1	716.5372
0	1	1	0	0	0	245.76	1	1	1	0	0	0	718.75
0	1	1	0	0	1	250	1	1	1	0	0	1	719.7344
0	1	1	0	1	0	311.04	1	1	1	0	1	0	748.0709
0	1	1	0	1	1	320	1	1	1	0	1	1	750
0	1	1	1	0	0	400	1	1	1	1	0	0	777.6
0	1	1	1	0	1	433.925	1	1	1	1	0	1	779.5686
0	1	1	1	1	0	531.25	1	1	1	1	1	0	781.25
0	1	1	1	1	1	537.6	1	1	1	1	1	1	625(10/8)(66/64)

Even though the context of this application note is the use of a crystal resonator, the AD9552 also provides an alternate input source. The user can connect a single-ended CMOS clock signal directly to the REF input pin of the AD9552 instead of using a crystal resonator.

The AD9552 offers two output clock signals, OUT₁ and OUT₂. OUT₁ is the primary output. OUT₂ is an auxiliary output that is programmable as an integer submultiple of the frequency at OUT₁ or as a copy of the frequency at the input to the phase-frequency detector (PFD) of the PLL.

The feedback divider of the AD9552 provides fractional division, but not to the exclusion of integer division. Fractional division offers a significant amount of flexibility because the frequency scale factor takes the form $N + F/M$ (where $F/M < 1$), instead of simply N as in Figure 1.

The benefit of fractional division is that it yields a much wider selection of VCO output frequencies (within the bandwidth of the VCO) for a given reference frequency. The reason is that the ratio, f_{VCO}/f_{REF} , must be an integer (N) for an integer-only PLL, but can be a fractional value ($N + F/M$) for a fractional PLL, which allows for a much larger set of valid frequency ratios.

For example, suppose the VCO range is 800 MHz to 1000 MHz and that f_{REF} is 25 MHz. For an integer-only PLL, the only possible VCO output frequencies are 800 MHz to 1000 MHz in 25 MHz steps (corresponding to N values 32 to 40). Conversely, a fractional PLL supports any output frequency between 800 MHz and 1000 MHz as long as the fraction, F/M , has the necessary resolution. In the case of the AD9552, fractional resolution is limited to 20 bits for both F and M , which yields a resolution of $1/1,048,575$. The user can program the 20-bit values for both F and M , allowing for a very large set of possible output frequencies.

The fractional feedback divider of the AD9552, along with its output dividers (P_0 and P_1), produces a primary output frequency (f_{OUT1}) given by

$$f_{OUT1} = [(N + F/M)/(P_0 \times P_1)] \times f_{PFD}$$

The secondary output frequency (f_{OUT2}) of the AD9552 is

$$f_{OUT2} = f_{OUT1}/P_2 \text{ or } f_{OUT2} = f_{PFD}$$

depending on the selection of the signal source for OUT_2 .

In the above equations, $f_{PFD} = f_{REF}$ or $f_{PFD} = 2 \times f_{REF}$, depending on the selection of the optional $2\times$ frequency multiplier.

For fractional frequency division, typically the feedback divider assumes one integer value most of the time (Q , for example), but periodically changes to $Q + 1$ in such a way that the average divide ratio is the desired fractional value. The word, *periodically*, is significant because it implies undesirable spurious artifacts in the output spectrum. To help mitigate the spurious artifacts that are normally associated with a fractional divider, the AD9552 uses a sigma-delta modulator (SDM) with a built-in pseudorandom binary sequence (PRBS) generator to spread out the spurious energy. The combination of an SDM and PRBS generator in the feedback divider provides sufficient spurious suppression to satisfy the specifications of many network clock applications.

Even though the AD9552 generates some spurious artifacts, thus limiting its usefulness as a general-purpose crystal oscillator replacement, it is still well suited for the network clocking

space. The reason is that the SDM moves the spurious energy far enough out of band to allow for relatively easy filtering. In fact, Figure 4 and Figure 5 show actual phase noise measurements of the AD9552 pin strapped to yield a 625 MHz output using a 26 MHz crystal resonator.

The phase noise plot shown in Figure 4 represents the unfiltered output of the AD9552 and demonstrates the raw performance of the device. Note the spurious components between 1 MHz and 100 MHz with magnitudes ranging from about -60 dBc to -90 dBc. The resulting rms jitter in the SONET OC-192 band (50 kHz to 80 MHz) is 0.74 ps. On the other hand, exclusion of the spurious artifacts (see Figure 5) yields 0.51 ps of rms jitter. Although not shown, measurements in the SONET OC-3 band (12 kHz to 20 MHz) indicate 0.65 ps of rms jitter, either with or without the inclusion of the spurious artifacts in the measurement.

For this particular application (synthesizing a 625 MHz output signal using a 26 MHz crystal), comparison of the rms jitter values, both with and without the spurious content in both the OC-3 and OC-192 bands, indicates that the spurs appearing in the 1 MHz to 10 MHz range have no significant impact on rms jitter performance. The AD9552 suppresses the spurs in the 1 MHz to 10 MHz range to the point of having no adverse affect on the rms jitter performance.

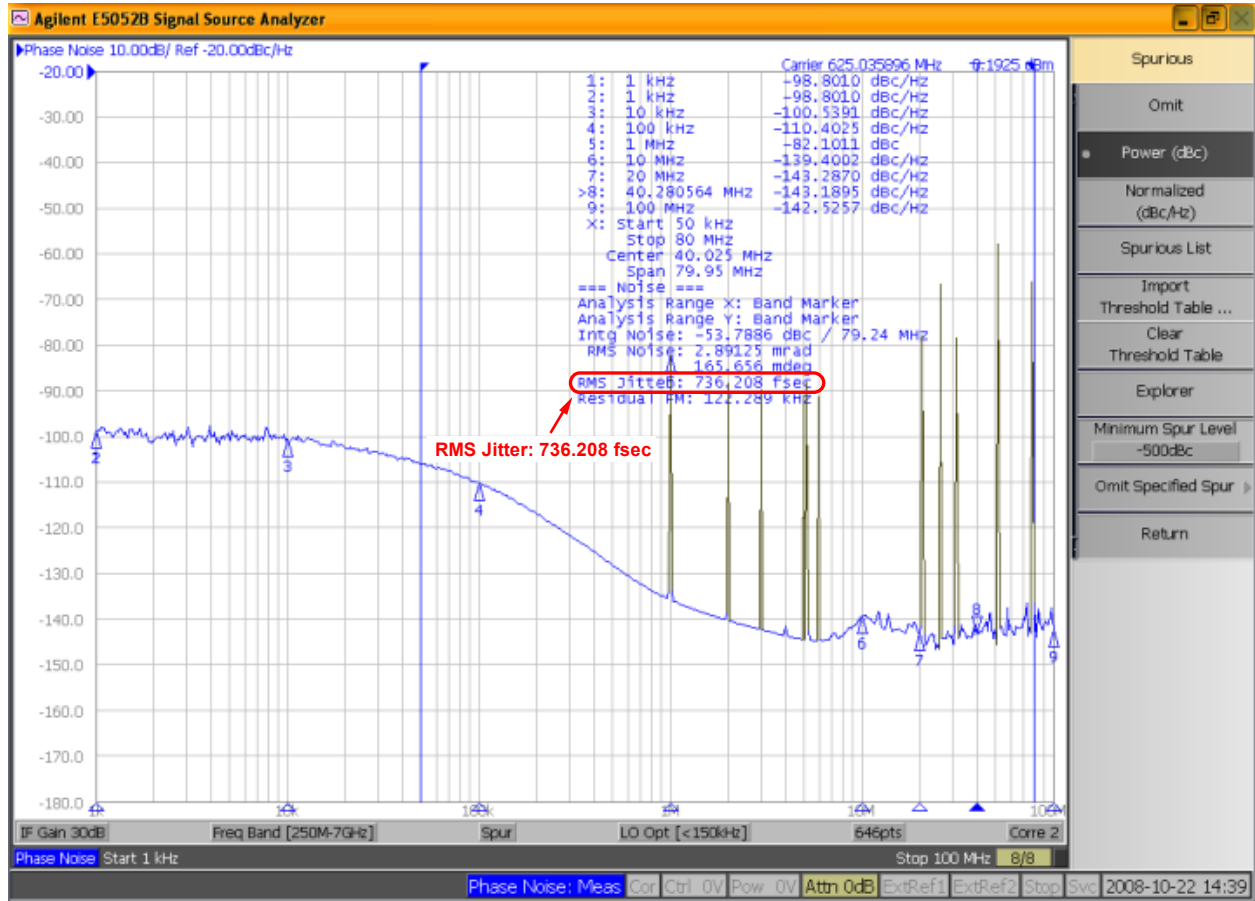


Figure 4. AD9552 Phase Noise Measurement

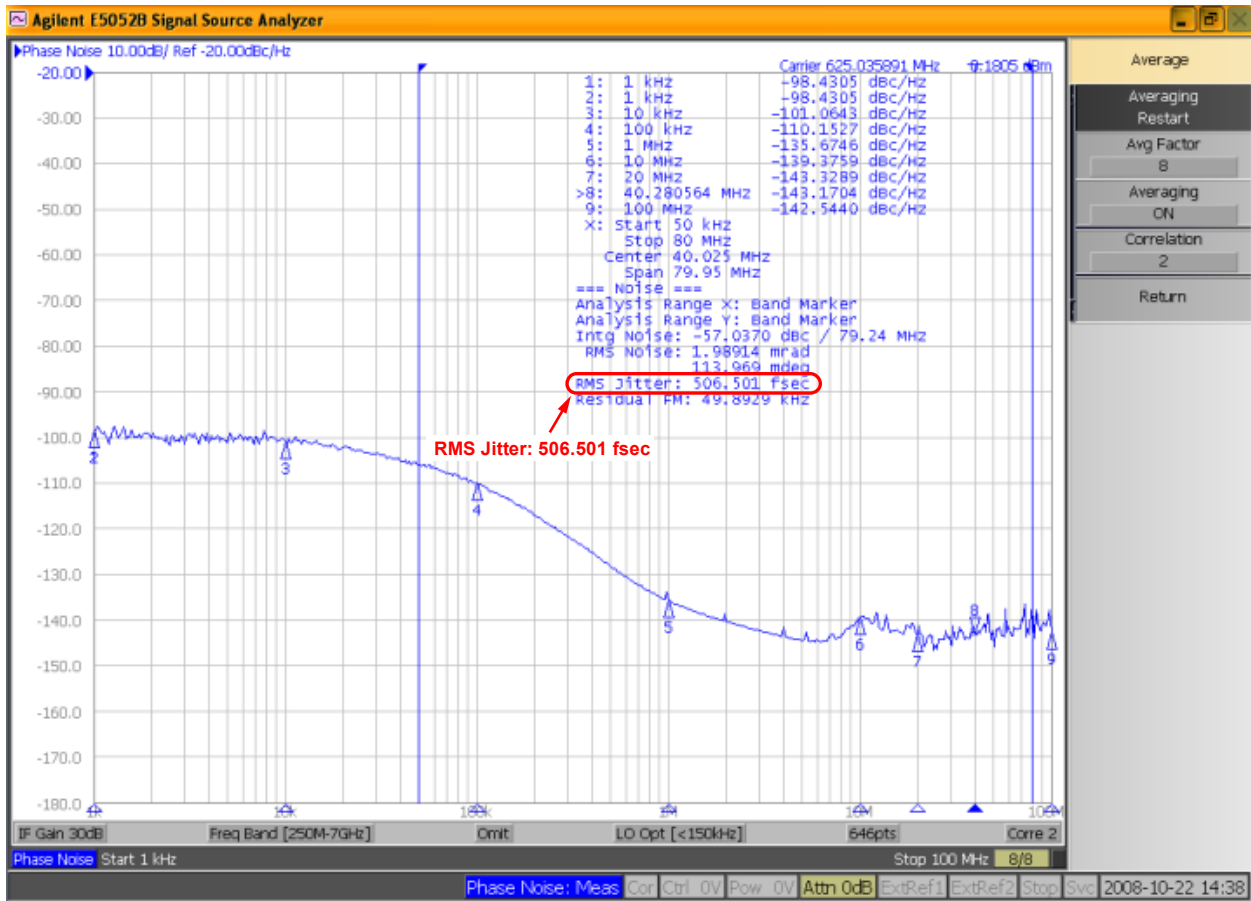


Figure 5. AD9552 Phase Noise Excluding Spurious Artifacts

CONCLUSION

The measurement results for this particular application (625 MHz out using a 26 MHz crystal) indicate that the AD9552 meets a 0.65 ps rms jitter requirement in the OC-3 band without the need for additional filtering of the output signal. On the other hand, it should be possible to achieve similar rms jitter performance (~0.6 ps) in the OC-192 band by using an external filter to suppress the spurs beyond the 1 MHz range. For example, one might use a SAW filter centered at 625 MHz with a 2 MHz bandwidth.

Applications using a different output/input frequency ratio have a different set of spurious artifacts. Thus, it is wise to analyze

the spurious content of each output/input frequency ratio in an application to determine if postfiltering is necessary. If external filtering is necessary, then the appropriate filter parameters (such as bandwidth, stop-band attenuation, and insertion loss) must be determined to generate the desired jitter performance.

Although the AD9552 is not the only solution for network clocking applications, its flexibility, low cost, high reliability, and ease of use are significant advantages over other solutions.