

87654321

REV A

Customer Bd.
AD9645
<PRODUCT_1>

DESIGN VIEW
<DESIGN_VIEW>

PTD ENGINEER
Umesh Jayamohan

DRAWING NO.
9645CE01

SIZE
D

SCALE
NONE

SHEET 1 OF 9

REV
A

SCHEMATIC

AD9655/45/35 CUSTOMER EVAL BOARD
16/14/12 BIT 80/125 MSPS ADC
DUAL LANE SERIAL LVDS

87654321

87654321

A

B

C

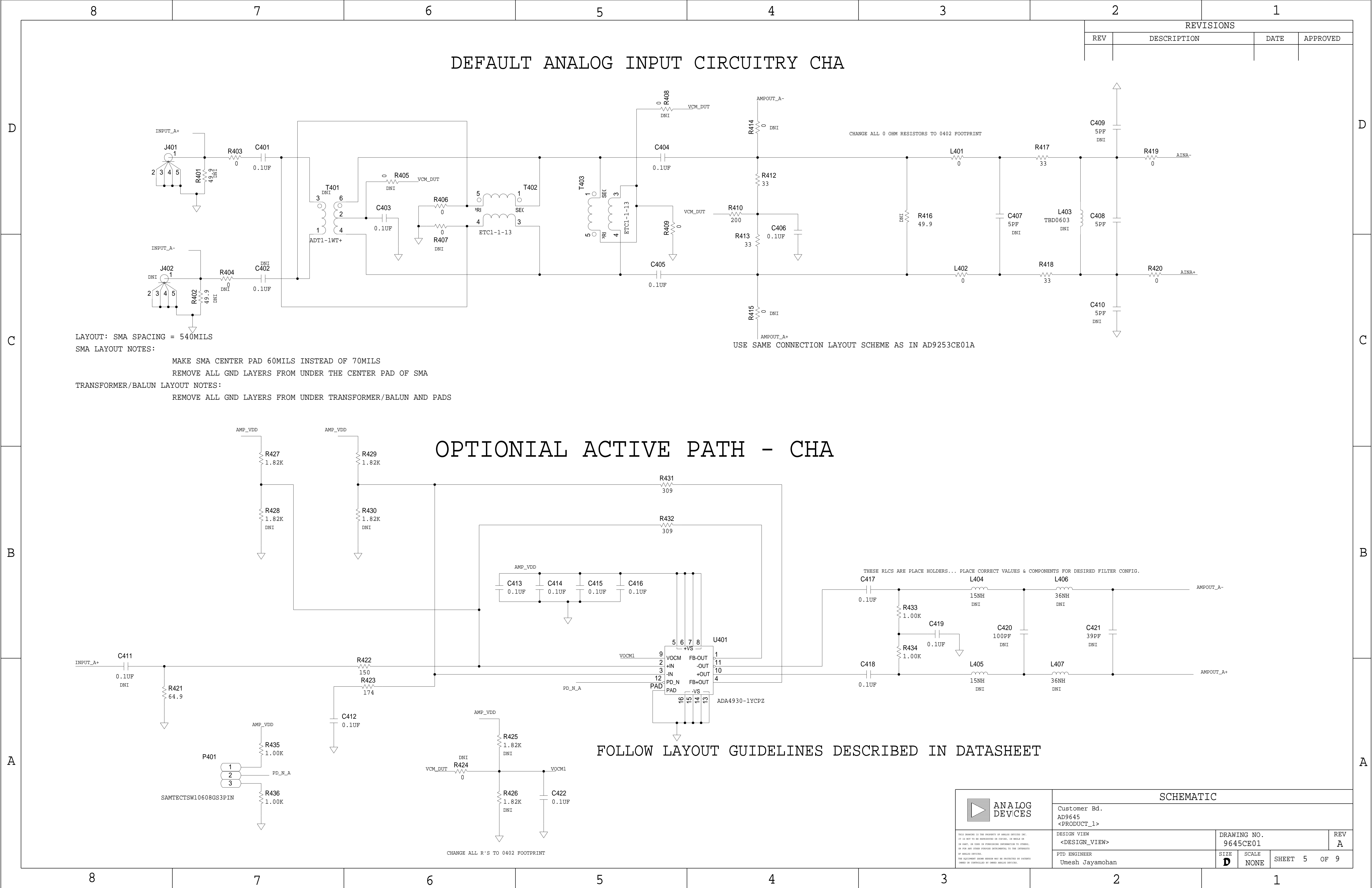
D

A

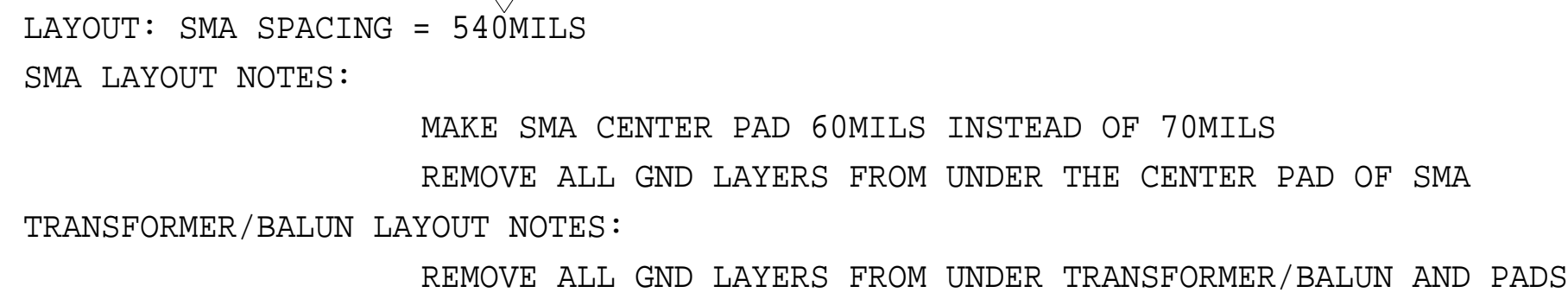
B

C

D



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



THESE RLCS ARE PLACE HOLDERS... PLACE CORRECT VALUES & COMPONENTS FOR DESIRED FILTER CONFIG.



Customer Bd.
AD9645
<PRODUCT_1>

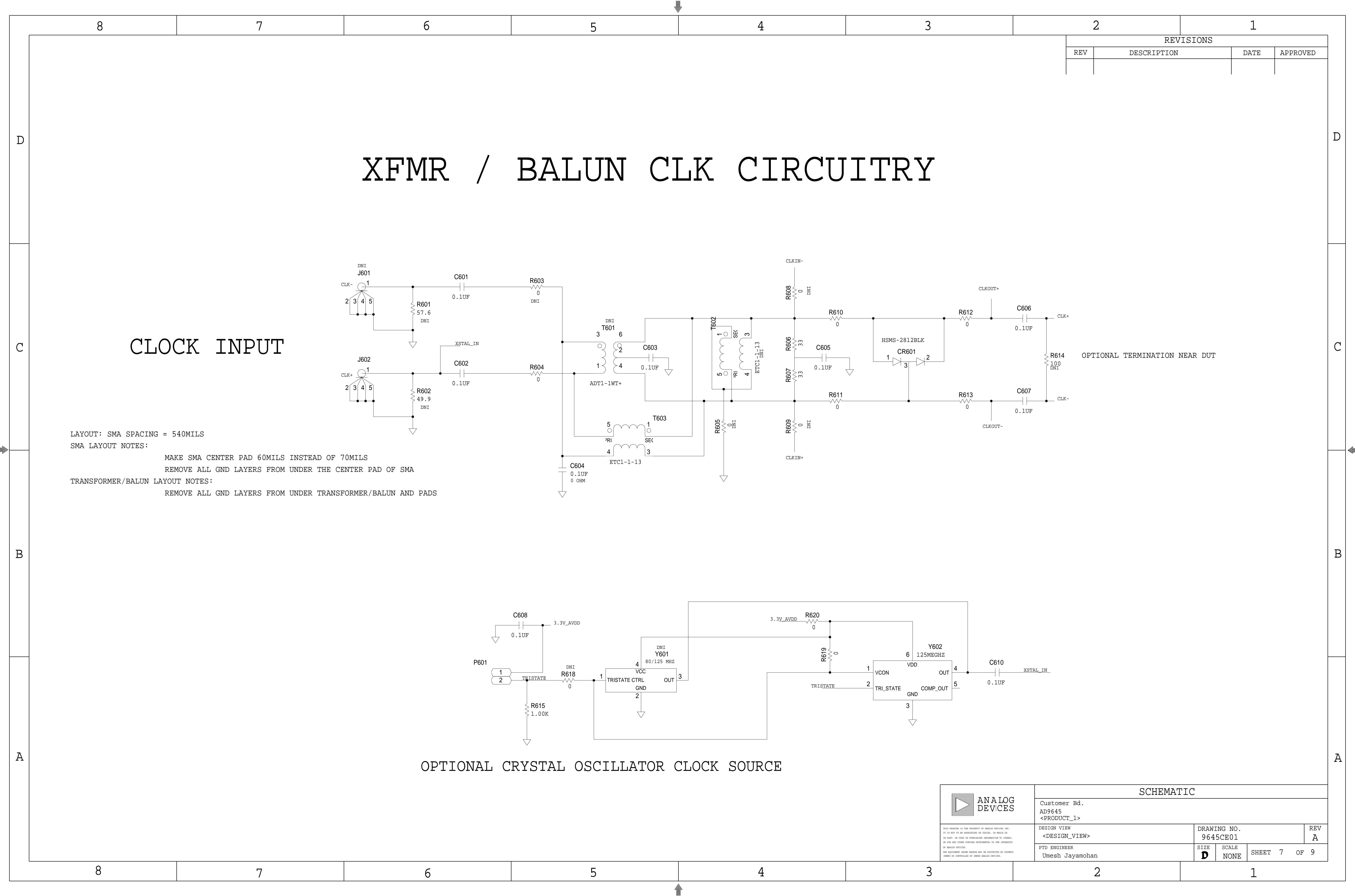
DESIGN VIEW
<DESIGN_VIEW>

PTD ENGINEER
Umesh Jayamohan

DRAWING NO.
9645CE01

SIZE D	SCALE NONE
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SHEET



D

C

B

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2

1

REV

DESCRIPTION

DATE

APPROVED

D

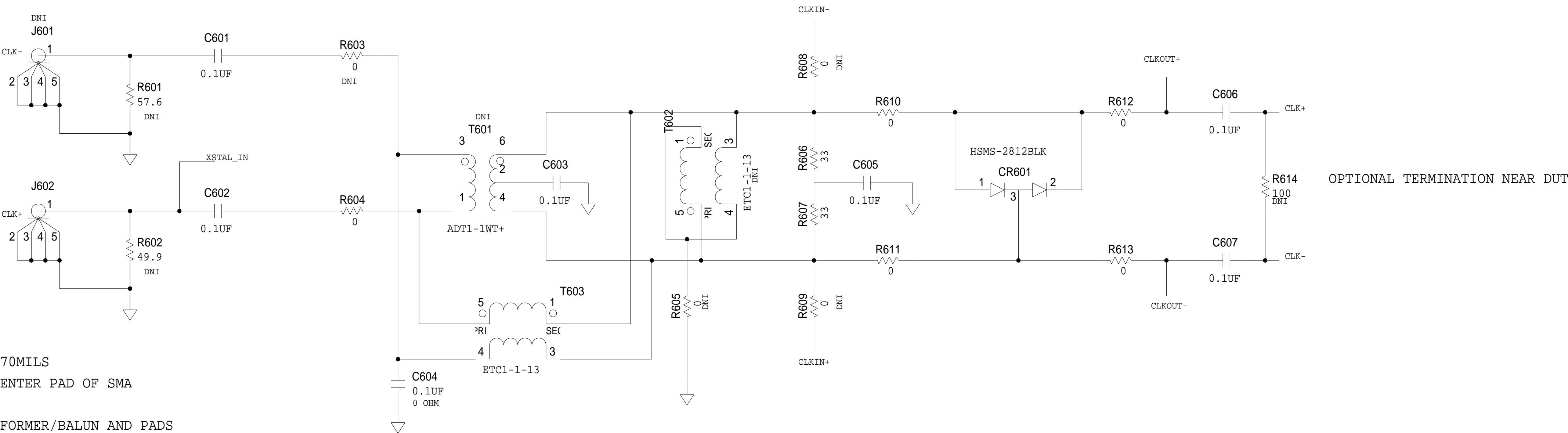
C

B

A

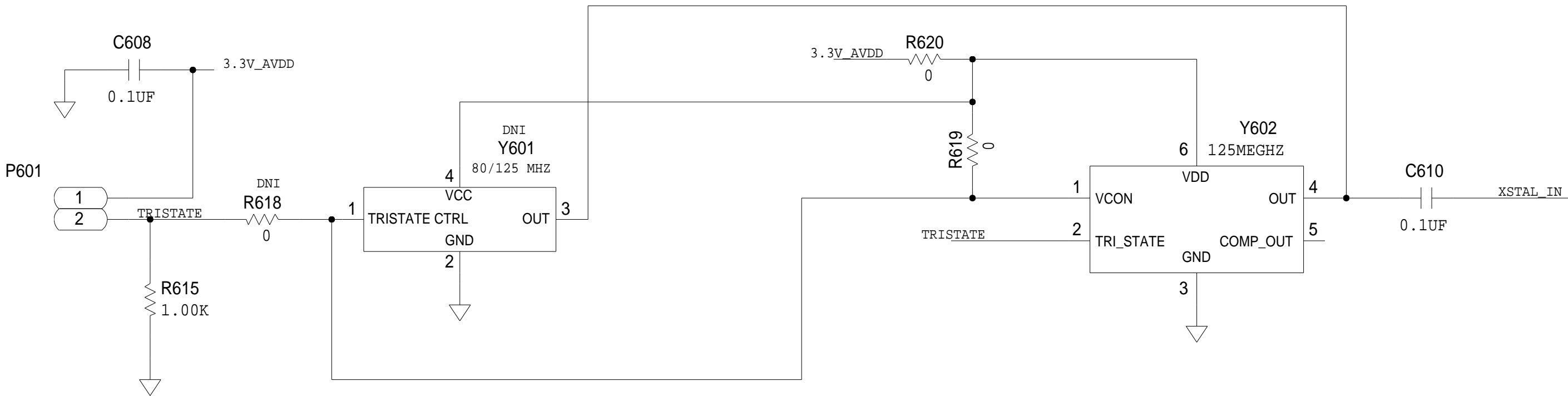
XFMR / BALUN CLK CIRCUITRY

CLOCK INPUT



LAYOUT: SMA SPACING = 540MILS
SMA LAYOUT NOTES:
MAKE SMA CENTER PAD 60MILS INSTEAD OF 70MILS
REMOVE ALL GND LAYERS FROM UNDER THE CENTER PAD OF SMA
TRANSFORMER/BALUN LAYOUT NOTES:
REMOVE ALL GND LAYERS FROM UNDER TRANSFORMER/BALUN AND PADS

OPTIONAL CRYSTAL OSCILLATOR CLOCK SOURCE



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DEVICES

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SCHEMATIC			
Customer Bd. AD9645 <PRODUCT_1>			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 9645CE01	REV A	
PTD ENGINEER Umesh Jayamohan	SIZE D	SCALE NONE	SHEET 7 OF 9

