

Evaluating the **AD9670** Octal Ultrasound AFE with Digital Demodulator

FEATURES

Fully featured evaluation board for the **AD9670**
PC software for controlling the **AD9670** via a USB interface

EVALUATION KIT CONTENTS

AD9670EBZ evaluation board
1 switching power supply (6.0 V, 2.5 A), CUI EPS060250UH-
PHP-SZ (provided)

EQUIPMENT NEEDED

Analog signal source and antialiasing filter
Linear benchtop dc voltage source (0 V to 1.6 V), not
required for CW Doppler mode
PC running Microsoft Windows® 7 and Windows 10 operating
system
USB 2.0 port, recommended (USB 1.1 compatible)
HSC-ADC-EVALCZ FPGA-based data capture kit
1 switching power supply (6.0 V, 2.5 A), CUI EPS060250UH-
PHP-SZ (provided with data capture kit)
Spectrum analyzer for CW Doppler mode

DOCUMENTS NEEDED

AD9670 data sheet

SOFTWARE NEEDED

VisualAnalog
SPIController

GENERAL DESCRIPTION

The AD9670EBZ evaluation board assists in evaluating all features of the **AD9670** octal ultrasound analog front end (AFE) device. The **AD9670** is low cost, low power, compact, and easy to use with medical ultrasound applications. The device provides eight voltage gain amplifier (VGA) channels, each with a low noise amplifier (LNA), a continuous wave (CW) harmonic rejection I/Q demodulator with programmable phase rotation, an antialiasing filter, an analog-to-digital converter (ADC), and a digital demodulator and decimator for both data processing and bandwidth reduction.

The evaluation board provides eight Subminiature Version A (SMA) connector inputs for all eight **AD9670** channels. The evaluation board mates with a field-programmable gate array (FPGA) data capture board (**HSC-ADC-EVALCZ**) that enables data capture through a USB connection to a computer.

The **SPIController** software provides flexible configuration of the **AD9670** and the **VisualAnalog**® software offers powerful data capture and signal analysis tools.

EVALUATION BOARD PHOTOGRAPH

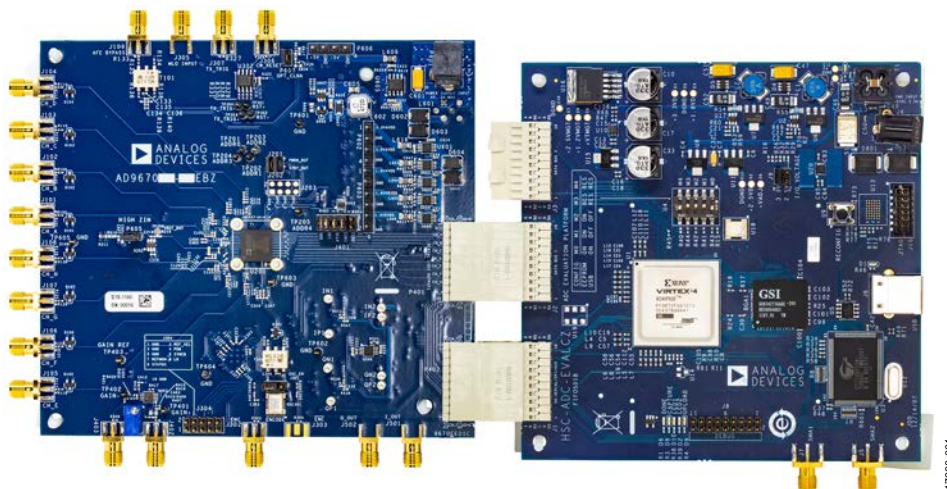


Figure 1.

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REVISION HISTORY

1/2019—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

POWER SUPPLIES

A switching power supply (6.0 V, 2.5 A) powers up the AD9670EBZ board.

INPUT SIGNALS

The AD9670EBZ board provides eight SMA connector inputs for the eight AFE channels. The SMA channel inputs directly connect to the [AD9670](#) LNA input. An optional, external clock SMA input bypasses the default on-board 40 MHz crystal by changing the J301 jumper. Figure 1 shows an image of all inputs.

Other SMA inputs include the VGA V_{GAIN} control, the CW Doppler $\text{MLO}\pm$, $\text{RESET}\pm$, and an optional $\text{TX_TRIG}\pm$ input. The V_{GAIN} single-ended signal is the default but a differential input configuration is also possible. The FPGA provides the $\text{TX_TRIG}\pm$ signal on the [HSC-ADC-EVALCZ](#) data capture board.

OUTPUT SIGNALS

The data capture board receives low voltage differential signaling (LVDS) digital output signals from the AD9670EBZ board through the on-board connectors (P401 and P402) (see Figure 1). The J501 jumper and J502 jumper SMA outputs are the CW Doppler summed in-phase quadrature (I/Q) outputs.

EVALUATION BOARD SOFTWARE SOFTWARE INSTALLATION PROCEDURES

To install the [VisualAnalog](#) and [SPIController](#) software packages, and configure and test the [AD9670](#), take the following steps:

1. Install the [VisualAnalog](#) software.
2. Install the [SPIController](#) software.
3. Plug the 6 V adapters into the AD9670EBZ evaluation board and the data capture board to power them up. Connect the data capture board to the PC with the USB cable that is provided with the data capture board.
4. Launch the [SPIController](#) software to open the window shown in Figure 2 and select the [AD9670.cfg](#) file from the dropdown list (under **File > Cfg Open Menu**). After the **Open File** dialog appears, browse for and select the [AD9670_14bit_125MSspiR03.cfg](#) file. The chip ID reads AD9670 (see Figure 2) after loading the [AD9670.cfg](#) file.

CHIP READS AD9670

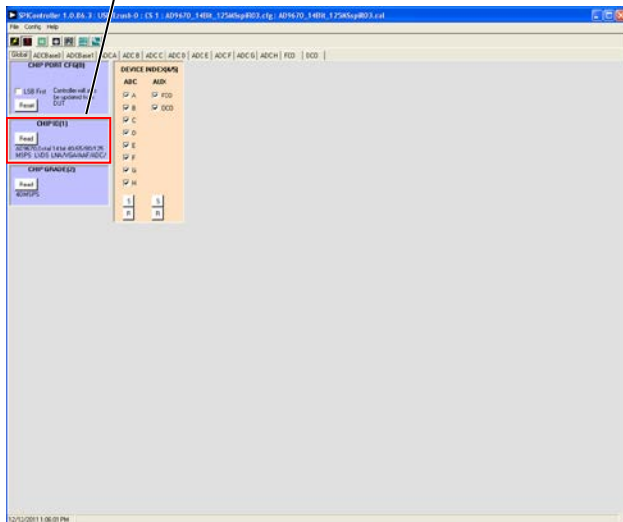


Figure 2. SPIController Main Window

5. From the **Config** menu, click **Launch Memory Map Dialog** to open the **Memory Map** window, as shown in Figure 3. Click the **Load File** button to open the [AD9670_14bit_125MSspiR03.mmp](#) file, which loads the coefficient and profile memory data into the [AD9670](#).

READS THE MEMORY ON THE DEVICE AND SAVES IT TO A FILE
DEMODULATION FREQUENCY CAN BE CHANGED BY UPDATING DEMOD AND SAMPLE FREQUENCY

UPDATING PROFILE NUMBER SELECTS A NEW DECIMATION RATE AND COEFFICIENT POINTER

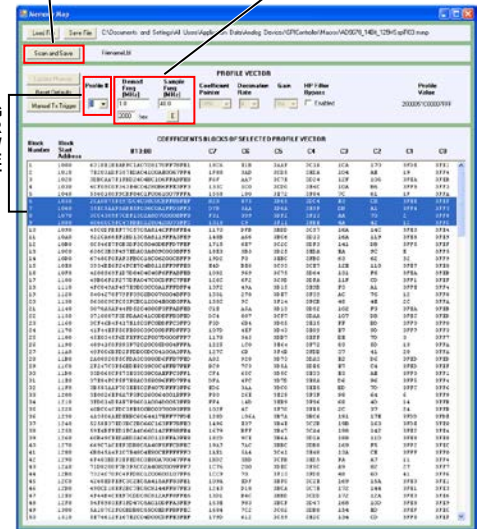


Figure 3. Memory Map Window

6. In the main [SPIController](#) window, open the **File** menu and click **Open Macrogroup**. Select the [AD9670_Initialization.mgp](#) macro file to open the **MacroEditor** window shown in Figure 4. The macro file is an **.XML** file that lists the serial peripheral interface (SPI) command macros in the [D6970_Initializaion_v2.mg](#) dropdown box (see Figure 4). Each command macro includes SPI writes that configure the [AD9670](#) for specific operating modes. The **MacroEditor** conducts a batch write of SPI registers to set up the [AD9670](#). The macro file contains the following two macros: **Real Mode, 40Msps** and **IQ Mode, 40Msps**. It is possible to add unique configuration macros to the **.XML** macro file and load the macros into the **MacroEditor** window.

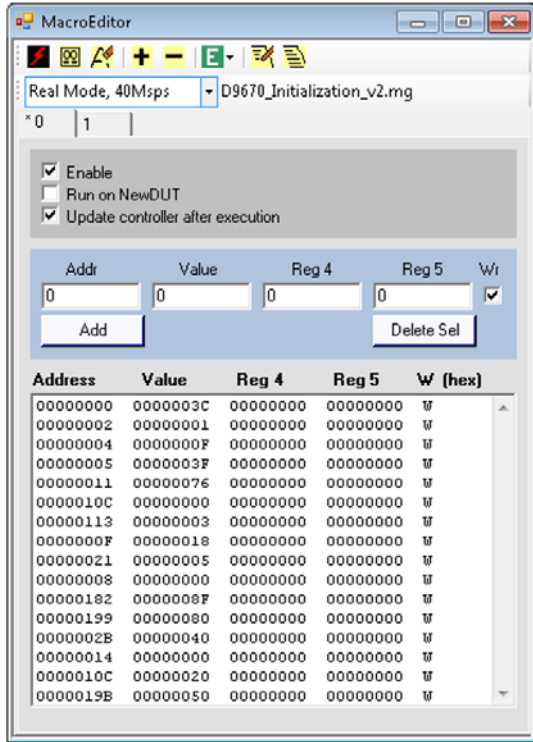


Figure 4. MacroEditor Window and D9670_Initialization_v2.mg Dropdown Box

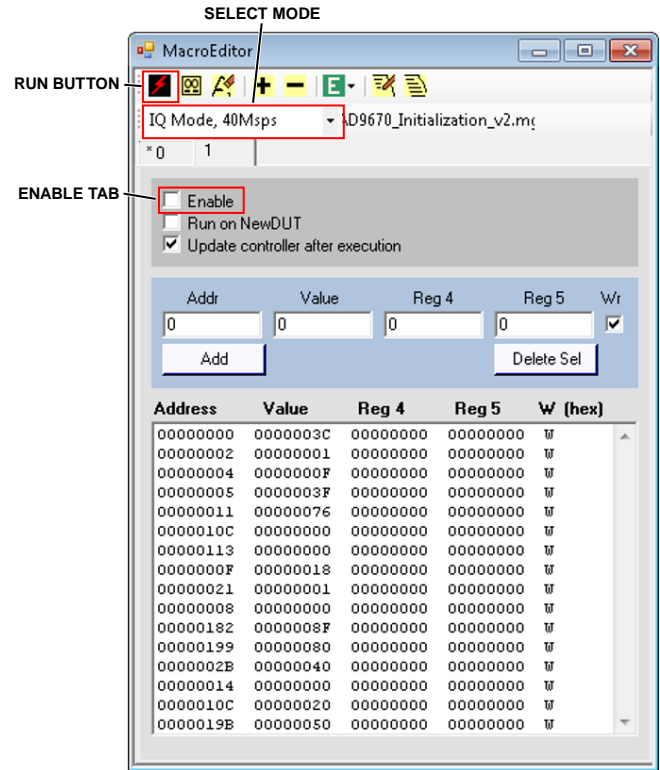


Figure 5. Select, Enable, and Run Commands in MacroEditor

Table 1. Procedural List of SPI Commands Configuring the AD9670

Register	Function
0x000	SPI reset.
0x002	Set speed mode.
0x004, 0x005	Set local registers to all channels.
0x011	Set LNA, VGA, and PGA gain.
0x10C	Set SPI TX_TRIG± and Index Profile 1.
0x113	Enable/bypass digital filters, demodulator, and decimator.
0x00F	Set low-pass filter cutoff frequency and mode.
0x021	16-bit, 8-lane, frame clock output (FCO) covers entire frame.
0x008	Time gain compensation (TGC) run mode.
0x182	Autoconfigure phase-locked loop (PLL).
0x199	Autoset FCO and data clock output (DCO).
0x02B	Set analog low-pass filter and high-pass filter to defaults and tunes filters.
0x014	Set output data format.
0x188	Enable start code.
0x10C	Set SPI TX_TRIG± and Index Profile 1.
0x19B	Serial format.

7. Select either the **Real Mode** or the **IQ Mode** macro from the dropdown box (see Figure 5) and select the **Enable** checkbox. To run the selected macro, click the **Run** button to conduct a write operation (see Figure 5).

8. Launch the **VisualAnalog** software to use the canvas templates listed in the **AD9670** directory in the **Categories** pane (see Figure 6). The **Samples** canvas shows time domain output samples vs. sample count.

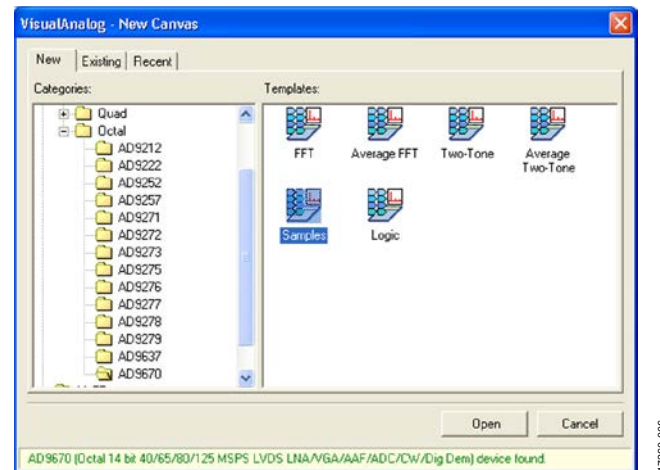


Figure 6. VisualAnalog Canvas Selection Window

9. If the **VisualAnalog** software opens and only shows the task bar, as shown in Figure 7, click the down arrow on the right side of the window to expand the **AD9670 Samples** canvas (shown in Figure 8) to see the signal processing flow.

10. Next, load the FPGA binary file into the hardware. To load the file, click the **Settings** button in the **ADC Data Capture** block (see Figure 8).

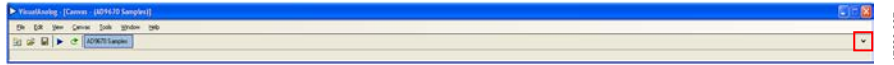


Figure 7. *VisualAnalog* in Window Collapse Mode

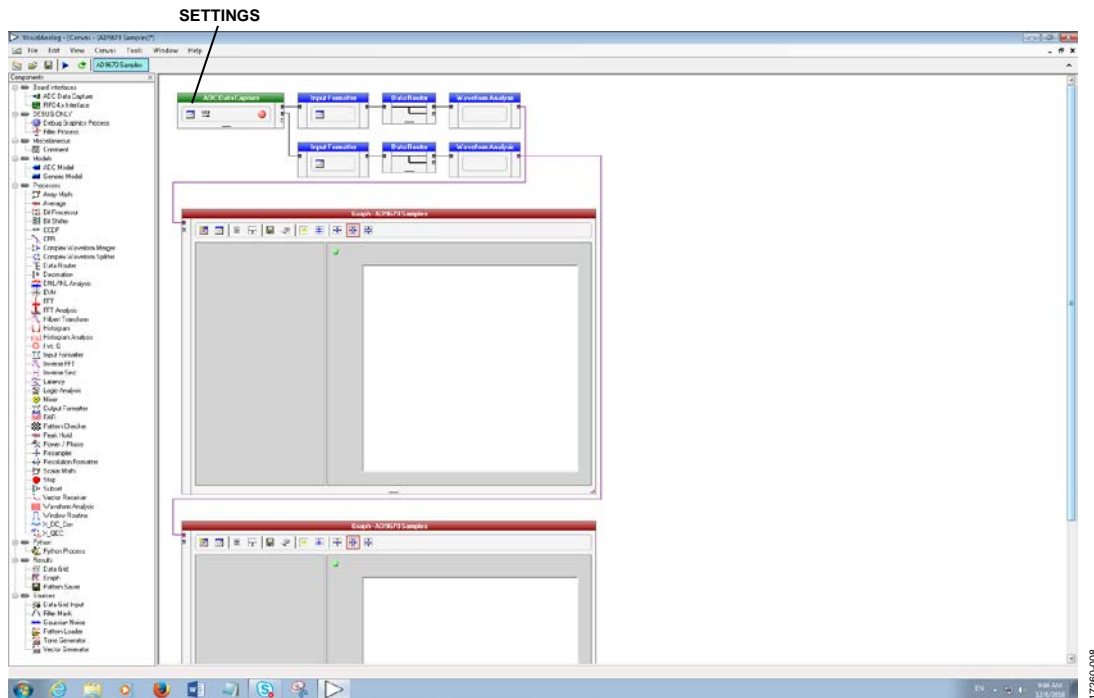


Figure 8. *VisualAnalog* Sample Canvas

- When the **ADC Data Capture Settings** window opens, click the **Capture Board** tab and then click the **Browse...** button. Select the **ad9670_lvds_mar2012.bin** file and click **Program**, which illuminates the **Done** LED D6 indicator on the **HSC-ADC-EVALCZ** board. Click **OK** to close the window.

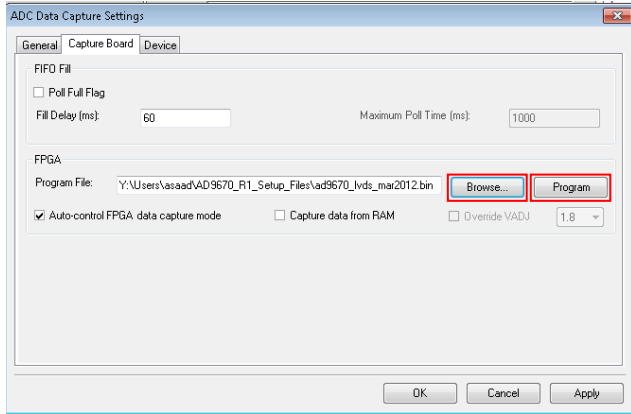


Figure 9. ADC Data Capture Settings Window

- The **AD9670** is now running and fully configured for data capture mode. The **VisualAnalog** software offers two data capture modes: onetime and infinite loop. Click the blue right arrow (see Figure 7 or Figure 8) to run the canvas in onetime mode and click the green repeat button (see Figure 7 or Figure 8) to run the canvas in infinite loop mode. The **Samples** canvas then opens two windows showing 8192 time domain samples for Channel A and Channel B (see Figure 10 for the Channel A window).

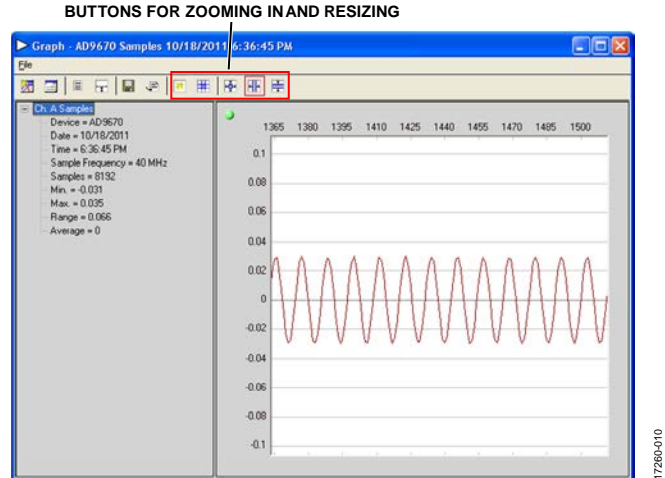


Figure 10. Data Capture Window

- Another loadable canvas, the **AD9670_Average_FFT.vac** canvas, runs average fast Fourier transform (FFT) calculations of the captured samples. The average count is set to five captures. Therefore, either run the canvas five times to display the first FFT output or leave it in continuous run mode to keep the canvas functioning.
- Figure 11 shows both the FFT output and how the analog and digital high-pass filters shape the noise floor in the low frequency region.

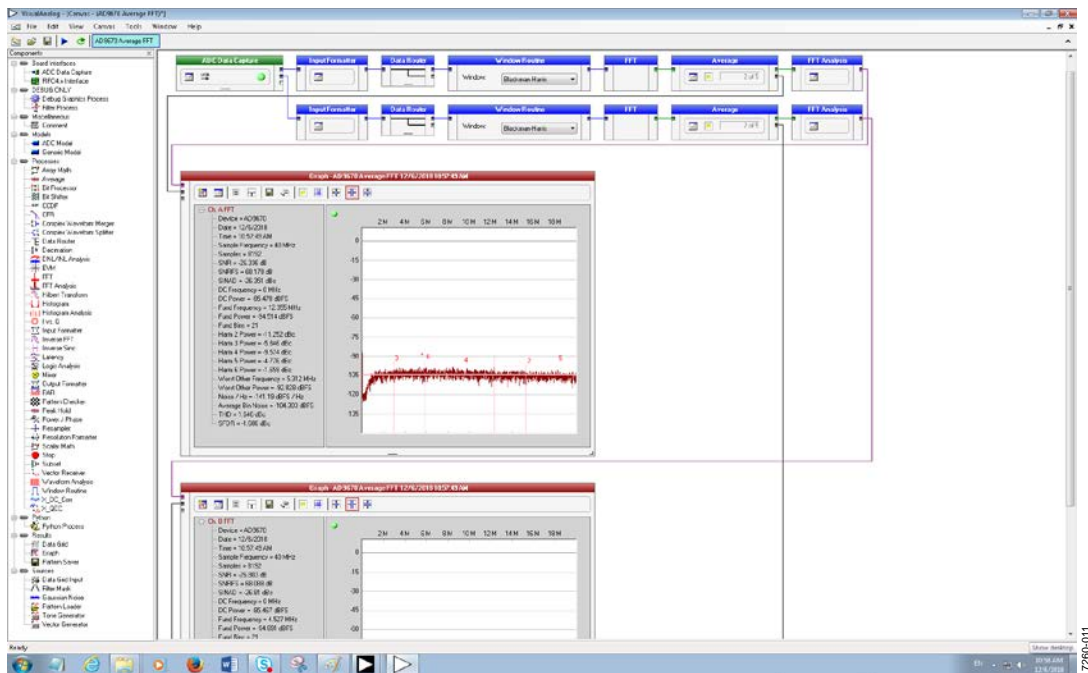


Figure 11. Average FFT Canvas

- To disable the digital high-pass filter, select the **HP Filter Bypass** checkbox in the **Memory Map** window (see Figure 12) and then click the **Manual Tx Trigger** button (see Figure 12).

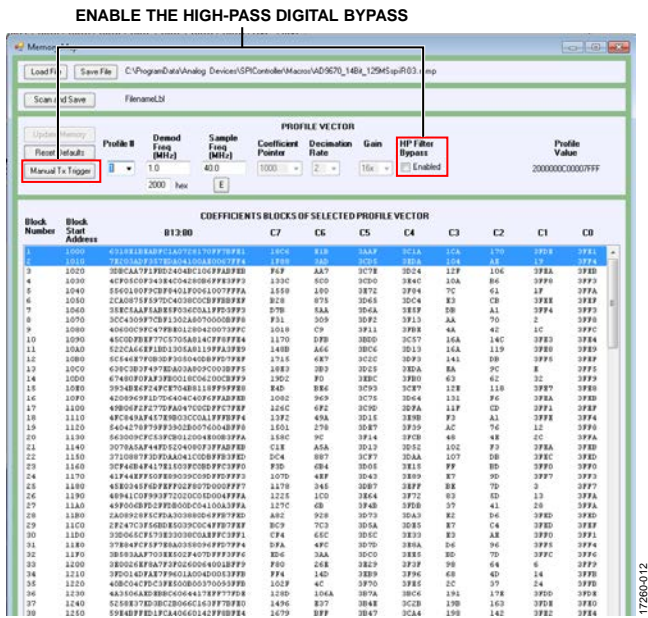


Figure 12. Disabling the Digital High-Pass Filter Bypass in the Memory Map Window

- Disabling the digital high-pass filter increases the noise floor shape at low frequencies and results in a flat noise floor (see Figure 13).

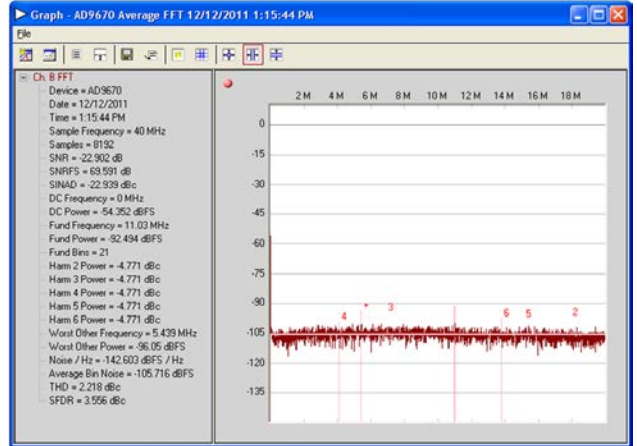


Figure 13. Average FFT Canvas with the Digital High-Pass Filter Disabled

- To enable the demodulator and decimator, select and run the **IQ Mode, 40Mpsps macro** in the **MacroEditor** window (see Figure 4).

EVALUATION BOARD SCHEMATICS AND ARTWORK

17286-015

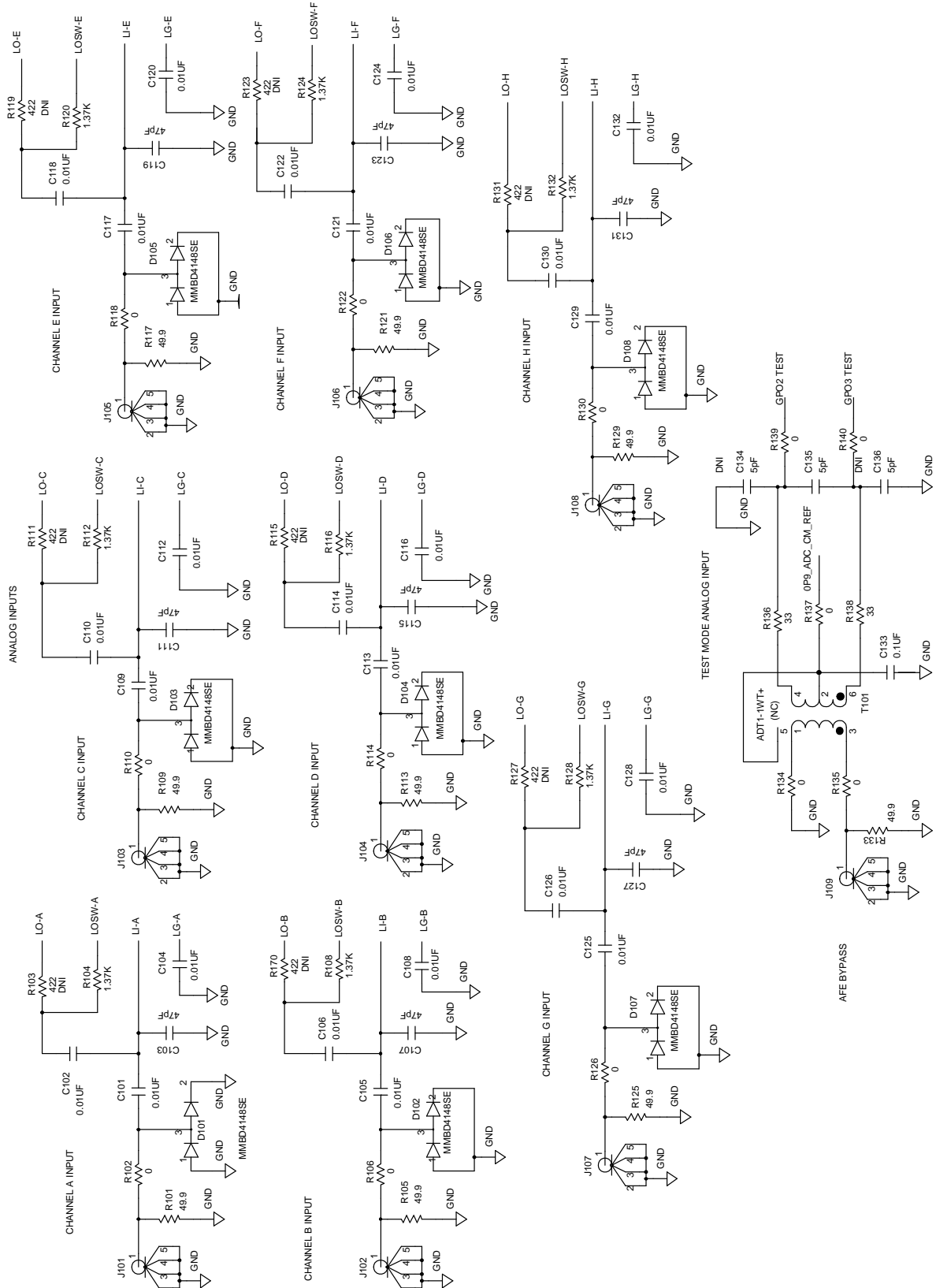


Figure 14. AD9670EBZ Schematics Page 1

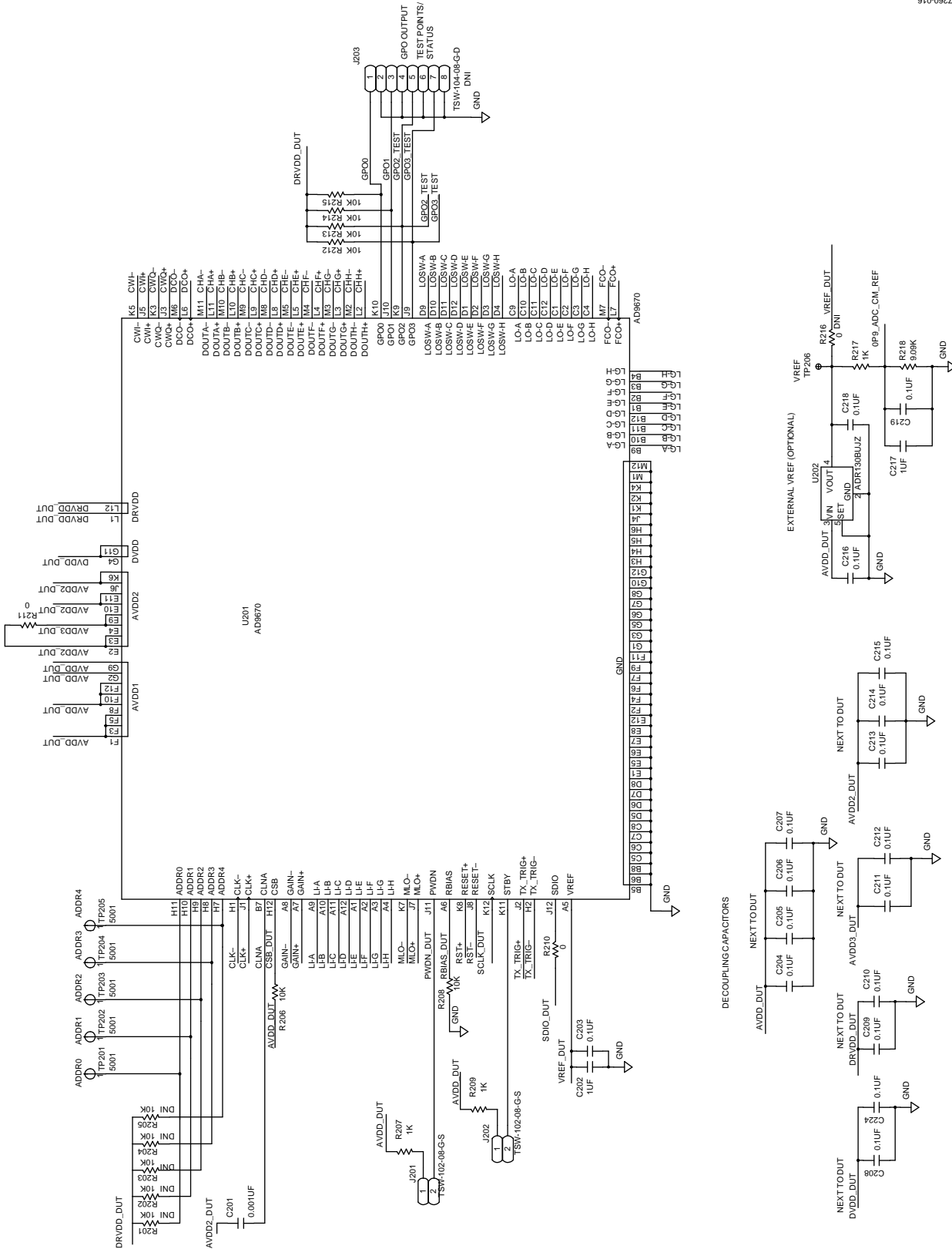


Figure 15. AD9670EBZ Schematics Page 2

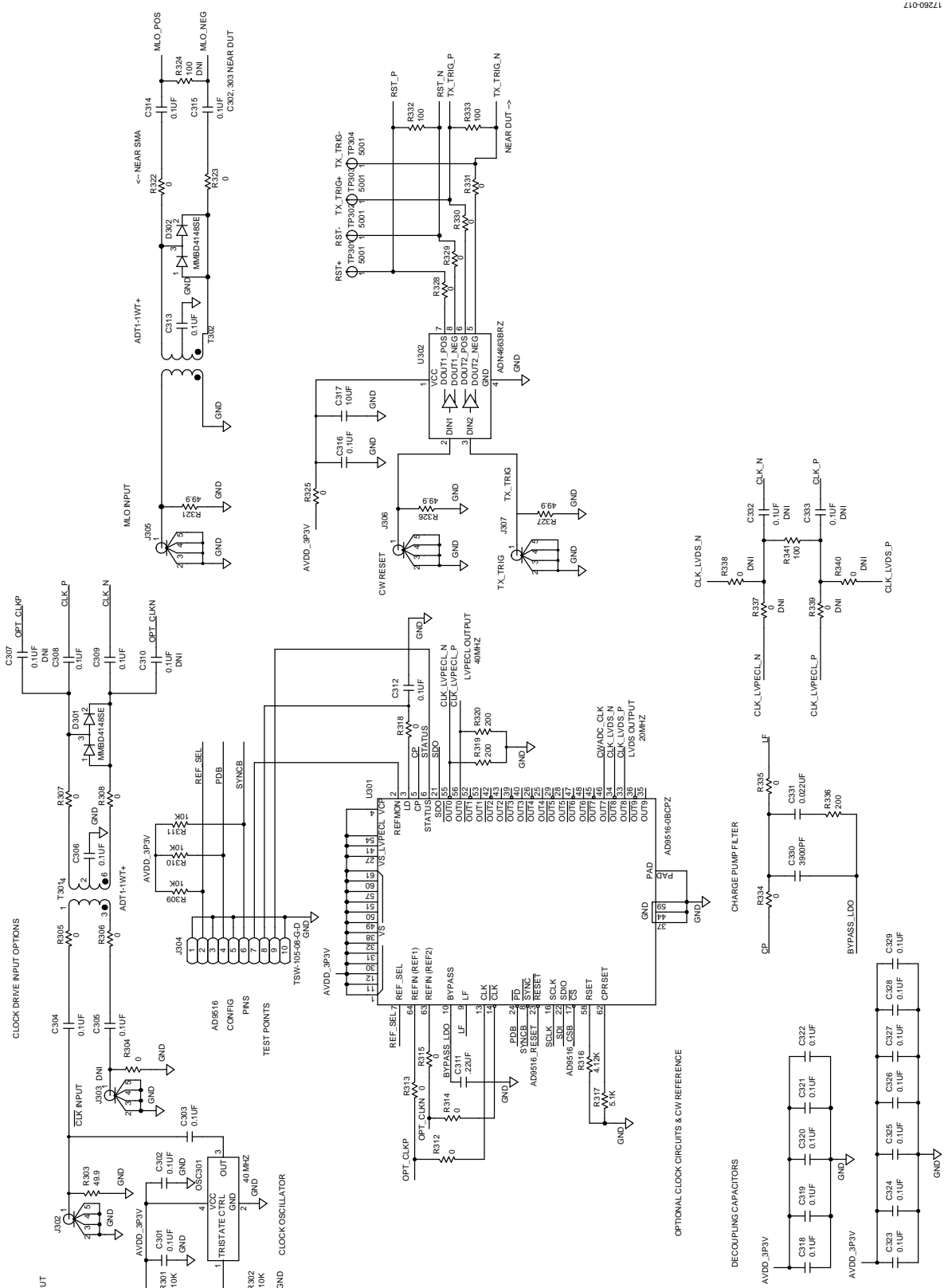


Figure 16. AD9670EBZ Schematics Page 3

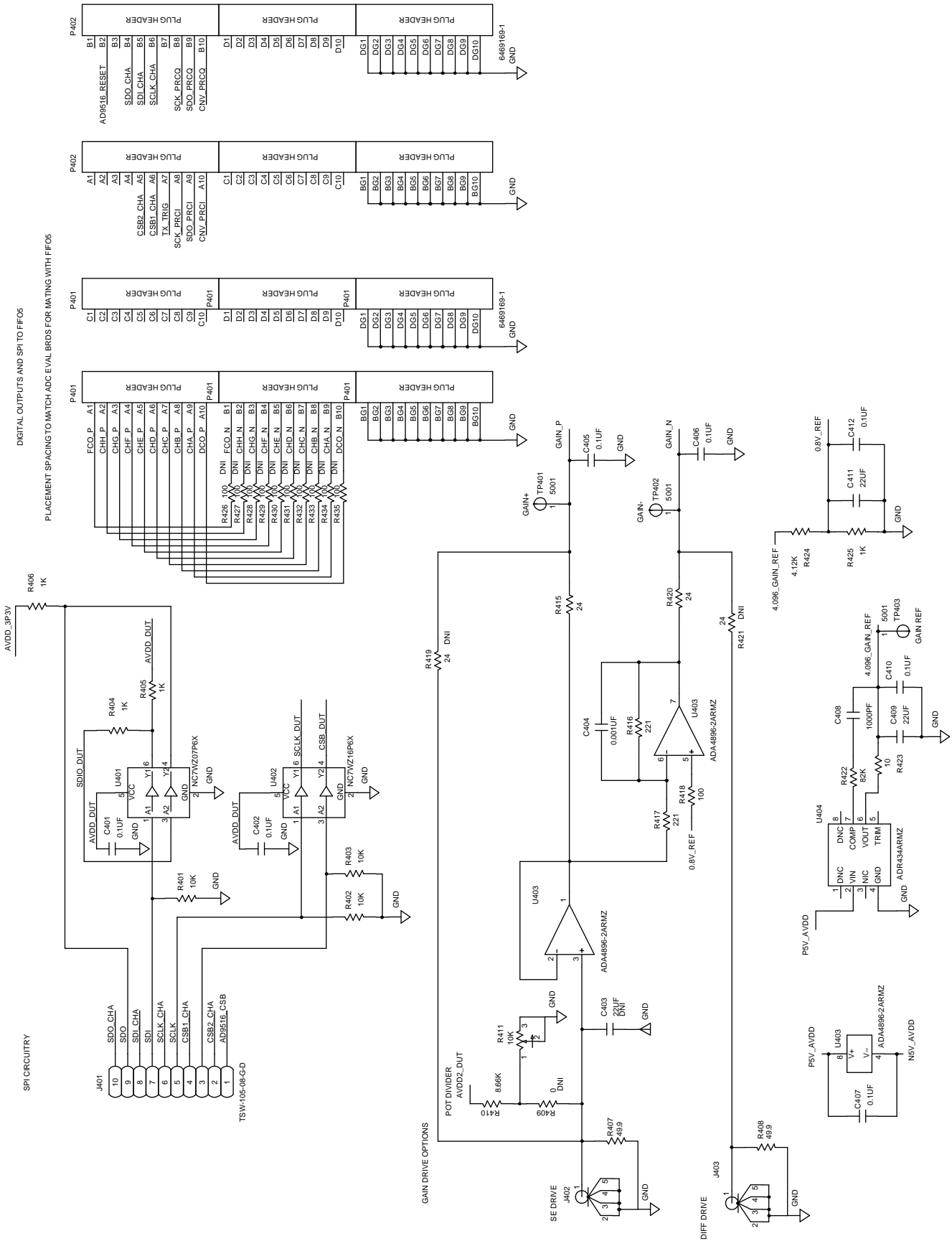


Figure 17. AD9670EBZ Schematics Page 4
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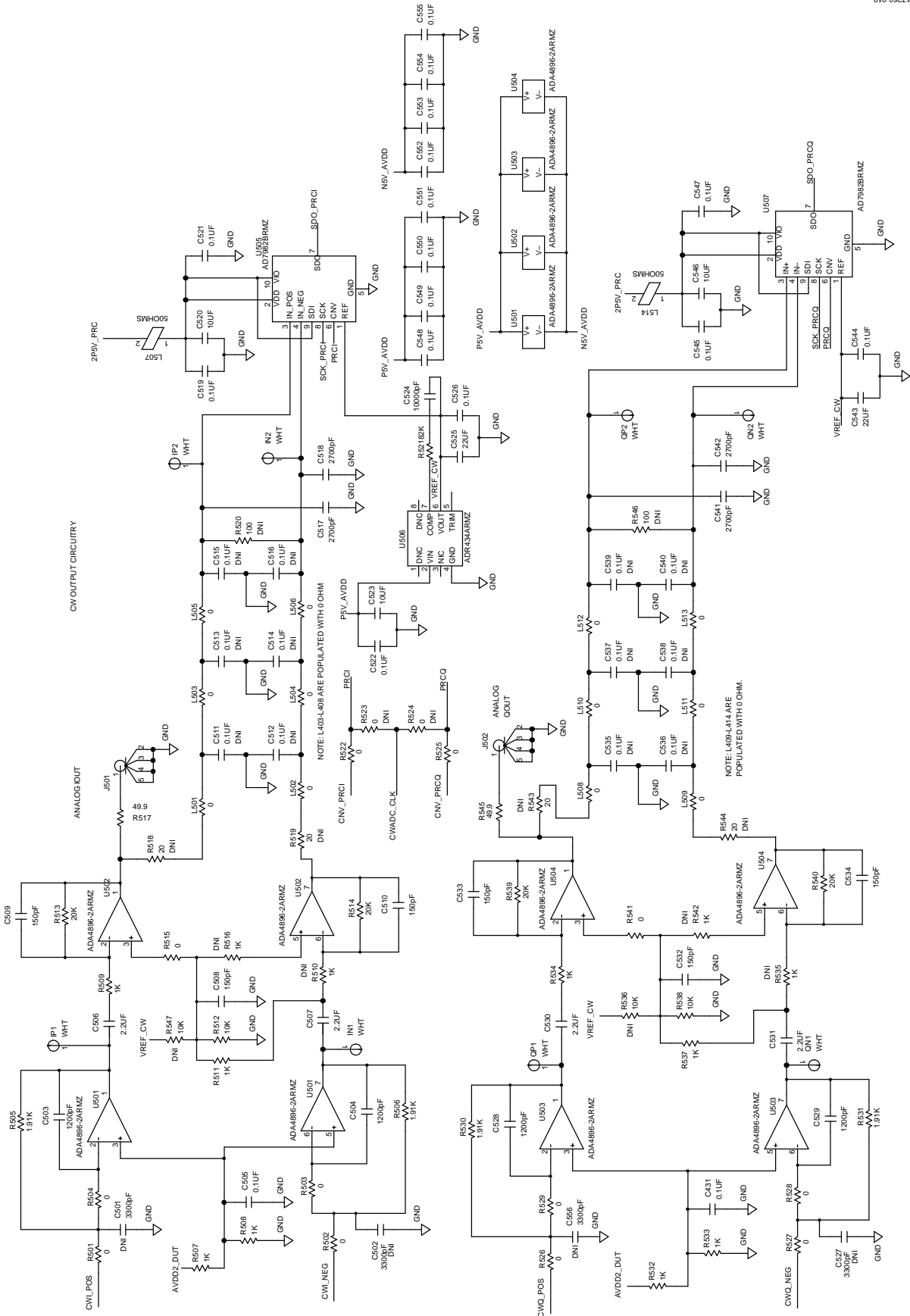


Figure 18. AD9670EBZ Schematics Page 5
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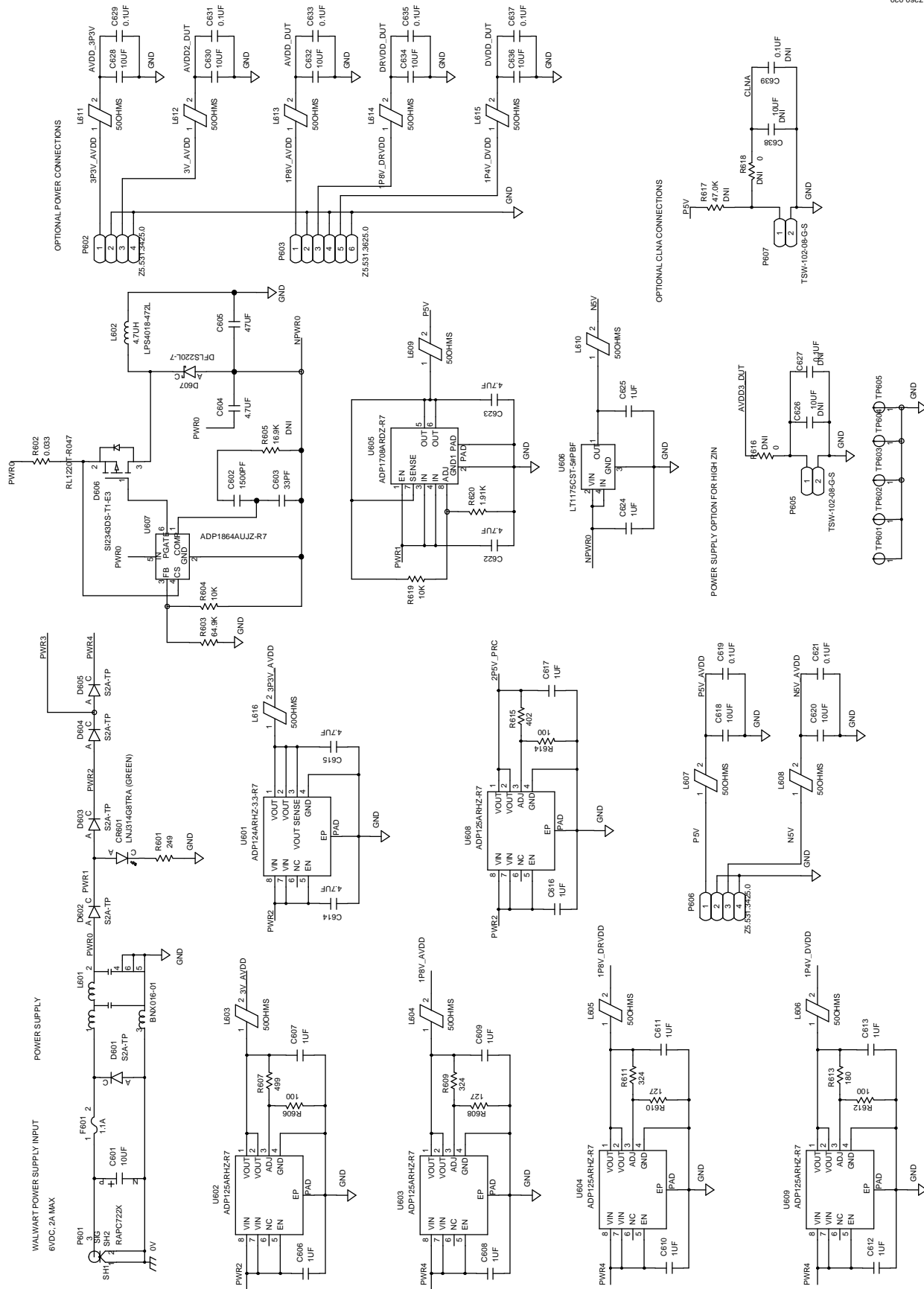


Figure 19. AD9670EBZ Schematics Page 6

NOTES

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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