Validating ADI Converters inter-operability with Xilinx FPGA and JESD204B/C IP

Introduction

ADI continues to develop world class converter technologies and as a result requires us to develop high throughput interfaces. To insure customer success, ADI and Xilinx collaborate on these interfaces to insure roadmap alignment on devices and our evaluation/development boards. ADI internally validates our devices interoperating with Xilinx to provide customer confidence when designing their systems with our devices.

Validation of Analog Devices high-speed converter products and evaluation boards are performed using a Xilinx Virtex or Kintex FPGA based platform board that incorporates Xilinx JESD204B/C IP. This document describes the testing methodology, as it applies to the validation of JESD204B/C interoperability, for testing converter evaluation platforms.

Products Tested

Table 1 lists the ADI products that have been tested with Xilinx IP.

Table 1. Xilinx Interoperability Device Listing

ADI Part #	Type	Xilinx Part#	IP rev.
AD6673	ADC	Virtex-6 LX75T	2.2
AD6674	ADC	Virtex-7 VX330T	6.1
AD6676	ADC	Virtex-6 LX75T	2.2
AD9081	ADC	KintexUS+ KU15P	204B 7.2 204C 4.0
AD9081	DAC		
AD9135	DAC	Virtex-7 VX330T	1.0 - 7.0
AD9136	DAC	Virtex-7 VX330T	1.0 - 7.0
AD9144	DAC	Virtex-7 VX330T	1.0 - 7.0
AD9152	DAC	Virtex-7 VX330T	1.0 - 7.0
AD9154	DAC	Virtex-7 VX330T	1.0 - 7.0
AD916x	DAC	Virtex-7 VX330T	1.0 - 7.0
AD917x	DAC	Virtex-7 VX330T	1.0 - 7.0
AD9208	ADC	Virtex-7 VX330T	6.2
AD9213	ADC	KintexUS+ KU040	204B 7.2 204C 4.0
AD9234	ADC	Virtex-7 VX330T	6.1
AD9250	ADC	Virtex-6 LX75T	2.2
AD9625	ADC	Virtex-6 LX75T	2.2
AD9656	ADC	Virtex-6 LX75T	2.2
AD9671	ADC	Virtex-6 LX75T	2.2
AD9680	ADC	Virtex-7 VX330T	6.1
AD9683	ADC	Virtex-6 LX75T	2.2
AD9689	ADC	Virtex-7 VX330T	6.2
AD9690	ADC	Virtex-7 VX330T	6.1
AD9691	ADC	Virtex-7 VX330T	5.2
AD9694	ADC	Virtex-7 VX330T	6.2
AD9695	ADC	Virtex-7 VX330T	6.2
AD9371	TRx	xc7z045ffg900-2	7.0
AD9375	TRx	xc7z045ffg900-2	7.0
ADRV9009	TRx	xc7z045ffg900-3	7.0
ADRV9008-1	TRx	xc7z045ffg900-3	7.0
ADRV9008-2	TRx	xc7z045ffg900-3	7.0
ADRV9026	TRx	KintexUS+ KU15P	204B 7.2 204C 4.0

Typical Setup

Hardware Requirements

- Converter Evaluation Board (AD9xxx-nnnnEBZ)
  - With FMC connector
- Xilinx-based evaluation platform boards
  - Virtex or Kintex Ultrascale FPGA
- Synchronized clock source to provide the following clocks:
  - ADC or DAC reference clock
  - FPGA reference clock
  - FPGA global clock
  - SYSREF input to converter and FPGA boards

Software Requirements

ADC Software

- ADI ACE software for configuring the ADC and FPGA and data evaluation

DAC Software

- ADI ACE Software for configuring the DAC and FPGA
- ADI Data Pattern Generator (latest revision)

FPGA Firmware:

Appropriate FPGA firmware is automatically downloaded from the Xilinx-based evaluation platform board upon power-up of the evaluation board system.

Each converter device requires its own FPGA firmware. The most current revision of the Xilinx JESD204B/C IP that is available at the time this firmware is being developed is used.

For ADC's, most testing is done in subclass 0 mode. When testing ADC's in subclass 1 mode, additional firmware is used.

Transceiver (TRx) Test Setup

For the test setup of AD9371 and AD9375, please refer to the Demonstration System Overview in the AD9371-AD9375 User Guide UG-922.

For the test setup of ADRV9009, ADRV9008-1, please refer to the ADRV9009 & ADRV9008 Prototyping Platform User Guide on www.analog.com.

System Configuration

Figure 1 illustrates the system level setup for ADC validation and JESD204B/C Inter-operability. Figure2 illustrates the system level setup for DAC validation and JESD204B/C Inter-operability.

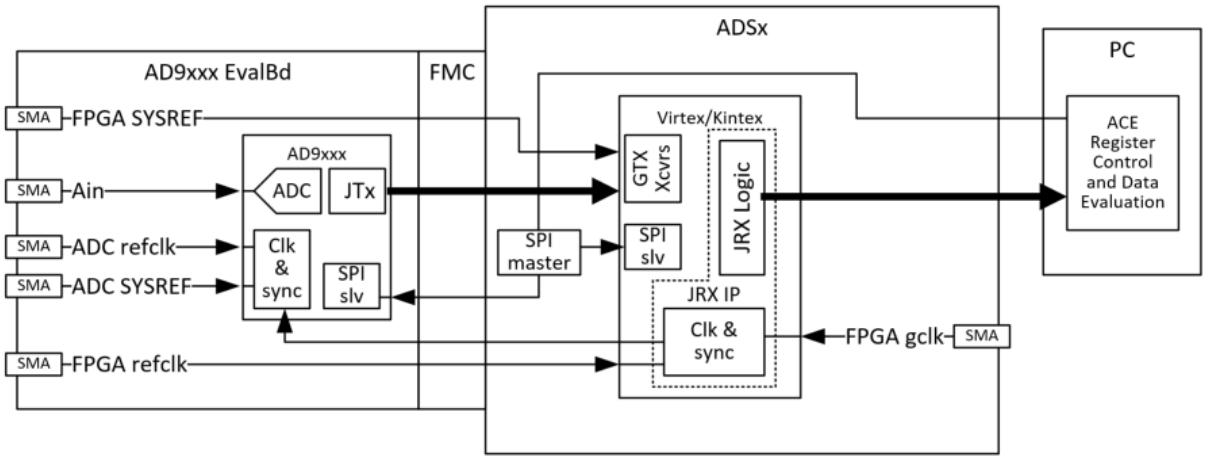

Figure 1: Typical system level diagram for ADC validation and JESD204B/C Inter-operability

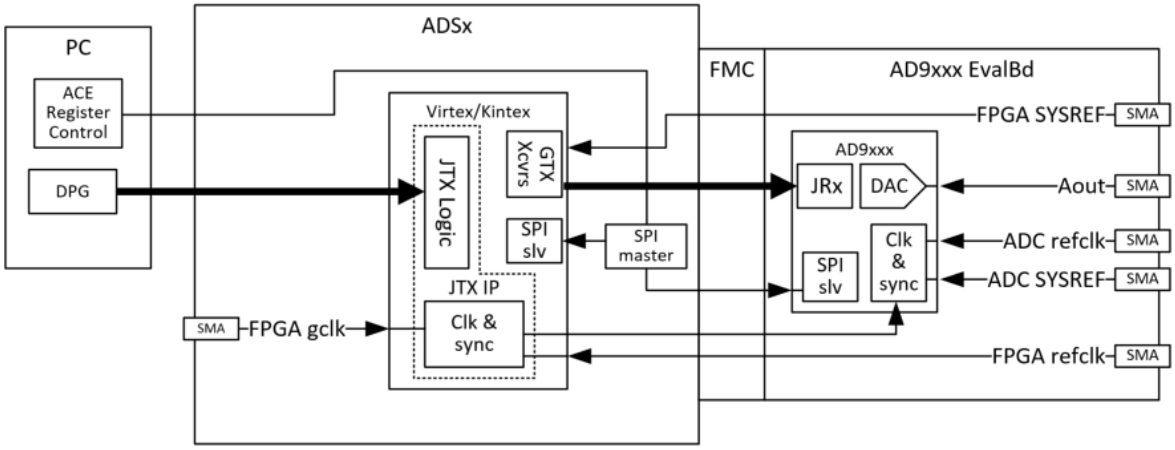

Figure 2: Typical system level diagram for DAC validation and JESD204B/C Inter-operability

ADC Specific Setup and Test

ADC device characterization and evaluation board testing encompasses every aspect of device function, performance, and robustness. For this document, the focus will be on how this testing validates the JESD204B/C link interoperability between the converter and Xilinx FPGA.

For each device, every JESD204B/C mode is thoroughly tested using a variety of signals and exercise every test mode at the ADC output, transport layer, data link layer, and physical layer inputs. These tests exercise the entire signal path from the ADC input to samples out at the FPGA's JESD204B/C receiver output.

Physical Layer Testing

When connected directly to the FPGA, the physical layer inter-operability is validated at the maximum lane rates by inserting a PRBS and other patterns at the ADC output and confirming the data samples and or measuring the bit error rate (BER) at the FPGA.

The PHY electrical specifications and features of ADI ADC's are tested thoroughly versus the JESD204B/C standard on boards specifically built for such testing. Each JESD204B-deifned PHY test mode is used and the following parameters are "swept" to ensure full compatibility between the Tx and Rx PHY's and to measure performance:

- Process, voltage, and temperature (PVT) of the ADC
- Pre-emphasis in the JTX and equalization at the JRX
- Voltage swing at the JTX output
- Insertion loss of the pcb channel

This testing is done independent of the FPGA. However, similar testing of the transceiver cores performed by Xilinx against the JESD204B/C standard ensures electrical compatibility between the devices.

Data Link Layer Testing

JESD204B Link Layer

Synchronization

The synchronization process for the link is validated every time the link is initialized and data capture takes place as part of the device characterization and board checkout. Every time a Visual Analog (VA) data capture takes place, CGS, ILAS, and data transmission is confirmed to have completed properly when valid data is observed in VA.

8B/10B Encode/Decode

Further data link layer compatibility is tested by validating the integrity of the samples through the link. 8b/10b encoding and decoding is confirmed to be correct when the samples provided to the JTX match the samples at the JRX output.

Scrambling

Scrambling is enabled and disabled on both sides of the link and the integrity of the data confirmed to ensure inter-operability between the scrambler and de-scrambler.

Alignment Character Insertion

Alignment character insertion and detection are validated by enabling insertion at the JTX, confirming their presence in the serial data stream, and confirming the integrity of the data at the JRX output (meaning the original data was recovered correctly).

Link Layer Test Modes

Each data link layer test mode is tested at the highest lane rates. These tests include:

- Continuous sequence of D21.5
- Continuous sequence of K28.
- Repeated ILAS

JESD204C Link Layer

Synchronization

The synchronization process for the link is validated every time the link is initialized and data capture takes place as part of the device characterization and

board checkout. The link establishment process when using the 64b/66b link layer starts automatically once the link is powered on. The process begins with synchronization header synchronizations, then progresses to extended multiblock synchronization, and then progresses to extended multiblock alignment.

64B/66B Encode/Decode

Further data link layer compatibility is tested by validating the integrity of the samples through the link. 64b/66b encoding and decoding is confirmed to be correct when the samples provided to the JTX match the samples at the JRX output.

Transport Layer Testing

As with many tests in this validation process, the data mapping into frames and multiframes is verified by the correct recovery of the sample data at the FPGA. Depending on the test being performed, sample verification is done through FFT analysis or by directly checking the samples (testing for bit errors). These test are performed across the operating range of the ADC and JESD204B/C interface.

Subclass 1 Testing

Most ADC performance testing is performed with the 204B interface in subclass 0 mode. There are many SYSREF features and parameters that are also tested. Each SYSREF mode is fully characterized as well as SYSREF timing parameters and features. Regarding interoperability with the Xilinx IP, the following subclass 1 test procedure validates that LMFC alignment takes place and deterministic latency is achieved.

Subclass 1 Test Setup Example

Figure 3 depicts the evaluation board setup, including the necessary clock and SYSREF connections for performing subclass 1 testing with ADI ADC's.

Subclass 1 interoperability testing is performed in all of the JESD204B/C modes supported by the ADC. These modes are described in detail in the devices data sheet.

A continuous SYSREF is applied to both the ADC and the FPGA, as well as to the ADC analog input.

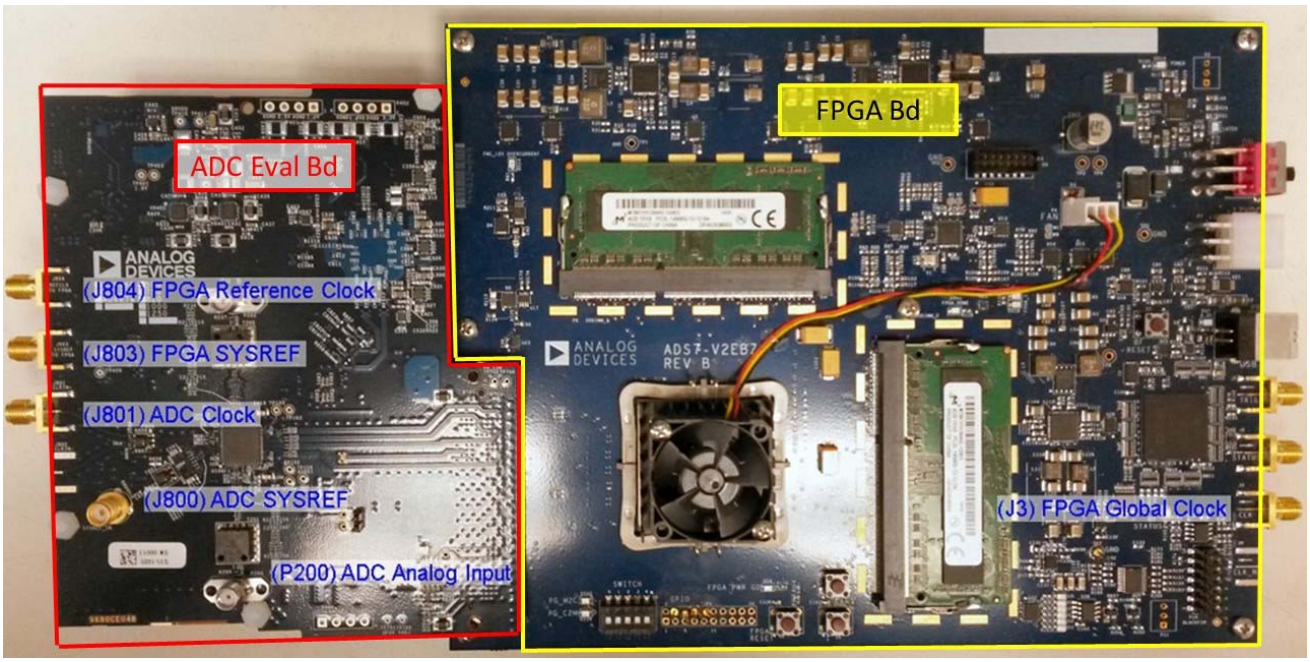

Figure 3: Evaluation Board Configuration for subclass 1 operation

Test Process

For each ADC, latency measurements are taken for all ADC and JESD204B/C operating modes. The various latencies that are measured are:

- Total ADC latency (Analog In to Data Out)
- SYSREF-to-LMFC
- Analog In to LMFC
- LMFC to Data Out

This testing is done while the JESD204B/C link is established. Therefore, data and total system latency can be observed at the FPGA.

To observe the LMFC and SYSREF at the FPGA, these signals are routed (in the FPGA logic) to the 2 LSB's of the 16-bit data samples (replacing the LSB's of the data or the JESD204B/C tail bits, depending on the resolution of the ADC). This way, these signals can be observed in ADI's Visual Analog software tool.

The digitized data, LMFC, and SYSREF are displayed independently in Visual Analog so the end-to-end latency can be observed and measured. For each JESD204B/C mode, these observations and measurements are made in both subclass 0 and subclass 1 modes. In subclass 1 mode, it is confirmed that the relationship between SYSREF and the LMFC and the end-to-end latency are consistent across all power cycles. Figure 4 shows the Visual Analog display of this this test in subclass 1 mode. Note the latency measurement in the data displayed at the bottom of the data section on the left-hand side of the display.

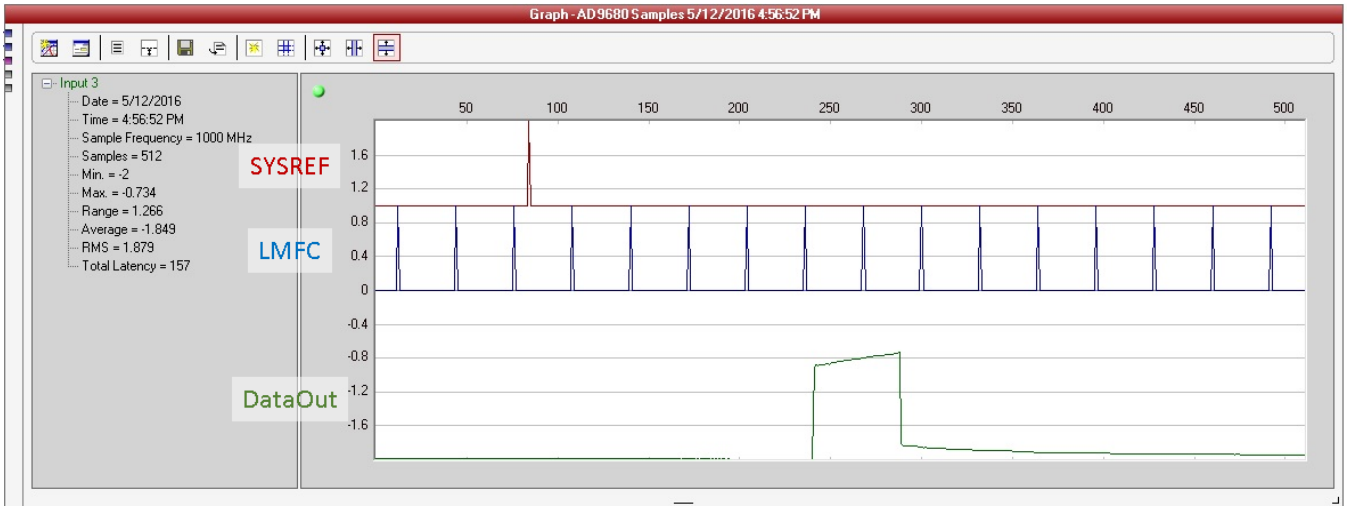

Figure 5: Graphical output of subclass 1 operation in Visual Analog

Conclusion

ADI works closely with Xilinx to ensure compatibility and inter-operability between our converter devices and the Xilinx FPGAs and JESD204B/C IP.

Users of ADI converter products and Xilinx FPGAs can be assured that inter-operability requirements have been thoroughly vetted so that users can focus on higher level system requirements. This vetting is achieved through the following:

- Strategic roadmap planning and alignment of interface technology
- Thorough testing against the JESD204B/C standard
- Converter testing with Xilinx FPGAs and the latest JESD204B/C IP that covers every aspect of the JESD204B/C link operation