

Coupling a Single-Ended Clock Source to the Differential Clock Input of Third-Generation TxDAC[®] and TxDAC+[®] Products

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INTRODUCTION

The third-generation TxDAC and TxDAC+ families* feature a flexible differential clock input. The differential clock inputs CLK+ and CLK- can be driven from a variety of single-ended and differential clock sources. Transformer coupling is useful in many single-ended-to-differential applications. However, a magnetically coupled transformer may not be convenient in some situations. A single-ended clock signal may be coupled to the clock inputs in a variety of ways. The CLK+ input can be driven while a suitable dc threshold voltage is applied to CLK- as shown in Figure 1. Resistors R1 and R2, along with capacitor C3, generate a dc level equal to CLKVDD/2 for the CLK- terminal. The clock source must be unipolar and swing nearly rail-to-rail. Although simple, this configuration does not provide the proper termination impedance for the source and has almost no immunity to noise on either the power supply or ground.

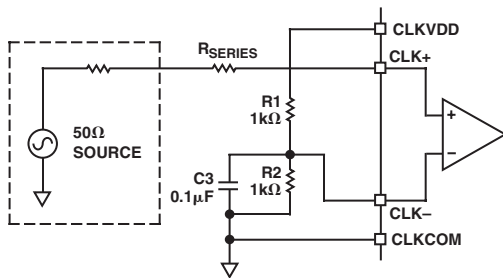


Figure 1. Single-Ended Interface

A somewhat better alternative is a simple broadband resistive matching network (Figure 2). As shown in Figure 1, resistors R1 and R2 and Capacitor C3 create the dc bias point at CLKVDD/2. Resistors R3 and R4 provide dc bias for the differential inputs CLK+ and CLK-. A termination resistor, R_{TERM} (50Ω) provides the required source termination, while capacitors C1 and C2 provide dc blocking. The termination resistor should preferably be placed directly across the input pins, CLK+ and CLK-, where it serves to lower the possible deleterious effects of dc offset voltages for smaller clock signal amplitudes. At low frequencies, this may not be quite as attractive since it necessitates the use of larger coupling capacitors. Unlike the circuit in Figure 1, the input source can be bipolar, and there is at least some rejection of supply and ground noise by virtue of the large ratio of R3 and R4 to the 50Ω R_{TERM}. However, the way in which the

common side of the coupling capacitor C2 is connected could adversely inject noise onto the CLK- input. Ideally, it should be connected at the same common point as the clock source (see Figure 2).

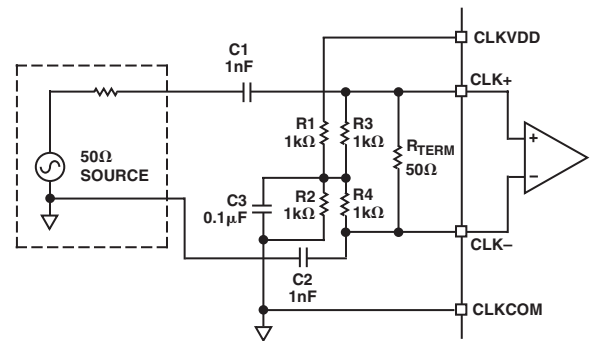


Figure 2. Resistive Matching Interface

The two 1 nF input coupling capacitors, C1 and C2, set the high-pass corner frequency of the network at approximately 5 MHz. The high-pass corner frequency can be set higher or lower according to the equation

$$f_{3dB} = \frac{1}{2\pi \times C \times 50}$$

where $C = \frac{C1 \times C2}{C1 + C2}$

NARROW-BAND MATCHING

Transformer coupling is useful in broadband applications. However, often in converter applications, the clock is at a single fixed frequency. At high clock frequencies or if the clock source is remote from the converters where it might pick up interference along its path, it is often preferable to use a narrow-band matching network. A narrow-band LC match can be implemented either as a series-inductance/shunt-capacitance or as a series-capacitance/shunt-inductance. However, the concurrent requirement that the clock inputs, CLK+ and CLK-, be ac-coupled makes

*AD9740ACP, AD9742ACP, AD9744ACP, AD9748ACP, AD9751, AD9753, AD9755, AD9772, AD9773, AD9775, AD9777

a series-capacitance/shunt-inductance type match more appropriate (see Figure 3).

There are several advantages to a band-pass network such as this. Some amount of voltage gain can be achieved because the input impedance of the differential inputs is high and almost purely capacitive. This can provide increased noise immunity when lower amplitude clock signals are all that is available. The component count is low: two capacitors and one inexpensive chip inductor in addition to the components needed to create the dc bias.

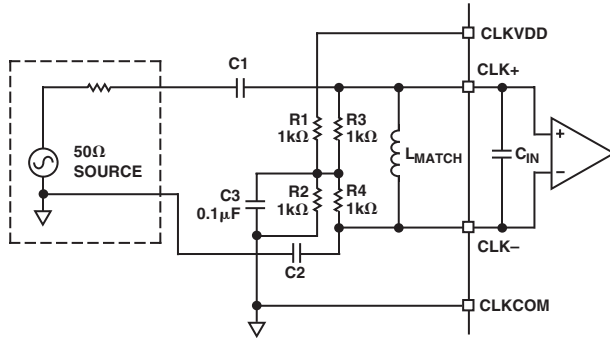


Figure 3. LC Matching Interface

A NARROW-BAND LC MATCHING EXAMPLE AT 100 MHz

While numerous software programs are available that allow the values of matching components to be easily calculated, a clear understanding of the calculations involved is valuable. A frequency value of 100 MHz has been used for this exercise because of the effects of PC board layout parasitics at higher frequencies. RF layout simulation software is useful when board design at higher frequencies is required.

Typically, the clock inputs will need to be matched to 50 Ω. To make the matching process simpler, the input capacitance of the CLK+ and CLK- inputs, C_{IN} , can be temporarily removed from the calculation by adding a virtual shunt inductor (L_2 , see Figure 4), which will resonate with C_{IN} at the desired frequency. This inductor will be factored into the determination of the matching inductor L_{MATCH} later (Figure 3). This allows the main calculation to be based on a simple resistive-to-resistive match between the 50 Ω source and the 1 kΩ dc bias resistors.

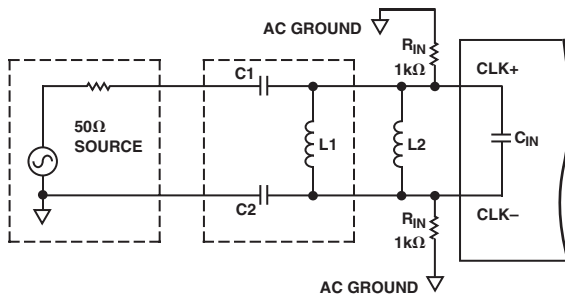


Figure 4. Input Matching Example

The resonant frequency is defined by the equation

$$2\pi \times f_0 = \frac{1}{\sqrt{L_2 \times C_{IN}}}$$

Therefore

$$L_2 = \frac{1}{(2\pi \times f_0)^2 \times C_{IN}}$$

For a center frequency of 100 MHz and $C_{IN} = 2.5$ pF, $L_2 = 1.01$ μH.

With C_{IN} temporarily out of the way, the calculation to match the 50 Ω source (R_S) to the 1 kΩ dc bias resistor (R_{IN}) and calculating values for C_{MATCH} and L_1 can take place.

When
$$R_S \times R_{IN} = \frac{L_1}{C_{MATCH}}$$

The input will look resistive at the frequency given by

$$f_0 = \frac{1}{2\pi \sqrt{L_1 \times C_{MATCH}}}$$

Solving for C_{MATCH} gives:

$$C_{MATCH} = \frac{1}{2\pi \times f_0 \sqrt{R_S \times R_{IN}}}$$

For $f_0 = 100$ MHz, $R_S = 50$ Ω, $R_{IN} = 1$ kΩ, $C_{MATCH} = 7.12$ pF

Next solving for L_1 gives:

$$L_1 = \frac{\sqrt{R_S \times R_{IN}}}{2\pi \times f_0}$$

For $f_0 = 100$ MHz, $R_S = 50$ Ω, $R_{IN} = 1$ kΩ, $L_1 = 356$ nH.

Because L_1 and L_2 are in parallel, they can be combined to give the final value for L_{MATCH}

$$L_{MATCH} = \frac{L_1 \times L_2}{L_1 + L_2}$$

with $L_1 = 356$ nH and $L_2 = 1.01$ μH, $L_{MATCH} = 263$ nH.

C_1 and C_2 can be chosen in a number of ways. First, C_2 can be set to a large value, such as 1000 pF, so that it appears as an RF short. C_1 would then be set equal to the calculated value of C_{MATCH} . Alternatively, C_1 and C_2 can each be set to twice C_{MATCH} so that the total series capacitance is equal to C_{MATCH} . By making C_1 and C_2 slightly unequal (i.e., select C_2 to be about 10% less than C_1) but keeping their series value the same, the amplitude of the signals on CLK+ and CLK- can be equalized so that the differential input is driven in a more balanced manner. Any one of the three options detailed above can be used as long as the combined series value of C_1 and C_2 (i.e., $(C_1 \times C_2)/(C_1 + C_2)$) is equal to C_{MATCH} .

In all cases, the values of C_{MATCH} (C1, C2) and L_{MATCH} must be chosen from standard values. The closest standard values are C1 = 16 pF, C2 = 15 pF, and L_{MATCH} = 270 nH (shown in Table I). At this point, these values now need to be installed and measured for performance at 100 MHz. Because of board and layout parasitics, the component values from the above example may need to be adjusted.

Further, by making these capacitors unequal, the amplitudes at CLK+ and CLK- may be equalized when driving from a single-sided source; that is, the network also serves as a balun. Figure 5 shows the response for a center frequency of 100 MHz; note the very high attenuation at low frequencies. The high frequency attenuation is due to the input capacitance of the clock input pins. The amplitude response is plotted differentially across CLK+ and CLK- as well as single ended for each input with respect to common. Due to the resonant nature of the matching network, there will be a phase shift of approximately 90° at the CLK+ and CLK- inputs. This is plotted in Figure 6. Care must be taken to account for this phase difference when adjusting the converter data setup and hold timing.

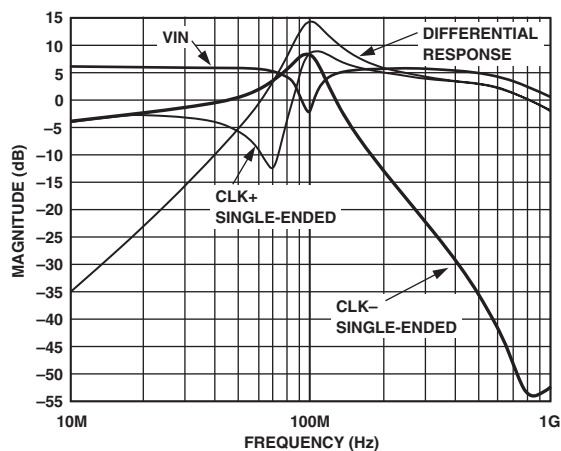


Figure 5. Amplitude Response of 100 MHz Matching Network

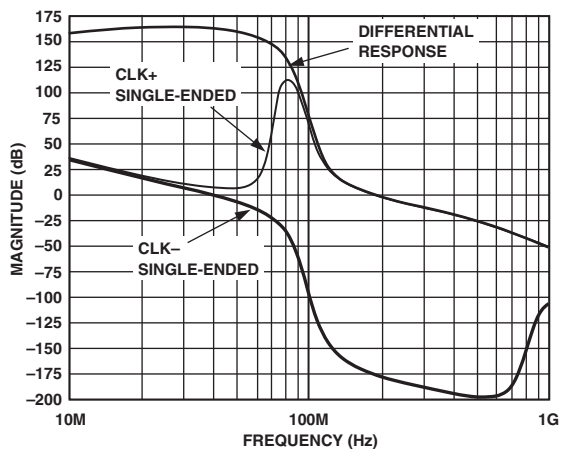


Figure 6. Phase Response of 100 MHz Matching Network

Table I shows the recommended values for the inductor and capacitors in Figure 3 for some selected RF frequencies. As previously discussed, a modification of the board layout will produce networks that may not perform as specified.

Table I. Recommended Values for C1, C2, and L_{MATCH} in Figure 4

Frequency (MHz)	L_{MATCH} (nH)	C1 (pF)	C2 (pF)
61.44	470	24	22
65.00	470	24	18
76.80	390	18	16
78.00	390	18	15
78.64	390	16	16
92.16	330	13	12
100.00	270	16	15
122.88	220	11	10
130.00	180	12	11
153.60	150	10	9
156.00	150	10	8
157.29	120	12	12
184.32	120	8	7
245.76	82	6	5
260.00	56	9	8
307.20	47	7	6
312.00	47	6	6
314.57	47	6	6
368.64	39	5	4
491.52	22	5	4
520.00	18	6	5
614.40	15	4	4
624.00	15	4	3
629.15	15	4	3
737.28	12	2	2

APPENDIX 1

Modeling and simulating this interface network with Spice is a useful alternative to the hand calculations shown here. It also allows the inclusion of more parasitic effects from such things as the package and PC board traces. The listing that follows is a Spice level subcircuit model for the clock input structure. Referring to the schematics in Figures 7 and 8 and in the top level of the listing, inductor L1 and capacitors C1 and C2 determine the center frequency of the network. The values listed are for a frequency of 100 MHz. Resistor R1 is the driving source (V3) impedance and resistors R2 and R3 provide the dc bias (set by voltage source V4) for the ac-coupled inputs.

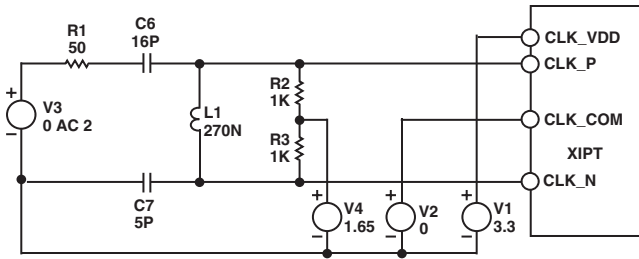


Figure 7. SPICE Model for Input Network

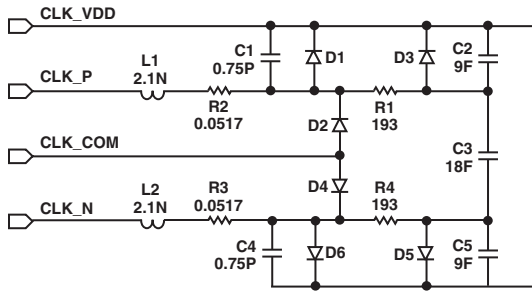


Figure 8. SPICE Subcircuit for XIPT Block

LISTING 1

Clock Input Matching Network Model
*

```
V1 CLK_VDD 0 3.3
V2 CLK_COM 0 0
V3 SRC_P 0 0 AC 2
V4 CML 0 1.65
R1 SRC_P CAP_P 50
R2 CLK_P CML 1K
R3 CLK_N CML 1K
C1 CAP_P CLK_P 16p
C2 CLK_N 0 15p
L1 CLK_P CLK_N 270n
XXIPT CLK_P CLK_N CLK_COM CLK_VDD CLK_INPUT
.SUBCKT CLK_INPUT CLK_P CLK_N CLK_COM CLK_VDD
C1 CLK_VDD C1_B 0.75p
C2 CLK_VDD C2_B 9f
C3 C2_B C3_B 18f
C4 CLK_VDD C4_B 0.75p
C5 CLK_VDD C3_B 9f
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```
D1 C1_B CLK_VDD DP1 1
D2 CLK_COM C1_B DN2 1
D3 C2_B CLK_VDD DP3 1
D4 CLK_COM C4_B DN2 1
D5 C3_B CLK_VDD DP3 1
D6 C4_B CLK_VDD DP1 1
L1 L1_A CLK_P 2.1n
L2 L2_A CLK_N 2.1n
R1 C2_B C1_B 193
R2 C1_B L1_A 0.0517
R3 C4_B L2_A 0.0517
R4 C3_B C4_B 193
.ENDS CLK_INPUT
```

```
.model DP1 D (bv=5.5 cjo=1.17088p eg=1.106 fc=500m
ibv=608.2p is=1.299342f m=632.669m)
.model DP3 D (bv=5.5 cjo=325.2446f eg=1.106 fc=500m
ibv=608.2p is=3.609284e-16 m=632.669m)
.model DN2 D (bv=8.0 ibv=1.54587E-06 cjo=1.411p
m=0.3675268 is=1.759f eg=1.140)
.AC DEC 400 10E6 1E9
.PROBE
.OP
.END
```

APPENDIX 2

Spice models for chip capacitors and inductors are available from manufacturers. Figure 9 is a common one used for inductors; Figure 10 is a common subcircuit used in model capacitors.

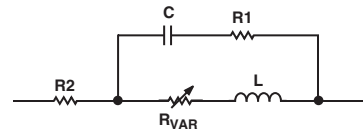


Figure 9.

Values for these models can be obtained from manufacturers' websites, such as www.coilcraft.com. R_{VAR} in Figure 9 is frequency dependent and relates to the skin effect and other inductor losses.

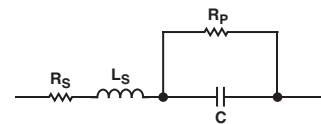


Figure 10.