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Evaluating the AD9740, AD9742, AD9744, and AD9748 TxDAC Product Family

FEATURES

High performance member of pin-compatible TxDAC product family
Excellent SFDR performance
Twos complement or straight binary data format
Differential current outputs: 2 mA to 20 mA
Power dissipation: 135 mW at 3.3 V
Power-down mode: 15 mW at 3.3 V
On-chip 1.2 V reference
CMOS-compatible digital interface
32-lead LFCSP package
Edge triggered latches

EVALUATION KIT CONTENTS

USB cable
Ribbon cable
AD9740ACP-PCBZ/AD9742ACP-PCBZ/AD9744ACP-PCBZ/AD9748ACP-PCBZ evaluation board
AD-DAC-FMC-ADP board
CMOS DAC/DPG2 board

EQUIPMENT NEEDED

System demonstration platform (SDP-H1) controller board (EVAL-SDP-CH1Z)
AD9740ACP-PCBZ/AD9742ACP-PCBZ/AD9744ACP-PCBZ/AD9748ACP-PCBZ evaluation board
3 coaxial cables
SMA tee adapter female to male to female
Spectrum analyzer
Signal generator
DC power supply
PC running Windows® 98 (2nd edition), Windows 2000, Windows ME, or Windows XP operating system (OS)

SOFTWARE NEEDED

DPGDownloader

GENERAL DESCRIPTION

The AD9740ACP-PCBZ/AD9742ACP-PCBZ/AD9744ACP-PCBZ/AD9748ACP-PCBZ evaluation board allows users to easily set up and test the 32-lead lead frame chip scale package (LFCSP) of the AD9740, AD9742, AD9744, and AD9748 devices. Paying careful attention to layout and circuit design, combined with a prototyping area, allows the user to effectively evaluate the AD9740, AD9742, AD9744, and AD9748 in applications that require high resolution and high speed conversion.

The AD9740ACP-PCBZ/AD9742ACP-PCBZ/AD9744ACP-PCBZ/AD9748ACP-PCBZ evaluation board provide flexibility to operate the AD9740, AD9742, AD9744, and AD9748 in various configurations. Possible output configurations include transformer coupled, resistor terminated, and single and differential outputs. The digital inputs are driven from various word generators, and an on-board option can add a resistor network for proper load termination. Users can use the power-down feature of the AD9740, AD9742, AD9744, and AD9748 and can select clock and data modes.

The AD9740, AD9742, AD9744, and AD9748 are wideband, 3G members of the TxDAC® series of high performance, low power CMOS, digital-to-analog converters (DACs). The TxDAC family, consisting of pin-compatible 14-, 12-, 10-, and 8-bit DACs, is specifically optimized for the transmit signal path of communication systems. All the devices share the same interface options, small outline package, and pinout. The AD9740, AD9742, AD9744, and AD9748 also provide an upward or downward component selection path based on performance, resolution, and financial cost. The AD9740, AD9742, AD9744, and AD9748 offer exceptional ac and dc performance while supporting update rates up to 210 MSPS.

The low power dissipation of the AD9740, AD9742, AD9744, and AD9748 makes these devices well suited for portable and low power applications. Lowering the full-scale output current further reduces the power dissipation to 60 mW, with only a slight degradation in performance. Power-down mode also reduces the standby power dissipation to approximately 15 mW. A segmented current source architecture is combined with a proprietary switching technique to reduce spurious components and enhance dynamic performance. Edge triggered input latches and a 1.2 V temperature compensated band gap reference are integrated to provide a complete, monolithic DAC solution. The digital inputs support 3 V logic families.

For more information about the AD9740, AD9742, AD9744, and AD9748, refer to the corresponding data sheets. Consult the data sheets in conjunction with this user guide when using the AD9740ACP-PCBZ/AD9742ACP-PCBZ/AD9744ACP-PCBZ/AD9748ACP-PCBZ evaluation board.

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REVISION HISTORY

3/2020—Rev. 0 to Rev. A

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Change to Figure 29 ... 15

1/2020—Revision 0: Initial Version

EVALUATION BOARD PHOTOGRAPH

Figure 1.

EVALUATION BOARD HARDWARE

COMPONENT FUNCTIONALITIES

The AD9740ACP-PCBZ/AD9742ACP-PCBZ/AD9744ACP-PCBZ/AD9748ACP-PCBZ evaluation board consists of a DAC, digital control logic, and full-scale output current control. The DAC contains a positive channel metal-oxide semiconductor (PMOS) current source array capable of providing up to 20 mA of full-scale current (I_{OUTFS}).

The PMOS current source array is divided into the following three segments: the MSBs, intermediate significant bits (ISBs), and LSBs. Together, these segments generate a current proportional to the value of the input data sample. The five uppermost bits, the MSBs, are made up of 31 equal current sources. The next four bits, the ISBs, consist of 15 equal current sources that are 1/16th of a single MSB current source. The remaining LSBs are binary weighted fractions of a single ISB.

Implementing the ISBs and LSBs with current sources, instead of an R-2R ladder, enhances the DAC dynamic performance for multitone or low amplitude signals and helps maintain a high output impedance that is greater than 100 kΩ.

All these PMOS current sources are switched to either of the two output pins, IOUTA or IOUTB, via the PMOS differential current switches. The switches are based on architecture pioneered in the AD9764 family with further refinements to reduce distortion contributed by the switching transient. This switch architecture also reduces various timing errors and provides matching complementary drive signals to the inputs of the differential current switches.

The analog and digital section of the AD9740, AD9742, AD9744, and AD9748 have the following separate power supply input pins: the AVDD (the positive analog supply) and the DVDD. These power supply inputs operate independently over a 2.7 V to 3.6 V range. The digital section, which operates at rates up to 210 MSPS, consists of edge triggered latches and segment decoding logic circuitry. The analog section includes the PMOS current sources, the associated differential switches, a 1.2 V band gap voltage reference, and a reference control amplifier.

The DAC full-scale output current is regulated by the reference control amplifier and can be set from 2 mA to 20 mA via an external resistor, R_{SET}, connected to the full-scale adjust (FS ADJ) pin. R_{SET}, in combination with the reference control amplifier and the voltage reference (V_{REFIO}), sets the reference current (I_{REF}). I_{REF} is then replicated to the segmented current sources with the proper scaling factor, resulting in $I_{OUTFS} = 32 \times I_{REF}$.

REFERENCE OPERATION

The AD9740, AD9742, AD9744, and AD9748 contain an internal 1.2 V band gap reference. The internal reference cannot be disabled but can be overridden by an external reference with no effect on performance. Figure 2 shows an equivalent circuit of the band gap reference. The REFIO pin serves as either an output or input, depending on whether an internal or external reference is used. To use the internal reference, decouple the REFIO pin to the analog common (ACOM) with a 0.1 µF capacitor and connect the REFLO pin to ACOM via a resistance less than 5 Ω. The internal reference voltage is present at the REFIO pin. If the voltage at the REFIO pin is needed elsewhere in the circuit, use an external buffer amplifier with an input bias current less than 100 nA. See Figure 3 for an example of how to use the internal reference.

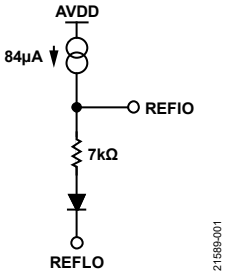

Figure 2. Equivalent Circuit of Internal Band Gap Reference

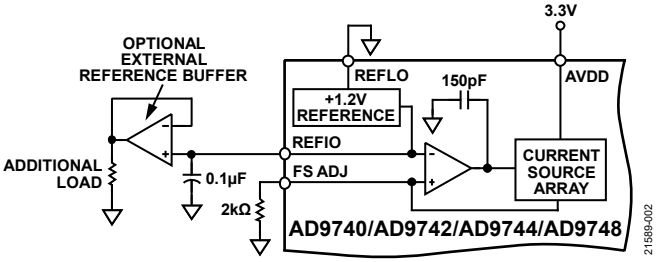

Figure 3. Internal Reference Configuration

An external reference can be applied to the REFIO pin as shown in Figure 4. The external reference can provide either a fixed reference voltage to enhance accuracy and drift performance, or a varying reference voltage for gain control. Note that the 0.1 µF compensation capacitor is not required because the internal reference is overridden, and the high input impedance of the REFIO pin minimizes any unnecessary loading of the external reference.

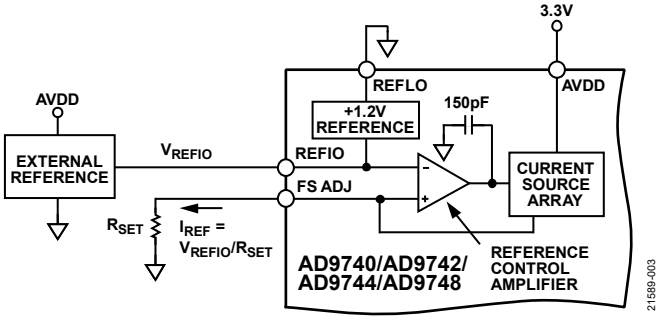

Figure 4. External Reference Configuration

REFERENCE CONTROL AMPLIFIER

The AD9740, AD9742, AD9744, and AD9748 contain a control amplifier that regulates I_{OUTFS}. The control amplifier is configured as a voltage to current (V-I) converter (see Figure 3) so that the V_{REFIO} to R_{SET} ratio, which is defined in Equation 4, can determine I_{REF}. I_{REF} is then copied to the segmented current sources with the proper scale factor to set I_{OUTFS} as detailed in Equation 3.

The control amplifier allows a wide I_{OUTFS} adjustment span (10:1) over the 2 mA to 20 mA range by setting I_{REF} between 62.5 µA and 625 µA. The I_{OUTFS} wide adjustment span has several benefits. First, the gain of the output signal can be set across a 20 dB adjustment range. Second, control over the power dissipation of the AD9740, AD9742, AD9744, and AD9748, which is proportional to I_{OUTFS} (see the Power Dissipation section).

The small signal bandwidth of the control amplifier is approximately 500 kHz and is used in low frequency, small signal multiplying applications.

DAC TRANSFER FUNCTION

The AD9740, AD9742, AD9744, and AD9748 generate the I_{OUTA} and I_{OUTB} currents from the IOUTA and IOUTB pins, respectively. The current delivered to the load is the difference between I_{OUTA} and I_{OUTB}, and the current is a function of both the input DAC sample code and I_{OUTFS}. When all bits are high, that is, when the DAC code = 16383, I_{OUTA} is nearly equal to I_{OUTFS} and I_{OUTB} is 0 mA. Conversely, when the DAC code = 0, I_{OUTA} is 0 mA and I_{OUTB} is equal to I_{OUTFS}. The following equation(s) express the relationship between I_{OUTA} and I_{OUTB}:

$$I_{OUTA} = (DAC\ CODE/16384) \times I_{OUTFS} \quad (1)$$

$$I_{OUTB} = (16383 - DAC\ CODE)/16384 \times I_{OUTFS} \quad (2)$$

where *DAC CODE* = 0 to 16383, which is the decimal representation.

As described in the DAC Transfer Function section, I_{OUTFS} is a function of I_{REF}, which is nominally set by V_{REFIO} and R_{SET}. The following equation expresses I_{OUTFS}:

$$I_{OUTFS} = 32 \times I_{REF} \quad (3)$$

where the following equation expresses I_{REF}:

$$I_{REF} = V_{REFIO}/R_{SET} \quad (4)$$

The IOUTA and IOUTB pins typically drive a resistive load (R_{LOAD}) directly or via a transformer. If dc coupling is required, connect each IOUTA pin and IOUTB pin to a matched R_{LOAD} that is then tied to ACOM. Note that R_{LOAD} represents the total equivalent load resistance seen by IOUTA or IOUTB, which can be lower in a doubly terminated 50 Ω or 75 Ω cable. The following equations express the single-ended voltage output at the IOUTA pin (V_{OUTA}) and the IOUTB pin (V_{OUTB}):

$$V_{OUTA} = I_{OUTA} \times R_{LOAD} \quad (5)$$

$$V_{OUTB} = I_{OUTB} \times R_{LOAD} \quad (6)$$

Note that the full-scale value of V_{OUTA} and V_{OUTB} must not exceed the specified output compliance range, see the AD9740, AD9742, AD9744, and AD9748 data sheets for more information, to maintain the specified distortion and linearity performance. The following equation defines the differential voltage (V_{DIFF}) across the load:

$$V_{DIFF} = (I_{OUTA} - I_{OUTB}) \times R_{LOAD} \quad (7)$$

Combining the values of I_{OUTA}, I_{OUTB}, I_{REF}, and V_{DIFF} from Equation 1 through Equation 4 results in the following equation:

$$V_{DIFF} = ((2 \times DAC\ CODE - 16{,}383)/16{,}384) \times (32 \times R_{LOAD}/R_{SET}) \times V_{REFIO} \quad (8)$$

Equation 7 and Equation 8 show the advantages to operating the AD9740, AD9742, AD9744, and AD9748 differentially. Differential operation helps cancel common-mode error sources associated with I_{OUTA} and I_{OUTB}, such as noise, distortion, and dc offsets. In addition, the differential code dependent current and V_{DIFF} is twice the value of the single-ended voltage output (V_{OUTA} or V_{OUTB}), which provides twice the signal power to the load.

Note that users can enhance the gain drift temperature performance for a single-ended V_{OUTA}, V_{OUTB}, or V_{DIFF} of the AD9740, AD9742, AD9744, and AD9748 by selecting temperature tracking resistors for R_{LOAD} and R_{SET}. This enhancement is due to the ratiometric relationship of R_{LOAD} and R_{SET} that is shown in Equation 8.

ANALOG OUTPUTS

The IOUTA pin and the IOUTB pin can be configured for single-ended or differential operation. The IOUTA pin and the IOUTB pin can be converted into V_{OUTA} and V_{OUTB} via R_{LOAD}, as described in the Reference Control Amplifier section.

As described in the DAC Transfer Function section, V_{DIFF} exists between V_{OUTA} and V_{OUTB} and a transformer or differential amplifier configuration converts V_{DIFF} to a single-ended voltage. The ac performance of the AD9740, AD9742, AD9744, and AD9748 is optimum and specified using a differential transformer coupled output in which the voltage swing at the IOUTA pin and the IOUTB pin is limited to ±0.5 V.

The distortion and noise performance of the AD9740, AD9742, AD9744, and AD9748 are enhanced when the devices are configured for differential operation. The common-mode error sources of both the IOUTA pin and the IOUTB pin is reduced by the common-mode rejection of the transformer or differential amplifier. These common-mode error sources include even order distortion products and noise.

The enhancement distortion performance becomes more significant as the frequency content of the reconstructed waveform increases and/or the amplitude decreases. This effect exists because of the first-order cancellation of various dynamic common-mode distortion mechanisms, digital feedthrough, and noise.

Performing a differential to single-ended conversion via a transformer makes it possible to deliver twice the reconstructed signal power to the load, assuming no source termination. Because the output currents of the IOUTA and the IOUTB pins are complementary, the currents become additive when processed differentially. A properly selected transformer allows the AD9740, AD9742, AD9744, and AD9748 devices to supply the required power and voltage levels to different loads.

The equivalent, parallel combination of PMOS switches associated with the current sources (typically 100 kΩ in parallel with 5 pF) determine the output impedance of the IOUTA and the IOUTB pins. The IOUTB pin output impedance also depends on V_{OUTA} and V_{OUTB} because of the nature of the PMOS device. As a result, maintaining the IOUTA pin and/or the IOUTB pin at a virtual ground via an I-V op amp configuration results in optimum dc linearity.

To achieve optimum performance, maintain the output voltage swing within the voltage compliance range of the IOUTA and IOUTB pins. The negative output compliance range of −1 V is set by the breakdown limits of the CMOS process. Operation beyond this maximum limit can result in an output stage breakdown and affects the reliability of the AD9740, AD9742, AD9744, and AD9748.

The positive output compliance range is dependent on I_{OUTFS}, and this compliance range degrades from the nominal 1.2 V at I_{OUTFS} = 20 mA to 1 V at I_{OUTFS} = 2 mA. The optimum distortion performance for a single-ended or differential output is achieved when the maximum full-scale signal at the IOUTA and the IOUTB pins does not exceed 0.5 V.

DIGITAL INPUTS

The AD9740, AD9742, AD9744, and AD9748 digital section consists of a clock input and a 10-, 12-, 14-, or 8-bit input channel, respectively. The parallel data inputs follow standard positive binary coding where DB0 is the LSB. The IOUTA pin produces a full-scale output current when all data bits are at Logic 1. The IOUTB pin produces a complementary output with the full-scale current split between the two outputs as a function of the input DAC code.

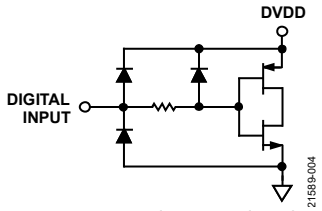

Figure 5. Equivalent Digital Mode

The digital interface is implemented using an edge triggered latch, as shown in Figure 5. The DAC output updates on the rising edge of the clock and supports a clock rate as high as 210 MSPS. The clock can operate at any duty cycle that meets the specified latch pulse width (see the corresponding AD9740, AD9742, AD9744, and AD9748 data sheets for more information). The setup and hold times can vary within the clock cycle as long as the specified minimum times are met (see the corresponding AD9740, AD9742, AD9744, and AD9748 data sheets for more information), although the location of the transition edges can affect digital feedthrough and distortion performance. Optimum performance is typically achieved when the input data transitions on the falling edge of a 50% duty cycle clock.

CLOCK INPUT

LFCSP

A configurable sample clock input is available in the LFCSP that can accommodate single-ended mode and two differential modes. The CMODE pin controls the mode selection, as detailed in Table 1.

Connecting the CMODE pin to the CLKCOM pin selects the single-ended clock input mode. In this mode, the CLK+ pin is driven with rail-to-rail swings, and the CLK− pin is left floating (see Figure 6).

If the CMODE pin is connected to the CLKVDD pin, a high impedance differential receiver mode is selected. In this mode, both the CLK+ and CLK− pins are high impedance.

If the CMODE pin is left floating, a positive emitter-coupled logic (PECL) differential receiver mode is selected. The internal PECL terminator are activated in this mode.

There is no significant performance difference among any of the three clock input modes.

Table 1. Clock Mode Selection

CMODE Pin Connection	Clock Input Mode
CLKCOM	Single-ended
CLKVDD	High impedance differential receiver
Floating	PECL differential receiver

In high impedance differential mode, the clock input functions as a high impedance differential pair. The common-mode level of the CLK+ and the CLK− pins can vary from 0.75 V to 2.25 V, and the differential voltage can be as low as 0.5 V p-p. The CLK+ and CLK− pins can be driven with a differential sine wave, as opposed to a square wave, because the high gain bandwidth of the differential inputs internally converts the sine wave into a single-ended square wave, resulting in a better slew rate.

The PECL mode allows fewer external components when the DAC clock is distributed using PECL logic levels. Figure 6 shows the internal termination configuration. These termination resistors are untrimmed and can vary up to ±20%. However, the matching between the resistor pair is generally within ±1%.

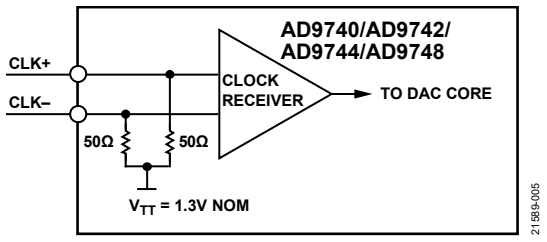

Figure 6. Clock Termination in PECL Mode

DAC TIMING

Input Clock and Data Timing Relationship

Dynamic performance in a DAC depends on the relationship between the clock edge position and the time at which the input data changes. The AD9740, AD9742, AD9744, and AD9748 are rising edge triggered and, therefore, exhibit dynamic performance sensitivity when the data transitions are close to this edge. In general, the goal when applying the AD9740, AD9742, AD9744, and AD9748 is to make the data transitions close to the falling clock edge, which becomes more important as the sample rate increases. Figure 7 shows the relationship between the spurious-free dynamic range (SFDR) and clock placement with different sample rates. Note that at lower sample rates, clock placements are more tolerant. However, at higher rates, take more care with clock placements.

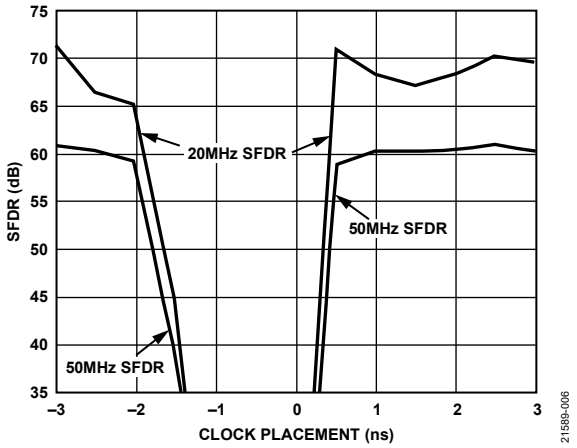

Figure 7. SFDR vs. Clock Placement at Output Frequency (f_{OUT}) = 20 MHz and 50 MHz (Lines Connect Outside the Plot)

Sleep Mode Operation

The AD9740, AD9742, AD9744, and AD9748 have a power-down function that turns off the output current and reduces the supply current to less than 6 mA over the specified supply range (2.7 V to 3.6 V) and temperature range specified in the AD9740, AD9742, AD9744, and AD9748 data sheets. Activate power-down by applying a Logic Level 1 to the SLEEP pin. The SLEEP pin logic threshold is equal to AVDD/2. The AVDD pin contains an active pull-down circuit that ensures that the AD9740, AD9742, AD9744, and AD9748 remain enabled, even if this pin is left disconnected. The AD9740, AD9742, AD9744, and AD9748 take less than 50 ns to power down and approximately 5 µs to power back up.

POWER DISSIPATION

The power dissipation of the AD9740, AD9742, AD9744, and AD9748 is dependent on the following factors: the power supply voltages of the AVDD, CLKVDD, and DVDD pins, the I_{OUTFS}, the clock rate (f_{CLOCK}), and the reconstructed digital input waveform.

The power dissipation is directly proportional to the analog supply current (I_{AVDD}), the digital supply current (I_{DVDD}), and to a lesser extent, to the clock supply current (I_{CLKVDD}). I_{AVDD} is directly proportional to I_{OUTFS}, as shown in Figure 8, and is insensitive to f_{CLOCK}. Conversely, I_{DVDD} is dependent on both the digital input waveform, f_{CLOCK}, and the DVDD pin. Figure 9 shows I_{DVDD} as a function of full-scale sine wave output ratios (f_{OUT}/f_{CLOCK}) for various update rates with the DVDD pin = 3.3 V. Figure 10 shows a minor contribution to I_{CLKVDD}, which depends on the clock input mode.

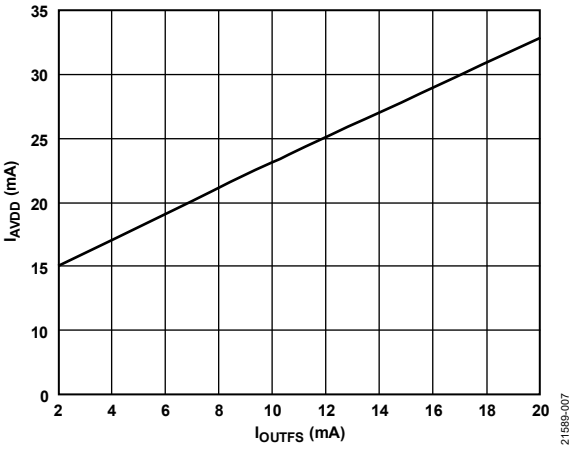

Figure 8. I_{AVDD} vs. I_{OUTFS}

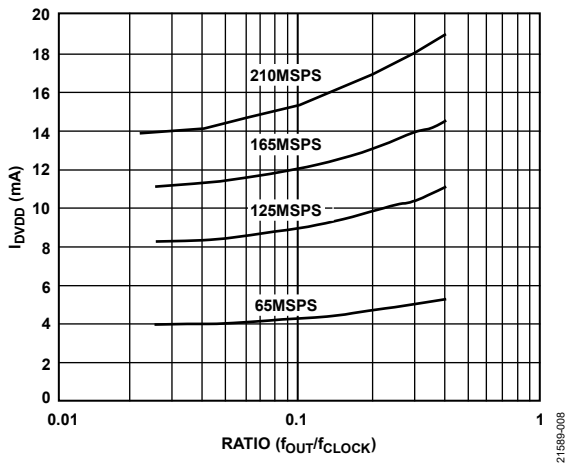

Figure 9. I_{DVDD} vs. Ratio (f_{OUT}/f_{CLOCK}) at DVDD = 3.3 V

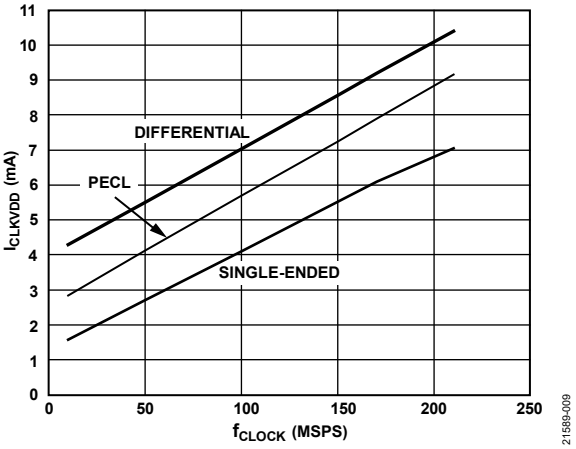

Figure 10. I_{CLKVDD} vs. f_{CLOCK} and Clock Mode

APPLYING THE AD9740, AD9742, AD9744, AND AD9748

Output Configurations

The following sections describe the typical output configurations for the AD9740, AD9742, AD9744, and AD9748. Unless otherwise noted, I_{OUTFS} is set to a nominal 20 mA. For applications requiring the optimum dynamic performance, users are recommended to use a differential output configuration. A differential output configuration can consist of either an RF transformer or a differential op amp configuration. The transformer configuration provides the optimum high frequency performance and is recommended for any application that allows ac coupling. The differential op amp configuration is suitable for applications requiring dc coupling, a bipolar output, signal gain, and/or level shifting within the bandwidth of the chosen op amp.

A single-ended output is suitable for applications requiring a unipolar voltage output. A positive unipolar output voltage results from connecting the IOUTA pin and/or the IOUTB pin to an appropriately sized R_{LOAD} that maintains the output within the compliance range. This R_{LOAD} is referenced to ACOM. This configuration is more suitable for a single-supply system requiring a dc-coupled, ground referred output voltage. Alternatively, an amplifier can be configured as an I-V converter, which converts I_{OUTA} or I_{OUTB} into a negative unipolar voltage. This configuration provides the best dc linearity, see the Single-Ended, Buffered Voltage Output Configuration section for more information.

DIFFERENTIAL COUPLING USING A TRANSFORMER CONFIGURATION

An RF transformer performs a differential to single-ended signal conversion, as shown in Figure 11. A differentially coupled transformer output provides the optimum distortion performance for output signals that contain spectral content in the pass band of the transformer. An RF transformer rejects common-mode distortion such as even order harmonics and noise over the operating frequency range. The RF transformer also provides electrical isolation and can deliver twice the power to the load. Transformers with different impedance ratios can be used for impedance matching purposes. Note that the transformer only provides ac coupling.

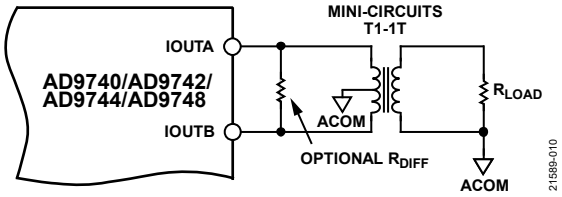

Figure 11. Differential Output Using an RF Transformer

The center tap on the primary side of the transformer must be connected to ACOM to provide the necessary dc current path for both the IOUTA pin and the IOUTB pin. V_{OUTA} and V_{OUTB} swing symmetrically around ACOM and must be maintained with the specified output compliance range of the AD9740, AD9742, AD9744, and AD9748, see the corresponding data sheets for more information.

A differential resistor, R_{DIFF}, can be added in applications where the DAC output drives a transformer (a balun) that is connected to a passive reconstruction filter or a long cable run ahead of a mismatched load impedance. Determine the value of R_{DIFF} such that the differential load seen from the IOUTA and IOUTB pins is maintained near 50 Ω. The total load impedance is equal to the parallel combination of R_{DIFF} and the impedance from the transformer input. Adjust R_{DIFF} for specific applications by optimizing the voltage standing wave radio (VSWR) at the output of the designed circuit. Note that approximately half the signal power is dissipated across R_{DIFF}.

DIFFERENTIAL COUPLING USING AN OP AMP CONFIGURATION

An op amp can perform a differential to single-ended conversion, as shown in Figure 12. The AD9740, AD9742, AD9744, and AD9748 are configured with two equal R_{LOAD}s of 25 Ω. The V_{DIFF} is developed across the IOUTA pin, and the IOUTB pin is converted to a single-ended signal via the differential op amp configuration.

Install an optional capacitor across the IOUTA and the IOUTB pins to form a real pole in the low-pass filter. Adding this optional capacitor enhances the distortion performance of the op amp by preventing the high slewing output of the DAC from overloading the op amp input.

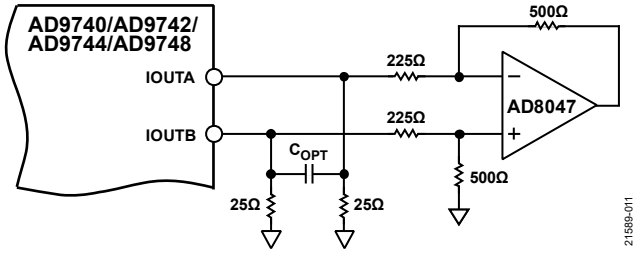

Figure 12. DC Differential Coupling Using an Op Amp

The common-mode rejection of this configuration is typically determined by how well the resistor values are matched. In this circuit, the differential op amp circuit using the AD8047 is configured to provide additional signal gain. The op amp must operate off a dual supply because the output is approximately ±1 V. Select a high speed amplifier to preserve the differential performance of the AD9740, AD9742, AD9744, and AD9748 and to meet other system level objectives such as cost or power. Consider the differential gain of the op amp, gain setting resistor values, and full-scale output swing capabilities when optimizing a particular circuit.

The differential circuit shown in Figure 13 provides the necessary level shifting required in a single-supply system. In this case, the AVDD pin and the op amp level shift the differential output of the AD9740, AD9742, AD9744, and AD9748 to midsupply (that is, AVDD/2). The AD8041 is a suitable op amp for this application.

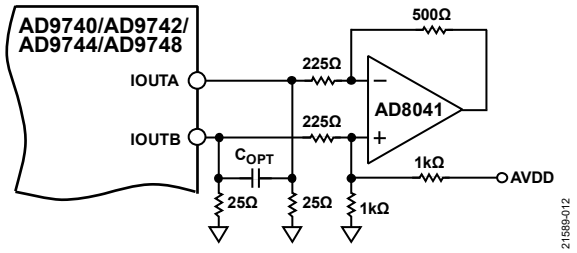

Figure 13. Single-Supply DC Differential Coupled Circuit

SINGLE-ENDED UNBUFFERED VOLTAGE OUTPUT CONFIGURATION

Figure 14 shows the AD9740, AD9742, AD9744, and AD9748 configured to provide a unipolar output range of approximately 0 V to 0.5 V to a doubly terminated 50 Ω cable because the nominal I_{OUTFS} (20 mA) flows through the equivalent R_{LOAD} of 25 Ω. In this case, R_{LOAD} represents the equivalent load resistance seen by the IOUTA pin or the IOUTB pin. The unused, complementary output pin (IOUTA or IOUTB) can be directly connected to ACOM or connected via a matching R_{LOAD}. Users can select different values of I_{OUTFS} and R_{LOAD} as long as users adhere to the positive compliance range, see the AD9740, AD9742, AD9744, and AD9748 data sheets for this range. For optimum integral nonlinearity (INL) performance, the single-ended, buffered voltage output configuration is recommended.

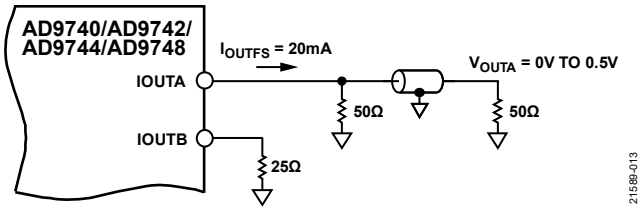

Figure 14. 0 V to 0.5 V Unbuffered Voltage Output

SINGLE-ENDED, BUFFERED VOLTAGE OUTPUT CONFIGURATION

Figure 15 shows a buffered single-ended output configuration in which the U1 op amp performs an I-V conversion on the output current of the devices. U1 maintains the IOUTA (or IOUTB) pin at a virtual ground, minimizing the nonlinear output impedance effect on the DAC INL performance as described in the Analog Outputs section. Although this single-ended configuration typically provides the best dc linearity performance, the ac distortion performance at higher DAC update rates can be limited by the U1 slew rate capabilities. U1 provides a negative unipolar output voltage and the full-scale output voltage is the product of the R_{FB} resistor (see Figure 15) and I_{OUTFS}. Set the full-scale output within the voltage output swing capabilities of U1 by scaling I_{OUTFS} and/or R_{FB}. The ac distortion performance can improve with a reduced I_{OUTFS} because the signal current of U1 is required to sink less signal current.

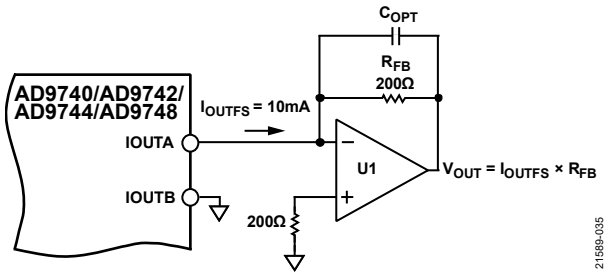

Figure 15. Unipolar Buffered Voltage Output

POWER AND GROUNDING CONSIDERATIONS, POWER SUPPLY REJECTION

Many applications require high performance under less than ideal operating conditions. In these applications, correctly designing and constructing the printed circuit board (PCB) is a vital part of the overall design. Use proper RF techniques for bypassing power supplies, grounding, and when selecting, placing, and routing the device.

A factor that can affect system performance is how the DAC output rejects dc variations or ac noise superimposed on the analog or digital dc power distribution. This rejection is referred to as the power supply rejection ratio (PSRR). For power supply dc variations, the resulting DAC performance corresponds to a gain error associated with the DAC I_{OUTFS}. AC noise on the dc supplies is common in applications where the power distribution is generated by a switching power supply. Switching power supply noise typically occurs over the spectrum from tens of kHz to several MHz. The AVDD PSRR vs. frequency is shown in Figure 16.

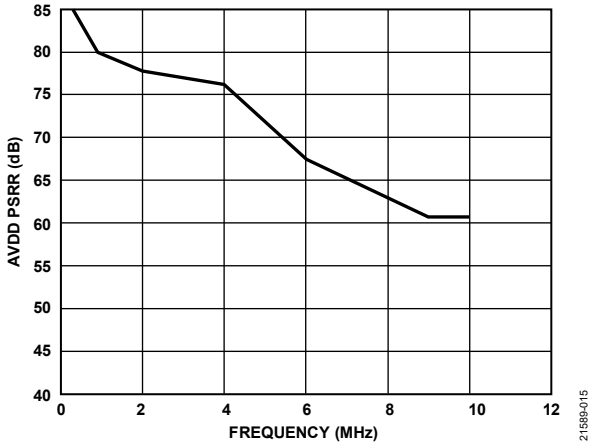

Figure 16. AVDD PSRR vs. Frequency

The ratio shown in Figure 16 is calculated as amps out with respect to volts in. Noise on the AVDD pin can modulate the internal switches and, therefore, modulate the output current. Therefore, the voltage noise on the AVDD pin is added in a nonlinear manner to the desired I_{OUTFS}.

Due to the different sizes of the internal switches, the PSRR is code dependent. This dependence can produce a mixing effect that modulates low frequency power supply noise to higher frequencies. The worst case PSRR for either differential DAC

output occurs when the full-scale current is directed toward that specific output. As a result, the PSRR measurement in Figure 16 represents a worst case condition where the digital inputs remain static, and the 20 mA full-scale output current is directed to the DAC output being measured.

To calculate how much of the power supply noise on AVDD appears as current noise superimposed on the DAC I_{OUTFS}, determine the PSRR at the frequency of interest. To calculate the PSRR for a current DAC, convert the PSRR from A/V to V/V. Adjust the curve in Figure 16 by a scaling factor of $20 \times \log(R_{LOAD})$. For example, if a switching regulator with a switching frequency of 250 kHz produces 10 mV of noise and, ignoring harmonics for simplicity, all the noise is concentrated at 250 kHz, the equivalent PSRR is 85 dB. If R_{LOAD} is 50 Ω, reduce PSRR by 34 dB, reducing the 81 dB at 250 kHz to 51 dB. As a result, the noise at the output is 51 dB lower than the 10 mV injected into the DAC.

Proper grounding and decoupling techniques are essential in any high speed, high resolution system. The AD9740, AD9742, AD9744, and AD9748 feature separate analog and digital supplies and ground pins to optimize the management of the analog and digital ground currents in a system.

In general, decouple AVDD to ACOM as close to the chip as physically possible. Similarly, decouple DVDD to DCOM as close to the chip as physically possible.

For applications that require a single 3.3 V supply for both the analog and digital supplies, generate a clean analog supply by using the circuit setup shown in Figure 17. The circuit consists of a differential inductor capacitor (LC) filter with separate power supply and return lines. Attain lower noise by using low equivalent series resistance (ESR) type electrolytic and tantalum capacitors.

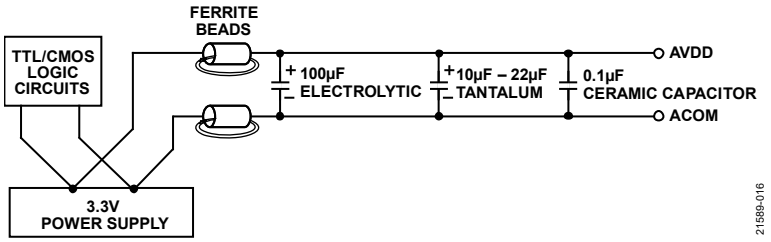

Figure 17. Differential LC Filter for Single 3.3 V Applications

EVALUATION BOARD SOFTWARE QUICK START PROCEDURES

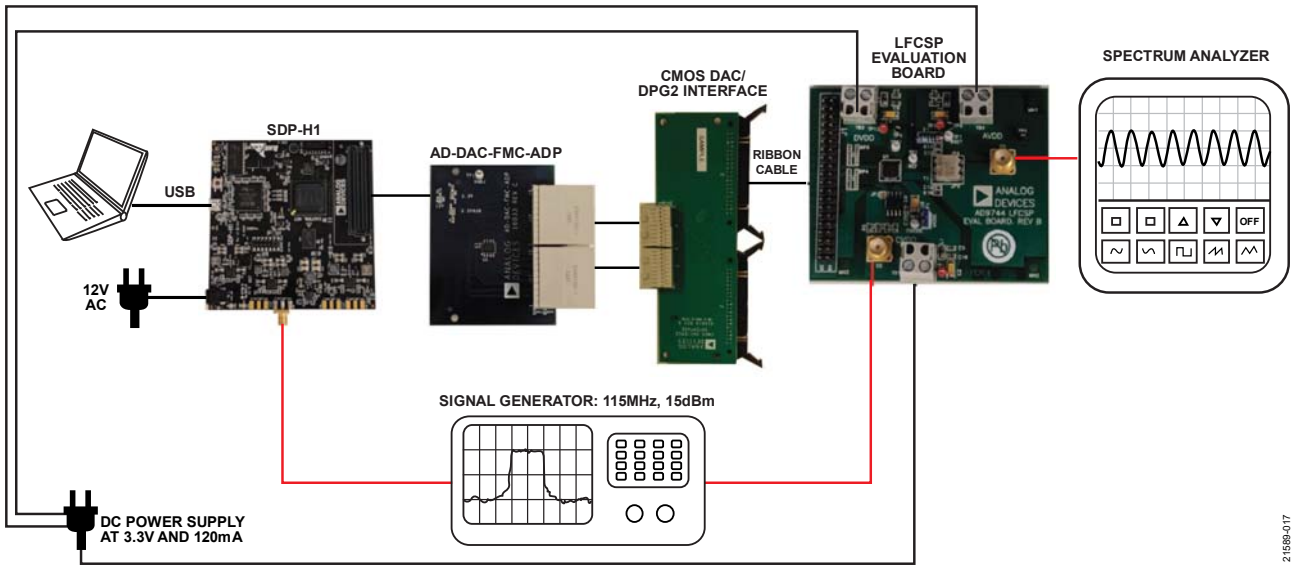

Figure 18. Hardware Connections

This section details the quick start procedures for using the AD9740ACP-PCBZ/AD9742ACP-PCBZ/AD9744ACP-PCBZ/AD9748ACP-PCBZ evaluation board. See Figure 18 for an overview on how to connect the hardware to evaluate the AD9740, AD9742, AD9744, and AD9748.

CONFIGURING THE LFCSP BOARD

Before setting up the **DPGDownloader** software, configure the AD9740ACP-PCBZ/AD9742ACP-PCBZ/AD9744ACP-PCBZ/AD9748ACP-PCBZ evaluation board with the following steps:

1. Ensure the JP1 jumper shunt is placed correctly on the evaluation board (circled in red in Figure 19).

Figure 19. Evaluation Board JP1 Jumper Shunt

2. Solder or install an edge mount Subminiature Version A (SMA) connector at J701 on the SDP-H1 (circled in red in Figure 20).

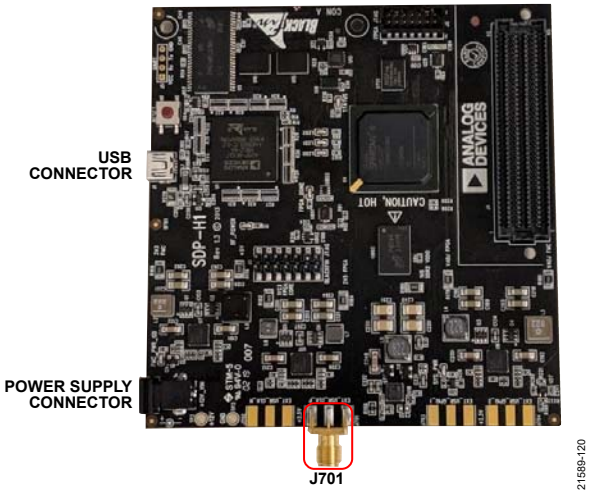

Figure 20. SDP-H1 Connectors

3. Connect a 12 V dc power supply to the power supply connector outlet on the SDP-H1, as shown in Figure 20.

4. Connect the provided USB cable from the PC to the USB connector on the SDP-H1.
5. Connect the AD-DAC-FMC-ADP board to the SDP-H1, as shown in Figure 24.
6. Connect the male interface of the CMOS DAC/DPG2 board to the AD-DAC-FMC-ADP female interface as shown in Figure 21.

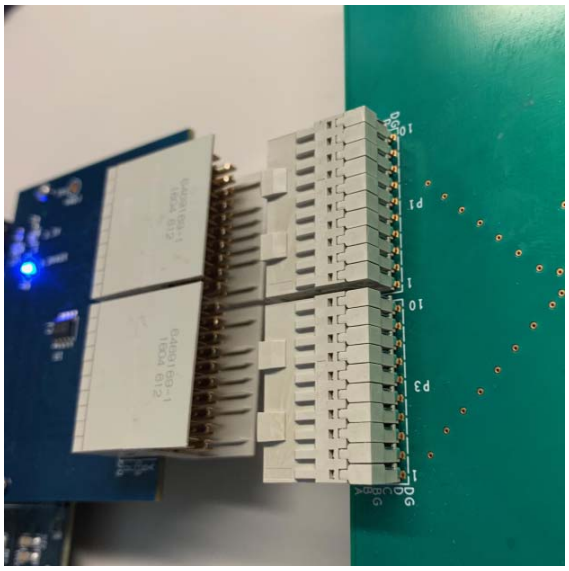

Figure 21. CMOS DAC/DPG2 Connected to AD-DAC-FMC-ADP

7. Connect a ribbon cable from the right side (P2) of the CMOS DAC/DPG2 board (supplied with the evaluation board) to J1 on the evaluation board. These connections are shown in Figure 24.
8. Connect one 3.3 V supply to the DVDD, AVDD, and CLKVDD connectors on the AD9740ACP-PCBZ/AD9742ACP-PCBZ/AD9744ACP-PCBZ/AD9748ACP-PCBZ evaluation board (see Figure 22).

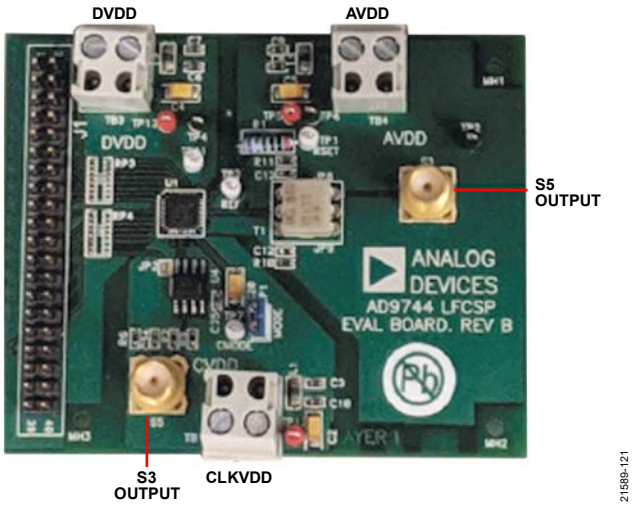

Figure 22. Evaluation Board Connectors

9. Connect an SMA tee adapter female to male to female (not provided in evaluation kit) to the output of a synthesized signal generator, as shown in Figure 25.
10. Connect a coaxial cable (shown in Figure 23) between one side of the SMA tee adapter and the J701 SMA port on the SDP-H1 (see Figure 20).

Figure 23. Coaxial Connector Cable

11. Connect a second coaxial cable between the clock input (S5) on the AD9740ACP-PCBZ/AD9742ACP-PCBZ/AD9744ACP-PCBZ/AD9748ACP-PCBZ evaluation board and the other side of the SMA tee adapter (see Figure 22).
12. Connect a third coaxial cable between the DAC output (S3) on the AD9740ACP-PCBZ/AD9742ACP-PCBZ/AD9744ACP-PCBZ/AD9748ACP-PCBZ evaluation board and the RF input on the spectrum analyzer (see Figure 26).
13. Set the synthesized signal generator frequency to 115 MHz with an amplitude of 15 dBm.
14. Apply power (3.3 V, 120 mA) to the AD9740ACP-PCBZ/AD9742ACP-PCBZ/AD9744ACP-PCBZ/AD9748ACP-PCBZ evaluation board.

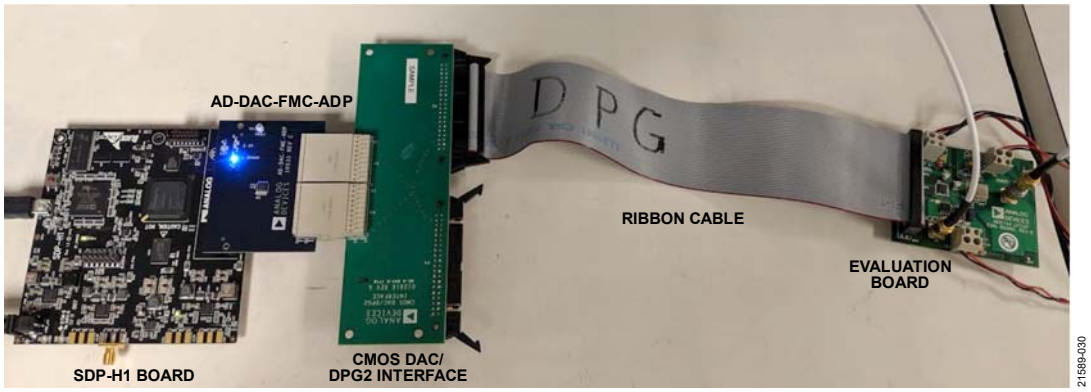

Figure 24. Hardware Setup

Figure 25. SMA Tee Adapter

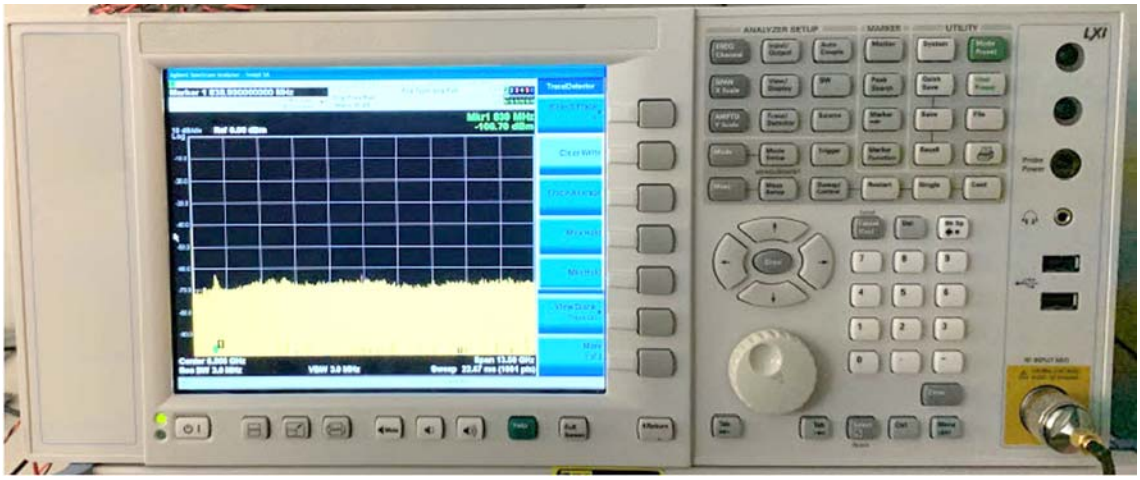

Figure 26. RF Input Connector on Spectrum Analyzer

DOWNLOADING AND SETTING UP THE DPGDOWNLOADER SOFTWARE

After configuring the AD9740ACP-PCBZ/AD9742ACP-PCBZ/AD9744ACP-PCBZ/AD9748ACP-PCBZ evaluation board, download and set up the **DPGDownloader** by using the following steps:

1. To download the **DPGDownloader** software, go to the DPG3 page and navigate to the **Software** section. Click on the **DAC Software Suite Download (Rev. 1.3.77. 154)** file.
2. After clicking the **.exe** file, run the installation wizard to install **DPGDownloader.**
3. Open the **DPGDownloader** software through **Start** > **Programs** > **Analog Devices** > **DPG** > **DPGDownloader** on the PC.
4. In the **DPGDownloader** window (see Figure 28), click the **Add Generated Waveform** dropdown menu and select **Single Tone** as the vector type.
5. Set the **Data Rate** field in this small window to **115.000 MHz** for 115 MHz (see Figure 27).

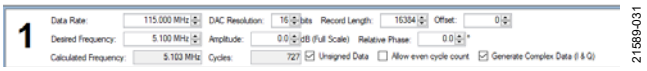

Figure 27. Single Tone Generation

6. Set the **Desired Frequency** field to **5.100 MHz** for 5.1 MHz (see Figure 27).
7. Set the **DAC Resolution** field to **16** (see Figure 27).
8. Select the **Unsigned Data** checkbox (see Figure 27).
9. Select the **Generate Complex Data (I & Q)** checkbox (see Figure 27).
10. In the **SDP-H1 Unit 1** panel (see Figure 29), select the **Generic** option from the **Evaluation Board** dropdown menu and select the **LVCMOS-3.3V** option from the **Port Configuration** dropdown menu.
11. In the **Data Playback** panel (see Figure 30), select the **1I: Single Tone - 5.201 MHz; 0.0 dB; 0.0° (In-Phase)** option from the **I Data Vector** dropdown menu.
12. Select the **1Q: Single Tone - 5.201 MHz; 0.0 dB; 0.0° (Quadrature)** option from the **Q Data Vector** dropdown menu (see Figure 30).
13. Click the **Download** button ( ) in the lower right of the **Data Playback** panel (see Figure 30).
14. Click the **Play** button ( ), located to the left of the **Download** button (see Figure 30), to begin vector playback.

The signal frequency output then appears on the spectrum analyzer.

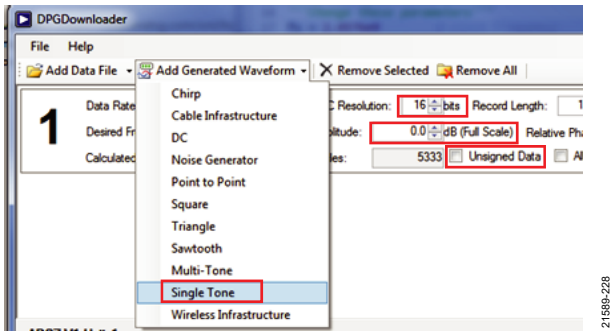

*Figure 28. Select **Single Tone***

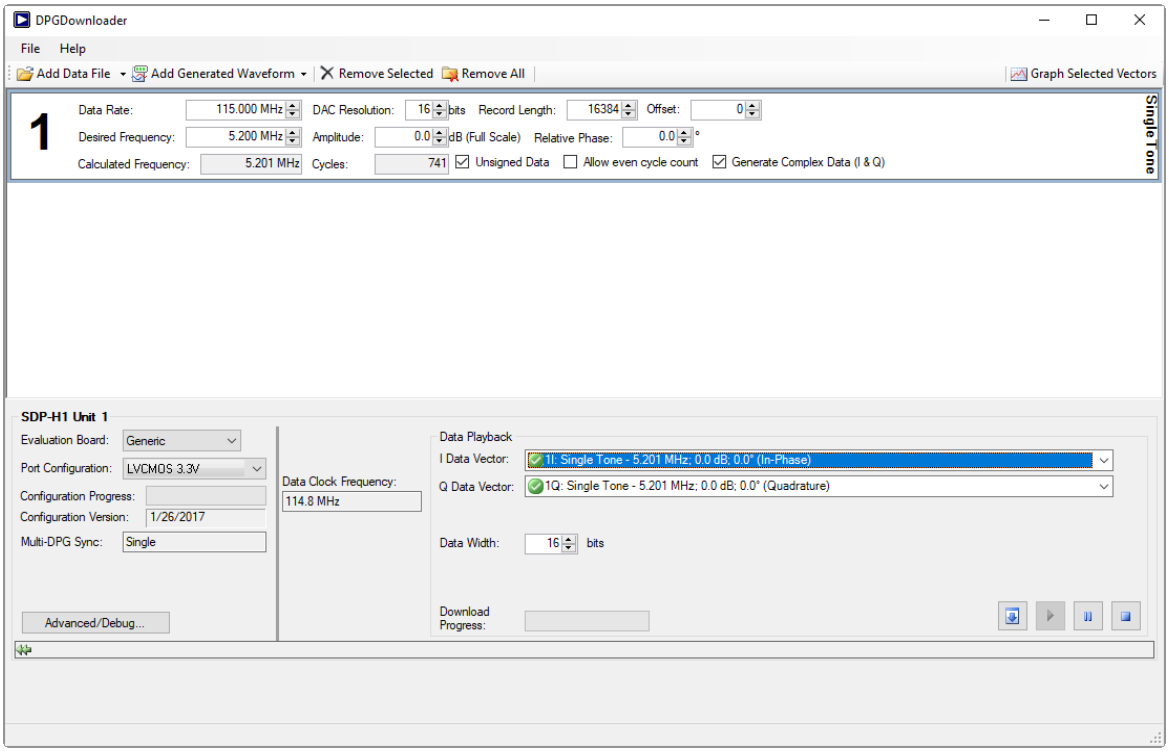

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*Figure 29. **SDP-H1 Unit 1** Panel*

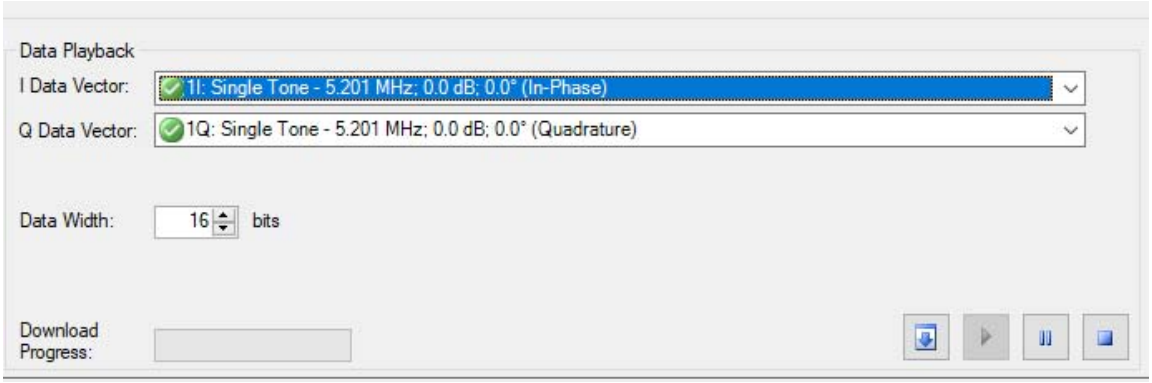

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Figure 30. Loading DPG2 Vectors

VERIFICATION

Figure 31 shows the spectrum analyzer output window that appears on the spectrum analyzer hardware (see Figure 26). Ensure that the following options are set:

1. Set the **Stop** frequency to **65.00 MHz**.
2. Set the **Ref** level to 0 dBm.
3. Set the **#Res BW** to 30 kHz.
4. Set the **VBW** to 30 kHz.
5. Check that the output from S3, the top left **Mrker1**, is approximately 5.200000000 MHz and check that the amplitude is approximately 0 dBm, the top right text (see Figure 31).

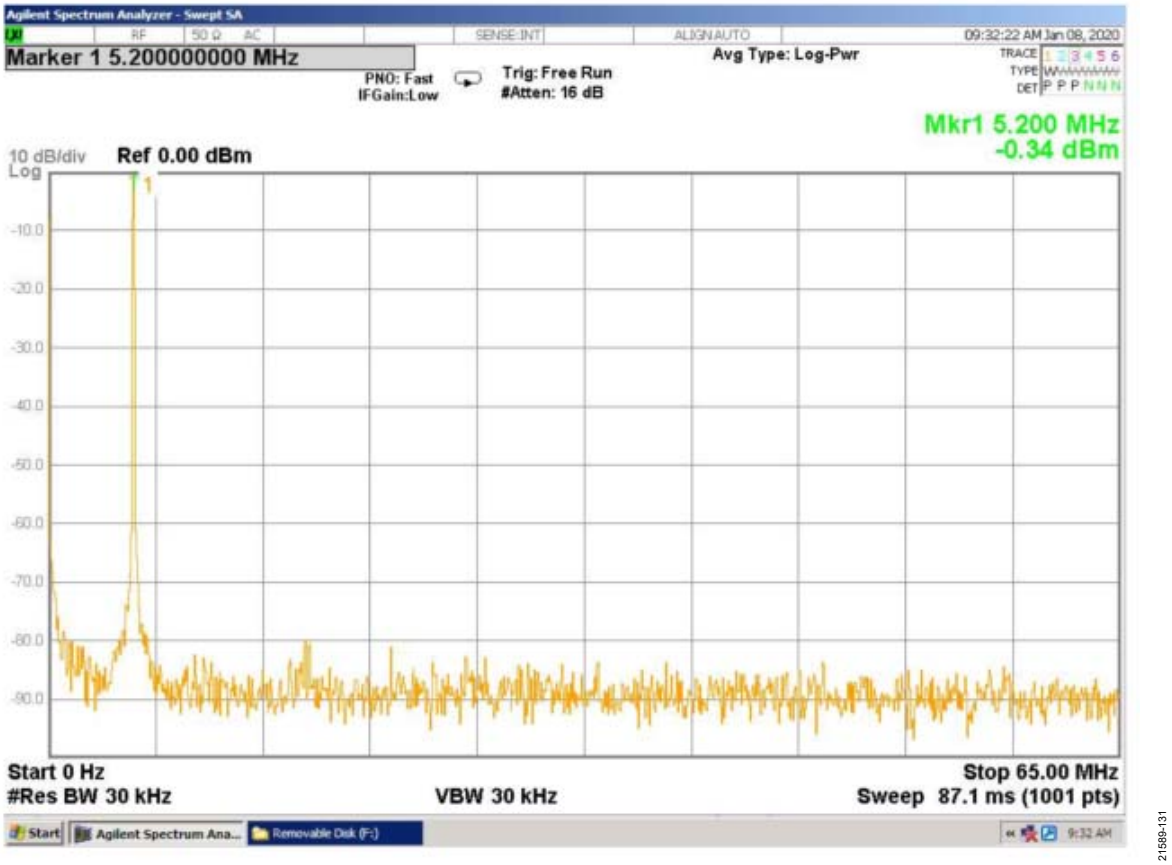

Figure 31. Spectrum Analyzer Output

EVALUATION BOARD SCHEMATICS

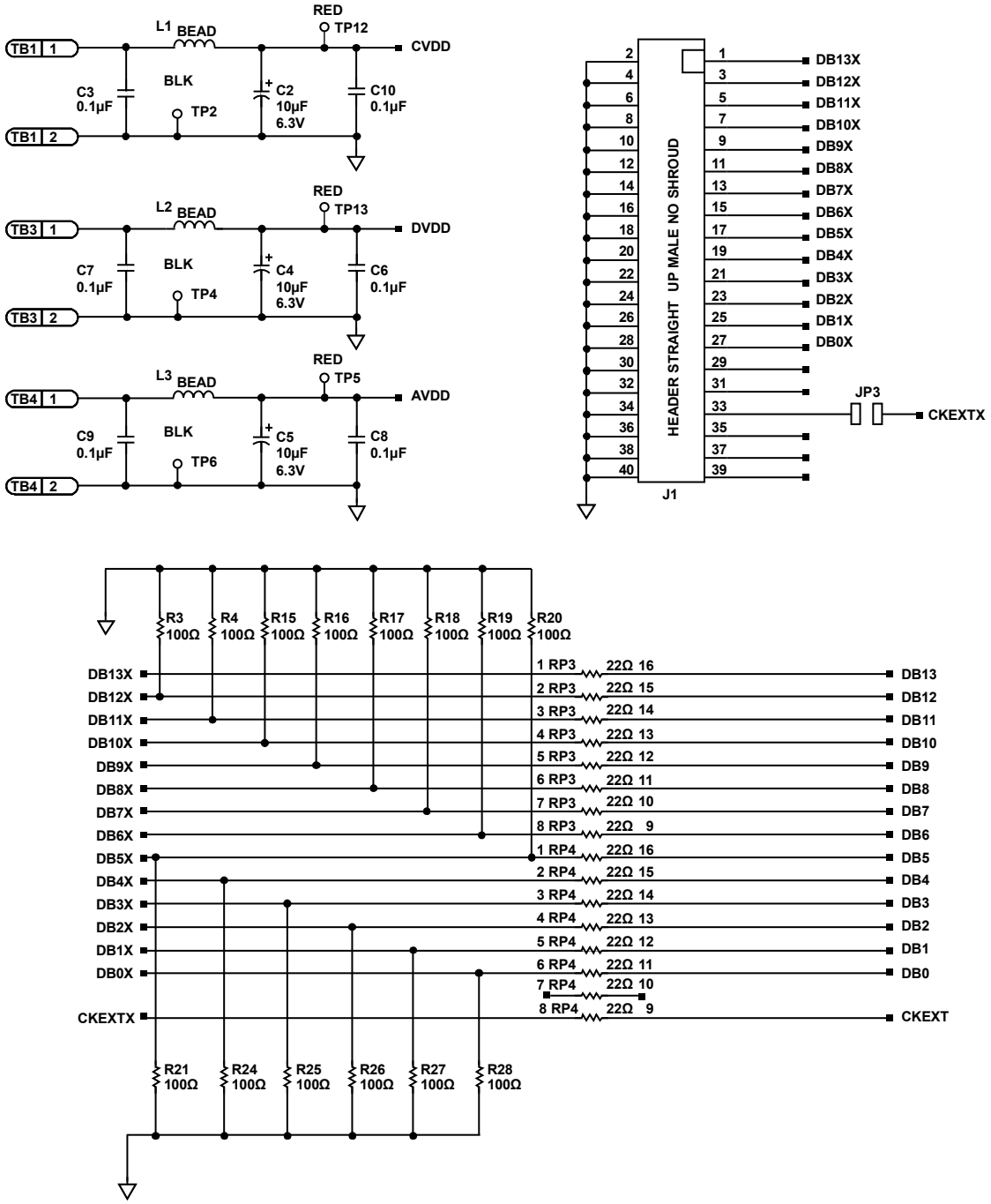

Figure 32. AD9740ACP-PCBZ/AD9742ACP-PCBZ/AD9744ACP-PCBZ/AD9748ACP-PCBZ LFCSP Evaluation Board Schematic—Power Supply and Digital Inputs

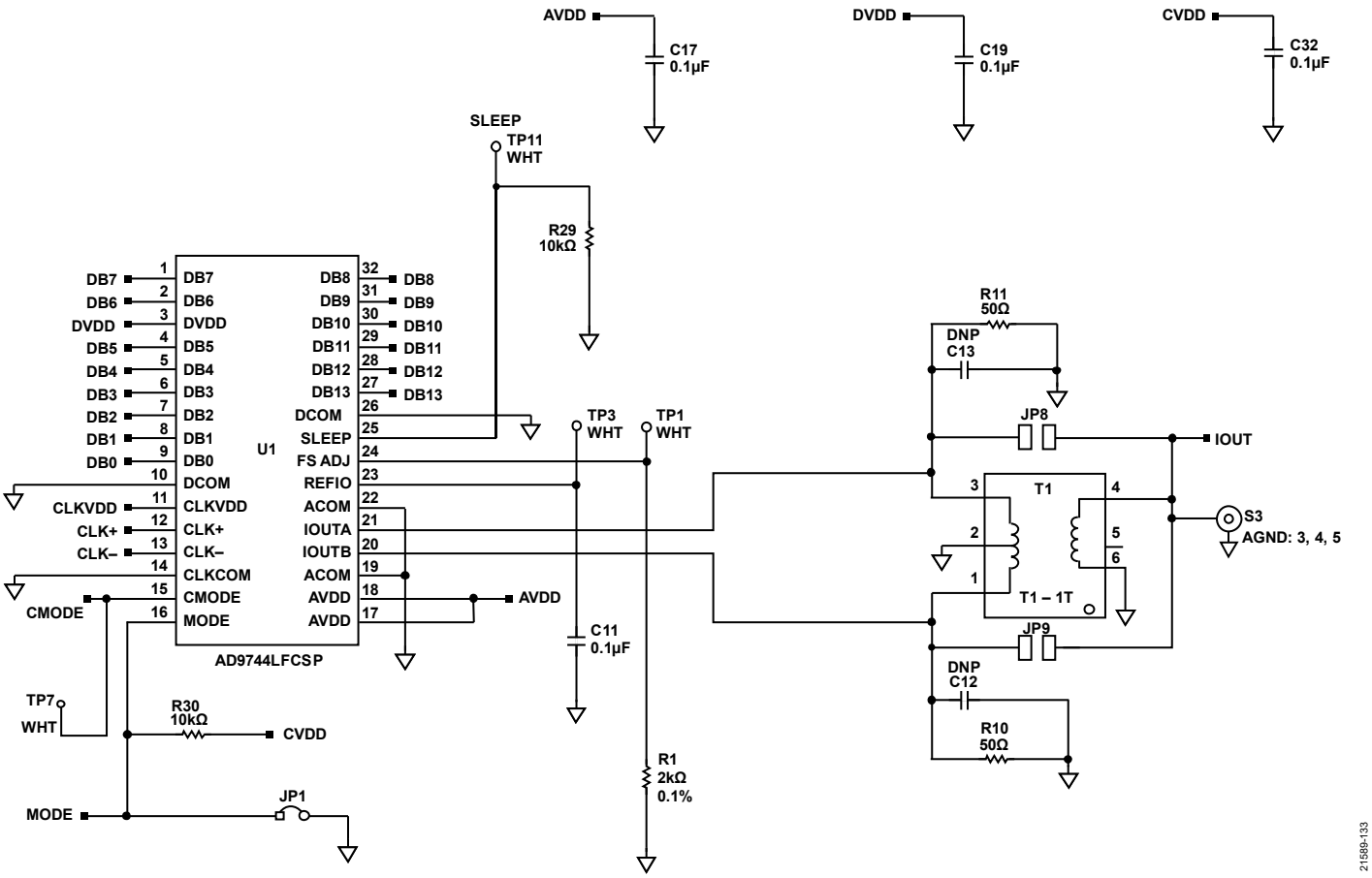

Figure 33. AD9740ACP-PCBZ/AD9742ACP-PCBZ/AD9744ACP-PCBZ/AD9748ACP-PCBZ LFCSP Evaluation Board Schematic—Output Signal Conditioning

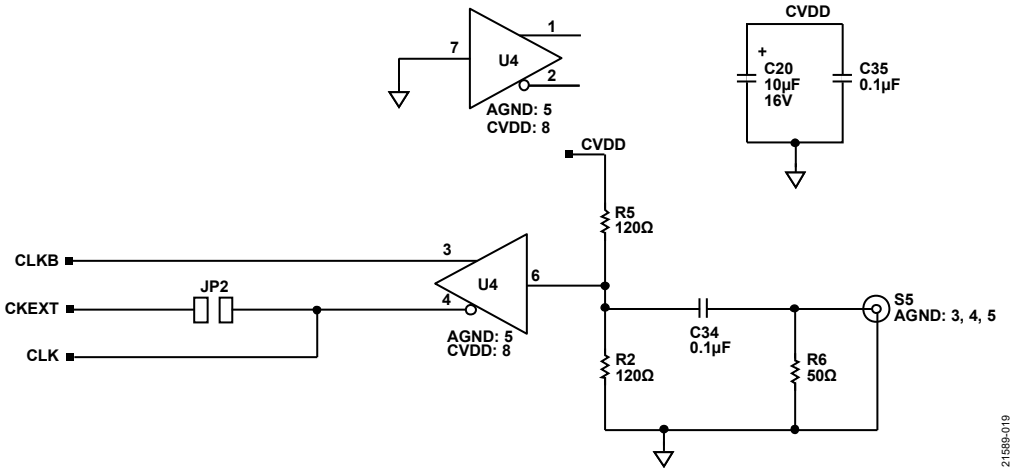

Figure 34. AD9740ACP-PCBZ/AD9742ACP-PCBZ/AD9744ACP-PCBZ/AD9748ACP-PCBZ LFCSP Evaluation Board Schematic—Clock Input

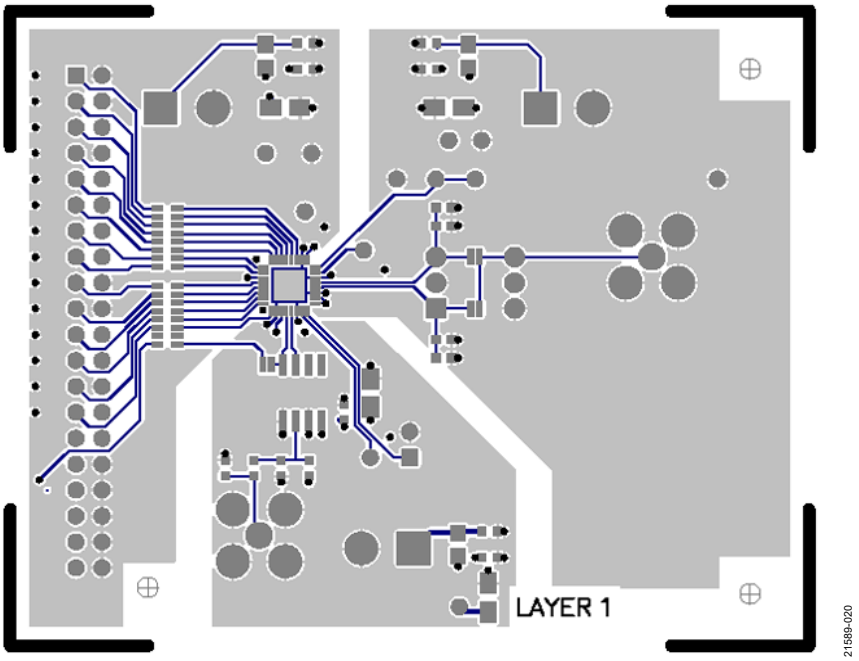

Figure 35. AD9740ACP-PCBZ/AD9742ACP-PCBZ/AD9744ACP-PCBZ/AD9748ACP-PCBZ LFCSP Evaluation Board Layout—Primary Side

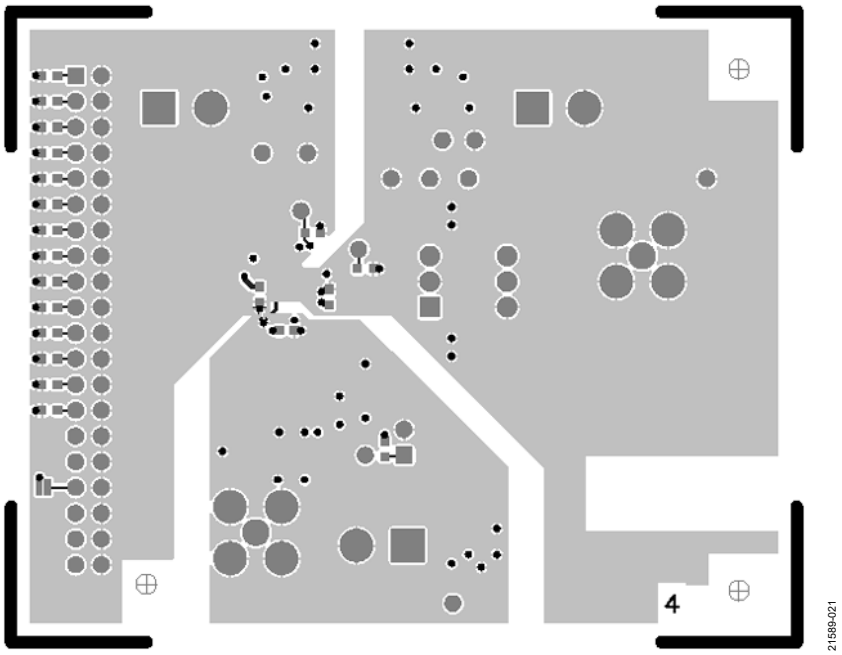

Figure 36. AD9740ACP-PCBZ/AD9742ACP-PCBZ/AD9744ACP-PCBZ/AD9748ACP-PCBZ LFCSP Evaluation Board Layout—Secondary Side

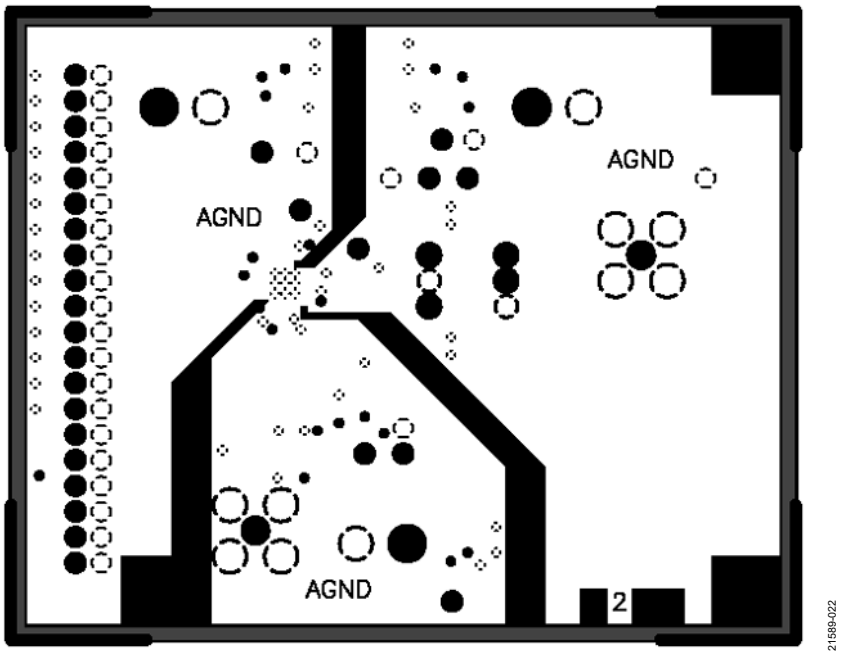

Figure 37. AD9740ACP-PCBZ/AD9742ACP-PCBZ/AD9744ACP-PCBZ/AD9748ACP-PCBZ LFCSP Evaluation Board Layout—Ground Plane

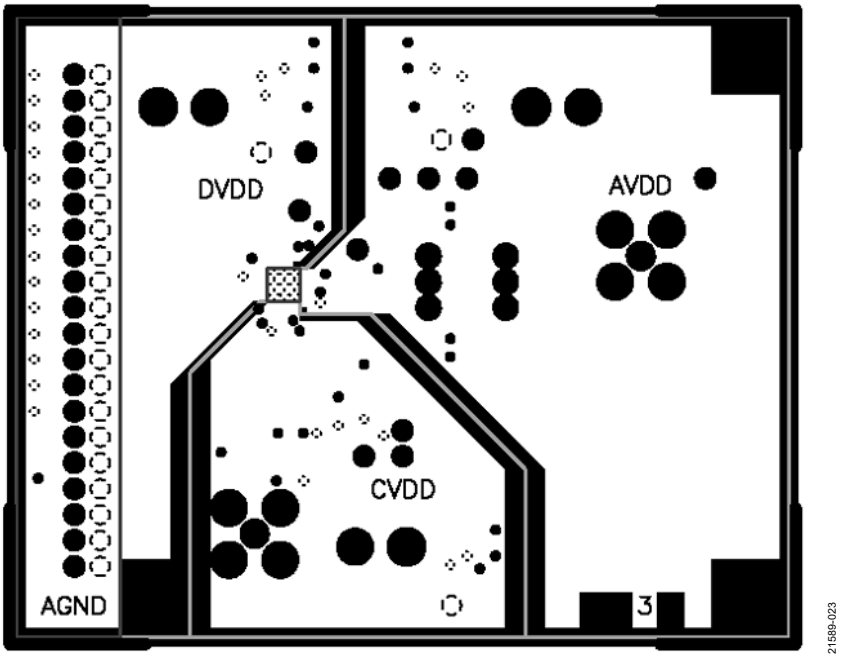

Figure 38. AD9740ACP-PCBZ/AD9742ACP-PCBZ/AD9744ACP-PCBZ/AD9748ACP-PCBZ LFCSP Evaluation Board Layout—Power Plane

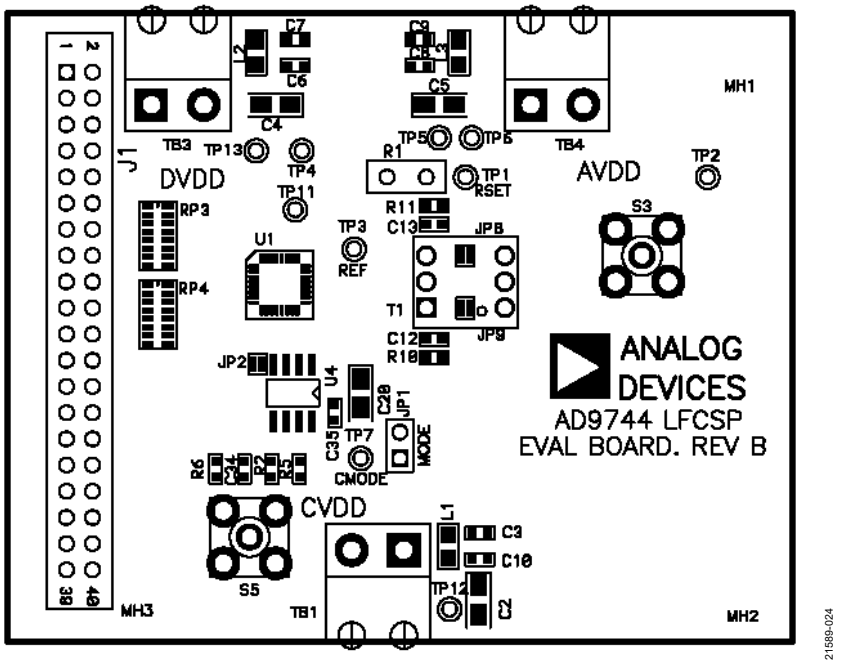

Figure 39. AD9740ACP-PCBZ/AD9742ACP-PCBZ/AD9744ACP-PCBZ/AD9748ACP-PCBZ LFCSP Evaluation Board Layout Assembly—Primary Side

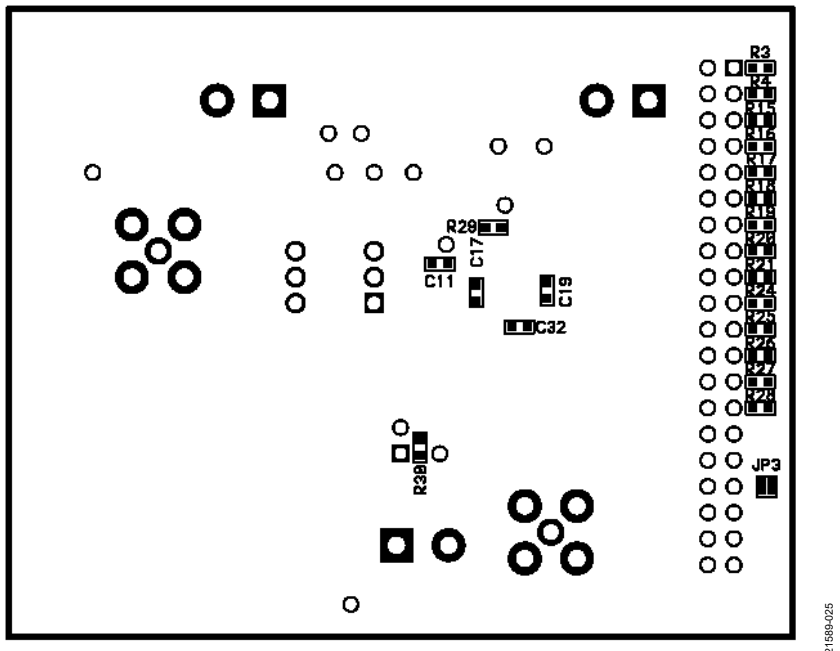

Figure 40. AD9740ACP-PCBZ/AD9742ACP-PCBZ/AD9744ACP-PCBZ/AD9748ACP-PCBZ LFCSP Evaluation Board Layout Assembly—Secondary Side

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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