ANALOG DEVICES

AN-420
APPLICATION NOTE

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Using the AD9708/AD9760/AD9762/AD9764-EB Evaluation Board

by Bill Odom

GENERAL DESCRIPTION

The AD9708-EB, AD9760-EB, AD9762-EB and AD9764-EB evaluation boards are used to evaluate the AD976x family of 8-, 10-, 12- and 14-bit D/A converters (AD9708, AD9760, AD9762, AD9764, respectively). This board allows the user to exercise the AD9708/AD9760/AD9762/AD9764's many features. They include resistor, transformer, op amp loading of the converter and sleep mode operation for reduced power consumption. For greater gain accuracy, an external reference may also be used with the converters. Each of these functions will be outlined in this note; however, the user should refer to the AD9708/AD9760/AD9762/AD9764 data sheet. It covers the operation and application in far greater detail than this evaluation board note.

Configuration

Although the AD9708/AD9760/AD9762/AD9764-EB evaluation board can exercise the many attributes of this D/A family, it is shipped with the following configuration in place:

Its digital input is designed for direct drive from various word generators. Looking into the input connector, the generator will see a high impedance load through small series resistors. Its output is constructed to drive resistive loads and a transformer. The AD9708/AD9760/AD9762/AD9764-EB evaluation board is shipped with its internal reference connected. If its other functions are to be exercised (external reference, external output amplification and sleep mode) the user must build up the applicable section of the board. Figures 1 and 2 illustrate the configuration of the board as shipped from the factory.

The entire family of converters is MSB-justified and may be soldered into the same 28-pin socket (they are all pin compatible), i.e., the MSB of all the members of the family is assigned to Pin #1. The unused DAC input pins will be floating. This allows the 8-, 10-, 12- and 14-bit DACs to be soldered to the same evaluation board.

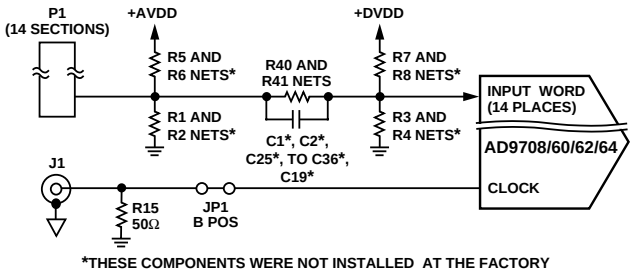

Figure 1. Input Word Configuration

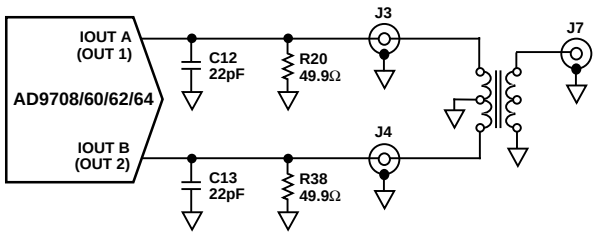

Figure 2. Resistor and Transformer Load

The parallel data input pins of the DAC follow standard positive binary coding. An input of all 1s will give a +FS output current at IOUTA. An input of all 0s will give a zero output current at IOUTA. (IOUTB is the inversion of IOUTA. All 1s will give zero current at IOUTB and all 0s will give it full-scale current.)

Note: The frequency domain data shown in this application note was gathered from an AD9760.

EVALUATION BOARD OPERATION

The AD9708/AD9760/AD9762/AD9764-EB is a 5 × 5.5 inch, four-layer board. Its layers are composed of component and solder signal layers, ground plane and power plane. A schematic and a parts list are on succeeding pages of this note.

The AD9708/AD9760/AD9762/AD9764 is shipped with JP2 "B" Pos, JP4 and JP1 "A" Pos installed.

For immediate operation, the user need only apply power and a CMOS level input word to P1 and a CMOS level clock to J1 (CMOS levels cross a threshold of {DVDD – DGND}/2). The analog output can be observed at J3, J4 or J7 (the transformer should be removed before making observations at J3 or J4). Refer to Figure 3 for setup. See sections on resistive and transformer loads.

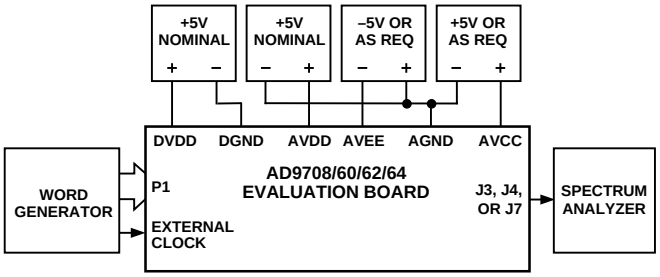

Figure 3. Equipment Setup

POWER CONNECTIONS

The AD9708/AD9760/AD9762/AD9764-EB is powered by two power supplies. They are shown in the table below with typical amplitudes for initial operation (setup is shown in Figure 3). Power is distributed on the board with power planes.

Table I. Power Supplies

DVDD +5 V	1 in = 10 mA typ*
AVDD +5 V	1 in = 30 mA typ*
AVEE† –5 V	
AVCC† +5 V	

*Current was measured with a 50 MHz clock, +5 V supplies and 50 Ω loads on the signal output pins.
†These supplies are not required for DAC operation. (Current drain depends on what components are mounted.)

AVDD and DVDD may be varied independently from +3 V to +5 V depending on the user's application (logic family, power limits, etc.). AVEE and AVCC are used to power the optional, external reference and output amplifier circuits. When using high supply potentials (voltages greater that ±6.5 V, the user should ensure that the AD9708/AD9760/AD9762/AD9764 device is not over stressed (i.e., don't let the AD9708/AD9760/AD9762/AD9764 device's reference or output pins see high voltage transients on turn-on). To avoid damage, please consult data sheet for maximum values.

GROUND

The AD9708/AD9760/AD9762/AD9764-EB has separate ground planes for analog and digital returns. The ground planes are tied together by a single trace under the AD9708/AD9760/AD9762/AD9764. Clock and the digital input word have been routed over the digital ground plane. Reference circuitry and output signal have been routed over the analog ground plane. As the users ponder the layout of their own board, they might consider using the ground planes to develop a controlled impedance with its associated signal layers. This is required if fast edge rates and/or long trace lengths are present. Propagation time and line loading will become a concern under these conditions.

DIGITAL INPUT SIGNAL CONFIGURATIONS

To allow flexibility in the input logic levels used, the AD9708/AD9760/AD9762/AD9764-EB allows several input coupling schemes. Refer to Figure 1.

Load impedance seen by the input word generator is controlled by R1, R2, R5 and R6. Resistor networks R1 and R2 are tied to DGND. Resistor networks R5 and R6 are tied to DVDD. Their values can be selected to present the desired load impedance and thevenin voltage to meet the user's signal generator requirements. R40 and R41 are series resistor networks of 22 Ω. If ac-coupled inputs are desired, R40 and R41 should be removed and ac-coupling capacitors soldered on the backside of the board (C19, C1, C2 and C25 through C36). Resistor networks R3, R4, R7 and R8 serve to determine the dc clamp voltage (level shift) of the ac-coupled signal. We recommend the clamp voltage be at the switching threshold of the AD9708/AD9760/AD9762/AD9764 device ({DVDD – DGND}/2).

Care should be made to properly load the input word at the input connector (P1, a 100 mil sq. ribbon connector) and at the AD9708/AD9760/AD9762/AD9764. Proper load termination at these points will insure that the digital input lines are not ringing at the AD9708/AD9760/AD9762/AD9764 device input pins. Note: alternate pins of the ribbon connector are grounded on the board.

The AD9708/AD9760/AD9762/AD9764-EB is shipped without R1 through R8 or the ac-coupling capacitors. Series input resistors R40 and R41 are installed.

CLOCK INPUT

The AD9708/AD9760/AD9762/AD9764's data input is triggered on the rising edge of its input clock. This clock signal is fed to the DAC through either J1 or P1.

The clock source may be taken from either J1 or P1, depending on the position of jumper JP1. If the jumper is in position "A," the clock is fed from J1 (SMA connector). If it is in position "B," it is fed through P1 (ribbon connector). J1 is terminated by a 49.9 Ω, 1/8 W resistor. P1's signal is routed through the same input loading/level-shifting scheme as the input data word (see digital input signal configurations). The board is shipped with the clock signal routed from J1 (JP1 "A" Pos connected).

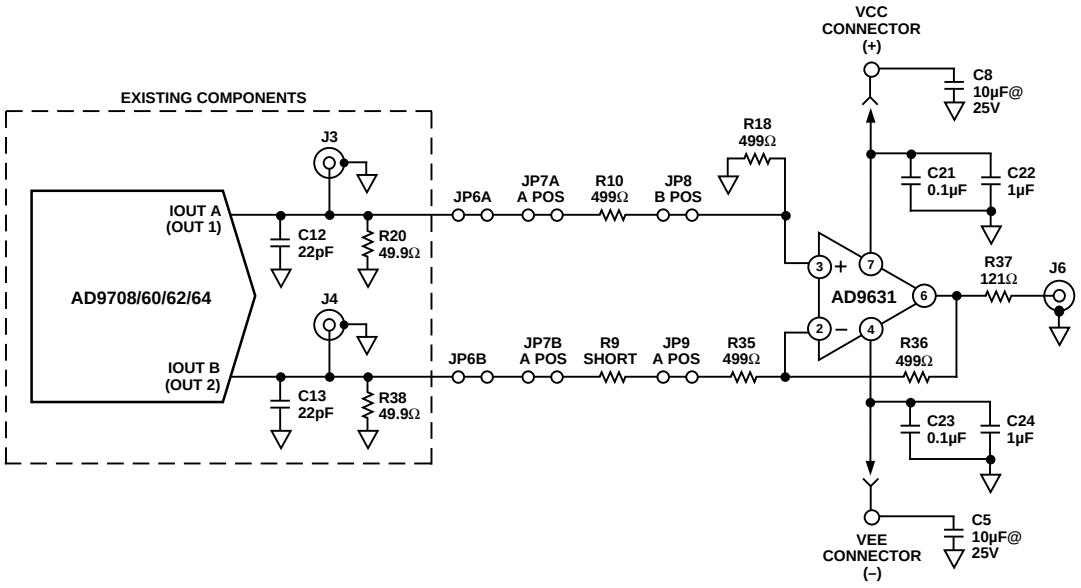

Figure 4. Differential Amplifier Configuration

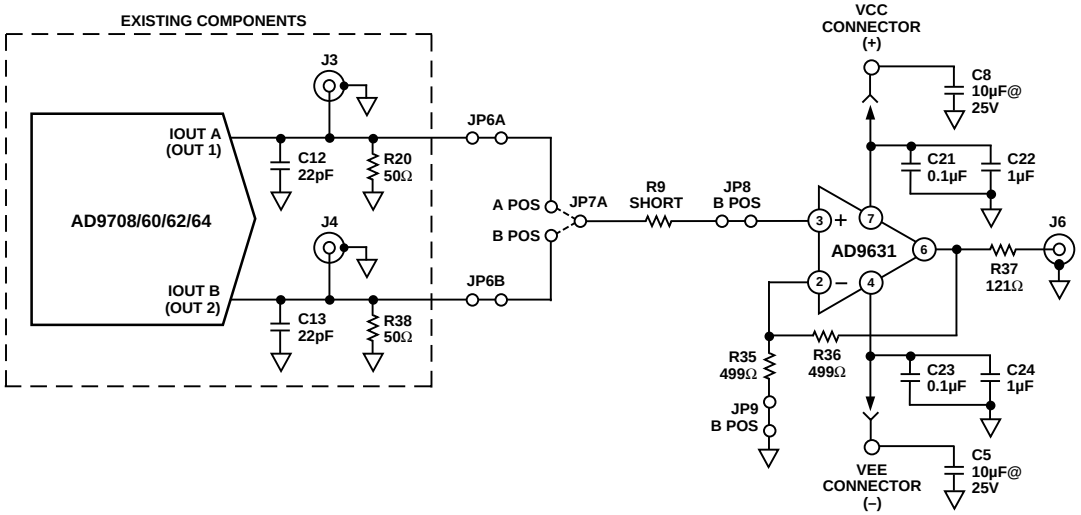

Figure 5. Noninverting Amplifier Configuration

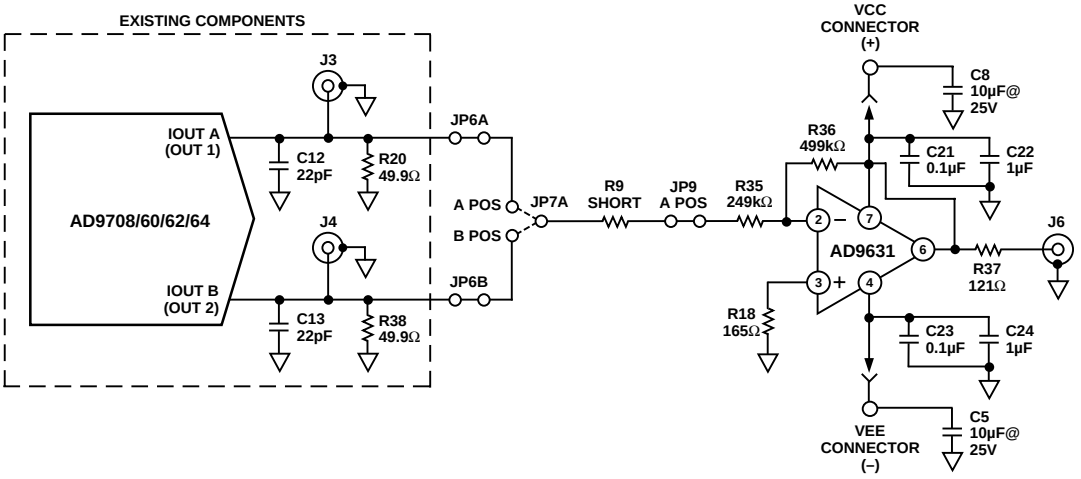

Figure 6. Inverting Amplifier Configuration

OUTPUT CONFIGURATIONS

Resistive Load

The single-ended outputs of the AD9708/AD9760/AD9762/AD9764 may be observed through J3 and J4. At these points the user will observe IOUTA and its complement, output IOUTB (respectively). The output voltage is developed by the flow of output current into 50 Ω resistors (R20, R38) and 20 pF capacitors (C12, C13). One RC net is shunted to ground for each output. The evaluation board is shipped with the RC networks installed. Refer to Figures 2 and 14 for schematics.

Figure 7 illustrates a frequency domain plot for the resistive load. It was obtained by connecting a spectrum analyzer to J3 with a 50 Ω cable. The spectrum analyzer input impedance was set to 50 Ω. There may be some difference between the frequency domain spurs between IOUTA and IOUTB. *The transformer must be removed for measurements using the resistive loads*.

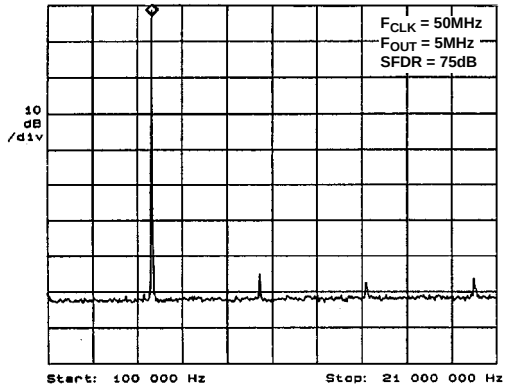

Figure 7. Resistive Output Load

Transformer Load

With T1 in place, the differential signals of IOUTA and IOUTB are converted from differential to single-ended mode. This signal can be observed at J7. It is derived by transformer T1 (mini-circuits T1–1T). The transformer is capable of processing signals above 350 kHz from the AD9708/AD9760/AD9762/AD9764 device. The transformer can process signals above 80 MHz, well beyond the Nyquist frequency of the DAC. The board is shipped with the transformer and its associated components in place. Refer to Figures 2 and 14 for schematics.

Figure 8 illustrates a frequency domain plot for the transformer load. It was obtained by connecting a spectrum analyzer to J7 with a 50 Ω cable. The spectrum analyzer input impedance was set to 50 Ω.

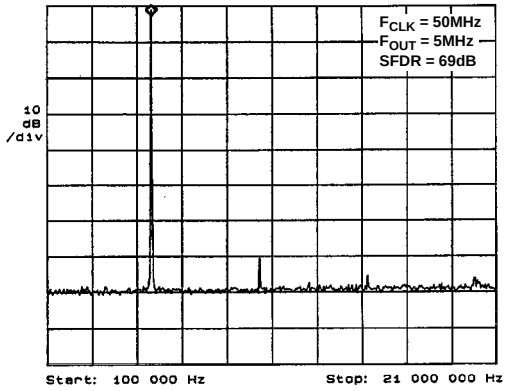

Figure 8. Transformer Output Load

Amplifier Load

The AD9708/AD9760/AD9762/AD9764 can be operated in differential or single-ended modes through the use of high quality amplifiers such as the AD9631. The op amp is especially useful at analog output frequencies below 300 kHz and where dc accuracy is important. The AD9708/AD9760/AD9762/AD9764-EB is shipped without the output op amp and its support components. Table II details the components that can be mounted with the amplifier (refer to the schematics in Figures 4, 5, 6 and 13). By mounting the components outlined in Table II, various amplifier configurations may be obtained. The transformer should be removed from the board before using the amplifier. Figures 9, 10 and 11 illustrate typical frequency domain plots for differential, inverting (AV = –2) and noninverting (AV = +2) configurations.

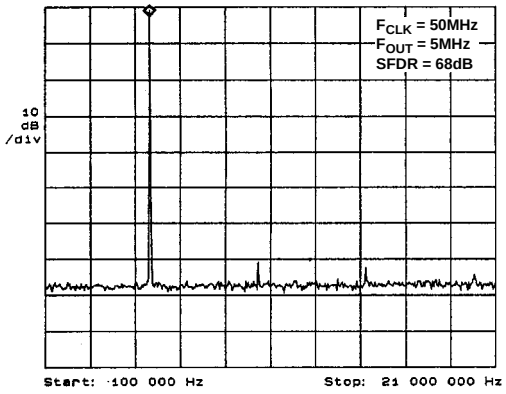

Figure 9. Differential Amplifier Output

Table II. Amplifier Circuit Configurations

Nomenclature	Description	Differential Gain of 2	Inverting Gain of 1	Noninverting Gain of 2
J6	SMA	Installed	Installed	Installed
JP6A	Jumper	Installed	Installed	Installed
JP6B	Jumper	Installed	Installed	Installed
JP7A "A" Pos	Jumper	Installed	Open	Installed for Out 1
JP7A "B" Pos	Jumper	Open	Open	Installed for Out 2
JP7B "A" Pos	Jumper	Installed	Installed for Out 2	Open
JP7B "B" Pos	Jumper	Open	Installed for Out 1	Open
JP8 "A" Pos	Jumper	Open	Open	Open
JP8 "B" Pos	Jumper	Installed	Open	Installed
JP9 "A" Pos	Jumper	Installed	Installed	Open
JP9 "B" Pos	Jumper	Open	Open	Installed
R9	Resistor	Shorted	Shorted	Open
R10	Resistor	499 Ω 1/8 W	Open	Shorted
R12	Resistor	Open	Open	Open
R13	Resistor	Open	Open	Open
R18	Resistor	499 Ω 1/8 W	165 Ω 1/8 W	Open
R35	Resistor	499 Ω 1/8 W	249 Ω 1/8 W	499 Ω 1/8 W
R36	Resistor	499 Ω 1/8 W	499 Ω 1/8 W	499 Ω 1/8 W
R37	Resistor	121 Ω 1/8 W	121 Ω 1/8 W	121 Ω 1/8 W
U4	Op Amp	AD9631	AD9631	AD9631

The plots shown in Figures 10, 11 and 12 were measured with a 10X, 10 MΩ, 13 pF probe connected to J7. The Spectrum analyzer input impedance was set to 1 MΩ.

An AD9631 op amp was used with the resistor values shown in Table II. Other op amps can be used to fit a specific application. A list of prospective Analog Device op amps is shown in Table III.

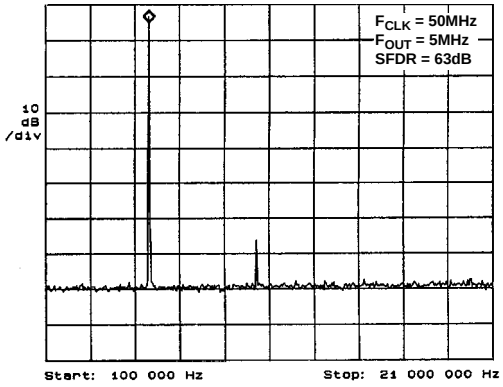

Figure 10. Inverting Gain of 2 Amplifiers

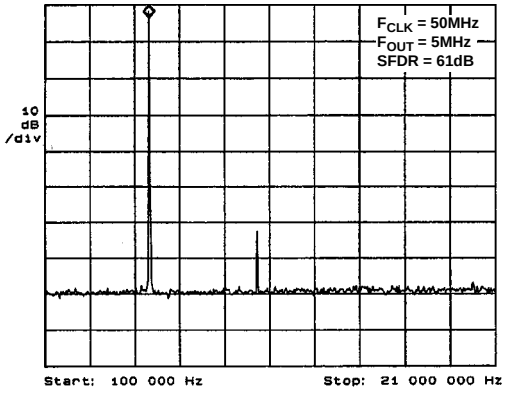

Figure 11. Noninverting Gain of 2 Amplifiers

Table III. Op Amp Selection Guide

AD8011	f –3 dB = 300 MHz, +5 V or ±5 V Supplies, Current Feedback
AD9631*	220 MHz Unity GBW, 16 ns Settling Time to 0.01%, ±5 V Supplies
AD8047	130 MHz Unity GBW, 30 ns Settling to 0.01%, ±5 V Supplies
AD8041	Rail-to-Rail, 160 MHz Unity GBW, 55 ns Settling to 0.01%, +5 V Supply, 26 mW

*Used to collect frequency domain plots

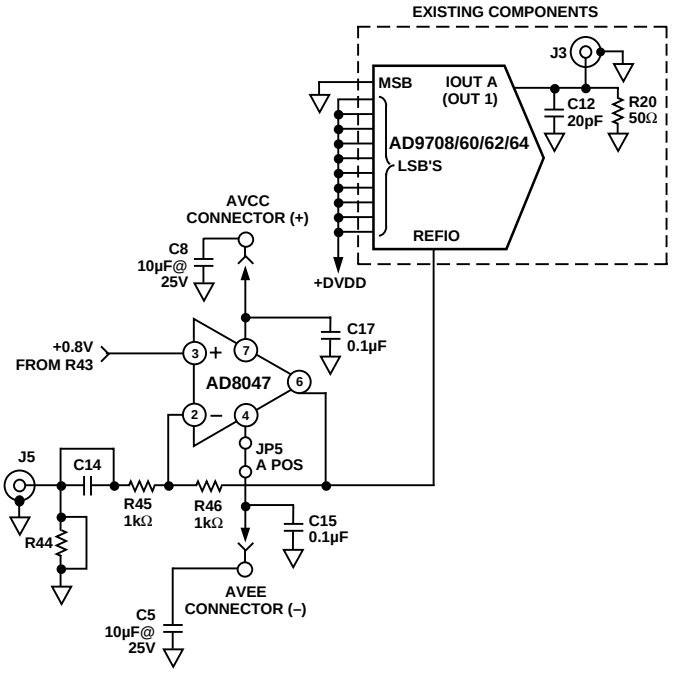

Figure 12. Gain Control Using an External Reference

REFERENCE CIRCUITS

External Reference

The external reference may be used by installing the components shown in Table IV. The dc reference is developed by U7 and buffered by U6. The dc level of VREF can be adjusted with R43.

Table IV. Reference Circuit Components

JP2 "A" Pos	Jumper	Installed for External Ref.
JP2 "B" Pos	Jumper	Installed for Internal Ref.
JP3 "A" Pos	Jumper	Connects Ext Ref. to REFIO with U6 Amp.
JP3 "B" Pos	Jumper	Connects Ext Ref. to REFIO with R43 and Reference U7.
JP4	Jumper	Installed
JP5 "A" Pos	Jumper	Installed. Connects –V of U6 to AVEE
JP5 "B" Pos	Jumper	Open. Connects –V of U6 to AGND
R42	Resistor	1 kΩ 1/8 W
R43	Pot	5 kΩ 1/8 W
R44	Short	
R45, R46	Resistor	1 kΩ 1/8 W
C14	Short	
C16	Chip Cap	1206 1 µF, 1206 Case
C15, C17, C18	Chip Cap	1206 0.1 µF, 1206 Case
U7	Reference	REF-43
U6	Op Amp	AD8047

Internal Reference

The internal reference current is set up by R16. It is roughly equal to 1.2 V/R16. It is enabled by grounding R16 and placing Pin 16 of the DAC at DGND with JP4. The center of JP3 is left floating (leaving the REFIO pin undriven). JP2 B position must also be connected.

The board is shipped with the internal reference enabled (JP4 and JP2 "B pos" are installed).

POWER-DOWN

(Sleep Mode)

By mounting J2 and R17, the AD9708/AD9760/AD9762/AD9764 device may be operated in the sleep mode. When JP2 (Pin 15) is pulled high, the DAC goes into a sleep state in which it consumes 25 mW (typ). Internally, the AD9708/AD9760/AD9762/AD9764's sleep pin attaches to an active pull-down circuit. The device will be functional until a pull-up is externally applied. Once the DAC is sleeping, 35 ms (typ) will be required for it to "wake up" after logic low is applied to Pin 15.

BOARD LAYOUT CONSIDERATIONS

1. Use separate analog and digital ground planes joined together at a single point near the AD9708/AD9760/AD9762/AD9764.

2. Power should be distributed from power planes or very wide traces (as wide as possible).

3. Power plane decoupling should be done with Tantalum capacitors. Ceramic chip capacitors should be used for reference and local power decoupling. These capacitors should be placed at the applicable DAC pins with traces no longer than 0.25 inches.

   Similar protocols should be observed with compensation capacitor placement.

4. Digital switching signals should only be routed only over the digital ground plane. Controlled impedance should be considered for the transmission line effects of fast rise and fall times. Analog signals should only be routed only over the analog ground plane.

Note: The frequency domain data shown in this application note was gathered from an AD9760.

BILL OF MATERIALS – AD9708/AD9760/AD9762/AD9764 EVALUATION BD

QTY PER	REFERENCE DESIGNATION	DESCRIPTION	P S	PKG	MFR DIST	MFR P/N DIST P/N
		BARE P.C. BOARD				
1	P1	CONNECTOR HDR RTA 4 0 PIN PROTECTED, W/EJECTORS	P		AMP (DIGI-KEY)	102159-9 AHR40G-ND
4	J1, J3, J4, J7 (J2, J5, J6 Optional)	CONNECTOR SMA VERTICAL P.C. MOUNT .2 CTRS	P		E.F. JOHNSON (POWELL ELECT)	142-0701-201
–	C1, C2, C19, C25-C36 (Optional)	CAPACITOR CHIP CERAMIC .1μF, 50V, NPO, 5%	S	0805		
1	R16	RESISTOR, 2.00K OHM 1% MF, 1/8 W	S	1206	PANASONIC (DIGI-KEY)	P2.00KFCT-ND
3	R15, R20, R38 R17, R44	RESISTOR, 49.9 OHM 1% MF, 1/8 W	S	1206	PANASONIC (DIGI-KEY)	P49.9FCT-ND
1	JP4, JP6A, JP6B	JUMPER HEADER 2 PIN .025 SQ PINS, .10 CTRS	P		COMPNT CORP (BISCO IND)	CSS-102-02
3	JP1, JP2, JP4	JUMPER SHUNTS 2 PIN .025 SQ PINS .10 CTRS	P		COMPNT CORP (BISCO IND)	CSS-101-03
1	U1	AD9708/AD9760/AD9762/AD9764		SOL-28	ANALOG DEVICES	AD9708, AD9760, AD9762, AD9764
2	JP1, JP2, JP3, JP5, JP7A, JP7B, JP8, JP9	JUMPER HEADER 3 PIN .025 SQ PINS, .10 CTRS	P		MOLEX (DIGI-KEY)	22-10-2031 WM2723
4	TP2, TP5, TP18, TP19	TEST POINT BLK	P		COMPNT CORP (BISCO IND)	TP-104-01-00
2	TP3, TP4, TP6, TP7	TEST POINT RED	P		COMPNT CORP (BISCO IND)	TP-104-01-02
7	TP1, TP8, TP9, TP10, TP11, TP13, TP14, TP12	TEST POINT WHT	P		COMPNT CORP (BISCO IND)	TP-104-01-09
4	B1– B4, B5-B6	BINDING POST METAL	P		CONCORD (BISCO IND)	01-2540-1-02
2	C3, C4, C5, C6	CAPACITOR CHIP TANT 10μF, 25V, TEH SERIES	S	D CASE	PANASONIC (DIGI-KEY)	ECS-H1ED106R PCT5106CT-ND
9	C8 –C11, C15, C17, C21, C23, C18	CAPACITOR CHIP CERAMIC .1μF, 50V, X7R, 10%	S	1206	PANASONIC (DIGI-KEY)	ECU-V1H104KBW PCC104BTR-ND
3	C7, C22, C24, C14, C16	CAPACITOR CHIP CERAMIC 1.0μF, 16V, +80-20%, Y5V	S	1206	MURATA (NEWARK)	93F2254
2	C12, C13	CAPACITOR CHIP CERAMIC 22pF, 50V, NPO, 5%	S	1206	PANASONIC (DIGI-KEY)	ECU-V1H220JCM PCC220CCT-ND
–	(C20)	CAPACITOR OPTIONAL	P			
–	(U4, U6)	Op Amp (Optional)	P	DIP-08	ANALOG DEVICES	
–	(R9, R10, R18, R35, R36, R37, R42, R45, R46)	RESISTOR (Optional) 1% MF, 1/4 W	P	RC07-S	YAGO (DIGI-KEY)	
–	(R42)	RESISTOR (Optional) 1% MF, 1/4 W	P	RC07-S	YAGO (DIGI-KEY)	
–	(R43)	RESISTOR POT (Optional) 5 kΩ	P		(DIGI-KEY)	3296W-502-ND
–	(U7)	2.5 VOLTAGE REFERENCE (Optional)	P	DIP-08	ANALOG DEVICES	REF43P
24	R9, R10, R12, R13, R18, R20, R35, R36, R37, R42, R45, R46	SOCKET LOOSE .015-.026 LEAD (.056 HOLE)	P		MILL-MAX MFG (HDWR SPEC)	0555-0-15-01-20-27-10-0
136	U4, U6, U7 R1–R8, R40, R41	SOCKET, SIP, JPEEL-A-WAY ICS).043 HOLE)	P		ADV. INTER. (CAL-CREG COMP)	KSS10085TG
1	T1	TRANSFORMER RF	P	DIP-06	MINI-CIRCUITS	MOD.T1-1T X65 CASE
–	(R1–R8)	RESISTOR NETWORK (Optional) 10 PIN SIP 9 RES	P	SIP-10		
2	R41, R40	RESISTOR NETWORK 10 PIN SIP 22 Ω	P	DIP-16	CTS (DIGI-KEY)	761-3-R22-ND

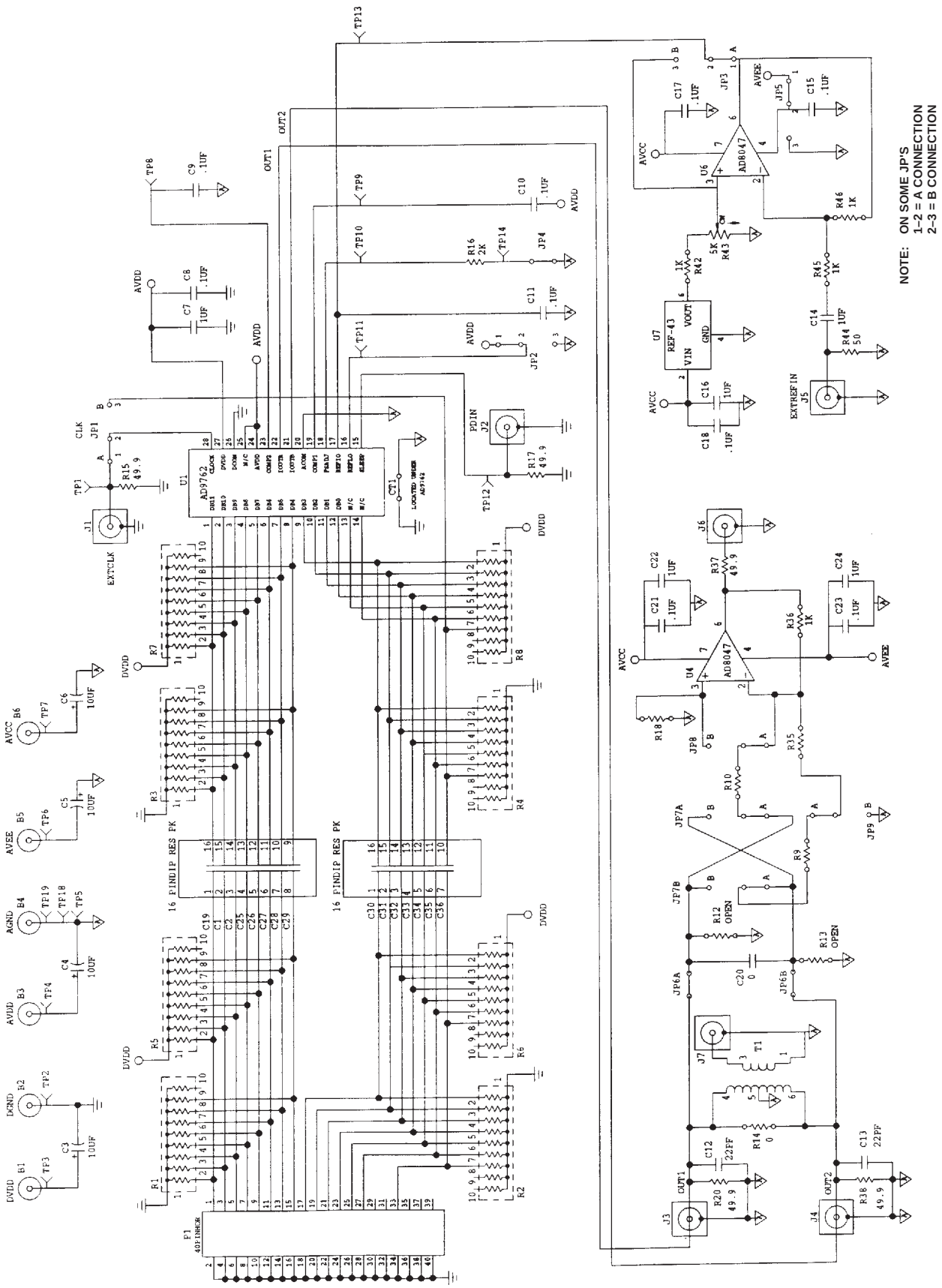

Figure 13. Complete Board Schematic

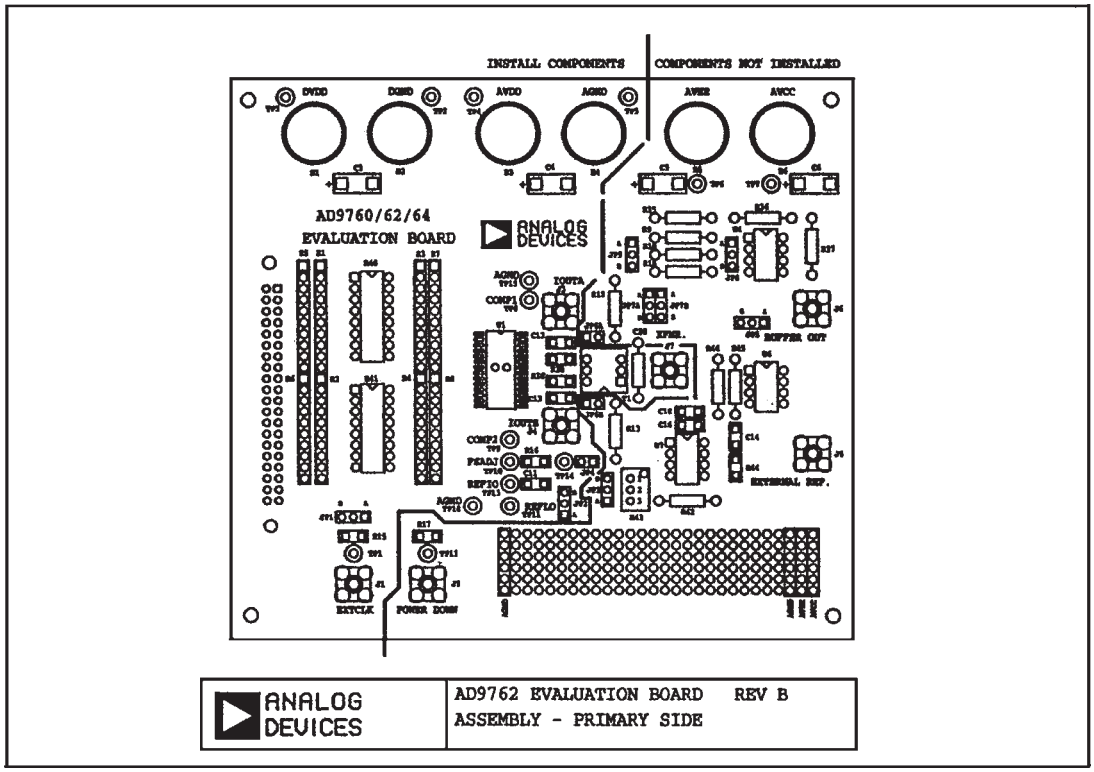

Figure 14. Silkscreen Layer—Top

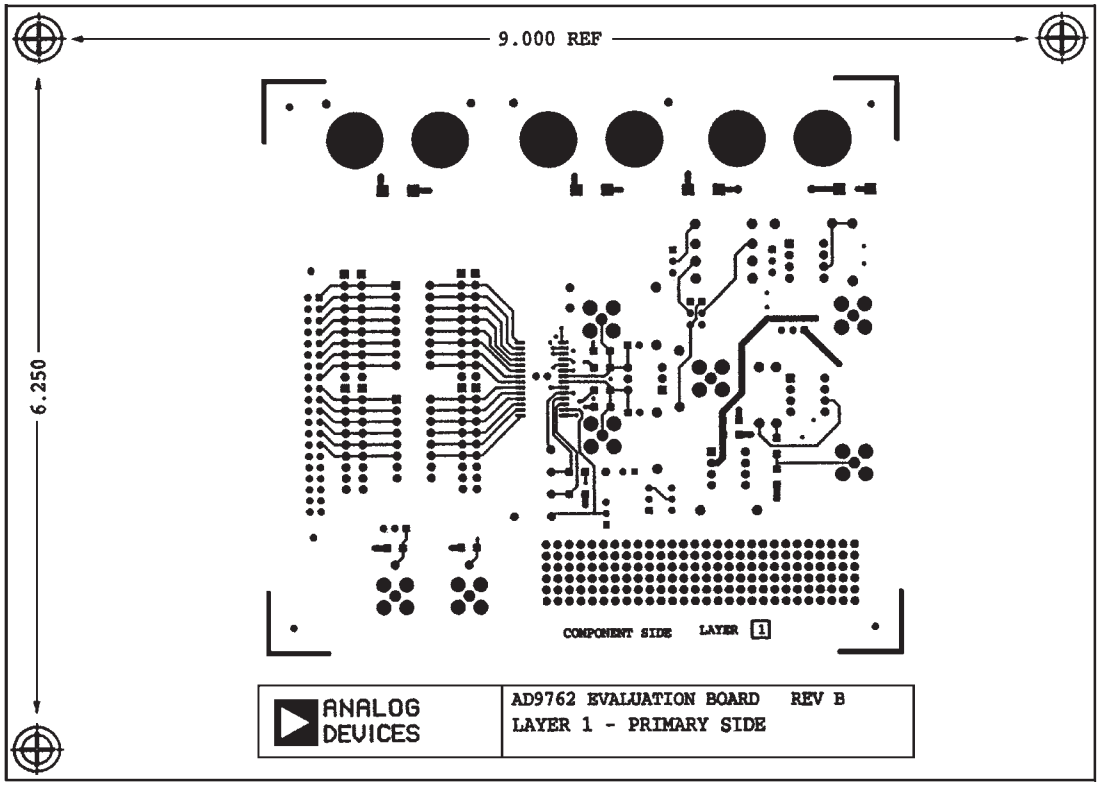

Figure 15. Component Side PCB Layout (Layer 1)

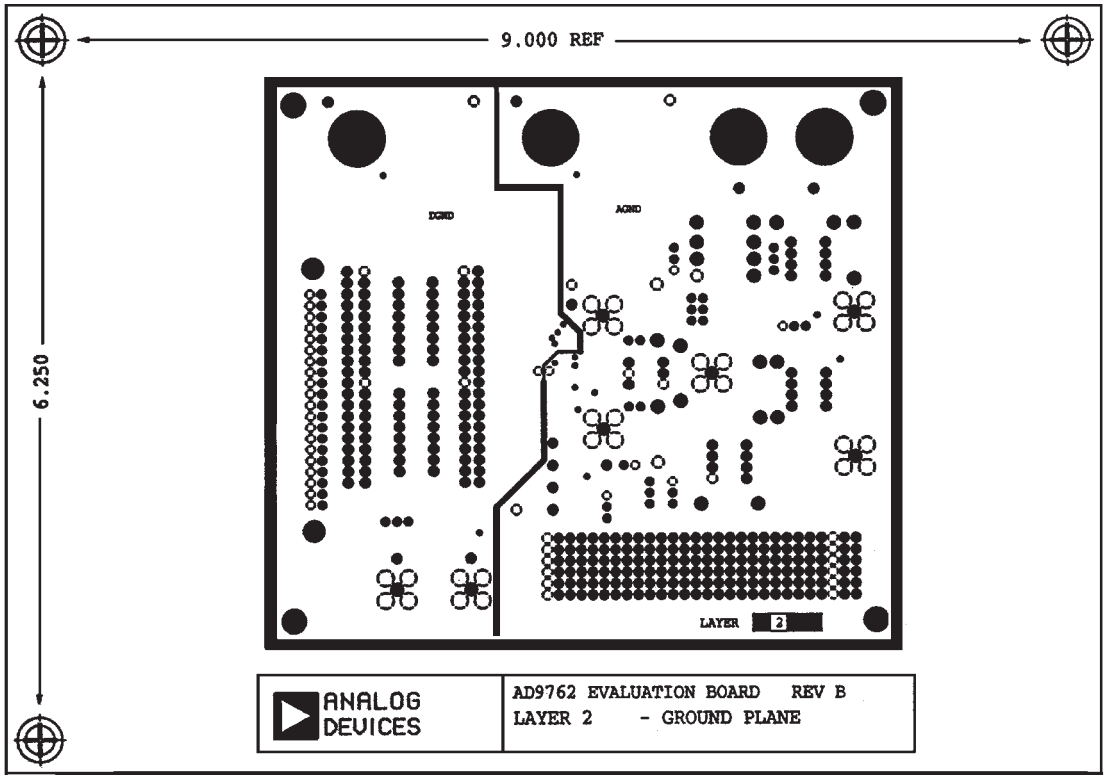

Figure 16. Ground Plane PCB Layout (Layer 2)

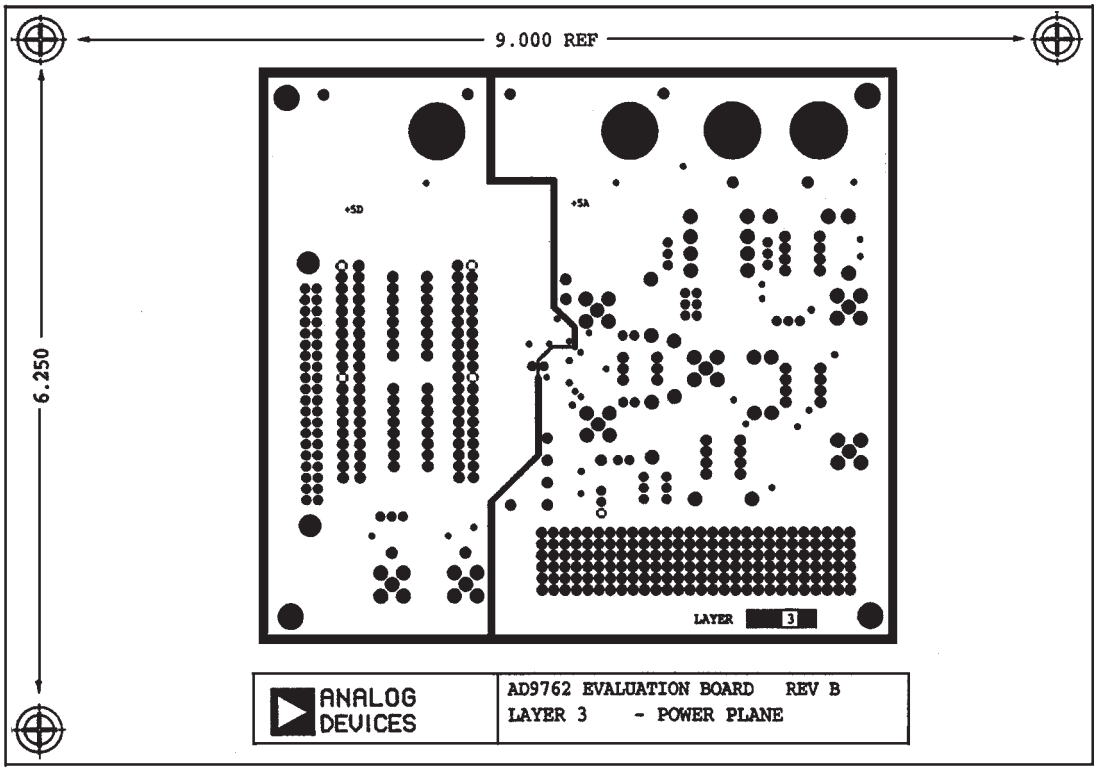

Figure 17. Power Plane PCB Layout (Layer 3)

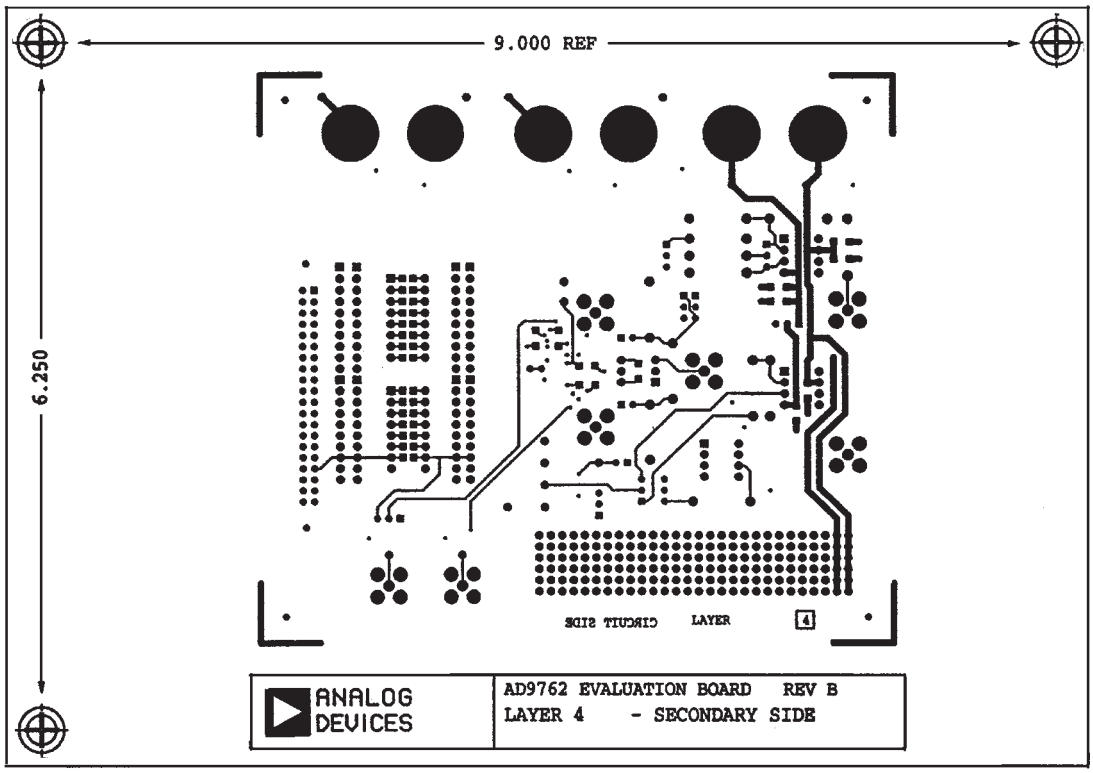

Figure 18. Solder Side PCB Layout (Layer 4)

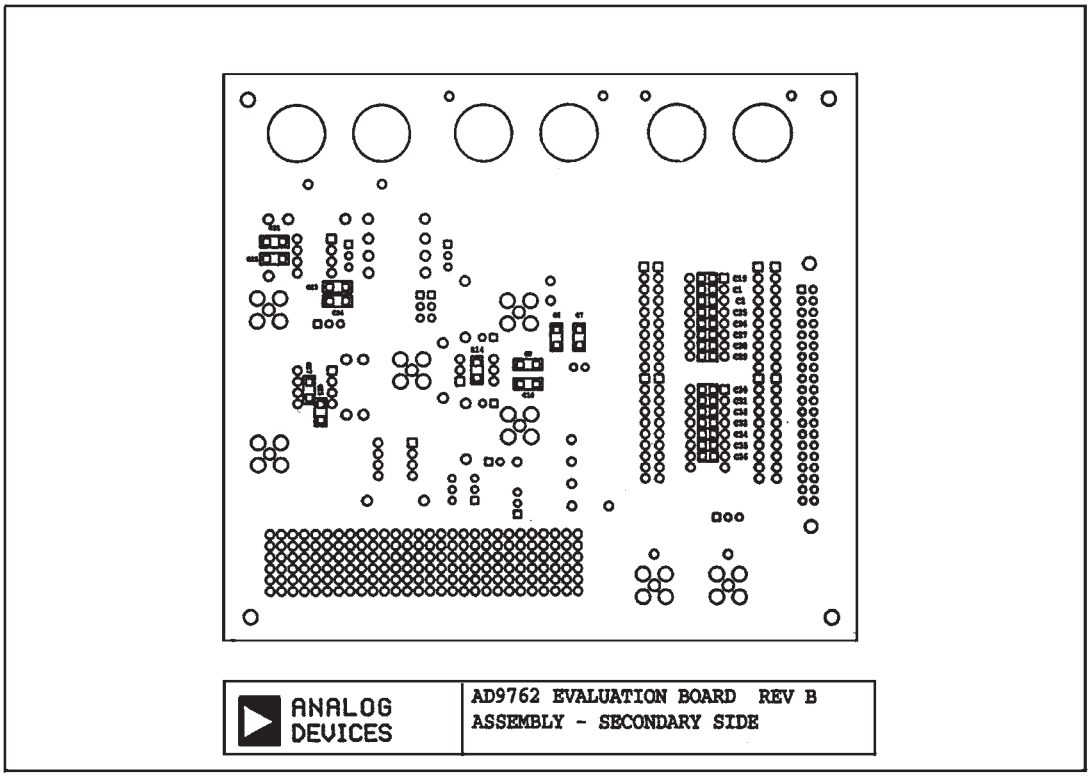

Figure 19. Silkscreen Layer—Bottom

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