Ultrahigh Speed IC D/A Converter

AD9768

FEATURES
5 ns Settling Time
100 MSPS Update Rate
20 mA Output Current
ECL-Compatible
40 MHz Multiplying Mode

APPLICATIONS
Raster Scan & Vector Graphic Displays
High Speed Waveform Generation
Digital VCOs
Ultrafast Digital Attenuators

GENERAL DESCRIPTION

The Analog Devices AD9768SD D/A converter is a monolithic current-output converter which can accept 8 bits of ECL-level digital input voltages and convert them into analog signals at update rates as high as 100 MSPS. In addition to its use as a standard D/A converter, it can also be utilized as a two-quadrant multiplying D/A at multiplying bandwidths as high as 40 MHz.

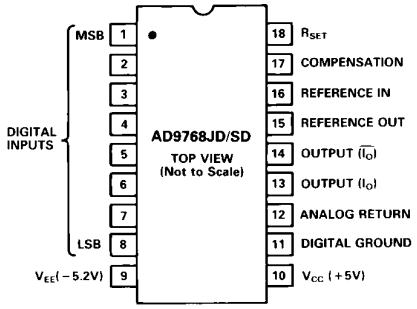
An inherently low glitch design is used, and the complementary current outputs are suitable for driving transmission lines directly. Nominal full-scale output is 20 mA, which corresponds to a 1 volt drop across a 50 Ω load, or ±1 volt across 100 Ω returned to +1 volt. The actual output current is determined by the on-chip reference voltage ($V_{REF} \approx -1.26$ V) and an external current setting resistor, R_{SET}.

Full-scale output current I_{OUT} with digital "1" at all inputs is calculated with the equation:

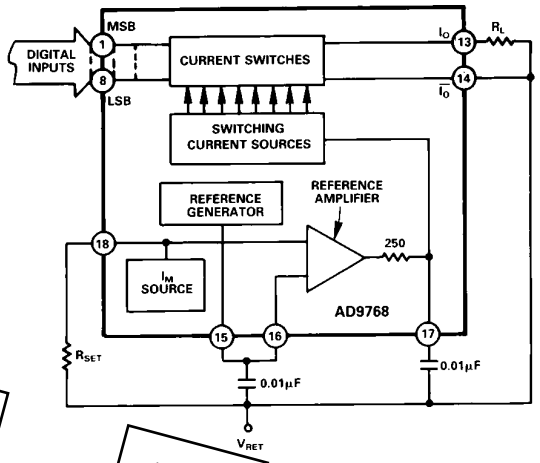
$$I_{OUT} = 4 \times \frac{V_{RET} - V_{REF}}{R_{SET}}$$

The setting resistor R_{SET} and the output load resistor should both have low temperature coefficients. A complementary $\overline{I_{OUT}}$ is also provided.

AD9768JD/SD PIN CONNECTIONS



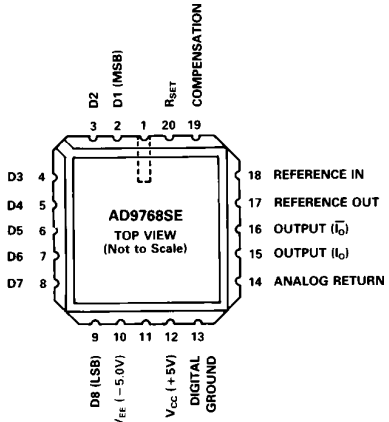
FUNCTIONAL BLOCK DIAGRAM



The reference voltage source is a modified bandgap type and is nominally –1.26 volts. This reference supply requires no external regulation. To reduce the possibility of noise generation and/or instability, Pin 15 (REFERENCE OUT) can be decoupled using a high-quality ceramic chip capacitor. Stabilization of the internal loop amplifier is by a single capacitor connected from Pin 17 (COMPENSATION) to ground. The minimum value for this capacitor is 3900 pF, although a 0.01 μF ceramic chip capacitor is recommended.

The incredible speed characteristics of the AD9768SD D/A converter make it attractive for a wide range of high speed applications. The ability of the unit to operate as a two-quadrant multiplying D/A converter adds another dimension to its usefulness and makes the AD9768SD a truly versatile device.

AD9768SE PIN CONNECTIONS



REV. A

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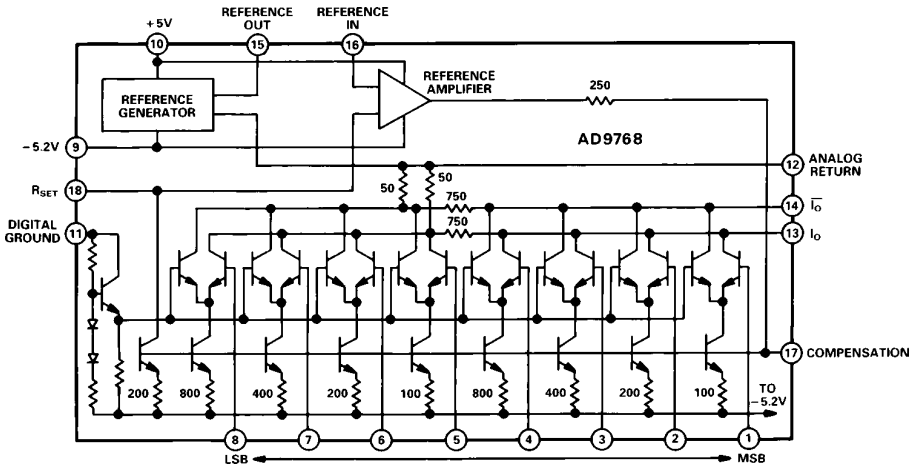
AD9768–SPECIFICATIONS (typical @ +25°C under following conditions unless otherwise noted; nominal digital input levels; nominal power supplies; R_L = 50 Ω; R_{SET} = 220 Ω; V_{RET} = 0 V)

Parameter	Unit	AD9768SJD/SD/SE
RESOLUTION(FS = FULL SCALE)	Bits	8
LSB WEIGHT (CURRENT)	µA	78
ACCURACY[1]		
Differential Nonlinearity	± % FS	0.2
Integral Nonlinearity	± % FS	0.2
Monotonicity		Guaranteed
Zero Offset (Initial)	µA	60
TEMPERATURE COEFFICIENTS		
Zero Offset	ppm/°C	1.5
Reference Voltage (–1.26 V)	ppm/°C	70
DIGITAL DATA INPUTS		
Logic Compatibility		ECL
Logic Voltage Levels "l" =	V	–0.9
"0" =	V	–1.7
Coding	Binary (BIN) = Unipolar Out	
	Offset Binary (OBN) = Bipolar Out	
OUTPUT		
Current (Unipolar) FS	mA (max)	2 to 20 (30)
I_{OUT} (@ Pin 13)		
All Digital "1" Input	mA	20
All Digital "0" Input	mA	0
I_{OUT} (@ Pin 14)		
All Digital "l" Input	mA	0
All Digital "0" Input	mA	20
Compliance	V (Pin 13)	–0.7 to +3.0
	V (Pin 14)	–1.1 to +3.0
Impedance	Ω (±15%)	750
SPEED PERFORMANCE		
Settling Time (to 0.2% FS)[2]	ns	5
Slew Rate	V/µs	400
Update Rate	MSPS	100
Rise Time	ns	1.8
Glitch Energy	pV-sec	200
REFERENCE		
Internal, Monolithic[3]	V	–1.26
External, Variable[4]		
Voltage-Multiplying Mode	V (max)	0 to –1.1 (–2)
Current-Multiplying Mode	mA (max)	0 to –5 (–7.5)
VOLTAGE-MULTIPLYING MODE[4] (See Figure 2)		
V_M Range (at Pin 16)	V	±0.5
V_M Center	V	–0.6
Resistance (at Pin 16)	kΩ	800
Transfer Function –	Measured at Pin 13; Digital "0" Applied to Bits 1-8:	
	–0.1 V_M Input = 0 mA I_{OUT}	
	–1.1 V_M Input = 0 mA I_{OUT}	
	Measured at Pin 13; Digital "1" Applied to Bits 1-8:	
	–0.1 V_M Input = 1 mA I_{OUT}	
	–1.1 V_M Input = 20 mA I_{OUT}	
Large Signal Bandwidth (–3 dB Point)	kHz	250

Parameter	Unit	AD9768SJD/SD/SE
CURRENT-MULTIPLYING MODE (See Figure 4)		
I_M Range (at Pins 17 & 18)	mA	0 to 5
Resistance (at Pin 18)	Ω	160
Transfer Function –	Measured at Pin 13; Digital "0" Applied to Bits 1-8:	
	1 mA I_M Input = 0 mA I_{OUT}	
	5 mA I_M Input = 0 mA I_{OUT}	
	Measured at Pin 13; Digital "1" Applied to Bits 1-8:	
	1 mA I_M Input = 4 mA I_{OUT}	
	5 mA I_M Input = 20 mA I_{OUT}	
Large Signal Bandwidth (–3dB Point)	MHz	40
POWER REQUIREMENTS		
–5.2 V ±0.25	mA (max)	66(70)
+5.0 V ±0.25	mA (max)	14(15)
Power Dissipation	mW (max)	410(430)
Power Supply Sensitivity[5]	%/%	0.07
TEMPERATURE RANGES[6]		
Operating		
AD9768JD	°C	0 to +70
AD9768SD/SE	°C	–55 to +125
Storage	°C	–55 to +150
THERMAL RESISTANCE[7]		
Junction to Air, θ_{JA} (Free Air)	°C/W	90
Junction to Case, θ_{JA}	°C/W	20
PACKAGE OPTION[8]		
Ceramic (D-18)	AD9768JD AD9768SD	
LCC (E-20A)	AD9768SE	

NOTES
[1]Relative to FS, including linearity (within voltage compliance limits).
[2]Worst case settling time; includes FS and Most Significant Bit (MSB) transitions.
[3]Applies when operating AD9768 as standard D/A.
[4]Based on R_L = 50 ohms; R_{SET} = 220 ohms; V_{RET} = 0 V.
[5]1% change in either power supply voltage causes 0.07% change in analog output.
[6]Case temperature.
[7]Maximum junction temperature 125°C.
[8]D = Ceramic DIP, E = Leadless Ceramic Chip Carrier.
Specifications subject to change without notice.



AD9768SD D/A Schematic

THEORY OF OPERATION

Refer to the AD9768SD schematic.

The transistors pictured on the bottom of the diagram, connected to paired transistors in the middle of the schematic, are current sources which are always "on". The paired transistors are differential current switches, designed to steer current from the current sources to either Pin 13 (I_O) or Pin 14 ($\overline{I_O}$).

Digital inputs applied to Pins 1-8 determine which transistors will be operating in each pair and establish what current will flow at Pins 13 and 14.

The transistor on the extreme left of the schematic is a base reference for the paired current switches and is used to assure the switches will be centered around an ECL voltage swing. The diodes connected to the base of this transistor are temperature compensation devices for the base reference circuit.

There are three different current sources in the AD9768 D/A. The eight transistors shown on the bottom of the schematic are structured as two identical groups of four current sources, each of which is binarily weighted. The MSB group, comprised of the four on the right, is connected to the LSB group through a 15:1 current divider made up of two 50 Ω and two 750 Ω resistor networks. The geometry of the AD9768 guarantees the binary weighing ratios among the 100, 200, 400 and 800 resistors in each emitter circuit are correct.

The resistor values which are shown indicate the ratios among the resistors, and not their nominal values.

The third current source is a single transistor, pictured in the lower left portion of the schematic with its collector connected to Pin 18 R_{SET}. Its function is to help establish the base voltage on the eight current sources; it works in conjunction with the external R_{SET} resistor selected by the user of the AD9768, and the reference amplifier. Current flowing through this transistor is referred to as I_M in the figures and text.

When the AD9768 is operating as a conventional current-output D/A converter, I_M develops a voltage across R_{SET} which is one of the inputs to the on-board reference amplifier shown in the schematic. The other input to this amplifier is the on-chip reference voltage of –1.26 volts.

The output of the reference amplifier adjusts the current-source base reference voltage at Pin 17; this, in turn, adjusts the value of I_M in the single-transistor current source and causes it to develop a voltage across R_{SET} which maintains Pin 18 at the –1.26 volts of the on-chip reference supply.

To maintain good stability in the internal loop reference amplifier, a ceramic chip capacitor with a nominal value of 0.01 µF should be connected to Pin 17 COMPENSATION; minimum recommended value for this capacitor is 3900 pF.

The temperature coefficient of the load resistor (R_L) can affect the performance of the AD9768 D/A converter, as it can with any current-output converter. The design and use of the AD9768 and its dependence on an external R_{SET} resistor, however, make it sensitive also to the tempco of R_{SET}. The user is cautioned to select R_L and R_{SET} resistors which have low temperature coefficients.

DIGITAL GROUND (Pin 11) and ANALOG RETURN (Pin 12) are normally connected together; this connection should be made as close as possible to the device case to minimize possible noise problems. The AD9768 D/A is similar to any other high-speed, high performance device: optimum use requires careful attention to all design details, including the layout of the circuit in which the converter is used.

CONVENTIONAL AD9768SD

Refer to Figure 1, Conventional AD9768SD.

The output current of the AD9768 appears at Pin 13 (I_O) and develops a voltage across the load resistor R_L which is based on:

A. I_M (the current flowing through the single-transistor source discussed above)

B. Value of R_L

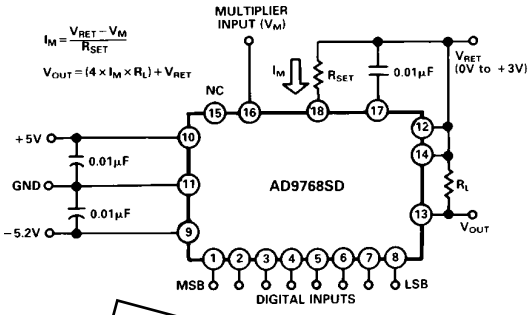


Figure 1. Conventional AD9768SD

I_M is a function of the return voltage (V_{RET}), the reference voltage (V_{REF}), and the value of R_{SET}, all of these are selected by the user for his application. The necessary equations for calculating precise values for each are part of Figure 1. As indicated, the voltage drop across R_L is added to the return voltage; the resulting voltage is the total V_{OUT} of the converter.

VOLTAGE MULTIPLYING MODE

In addition to its use as an ultra-high speed current output D/A converter, the AD9768 can also be used as a two-quadrant multiplying D/A in either a voltage mode or a current mode.

Refer to Figure 2, Multiplying AD9768 (Voltage Mode).

When operating in this mode, the analog output of the AD9768 is influenced by the digital inputs and an external multiplying voltage (V_M) applied to Pin 16 REFERENCE IN, which takes the place of the internal reference used when the D/A is operating in a conventional manner.

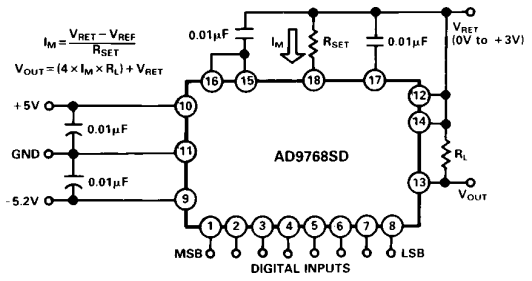


Figure 2. Multiplying AD9768 (Voltage Mode)

The value of I_M flowing through R_{SET} is set by the voltage of V_{RET} minus the multiplying voltage (V_M), divided by R_{SET}; the amount of this current is part of the equation which establishes the analog output (V_{OUT}) of the AD9768 and is chosen by the user for his application. As it is when operating the D/A in a conventional fashion, V_{RET} can be any value between 0 volts and +3 volts. V_M (for purposes of discussion here) is some negative voltage and can be varied over a range which is approximately 1 volt peak-to-peak.

If the load resistor (R_L) has a value of 50 ohms, if R_{SET} has a value of 220 ohms, and if V_{RET} is 0 V, the center of the V_M voltage will be –0.6 V; and it can vary from –0.1 V to –1.1 V. Typically, the frequency of these variations has an upper limit of 250 kHz when operating in the voltage multiplying mode; that frequency is the 3 dB point of the bandwidth of the internal reference amplifier.

The combined effects of variations in V_M and changes in digital input values are shown in Figure 3, I_{OUT} vs. Multiplying Voltage. In this illustration, the ordinate of the graph is expressed in terms of milliamps of I_{OUT} current at Pin 13. V_{OUT}, of course, will be a function of the value of R_L chosen by the user.

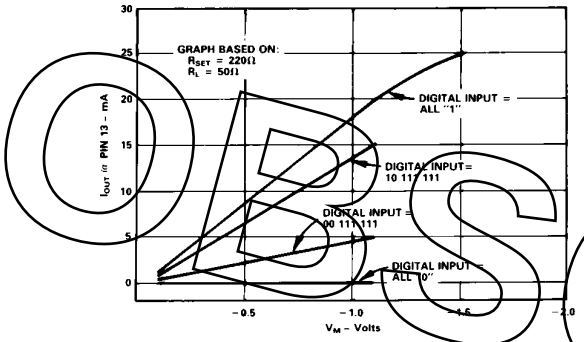


Figure 3. I_{OUT} vs. Multiplying Voltage

The negative value of V_M on the horizontal axis is shown starting at approximately –0.1 V, rather than 0 V, because the AD9768 must have some small value of voltage applied to perform a multiplying function. For the conditions shown in the figure, output current starts to become nonlinear at approximately 20 mA because of the maximum 30 mA output drive capabilities of the device. Different values for R_{SET} and R_L would alter the point where limiting first appears.

CURRENT MULTIPLYING MODE

The AD9768 D/A converter can be operated at markedly higher multiplying rates when operated in a current-multiplying mode, as contrasted with the voltage multiplying mode. Refer to Figure 4, Multiplying AD9768SD (Current Mode).

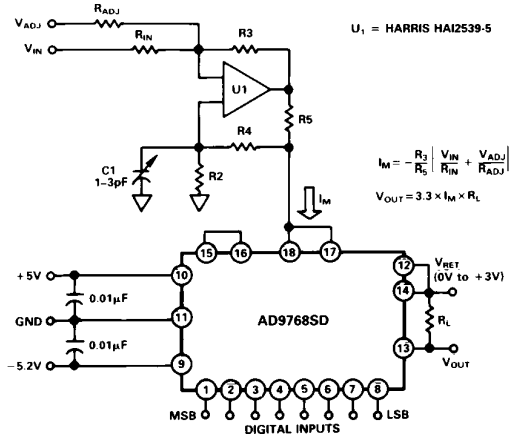


Figure 4. Multiplying AD9768SD (Current Mode)

In this mode, the internal reference amplifier and its inherent frequency limitations are replaced by a current source comprised of U1 and associated circuits. These circuits supply a unipolar current I_M which is one-fourth the full-scale output current (with digital "1" applied to all inputs) and set current flow through the load resistor.

V_{IN} is some voltage chosen by the user for his particular application; the value of this voltage is based in part on the size of the load resistor and the 0 mA to 5 mA range of I_M. V_{IN} can have frequency components as high as 40 MHz. V_{ADJ} and R_{ADJ} provide an offset adjustment to compensate for the dc component of V_{IN} to assure I_M is always a unipolar current between 0 mA and 5 mA. The values of the required voltages and resistors can be calculated using the equations which are part of Figure 4.

Refer to Figure 5, I_{OUT} vs. Multiplying Current.

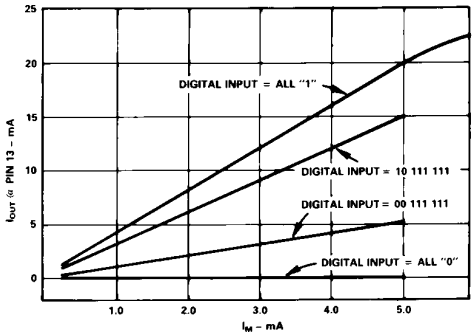


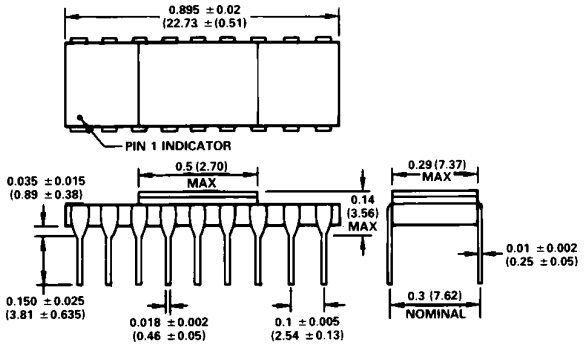
Figure 5. I_{OUT} vs. Multiplying Current

As shown, I_M can vary over the range of 0 mA to 5 mA; a value of approximately 0.3 mA may be the practical lower limit because of nonlinearities at extremely small current levels. These changes in I_M are combined with variations in digital inputs, producing complex changes in the output current (at pin 13) and in V_{OUT}. The "rounding" of the current curve in the graph is the result of I_{OUT} approaching the 30 mA maximum drive capabilities of the AD9768 and needs to be taken into account to assure optimum performance in the selected application.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Ceramic (D-18)



LCC (E-20A)