AD9854/52 Rev E Evaluation Board Instructions

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Introduction:
The AD9854/52 Rev E evaluation board includes either an AD9854ASQ or AD9852ASQ IC. The ASQ package permits 300 MHz operation by virtue of its thermally enhanced design. This package has a bottom-side heat "slug" that must be soldered to the ground plane of the PCB directly beneath the IC. In this manner, the evaluation board, PCB ground plane layer extracts heat from the AD9854/52 IC package. If device operation is limited to 200 MHz and below, the AST package without a heat "slug" may be used in customer installations over the full temperature range. The AST package is less expensive than the ASQ package and those costs are reflected in the price of the IC.

Evaluation boards for both the AD9854 and AD9852 are identical except for the installed IC.

The AD9852 or AD9854 data sheet is essential to understand all of their modes of operation. While various *Preliminary* data sheets have been prepared and disseminated only the released data sheet should be used since errors and omissions in the preliminary data sheets are inevitable. A released data sheet will have no Preliminary markings and will display a revision status such as "REV 0" or "REV A" at the lower left corner of each page.

To assist in proper placement of the pin-header shorting-jumpers, the instructions on page 2 will refer to direction (left, right, top, bottom) as well as header pins to be shorted. Pin #1 for each three pin-header has been marked on the PCB corresponding with the schematic diagram. When following these instructions, position the PCB so that the PCB text can be read from left to right. The board is shipped with the pin-headers configuring the board as follows:

1) REFCLK for the AD9854/52 is configured as differential. The differential clock signals are provided by the MC100LVEL16D differential receiver.
2) Input clock for the MC100LVEL16D is single-ended via J25. This signal may be 3.3VCMOS or a 2V p-p sine wave capable of driving 50 ohms (R13).
3) Both DAC outputs from the AD9854/52 are routed through the two 120 MHz elliptical LP filters and their outputs connected to J7 (Q) and J6 (I).
4) The board is setup for software control via the printer port connector.
5) The DAC's output currents are configured for 10 mA.

General operating Instructions:

Load the Version 1.72 software from the provided CD onto your PC's hard disk. Connect a printer cable from the PC to the AD9854 Evaluation Board printer port connector labeled "J11". Version 1.72 software will support Windows 95, Windows 98, Windows Me, Windows NT, Windows 2000 or Windows Xp.

Hardware Preparation: Using the schematic in conjunction with these instructions will be helpful in acquainting the user with the electrical functioning of the evaluation board.

Attach power wires to connector labeled "**TB1**" using the screw-down terminals. This is a plastic connector that press-fits over a 4-pin header soldered to the board. Table below shows connections to each pin. DUT = "device under test"

AVDD +3.3V for all DUT analog pins	DVDD +3.3V for all DUT digital pins	VCC +3.3V for all other devices	Ground – for all devices

Attach REFCLK to clock input, J25**.**

Clock input, J25. This is actually a single-ended input that will be routed to the MC100LVEL16D for conversion to differential PECL output. This is accomplished by attaching a 2V p-p clock or sine wave source to J25. Note that this is a 50-Ohm impedance point set by R13. The input signal will be ac-coupled and then biased to the center-switching threshold of the MC100LVEL16D. To engage the differential-clocking mode of the AD9854 **W3** pins 2 & 3 (the bottom two pins) must be connected with a shorting jumper.

   The signal arriving at the AD9854 is called the **Reference Clock**. If you choose to engage the on-chip PLL clock multiplier, then this signal is the reference clock for the PLL and the multiplied PLL output becomes the **SYSTEM CLOCK**. If you choose to bypass the PLL clock multiplier, the reference clock that you have supplied is directly operating the AD9854 and is therefore the system clock.

Tri-state control or switch headers W9, W11, W12, W13, W14 and W15 must be shorted to allow the provided software to control the AD9854 evaluation board via the printer port connector J11.

If programming of the AD9854 is not to be provided by the users PC and ADI software then headers W9, W11, W12, W13, W14 and W15 should be opened (shorting jumpers removed). This effectively detaches the PC interface and allows the 40-pin header, **J10**, and **J1** to assume control without bus contention. Input signals on J10 and J1 going to the AD9854 should be 3.3V CMOS logic levels.

Low pass filter testing. The purpose of 2-pin headers **W7** and **W10** (associated with J4 and J5) are to allow the two 50-ohm 120 MHz filters to be tested during PCB assembly without interference from other circuitry attached to the filter inputs. *Normally, a shorting jumper will be attached to each header to allow the DAC signals to be routed to the filters.* If the user wishes to test the filters, the shorting jumpers at W7 and W10 should be removed and 50-Ohm test signals applied at J4 and J5 inputs to the 50-ohm elliptic filters. User should refer to the provided schematic and the following sections to properly position the remaining shorting jumpers.

Observing the <u>unfiltered</u> Iout1 and the <u>unfiltered</u> Iout2 DAC signals. This allows the viewer to observe the unfiltered DAC outputs at J5 (the "I" signal) and J4 (the "Q" or Control DAC signal). The procedure below simply routes the two 50-ohm terminated analog DAC outputs to the SMB connectors and disconnects any other circuitry. The "raw" DAC outputs may appear as a series of quantized (stepped) output levels that may not resemble a sine wave until they have been filtered. The default 10 mA output current will develop a 0.5 volts p-p signal across the on-board 50-Ohm termination. If your "observation" equipment offers 50-Ohm inputs, then the DAC will develop only 0.25 volts p-p due to the double termination.

1. Install shorting jumpers at W7 and W10.
2. Remove shorting jumper at W16
3. Remove shorting jumper from 3-pin header W1.
4. Install shorting jumper on pins 1 & 2 (bottom two pins) of 3-pin header W4

If using the AD9852 evaluation board, Iout2, the Control DAC output is under user control through the serial or parallel ports. 12-bit, <u>2's-complement</u> value(s) is/are written to the Q-DAC register that will set the Iout2 output to a static dc level. Allowable hexadecimal values are 7FF (maximum) to 800 (minimum) with all 0's being mid-scale. Rapidly changing the contents of the Q-DAC register (up to 100 MSPS) allows Iout2 to assume any waveform that can be programmed.

Observing the <u>filtered</u> Iout1 and the <u>filtered</u> Iout2. This allows viewer to observe the filtered "I" & "Q" (or Control) DAC outputs at J6 (the "I" signal) and J7 (the "Q" or Control signal). This places the 50–ohm (input and output Z) low pass filters in the "I" and "Q" (or Control) DAC pathways to remove images and aliased harmonics and other spurious signals above approximately 120 MHz. For "I" & "Q" signals, these signals will appear as nearly pure sine waves and 90 degrees out-of-phase with each other. These filters are designed with the assumption that the system clock speed is at or near maximum (300 MHz). If you system clock speed is much less than 300 MHz, for example 200 MHz, then it is possible or inevitable that unwanted DAC products other than the fundamental signal will be passed by the low pass filters.

If you are using the AD9852 evaluation board then any reference to the "Q" signal should be interpreted to mean "Control DAC".

1. Install shorting jumpers at W7 and W10
2. Install shorting jumper at W16
3. Install shorting jumper on pins 1 & 2 (bottom two pins) of 3-pin header W1
4. Install shorting jumper on pins 1 & 2 (bottom two pins) of 3-pin header W4
5. Install shorting jumper on pins 2 & 3 (bottom two pins) of 3-pin header W2 and W8

Observing the <u>filtered</u> Iout1 and the <u>filtered</u> Iout1B. This allows viewer to observe only the filtered "I" DAC outputs at J6 (the "true" signal) and J7 (the "complementary" signal). This places the 120 MHz low pass filters in the true and complementary outputs paths of the "I" DAC to remove images and aliased harmonics and other spurious signals above approximately 120 MHz. These signals will appear as nearly pure sine waves and 180 degrees out-of-phase with each other.). If you system clock speed is much less than 300 MHz, for example 200 MHz, then it is possible or inevitable that unwanted DAC products other than the fundamental signal will be passed by the low pass filters.

1. Install shorting jumpers at W7 and W10
2. Install shorting jumper at W16
3. Install shorting jumper on pins 2 & 3 (top two pins) of 3-pin header W1
4. Install shorting jumper on pins 2 & 3 (top two pins) of 3-pin header W4
5. Install shorting jumpers on pins 2 & 3 (bottom two pins) of 3-pin header W2 and W8

To connect the high-speed comparator to the DAC output signals you can choose either the quadrature filtered output configuration (AD9854 only) or the complementary filtered output configuration outlined above (both AD9854 and AD9852). Follow steps 1 through 4 for either filtered configuration as above. Step 5 below will re-route the filtered signals away from their output connectors (J6 and J7) and to the 100-Ohm configured comparator inputs. This sets-up the comparator for **differential input without control of the comparator output duty cycle**. The comparator output duty cycle should be close to 50% in this configuration.

5. Install shorting jumper on pins 1 & 2 (top two pins) of 3-pin header W2 and W8

User may elect to change the Rset resistor, R2 from 3.9k ohms to 1.95k ohms to get a more robust signal at the comparator inputs. This will decrease jitter and extend comparator-operating range. User can accomplish this by installing a shorting jumper at **W6,** which provides a second 3.9k chip resistor (R20) in parallel with the provided R2. This boosts the DAC output current from 10 mA to 20 mA and doubles the p-p output voltage developed across the loads

To connect the high-speed comparator in a single-ended configuration that will allow duty cycle or pulse width control requires that a dc threshold voltage be present at one of the comparator inputs. You may supply this voltage using the "Q-DAC or Control DAC" by configuring it as a control DAC in software. A 12-bit, <u>2's-complement</u> value is written to the Q-DAC register

that will set the Iout2 output to a static dc level. Allowable hexadecimal values are 7FF (maximum) to 800 (minimum) with all 0's being mid-scale. The Iout1 channel will continue to output a filtered sine wave programmed by user. These two signals are routed to the comparator using W2 and W8 3-pin header switches. You must be in the configuration described in the section "Observing the filtered Iout1 and the filtered Iout2". Follow steps 1 through 4 in that section and then the following:

5. Install shorting jumper on pins 1 & 2 (top two pins) of 3-pin header W2 and W8

The user may elect to change the Rset resistor, R2 from 3.9k ohms to 1.95k ohms to get a more robust signal at the comparator inputs. This will decrease jitter and extend comparator-operating range. User can accomplish this by installing a shorting jumper at **W6,** which provides a second 3.9k chip resistor (R20) in parallel with the provided R2.

Using the provided software:

The software is provided on a CD. If your circumstances require 3.5 inch disks, contact the applications engineer via email (david.brandon@analog.com) to obtain disks. This brief set of instructions should be used in conjunction with the AD9854 or AD9852 data sheet and the AD9854/52 Evaluation Board schematic.

Version 1.72 Software has been improved from previous versions in the following ways:

* Now works with all Windows Operating Systems except Windows NT 3.5

The CD-ROM contains the following

* The AD9852/54 Evaluation Software.
* The latest AD9852 and AD9854 datasheets.
* The DDS Tutorial
* Installers for all supported Windows Operating Systems
* Evaluation Board Schematics
* Evaluation Board PCB Layout Gerber Files

Several numerical entries, such as frequency and phase information, et al, require that the **ENTER key** by pressed to register that information. So, for example, if you input a new frequency and hit the load button and nothing new happens, it is probably because you forgot to press the enter key after typing the new frequency information.

1) Normal operation of the AD9854/52 evaluation board begins with a **master reset**. Many of the default register values after reset are depicted in the software "control panel". The reset command sets the DDS output amplitude to minimum and 0 Hz, 0 phase-offset as well as other states that are listed in the AD9854/52 Register Layout table in the data sheet.

2) The next programming block should be the "**Reference Clock & Multiplier**" since this information is used to determine the proper 48-bit frequency tuning words that will be entered and calculated later.

3) The output amplitude defaults to the 12-bit straight binary multiplier values of the "I" and "Q" multiplier registers of 000hex and no output should be seen from the DAC's. Set both multiplier amplitudes in the **Output Amplitude window** to a substantial value, such as FFFhex. You may bypass the digital multiplier by clicking the box "Output Amplitude is always Full-Scale" but experience has shown that doing so does not result in best SFDR. **Best SFDR, as much as 11 dB better,** is obtained by routing the signal through the digital multiplier and "backing off" on the multiplier amplitude. For instance, FC0 hex produces less

spurious signal amplitude than FFF hex. It's an exploitable and repeatable phenomenon that should be investigated in your application if SFDR (spurious-free dynamic range) must be maximized. This phenomenon is more readily observed at higher output frequencies where good SFDR becomes more difficult to achieve.

4) The user of this evaluation board is assumed to be a technically orientated person with basic knowledge of DDS, familiar with binary mathematics and digital / analog / RF electronics. The user should be able to "play" with the software from this point and learn how to operate the evaluation board intuitively.   Refer to the datasheet and evaluation board schematic to understand all the functions of the AD9854/52 available to the user and to gain an understanding of what the software is doing in response to your commands. The AD9854 and AD9852 final data sheets will become available the first week of November 1999.

In the event that you encounter difficulty, contact the applications engineer, david.brandon@analog.com, for help.

End of instructions.