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Evaluating the AD9912 1 GSPS Direct Digital Synthesizer with 14-Bit DAC

FEATURES

Flexible system clock input accepts crystal, crystal oscillator, or external reference clock
Dedicated pad for mounting crystal or crystal oscillator
DAC output easily accessible via SMA connector
SMA connectors provided for external reconstruction filter
Easy to use Windows graphical user interface
Software control of all AD9912 features
Power supplies that are easily separated
Connection via USB port
Dedicated SMA connectors for CMOS, DAC, and HSTL outputs
Residual phase noise at 250 MHz
   10 Hz offset: −113 dBc/Hz
   1 kHz offset: −133 dBc/Hz
   100 kHz offset: −153 dBc/Hz
   40 MHz offset: −161 dBc/Hz

PACKAGE CONTENTS

AD9912 evaluation board
USB cable

ONLINE RESOURCES

Note that the following items can be downloaded from the AD9912 Evaluation Board page at www.analog.com:
Evaluation software
Instructions
Data sheet
Schematics

GENERAL DESCRIPTION

The AD9912 evaluation board is an evaluation platform for the AD9912 direct digital synthesizer (DDS). It easily connects to a host computer via a USB interface and allows easy access to all AD9912 features via the Windows®-based evaluation software and graphical user interface.

This document provides instructions for the setup and installation of the board and software and includes a description of the various software menus and hardware connections. Additional evaluation board details, such as schematics, are available on the AD9912 evaluation board page at www.analog.com.

This document covers both Revision A and Revision B of the AD9912 evaluation board. The two versions differ in that Revision B has a convenient connection for a 1 kΩ pull-down resistor on the loop filter pin, whereas Revision A does not. Please note that Revision A of the AD9912 evaluation board is no longer in production.

The AD9912A/PCBZ operates over an industrial temperature range, spanning −40°C to +85°C.

EVALUATION BOARD BLOCK DIAGRAM
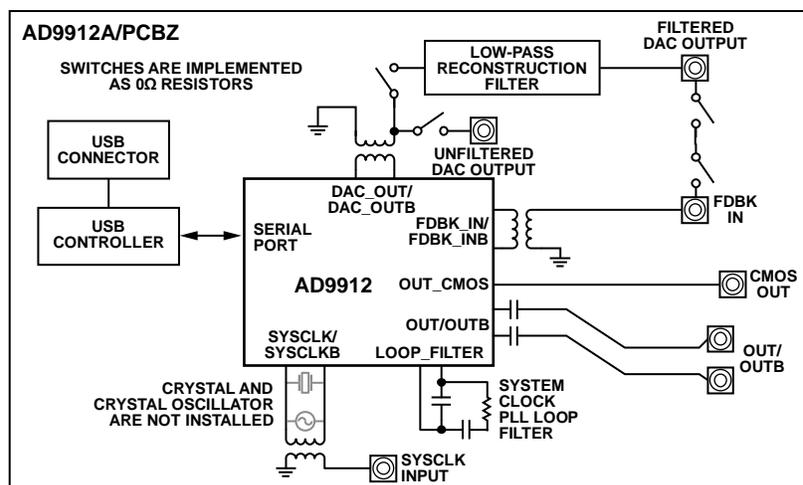
Figure 1.

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REVISION HISTORY

3/14—Rev. 0 to Rev. A

1/08—Revision 0: Initial Version

EVALUATION BOARD PHYSICAL CONNECTIONS
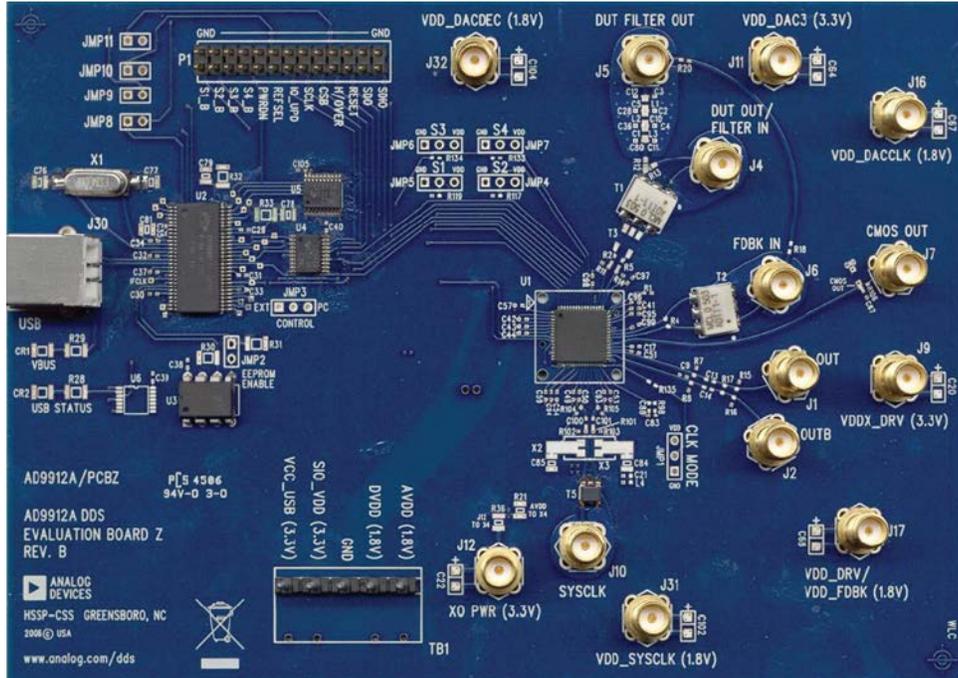
Figure 2. AD9912 Evaluation Board, Rev. B

The following instructions are for setting up the physical connections to the AD9912 evaluation board. They assume that the evaluation software has already been installed. The physical connections for Revision A and Revision B of the AD9912 evaluation board are identical.

The following case is used as an example: output frequency: 155.52 MHz; DAC system clock: 1000 MHz input provided on the SYSCLK SMA connector; system clock PLL is disabled.

POWER CONNECTIONS

1. Connect power and ground to the main power connector labeled TB1, and follow the silkscreen labels describing each power connection.

2. Connect a 1.8 V supply to VDD_DACDEC (J32).

3. Connect a 3.3 V supply to the following AD9912 SMA connectors: VDD_DAC3 (J11) and XO_PWR (J12) (XO_PWR is only necessary if there is a crystal oscillator mounted on the board).

4. If using the CMOS OUT (J7), power must also be applied to VDDX_DRV (J9), and R106 must be populated with a 0 Ω resistor. VDDX_DRV can be either 1.8 V or 3.3 V. Note that the power-on default of the AD9912 is CMOS driver enabled, HSTL driver disabled.

5. Ensure that the S1 to S4 jumpers are tied to VDD. These settings are only for generating 155.52 MHz at startup and register programming overrides these settings.

6. Apply power.

Note that there are two other 1.8 V power connectors, VDD_DACCLK (J16) and VDD_DRV/VDD_FDBK (J17), on the evaluation board. These power supplies are fed by the AVDD supply on connector TB1 when the following 0 Ω resistors are in place (on the back of the board): R9, R10, R23, R60, R63, R64, R65, R66, R19, R22, and R132.

CONNECTIONS TO PC

1. Connect the USB cables to the evaluation board and the computer. The LED labeled USB on the AD9912 evaluation board should be blinking.

2. See the Evaluation Board Software Setup section for details on running the AD9912 evaluation board software.

SIGNAL CONNECTIONS

1. Ensure that JMP1 connects VDD to the center pin.

2. Connect the 1 GHz signal generator to SYSCLK (J10). An amplitude setting of 0 dBm to +3 dBm is fine. If a crystal oscillator is used for generating SYSCLK, the SYSCLK (J10) input can be left open.

3. The user has the following four output options on the AD9912:

   - CMOS driver (default): connect an oscilloscope/ spectrum analyzer to CMOS_OUT (J7). Note that R106 must be installed to connect J7 to the CMOS out on the AD9912. Connect DUT FILTER OUT (J5) to FDBK IN (J6). Note that this step is not necessary if R20 (near J5) and R18 (near FDBK IN/J6) are stuffed.

- HSTL driver: put a 50 Ω terminator on OUTB (J2), and connect OUT (J1) to a spectrum analyzer. Connect DUT FILTER OUT (J5) to FDBK IN (J6). Note that this step is not necessary if R20 (near J5) and R18 (near FDBK IN/J6) are stuffed. Enable the HSTL driver in the evaluation software.

- Filtered DAC output: remove R13, and put a 0 Ω resistor across R12. Remove R20. Connect a spectrum analyzer to DUT FILTER OUT (J5).

- Unfiltered DAC output: remove R12, and put a 0 Ω resistor across R13. Connect a spectrum analyzer to DUT OUT/FILTER IN (J4).

USING AN OSCILLATOR FOR THE SYSTEM CLOCK

1. Solder the 5 mm × 7 mm oscillator to X4.

2. R101, R102, and R103 may need to be adjusted or removed depending on the oscillator output type. Refer to the evaluation board schematic for details.

3. Install the appropriate system clock PLL loop filter, and remove the 1 kΩ pull-down resistor on the LF pin. Refer to the evaluation board schematic on www.analog.com for details.

USING A CRYSTAL FOR THE SYSTEM CLOCK

1. Remove C100, C101, and Transformer T5.

2. Solder crystal to X2 or X3, depending on size.

3. Install R104 and R105. 0 Ω is a recommended starting point, but the user may need to experiment with higher values if the crystal is being overdriven.

4. Refer to the evaluation board schematic for recommended values of C84, C21, and L4.

5. Change JMP1 to straddle the center pin and GND.

6. Install the appropriate system clock PLL loop filter, and remove the 1 kΩ pull-down resistor on the LF pin. Refer to the evaluation board schematic for details.

USING AN EXTERNAL RECONSTRUCTION FILTER

1. Install a 0 Ω resistor at R13, and remove R20 and R18.

2. Connect the single-ended reconstruction filter to J4 and J6.

EVALUATION BOARD SOFTWARE SETUP

The following instructions are for setting up the AD9912 evaluation board software. The same software can be used for both Revision A and Revision B of the AD9912 evaluation board.

The following case is used as an example: output frequency: 155.52 MHz; DAC system clock: 1000 MHz input provided on the SYSCLK SMA connector; system clock PLL is disabled.

HOST PC REQUIREMENTS

To successfully use the evaluation board and run the software, the requirements listed in Table 1 must be met.

Table 1. AD9912A/PCBZ Requirements

Item	Requirement
Operating System	32-bit Windows® 7/98/ME/2000/XP Note: 64-bit Windows® is supported by running Windows® XP under Windows® Virtual PC
Processor	Pentium® I or later
Memory	128 MB minimum
Ports	One USB port
Clocking	Signal generator capable of generating sinusoidal waves of at least 0 dBm, up to at least 10 MHz
Power Supplies	Capability to generate at least two independent dc voltages (1.8 V/3.3 V)
Measurement	Appropriate measurement device, such as a spectrum analyzer or a high bandwidth oscilloscope
Cables	USB 1.1/2.0 cable and SMA-to-X cables (X = SMA or BNC, depending on the connector of the device interfacing with the board)

SOFTWARE INSTALLATION

1. Download the AD9912 Evaluation Software by visiting www.analog.com and searching **AD9912**.

2. Click the **Evaluation Boards & Kits** link. The AD9912 evaluation software page has links to the evaluation software, as long as schematics and Gerber files.

3. Click the **AD9912 Evaluation Software** link.

4. Double-click the downloaded file to install the software.

5. Follow the installation instructions.

    The default location for the evaluation software is **C:\Program Files\ADI\AD9549_9912 Eval Software**.

RUNNING THE SOFTWARE

1. If you have not connected your evaluation board yet, refer to the Evaluation Board Physical Connections section.

2. Double-click **AD9549 & AD9912 Evaluation Software**.

3. Run the AD9912 evaluation software, and click the splash screen when the **Software Ready** message is displayed. You will see the **Interactive Block Diagram** window, which is the main window for the software.

4. If you have not yet connected your evaluation board, you will be prompted to choose AD9912 or AD9549 evaluation board. Click **AD9912 Evaluation Board**.

    Note that Windows will indicate **Found New Hardware** the first time you connect the evaluation board. Nothing special needs to be done when this happens, and Windows will install the software driver. It may be necessary to disconnect and reconnect the USB cable after this happens.

5. In the lower left corner of the window, look for **Ezssp-0**, **Ezssp-1**, or **Ezssp-2** in green letters. This indicates that the software has found and connected to the evaluation board. If you see **not connected**, the software cannot locate the evaluation board. Try selecting **Select Evaluation Board** from the **I/O** menu and see if **Ezssp-0**, **Ezssp-1**, or **Ezssp-2** can be selected. If not, check your cable connections, power cycle the board, and rerun the software to remedy this problem.

6. The main window is the **Interactive Block Diagram** window. Click the **Reset** button at the top of the **Interactive Block Diagram** window.

7. If you have a setup file, click **Load Eval Board Setup** at the top of the window and select the desired setup .STP file.

8. If the reference frequency that is provided to the system clock input is different from 25 MHz, click the **DDS** box, and enter the frequency in the **External Clock** box. This is critical because the evaluation software relies on the correct system clock in order to calculate the various frequencies used on the AD9912.

9. You should now see the 155.52 MHz output. If HSTL output on Connector J1 and Connector J2 are desired, enable the 1.8 V HSTL driver by clicking the triangle inside the dashed box in the **Interactive Block Diagram** window.

10. If the CMOS driver is not being used, it can be powered down by clicking the triangle inside the dashed box in the **Interactive Block Diagram** window.

See the Evaluation Software Main Window section for a description of the main window features, or see the Evaluation Software Functional Blocks section for details on the individual blocks of the AD9912.

# EVALUATION SOFTWARE MAIN WINDOW
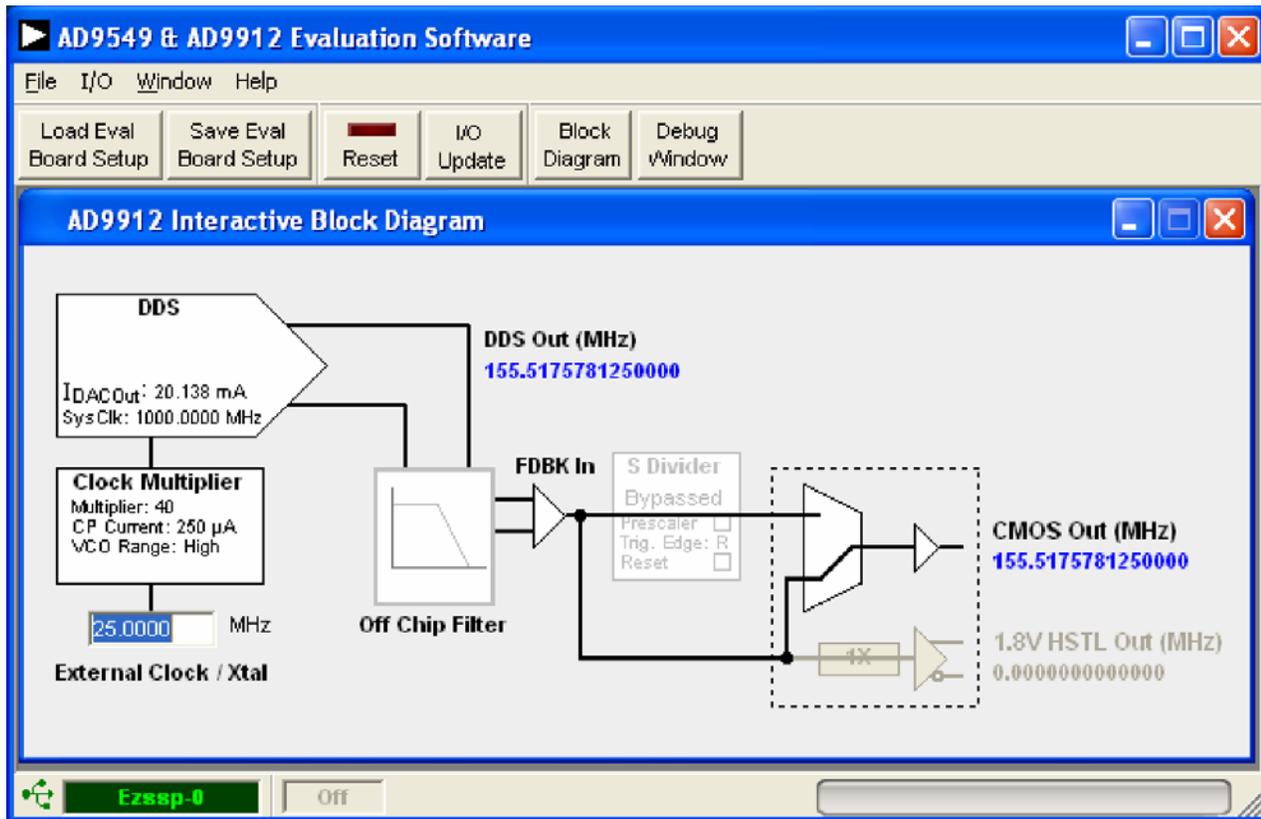
Figure 3. AD9912 Interactive Block Diagram

The main window of the evaluation software consists of three major areas: the menu bar, the button bar, and the window display area. The window display area is where windows such as the **Interactive Block Diagram** window appear.

Note that the AD9549 and AD9912 share the same evaluation software. If the evaluation board is not found, the software prompts the user to select which evaluation board will be connected.

Access to the individual components and features of the AD9912 can be accomplished in two ways. The user can click a given block from the **Interactive Block Diagram** window, and that block's own window will open. The same window can also be accessed from the **Window** menu in the menu bar.

INTERACTIVE BLOCK DIAGRAM

The **Interactive Block Diagram** window shows all of the major blocks of the chip, and clicking a block, such as **DDS**, brings up a window where the user can change the settings for that block. It displays the current settings for the entire chip, such as input and output frequency, system clock, reference selected, and the status of the S1 to S4 pins.

Figure 3 shows the default condition for S1 to S3 = 1, and S4 = 0.

MENU BAR

File Menu

Load Evaluation Setup File/Save Evaluation Setup File

Identical to selecting the **Load Eval Board Setup/Save Eval Board Setup** buttons on the button bar, this loads/saves an AD9912 setup file (.STP). A setup file is a text file that contains the AD9912 register setup file, plus any evaluation board settings.

Note that when saving register setup files, it is important to select single-tone mode before saving the file. Register setup files are loaded into the AD9912 sequentially, and the loop should only be locked once all registers are loaded. Otherwise, the part may need to be reset.

Options

Allows the user to control whether the software polls the evaluation board. The startup log can also be viewed by clicking **View Startup Log** from this window.

Exit

Exits the evaluation software. No checking is done to ensure that the existing setup is saved.

I/O Menu

Select Evaluation Board

The AD9912 evaluation system allows one PC to control multiple evaluation boards. This command allows the user to select which evaluation board the software controls.

DUT I/O Configure

This command selects 3- or 4-wire serial port mode, LSB first, and contains a button for a soft I/O reset.

Window Menu

This menu allows the user to select any of the 14 windows that are associated with the major functional blocks of the AD9912. These windows are also accessible by going to the **Interactive Block Diagram** window and clicking the block of interest. See the Evaluation Software Functional Blocks section for a description of each of these windows.

Help Menu

Selecting **Help** brings up the **About AD9912** splash screen. It contains information such as revision number, region information, and contact information.

BUTTON BAR

The following buttons are provided for easy access to common features.

Load Eval Board Setup/Save Eval Board Setup

These buttons allow the user load/save an AD9912 setup file (.STP). A setup file is a text file that contains the AD9912 register setup file, plus any evaluation board settings.

Note that when saving register setup files, it is important to select single-tone mode before saving the file. Register setup files are loaded into the AD9912 sequentially, and the loop should only be locked once all registers are loaded. Otherwise, the part may need to be reset.

Reset

This button resets the evaluation board and restores the AD9912 to its default power-up state.

I/O Update

This button toggles the IO_UPDATE pin on the AD9912.

Block Diagram

This button selects the **Interactive Block Diagram** window.

Debug Window

This button selects the **Debug** window. See the Debug Window section for a description.

EVALUATION SOFTWARE FUNCTIONAL BLOCKS

The AD9912 evaluation software is made up of subsections that correspond to the AD9912's major functional blocks. These subsections are listed in the following sections, and each of these has its own window.

The main window is the **Interactive Block Diagram** window, and from it, the window for each functional block can be accessed by clicking that block. The user can also access each of these windows from the **Window** menu at the top of the window.

Each window has a check box labeled **Auto I/O Update**. If this box is checked, the software performs an I/O update operation any time there is a setting change in that box.

For convenience, some detailed information from the AD9912 data sheet is included here. In cases where there is an inconsistency between this document and the AD9912 data sheet, assume that the data sheet is correct. Please inform us of this inconsistency so that it can be corrected.

INTERACTIVE BLOCK DIAGRAM

The **Interactive Block Diagram** (IBD) window shows all of the major blocks of the chip, and clicking a block, such as **DDS**, brings up a window where the user can change the settings for that block.

S-DIVIDER SETTINGS WINDOW

Clicking the **S-Divider** box brings up the **S-Divider Settings** window.

This window is used for setting the output divider for the CMOS output and for setting the divide-by-2 prescaler. Note that this bit must be set if the signal present on FDBK_IN is 400 MHz or greater.

DDS AND CLOCK MULTIPLIER CONTROL

Clicking the **DDS** and **Clock Multiplier** box brings up the **DDS and Clock Multiplier** window. This window is used to set up the system clock PLL and is frequently used. It contains two tabs: **DDS** and **Harmonic Spur Reduction**.

The **DDS** tab has three sections: **DDS Clock**, **DDS Settings**, and **DAC Control**.

In the **DDS Clock** section of the tab, the frequency of the external clock source driving the system clock is entered into the box labeled **External Clock**. The default is 25 MHz. If the system clock is supplied directly, be sure to put a check in the **Bypass Multiplier** check box.

If the system clock PLL (SYSCLK PLL) is to be used, enter the desired multiplication factor. The multiplier value in the panel does not factor in the bipolar edge detector. Therefore, if an overall multiplication factor of 40 is desired when using the bipolar edge detector, ×20 should be entered for the multiplier.

It is recommended to put a check in the **Auto Range** check box. This is especially true for system clocks in the 800 MHz to 900 MHz range. Refer to the AD9912 data sheet on the use of VCO Auto Range.

The charge pump current of 250 μA (default) is fine for most applications, but it can be adjusted here if desired.

The **Clock Multiplier** section has an ×**2 Reference** check box, and it controls the bipolar edge detector of the system clock PLL. This frequency doubler can reduce the in-band jitter of the system clock PLL, and it is described in detail in the AD9912 data sheet. When this box is checked, the multiplier must be cut in half to maintain the same overall frequency multiplication.

The desired output frequency is entered in the **DDS Settings** section. Note that loading the DPLL settings that are generated using FilterDesign.xls automatically sets the output frequency calculated in FilterDesign.xls. The primary value of entering an output frequency here is to set up single-tone mode without having to configure the DPLL loop filter. The **DDS Settings** section also features a place to enter a static phase offset. Bear in mind that this static phase offset is not active when the DPLL loop is closed.

DAC Control is the last section of the DDS tab. The DDS DAC current can be altered here. However, the default values are recommended, and these values are not normally altered. Increasing the DAC current increases the output amplitude but can degrade the harmonic performance of the DAC. One case where this might be useful is when using a SAW filter because they can have high insertion loss.

CMOS DRIVER AND CLOCK OUT

Clicking the mux symbol near the CMOS output driver in the **Interactive Block Diagram** window brings up the **CMOS Driver and Clock Out** window. Features that are accessed here include the CMOS output divider, HSTL driver power-down, and the HSTL output doubler.

STATUS AND IRQ CONTROL WINDOW

This feature is not applicable to the AD9912.

DEBUG WINDOW

Clicking the **Debug** button at the top of the evaluation software window brings up the **Debug** window. This is a legacy window, and the user should not normally need to access it.

The **Serial I/O** section of this window provides a handy way to read and write registers directly.

Quick Edit provides an easy way to get a quick look at the **DPLL Registers and Settings**. This includes the digital loop filter coefficients, the dividers, and the frequency tuning word.

REGISTER MAP (REGMAP VALUES) WINDOW

Clicking **RegMap Values** in the **Window** menu brings up the **Register Map** window. This is a handy text window for quickly viewing the register map.

AD9912 EVALUATION BOARD RECONSTRUCTION FILTER

Revision A of the AD9912 evaluation board has a 240 MHz low-pass reconstruction filter that is shown in Figure 4. Revision B has a 400 MHz low-pass reconstruction filter. This filter is implemented as a single-ended filter with a transformer on both sides to convert to/from a differential configuration. The transformer used is a Mini-Circuits ADTT-1, and its −3 dB bandwidth is approximately 0.3 MHz to 300 MHz.

SINGLE-ENDED FILTER DESIGN

The single-ended design with transformers is less susceptible to component variation and is strongly recommended for cases where the cutoff frequency must be tightly controlled, or in designs using a pass-band reconstruction filter. See the AD9912 evaluation board schematic for the exact circuit implementation.

7th Order Single-Ended Low-Pass Elliptical Filter (Rev. A)

- Pass-band frequency: 240 MHz

- Pass-band ripple: 0.1 dB

- Stop-band ratio: 1.3

- Stop-band frequency: 312 MHz

- Stop-band attenuation: 60 dB

Location of Filter Components on Evaluation Board

Note that when the on-board reconstruction filter is bypassed, R12 is removed. R13 is installed and the output is on Connector J4. The following values are for the 240 MHz reconstruction filter:

- 9 pF shunt capacitor: C11 = 4.7 pF in parallel with C80 = 4.7 pF

- 20 pF shunt capacitor: C4 = 10 pF in parallel with C36 = 10 pF

- 23 pF shunt capacitor: C2 = 12 pF in parallel with C28 = 12 pF

- 14 pF shunt capacitor: C3 = 6.8 pF in parallel with C14 = 6.8 pF

- 1st LC combination: C1 = 8.2 pF, L3 = 27 nH

- 2nd LC combination: C10 = 4.7 pF, L2 = 39 nH

- 3rd LC combination: C5 = 1.5 pF, L1 = 47 nH
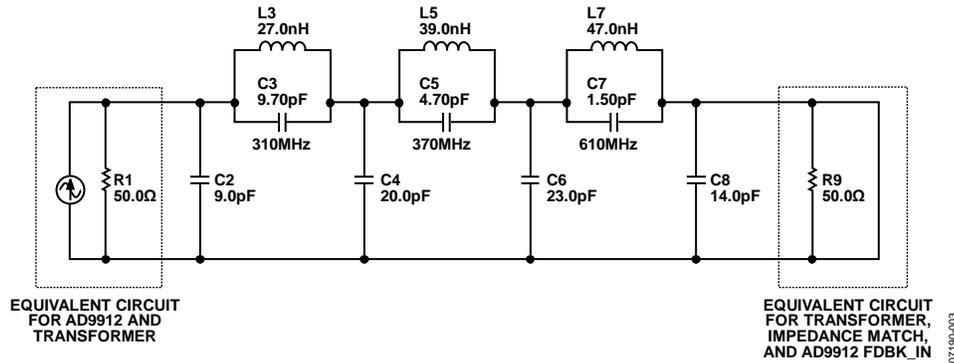
Figure 4. AD9912 Evaluation Board 240 MHz Single-Ended Reconstruction Filter
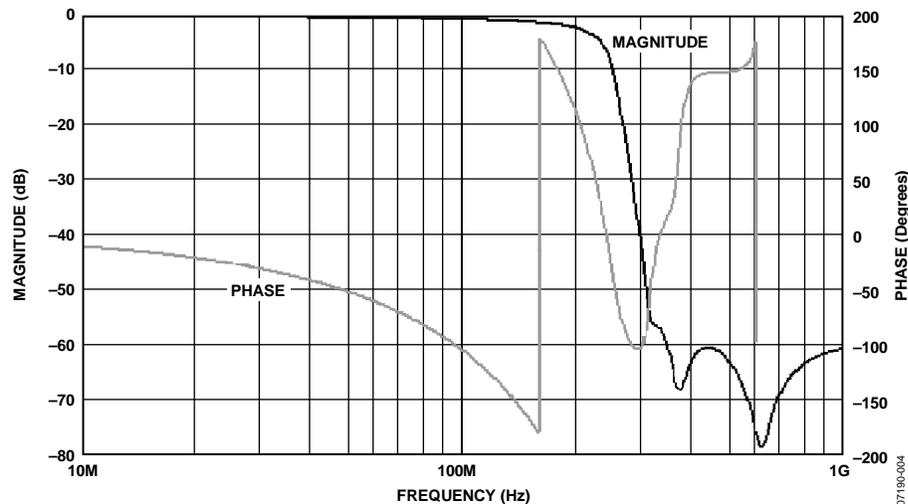
Figure 5. Frequency Response of Single-Ended Reconstruction Filter Shown in Figure 4

DIFFERENTIAL FILTER DESIGN

The differential filter advantages include fewer components and a simpler design when the AD9912 is used in an actual design. Note that the 100 Ω differential source impedance is internal to the IOUT/IOUB driver. Also, note that the ac coupling between the IOUT differential pair and the FDBK_IN differential pair is critical. Component matching between the corresponding LC sections is important in this design. The example shown in Figure 6 is for a cutoff of 240 MHz.

7th Order Elliptical Differential Low-Pass Filter

- Pass-band frequency: 240 MHz

- Pass-band ripple: 1.0 dB

- Stop-band ratio: 1.3

- Stop-band frequency: 312 MHz

- Stop-band attenuation: 70 dB
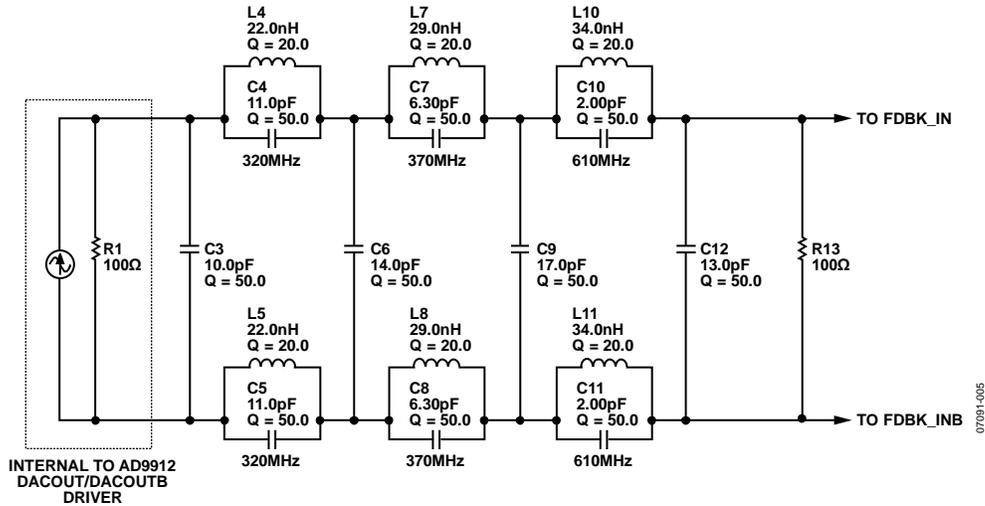
Figure 6. Differential Low-Pass Reconstruction Filter
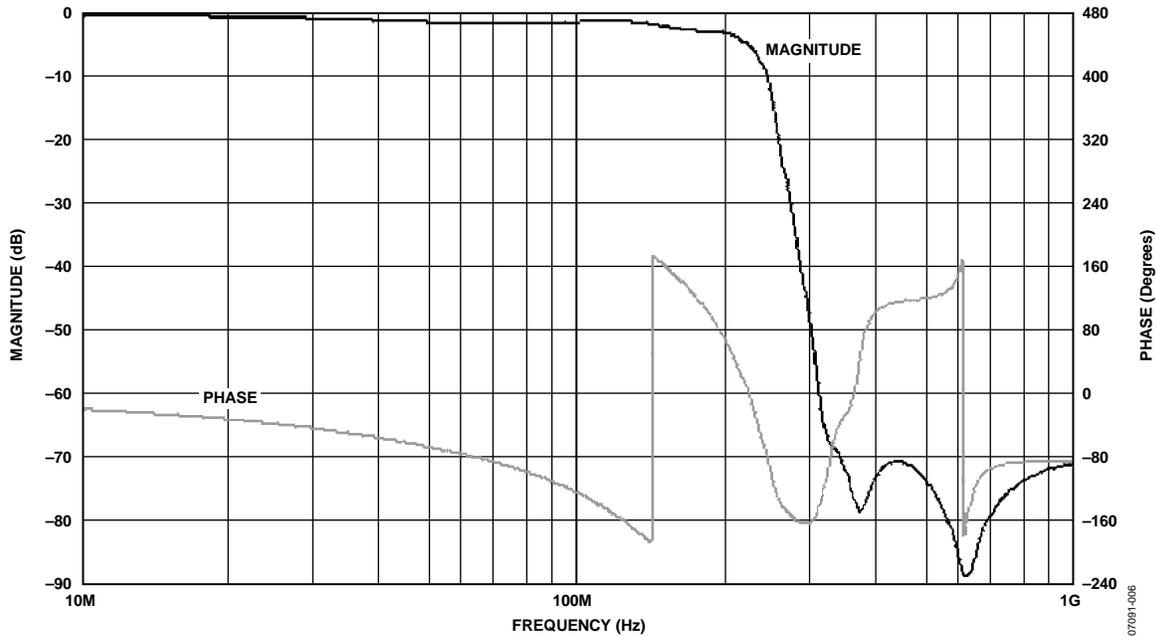
Figure 7. Frequency Response of Differential Reconstruction Filter Shown in Figure 6

AD9912 SYSTEM CLOCK PLL LOOP FILTER

The AD9912 system clock PLL has an external loop filter whose components are tailored for different applications.

If the system clock PLL is bypassed, the LOOPFILTER pin should be pulled down to ground with a 1 kΩ resistor.

The loop bandwidth of the SYSCLK multiplier PLL can be adjusted by means of three external components, as shown in Table 2. The nominal gain of the VCO is 800 MHz/V. The recommended component values and their locations on the evaluation board are shown in Table 2. They establish a loop bandwidth of approximately 1.6 MHz with the charge pump current set to 250 μA. The default case is N = 40 and assumes a 25 MHz SYSCLK input frequency and generates an internal DAC sampling frequency (f_S) of 1 GHz.

When modeling the AD9912 system clock PLL, bear in mind that there is approximately 5 pF of parallel capacitance internal to Shunt C (C88). The values in Table 2 are the actual values

that should be used on the board and do not include this internal capacitance.

The AD9912 features a bipolar edge detector that doubles the rate of the clock going into the system clock PLL. The multiplication factors in Table 2 are for the system clock PLL only. Refer to the AD9912 data sheet for more details on the system clock PLL and bipolar edge detector.

Table 2. Recommended SYSCLK PLL Loop Filter Values

SYSCLK Multiplier	Series R (R98)	Series C (C83)	Shunt C (C88)
8 (or less)	390 Ω	1 nF	82 pF
10	470 Ω	820 pF	56 pF
20	1 kΩ	390 pF	27 pF
40 (default)	2.2 kΩ	180 pF	10 pF
60	2.7 kΩ	120 pF	5 pF

NOTES

ANALOG DEVICES

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