

Synchronizing Multiple **AD9915** DDS-Based Synthesizers

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INTRODUCTION

Various applications require the generation of two or more sinusoidal or square wave signals with a known phase relationship between them. The **AD9915** DDS IC from Analog Devices, Inc., is capable of providing such signals. This application note offers detailed instructions on how to synchronize two or more of these devices and considers possible sources of phase error.

For successful synchronization, the user must have control over the timing of the REF CLK, SYNC_CLK, and the IO_UPDATE to each device. The goal is to have all DDS devices operating on the same internal system clock count and not off by ± 1 or more counts between devices. Therefore, the SYNC_CLK of each device must be aligned to one another and the IO_UPDATE of

each device must be made synchronous to the SYNC_CLK. As a result, all output phase error uncertainty of ± 1 or more system clock period(s) is eliminated.

Note that any output phase error due to output filtering mismatches, REF CLK skew, and other external sources typically manifests as a fixed source of error. However, the DDS provides programmable output phase adjust features that can null out fixed sources of phase error. This application note describes the basic requirements to synchronize multiple DDS parts. Successful synchronization starts with the distribution of the REF CLK signal.

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REVISION HISTORY

12/13—Revision 0: Initial Version

HOW TO SYNCHRONIZE MULTIPLE PARTS

PROVIDE A COINCIDENT REF CLK TO ALL DDS PARTS TO BE SYNCHRONIZED

The first requirement for successful synchronization of multiple AD9915 parts is that there must be minimal phase error between the REF CLK inputs to each DDS. If the REF CLK input signal is misaligned across multiple DDS parts, the outputs (at a minimum) will be misaligned by the same amount, less any other causes. Therefore, the user must employ careful clock distribution practice in the layout of the PCB (see Figure 1).

In reality, too much REF CLK misalignment or input clock skew can inhibit the ability to align the SYNC_CLK across multiple DDS parts to the same REF CLK edge. Without SYNC_CLK alignment, multichip synchronization is not possible. Note that the internal system clock of the DDS is a delayed copy of the REF CLK, so each device has the same internal clock rate. This assumes the internal PLL is disabled. If this is not the case, the system clock rate equals the REF CLK rate times the PLL multiplication factor programmed.

The maximum system clock rate supported for multiple synchronized DDS parts is 2.5 GSPS. Running beyond this rate makes it more difficult to implement a robust timing solution. The internal PLL supports multiple chip synchronization, if desired.

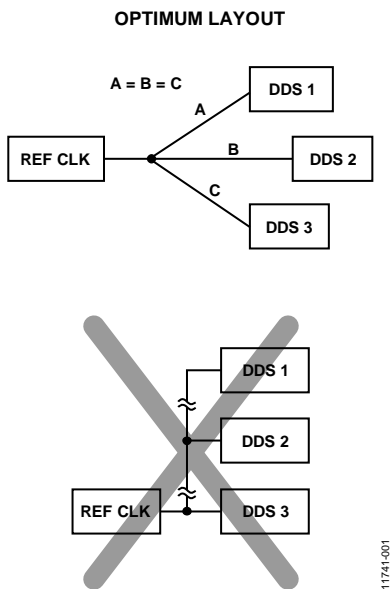


Figure 1. Recommended Layout (Top) vs. Suboptimal Layout (Bottom)

ALIGN THE SYNC_CLK TO ALL DDS PARTS

The SYNC_CLK is a CMOS clock output with an output frequency equal to the system clock divided by 16. The SYNC_CLK internally samples IO_UPDATE, thus the SYNC_CLK output is externally provided to synchronize to an external IO_UPDATE. At power up, the SYNC_CLK edges of each part are randomly in one of 16 phase states with respect to one another, even if the REF CLK is in perfect alignment across multiple devices.

For this reason, the SYNC_CLK edges must be aligned to one another first for proper synchronization. If not, the phase accumulators of multiple devices will not accumulate on the same system clock count in time.

Synchronization of the SYNC_CLK across multiple devices requires several register bit settings, a coincident SYNC_IN signal, and issuing an automatic DAC calibration to each part. Essentially, the goal is to reset (via the SYNC_IN signal) the internal divider that generates the SYNC_CLK. This is accomplished by sending a coincident SYNC_IN to each DDS. In addition, the SYNC_IN must meet the internal setup time to the internal system clock.

In most cases, the SYNC_IN signal is derived from the SYNC_OUT signal generated by the master DDS. Both the SYNC_IN and SYNC_OUT signals are 3.3 V CMOS logic signals. The SYNC_OUT clock rate equals 1/384th of the system clock rate. Note that SYNC_IN is not required to be driven by the SYNC_OUT output of the master DDS device, but the SYNC_IN source rate must be at an integer submultiple of the system clock rate and less than 50 MHz for synchronization.

At 2.5 GSPS maximum operation, the period of the internal system clock is 400 ps. For synchronization of multiple devices and the best internal timing margin, the SYNC_IN should be placed in the middle of the system clock period as shown in Figure 2.

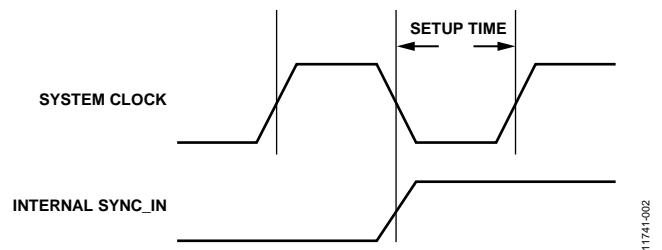


Figure 2. Desired Internal Timing

However, the user does not have direct access to the internal timing relationship between the SYNC_IN and REF CLK signals in Figure 2 because they propagate internally. Note that at the external SYNC_IN pin and external REF CLK pin, the AD9915 is designed to meet the minimum internal setup time (up to 2.5 GSPS), as long as the rising edge of the SYNC_IN signal is coincident in time to the rising edge of the REF CLK signal. See Figure 3 for the timing relationship.

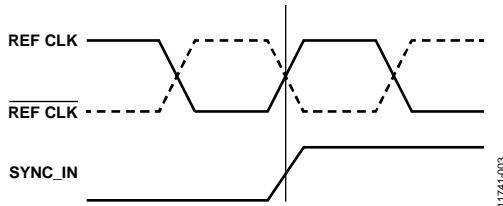


Figure 3. Desired External Timing

If this timing relationship is not satisfied at the external pins to all devices, then the SYNC_IN signal can still be adjusted relative to the REF CLK edge. This is accomplished via the SYNC_OUT internal programmable delay bits in Register 0x1B. Thus, as the SYNC_OUT is adjusted, the SYNC_IN edge to all devices should adjust accordingly. See the AD9915 data sheet for more details.

In addition, the internal SYNC_IN signal path has delay adjustment bits via Register 0x1B. As a result, the internal SYNC_IN can be delayed to individual devices with respect to the system clock. If too much delay is programmed, the SYNC_CLK output jumps by discrete system clock periods between devices depending on the amount of SYNC_IN delay applied causing misalignment of the SYNC_CLK edges. A procedure for aligning the SYNC_CLK can be found in the Align the SYNC_CLK Across Multiple Parts section. After the SYNC_CLK of each device is aligned, the SYNC_OUT signal can be disabled.

PROVIDE A COINCIDENT IO_UPDATE TO ALL DDS DEVICES

After the SYNC_CLK of each part is aligned, further programming requires a common IO_UPDATE. For example, without sending an IO_UPDATE, the frequency tuning word register and the phase offset word register of each device could be first preprogrammed with the desired values asynchronously device by device. As a result, the DDS core to all devices does not act upon these changes until the IO_UPDATE is issued. Accordingly, a common IO_UPDATE to all devices thereafter forces the frequency tuning word and phase word to simultaneously update on the same internal system clock count to all devices with the desired outcome.

The IO_UPDATE must occur synchronous to the SYNC_CLK. The minimum setup time is 2 ns and the minimum hold time is 0 ns. If this timing is satisfied and the SYNC_CLK is aligned across all devices, then synchronization is possible.

ALIGN THE SYNC_CLK ACROSS MULTIPLE PARTS

This is an eight step procedure.

1. Power up all devices and apply the REF CLK source. A circuit block diagram is shown in Figure 4. Note that the REF CLK signal should have the lowest REF CLK timing skew possible across all devices. Attempting to operate with a system clock greater than 2.5 GSPS reduces the probability of successful multichip synchronization.
2. Send a common master reset to all DDS devices. The master reset signal can be sent asynchronous to each part. A master reset places the internal registers to predefined default states.
3. Issue a DAC CAL to all DDS devices. Set the DAC CAL bit in Register 0x03 to Logic 1 and then clear afterwards. That is, apply one IO_UPDATE to set the DAC CAL bit high and another IO_UPDATE to clear the DAC CLK bit. At this point, the IO_UPDATE can be applied asynchronous to the devices.
4. Set the SYNC_OUT enable bit, Bit 9, in Register 0x01 to Logic 1 on the master DDS device only. Apply an IO_UPDATE. This should turn on the SYNC_OUT driving the SYNC_IN pin of the master and all the SYNC_IN pins of the slave devices. In most cases, the SYNC_OUT should be buffered with an external fan out device to drive multiple devices. The frequency of the SYNC_OUT is $1/384^{\text{th}}$ of the system clock. At this point, the IO_UPDATE can be applied asynchronous to the devices.
5. Set the CAL with SYNC bit in Register 0x1B to Logic 1 for all devices. Again, the IO_UPDATE can be applied asynchronous to the devices at this point.
6. Using the programmable SYNC_OUT delay bits in Register 0x1B, adjust the bits to best align the rising edge of the SYNC_IN and REF CLK signals at the master device (see Figure 3).
7. Perform another DAC CAL to each part (repeat Step 3), including the master device. Again, the IO_UPDATE can be applied asynchronous at this time. This step should cause the SYNC_CLK of each device to be aligned with the SYNC_CLK of the master device.
8. With the SYNC_CLK of each part aligned to the master device, the next step is to test for proper synchronization. Set the three profile pins to Logic 0 on all devices.
 - Without sending an IO_UPDATE, program all devices individually to enable profile mode and program the desired frequency tuning word into the Profile 0 register.
 - Next, send a common or coincident IO_UPDATE to all devices. The IO_UPDATE must meet the setup and hold time to the SYNC_CLK. This step should cause the DDS outputs to be aligned to one another.

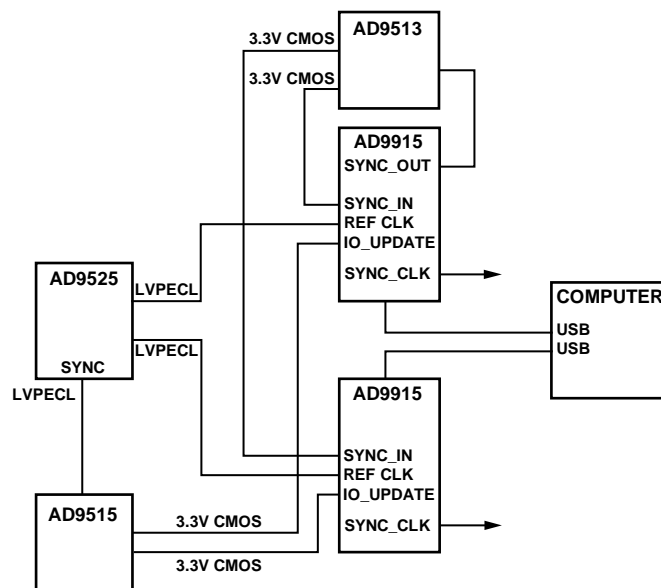


Figure 4. Concept Circuit

SUMMARY

With proper care and the use of the procedure described in this application note, output synchronization can be achieved among multiple DDS parts.

Figure 5 through Figure 7 illustrate what could be expected for the various timing relationships between four devices. Figure 5 represents the random SYNC_CLK alignment between four devices upon power up and before any synchronization steps are taken, even if the REF CLK to each part is perfectly phase aligned to each other.

Figure 6 and Figure 7 represent SYNC_CLK and DDS output alignment following the SYNC_CLK alignment procedure along with issuing a coincident IO_UPDATE in Step 8.

Note that the phase offset value between devices in Figure 7 is presumed the same value. If the phase offset value of one device was changed by 90° that device output would shift 90° with respect to the other three outputs.

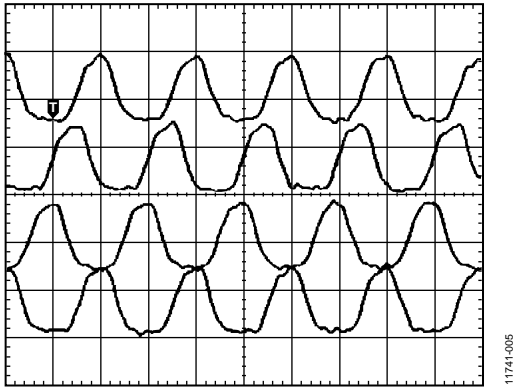


Figure 5. Random Alignment of the SYNC_CLK between Devices after Power Up

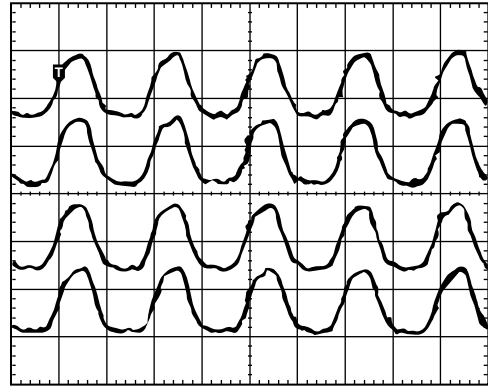


Figure 6. Alignment of SYNC_CLK between Devices after the SYNC_CLK Alignment Procedure

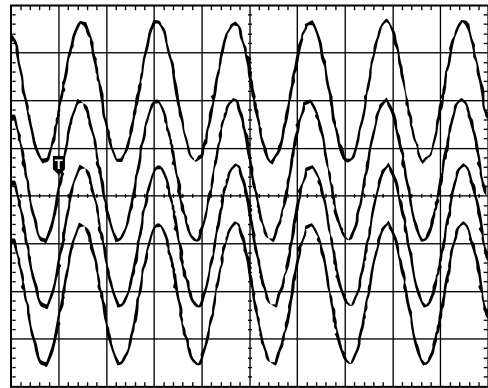


Figure 7. Output between Devices after the SYNC_CLK Alignment Procedure and a Coincident IO_UPDATE

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