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Low Jitter Sampling Clock Generator for High Performance ADCs Using the AD9958 500 MSPS DDS or the AD9858 1 GSPS DDS and the AD9515 Clock Distribution IC

CIRCUIT FUNCTION AND BENEFITS

This circuit uses a direct digital synthesizer (DDS) with subHertz tuning resolution as a low jitter sampling clock source for high performance analog-to-digital converters (ADCs). The AD9515 clock distribution IC provides positive emitter-coupled logic (PECL) logic levels to the ADC. However, the AD9515 internal divider feature also allows the DDS to run at a higher frequency into the AD9515 front-end, effectively increasing input slew rate. A higher slew rate into the AD9515 input squaring circuit can help reduce broadband jitter in the clock path.

Jitter on the ADC sampling clock produces degradation in the overall signal-to-noise ratio (SNR).

The relationship is given by the following equation:

$$SNR = 20 \log_{10}\left(\frac{1}{2\pi f t_j}\right) \quad (1)$$

where:
SNR is the signal-to-noise ratio due solely to clock jitter and does not depend on the resolution of the ADC.
f is the full-scale analog input frequency.
t_j is the rms jitter.

The data in this application note supports low jitter that can be attained from a DDS in clocking applications. See the Application Note AN-501 for details on Equation 1 and its use for evaluating the jitter on ADC sampling clocks.

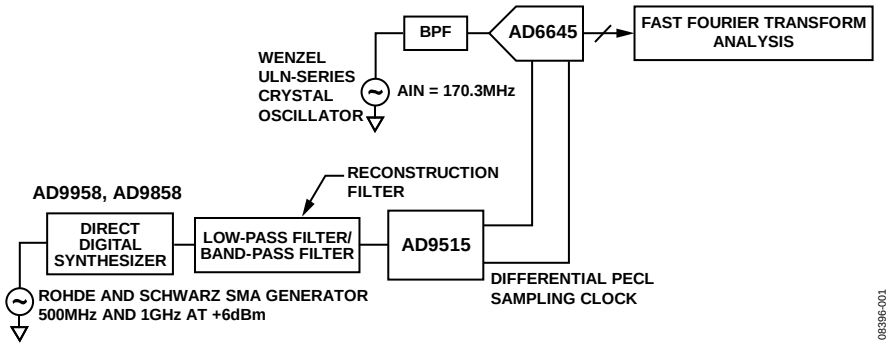

Figure 1. DDS-Based ADC Sampling Clock Generator (Simplified Diagram)

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REVISION HISTORY

8/2018—Rev. 0 to Rev. A

Document Title Changed from CN0109 to AN-1576 ..... Universal
Changes to Circuit Function and Benefits Section and Figure 1 1
Changes to Table 1 3
Changes to Table 2 4
Deleted Data Sheets and Evaluation Boards Section 4

7/2009—Revision 0: Initial Version

CIRCUIT DESCRIPTION

The circuit configuration in Figure 1 shows a DDS-based clock generator, which consists of DDS followed by a reconstruction filter and an AD9515 clock distribution IC that are used to provide the sampling clock for an ADC. The DDS sampling clock is derived from a Rohde and Schwarz SMA signal generator. The jitter measurement was made by using the clock derived from the DDS and the AD9515 as the sampling clock for the high performance AD6645 14-bit, 80 MSPS/105 MSPS ADC. The analog input signal for the ADC is a filtered 170.3 MHz sine wave derived from a low jitter Wenzel crystal oscillator. Data was taken on the AD9958 (500 MSPS) and the AD9858 (1 GSPS).

By evaluating the contribution of the differential non-linearity (DNL) and thermal noise of the ADC and then applying the DDS-based clock and measuring the ADC SNR, the added jitter that can be attributed to the DDS-based clock can be derived. For details on the measurement setup and the jitter calculations, refer to the Application Note AN-823. Additionally, the Application Note AN-837 is instructive for designing DAC reconstruction filters with optimal stop band performance.

Table 1 shows data for the AD9958 test results. The data confirms that better jitter performance is achieved as the frequency, or slew rate, of the DDS output frequency (f_{OUT}) is increased and the DDS output filter pass band is decreased. Table 2 shows the AD9858 with a 5% band-pass filter, a 225 MHz low-pass filter, and various levels of DDS output power. As expected, lower jitter is achieved as power is increased and the bandwidth is reduced. When using a 5% band-pass filter, the majority of the spurs from the DAC are attenuated. The jitter in this case is much more dependent on noise coupling between the digital-to-analog converter (DAC) output and the limiter input. This dependency is proven by the strong correlation between jitter reduction and increased slew rate. Note that rms jitter values that are consistently <1 ps can be achieved using the AD9858 circuit.

These circuits must be constructed on multilayer printed circuit boards (PCBs) with large area ground planes using proper grounding, layout, and decoupling techniques (see MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"* and MT-101 Tutorial, *Decoupling Techniques*) to achieve these performance levels. Consult the evaluation board documentation for the EVAL-AD9958, EVAL-AD9858, EVAL-AD9515, and the EVAL-AD6645 for more guidance.

Table 1. Jitter Response of the AD9958 and the AD9515 vs. f_{OUT}, Power, Frequency, and Filter Bandwidth

DDS Sample Rate (MHz)	DDS Output Frequency (MHz)	DDS Output Power (dBm)	DDS Reconstruction Filter	AD9515 Divider Output Setting	AD9515 f_{OUT} (MHz)	Jitter rms (ps)
500	38.88	−3.6	200 MHz, low-pass	1	38.88	4.1
500	38.88	−3.6	200 MHz, low-pass	2	19.44	4.1
500	38.88	−4.7	47 MHz, low-pass	1	38.88	2.4
500	38.88	−4.7	47 MHz, low-pass	2	19.44	2.4
500	38.88	−3.3	5%, band-pass	1	38.88	1.5
500	38.88	−3.3	5%, band-pass	2	19.44	1.5
500	77.76	−3.8	200 MHz, low-pass	1	77.76	2.5
500	77.76	−3.8	200 MHz, low-pass	2, 4	38.88, 19.44	2.5
500	77.76	−4.9	85 MHz, low-pass	1	77.76	1.5
500	77.76	−4.9	85 MHz, low-pass	2, 4	38.88, 19.44	1.5
500	77.76	−3.8	5%, band-pass	1	77.76	1.1
500	77.76	−3.8	5%, band-pass	2, 4	38.88, 19.44	1.1
500	155.52	−5.5	200 MHz, low-pass	2	77.76	1.5
500	155.52	−5.5	200 MHz, low-pass	4, 8	38.88, 19.44	1.5
500	155.52	−5.6	5%, band-pass	2	77.76	0.68
500	155.52	−5.6	5%, band-pass	4, 8	38.88, 19.44	0.68

Table 2. Jitter Response of the AD9858 and the AD9515 vs. f_{OUT}, Power, Frequency, and Filter Bandwidth

DDS Sample Rate (MHz)	DDS Output Frequency (MHz)	DDS Output Power (dBm)	DDS Reconstruction Filter	AD9515 Divider Output Setting	AD9515 f_{OUT} (MHz)	Jitter rms (ps)
1000	155.52	7.7	225 MHz, low-pass	2	77.76	0.56
1000	155.52	7.7	225 MHz, low-pass	4,8	38.88, 19.44	0.56
1000	155.52	7.7	5%, band-pass	2	77.76	0.33
1000	155.52	7.7	5% band-pass	4, 8	38.88, 19.44	0.33
1000	155.52	2.6	225 MHz, low-pass	2	77.76	0.63
1000	155.52	2.6	225 MHz, low-pass	4, 8	38.88, 19.44	0.63
1000	155.52	1.1	5%, band-pass	2	77.76	0.42
1000	155.52	1.1	5%, band-pass	4, 8	38.88, 19.44	0.42
1000	155.52	−3.2	225 MHz, low-pass	2	77.76	0.73
1000	155.52	−3.2	225 MHz, low-pass	4, 8	38.88, 19.44	0.73
1000	155.52	−4.6	5%, band-pass	2	77.76	0.64
1000	155.52	−4.6	5%, band-pass	4, 8	38.88, 19.44	0.64

COMMON VARIATIONS

Analog Devices, Inc., offers a variety of direct digital synthesizers, clock distribution chips, and clock buffers to build a DDS-based clock generator. Refer to the Direct Digital Synthesis page and the Clock & Timing page on the Analog Devices website for more information.

REFERENCES

AN-501 Application Note. *Aperture Uncertainty and ADC System Performance*. Analog Devices.

AN-823 Application Note. *Direct Digital Synthesizers in Clocking Applications Time Jitter in Direct Digital Synthesizer-Based Clocking Systems*. Analog Devices.

AN-837 Application Note. *DDS-Based Clock Jitter Performance vs. DAC Reconstruction Filter Performance*. Analog Devices.

Kester, Walt. 2005. *The Data Conversion Handbook*. Chapter 6 and Chapter 7. Analog Devices.

Kester, Walt. 2006. "Optimizing Data Converter Interfaces". *High Speed System Applications*. Chapter 2. Analog Devices.

Kester, Walt. 2006. "DACs, DDSs, PLLs, and Clock Distribution". *High Speed System Applications*. Chapter 3. Analog Devices.

MT-031 Tutorial. *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*. Analog Devices.

MT-101 Tutorial. *Decoupling Techniques*. Analog Devices.

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