ANALOG DEVICES

AN-784
APPLICATION NOTE

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10-Bit Interface Board for High Performance Display Interface Evaluation Boards

by Del Jones

INTRODUCTION

The purpose of the 10-bit display interface board (DIB) is to aid in the evaluation of the AD9981 or AD9980. It is designed to be used in conjunction with the evaluation boards for these parts, and is included as part of the evaluation board kits. It is a conduit for displaying images on any flat panel monitor, CRT, LCD (or DLP) projector, or TFT panel (with LVDS interface).

LIMITATIONS

The evaluation system using the 10-bit DIB is intended to provide the user a platform with which to evaluate the functionality and, to a limited extent, performance of the AD9981 or AD9980. When evaluating the 8-bit AD9980, the DVI or LVDS outputs of the 10-bit DIB offer the highest quality image for performance evaluation. However, since both of these ports only offer 8-bit accuracy, they cannot truly reflect the enhanced performance provided by the 10-bit ADCs of the AD9981. The analog output of the 10-bit DIB uses high accuracy 12-bit DACs and can potentially offer a preferred interface for evaluation, depending on the display device that is used.

PACKAGE CONTENTS

- An evaluation board for the AD9981 or AD9980
- A 5 V dc power supply
- A Centronix printer cable or USB A to B cable for serial bus programming

REQUIREMENTS

In addition to the items included with the kit, the following items are needed to run this board:

- A computer with the evaluation software installed
- A 5 V dc power supply
- Any flat panel monitor, CRT, or projector 10-bit display interface board

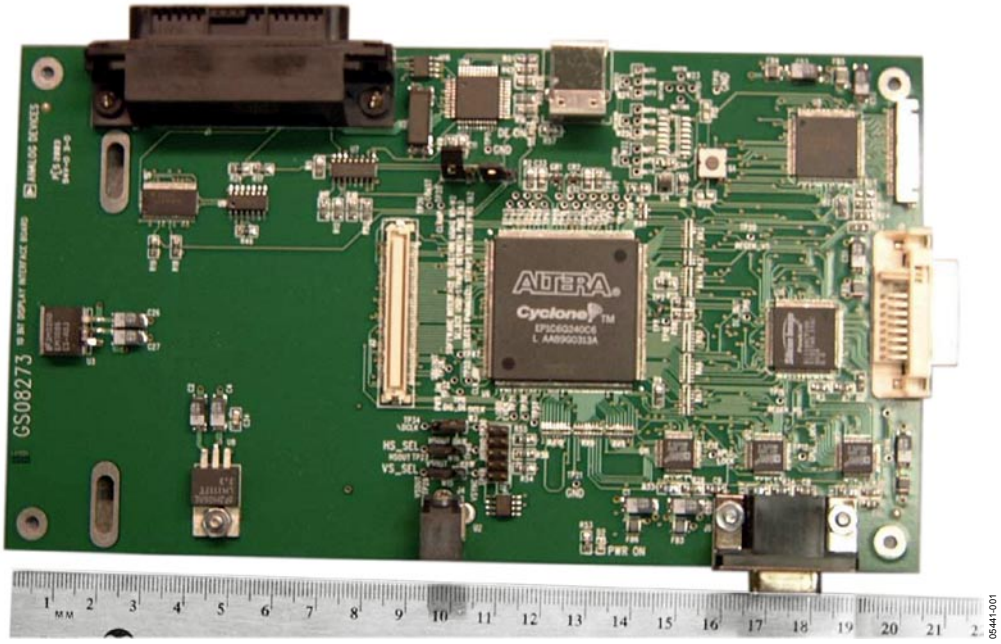

Figure 1. Board Shown in Centimeters

EVALUATION BOARD HARDWARE

POWER

This board is designed to receive 5 V dc through connector J4. The power supply that is included in the kit plugs into this connector.

BOARD FUNCTIONS

A block diagram of the 10-bit display interface board is shown in Figure 2. The following sections briefly describe these functional blocks.

DATA DEMULTIPLEXING

The Altera EP1C6QC240 FPGA (U6) performs most of the logic functions on the 10-bit display interface board. Among these functions is the demultiplexing of the digital RGB data output from the AD998x when it is in single-port data output (30-bit) mode (the AD9981 and AD9980 are 30-bit only). The DVI and LVDS transmitters, as well as the digital-to-analog converters (DACs), require dual-port digital RGB data. Therefore, demultiplexing is required when in single-port mode.

DE GENERATION

The DVI and LVDS interfaces require a data enable (DE) signal which indicates when there is active image data. Since the analog graphics signal does not contain DE, the FPGA on the 10-bit display interface board is required to generate it. The duration of DE is programmable via the 10-bit DIB register map of the display electronics (DEPL) evaluation software and supports any display resolution up to 4096 pixels × 4096 pixels.

COLOR SPACE CONVERSION

The FPGA contains circuitry to perform color space conversion for 30-bit YPbPr data. This can be enabled via the 10-bit DIB register map of the DEPL evaluation software. This can be used in conjunction with the midscale clamp feature on the analog interface of the AD998x devices to provide the proper colors for an YPbPr video signal. The color space conversion also works with YPbPr signals transmitted over the DVI interface. For the most accurate color space conversion, the conversion results in a 12-bit output for each of the digital RGB output channels. This minimizes the rounding errors that can result from the conversion process.

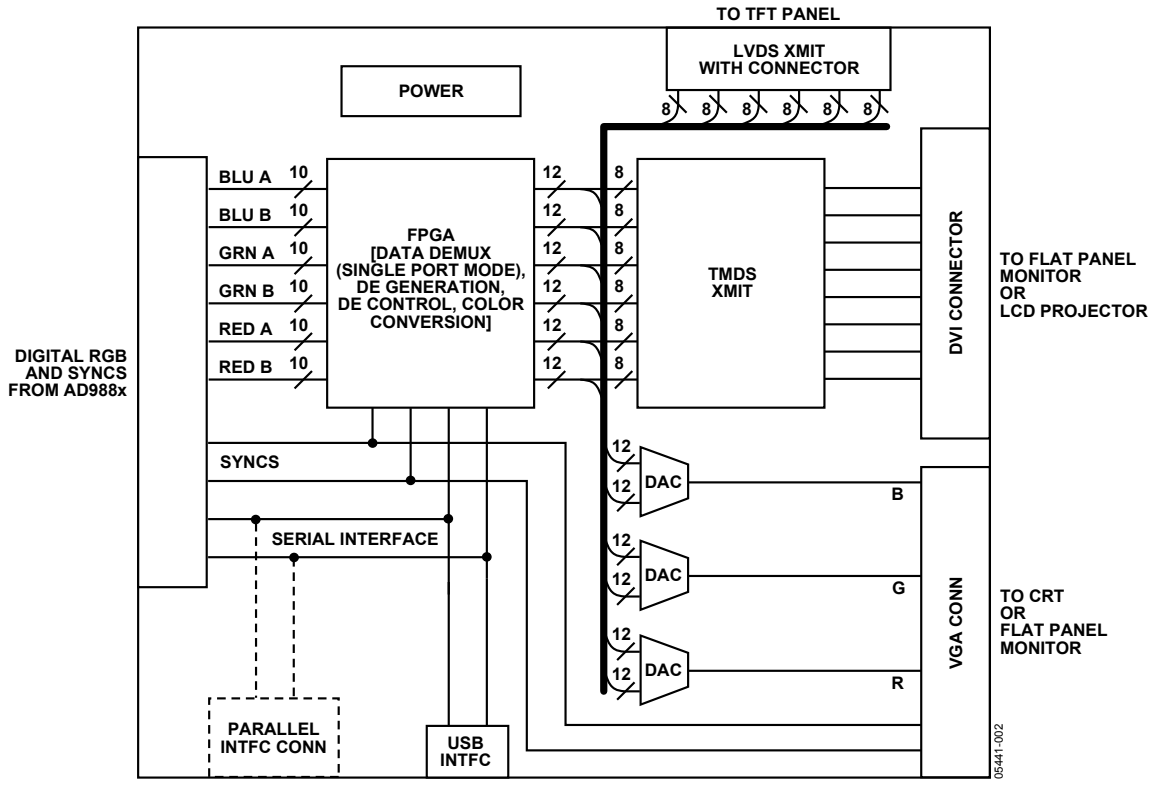

Figure 2. 10-Bit Display Interface Board Block Diagram

DVI OUTPUT

The 10-bit display interface board provides a DVI output via Sil160 transmitter (U15) and DVI-I connector (J8). This can be connected via DVI cable to any display device (flat panel monitor or LCD projector) to display any image from VGA to UXGA-60 (the Sil160 is limited to 25 MHz to 165 MHz operation). Note that the Sil160 is capable of processing only 8-bit data. Therefore, only the 8 MSBs of the data output from the FPGA are used for the DVI output.

LVDS OUTPUT

The 10-bit display interface board provides an LVDS output via DS90C387 transmitter (U5) and LVDS data connector (J9). This can be connected via user-provided cable to any board flat panel with LVDS interface (such as Samsung's 21.3'' UXGA panel, LTM213U3-L01-0, or Sharp's 18'' SXGA panel, LQ181E1LW31) to display an image using that panel's native resolution. This interface is capable of operating up to UXGA-75 (202.5 MHz). Note that the DS90C387 is capable of processing only 8-bit data. Therefore, only the 8 MSBs of the data output from the FPGA are used for the DVI output.

ANALOG OUTPUT

The 10-bit display interface board provides an analog output via high performance AD9753 DACs (U11 to U13) and 15-pin VGA connector (J6). The AD9753 is a 12-bit DAC that provides precision digital-to-analog conversion. Therefore, the analog output port is the best choice to demonstrate the full 10-bit performance of the AD998x devices. The analog output can be connected via VGA cable to any display device (flat panel monitor, CRT, or projector) to display any image from VGA to UXGA-75.

SERIAL BUS TO COMPUTER INTERFACE (USB OR PRINTER PORT)

Some circuitry is needed in order to interface the AD998x and the 10-bit display interface board's serial register interface with a computer. The 10-bit display interface board provides both a USB and a parallel (printer) port interface. The USB interface consists of a USB-B connector (J2), USB controller (U14), and an EEPROM (U16) that contains board ID information. The circuitry for the printer port's serial interface use U1 and U9, in addition to the Centronix connector, J1.

POWER

The 10-bit display interface board has two voltage regulators that generate 1.5 V and 3.3 V for its own logic. These voltages are regulated off of the 5 V input at J4. The 5 V input is also routed to the AD998x evaluation board interface connector (J3) to provide power for the AD998x evaluation board.

EVALUATION BOARD CONNECTIONS

Figure 3 shows how the 10-bit display interface board interfaces with the AD9981 evaluation board. It also indicates the various connections needed to evaluate an image.

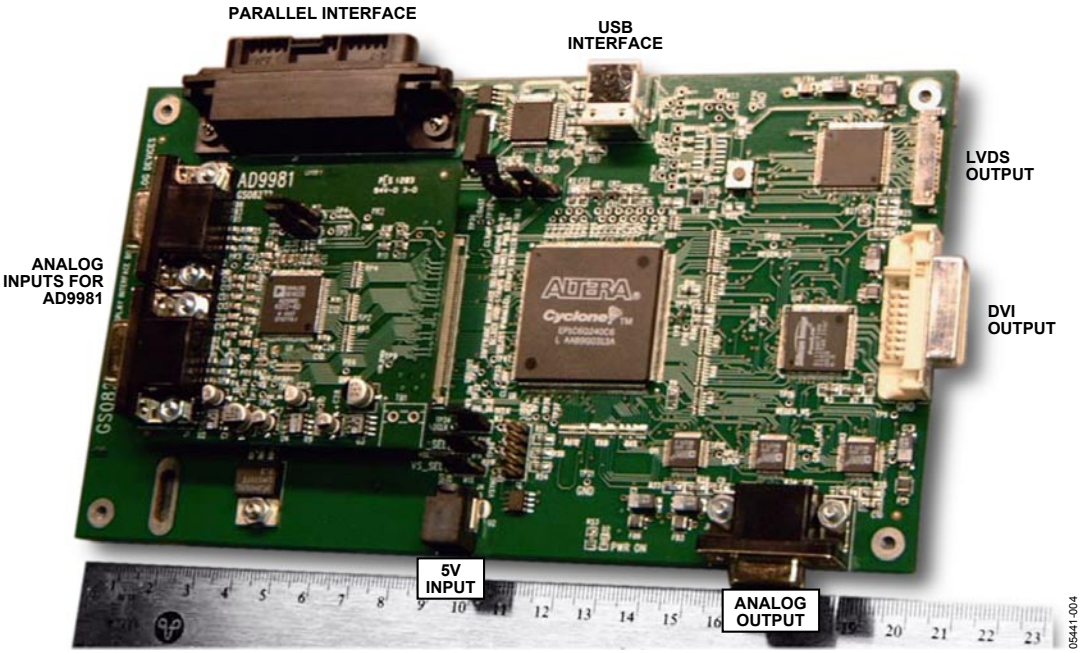

Figure 3. 10-Bit Display Interface Board with AD9981 Evaluation Board

CONFIGURING THE BOARD

DE Generation

The VS_SEL (W15 on schematic) and HS_SEL (W16 on schematic) jumpers allow you to choose raw VSYNC and HSYNC or the VSOUT and HSOUT outputs of the AD998x to generate DE. If the jumpers are placed between Pins 1 and 2 (closer to U2), the raw HSYNC and VSYNC are selected. If the jumpers are placed between Pins 2 and 3, the sync outputs (HSOUT and VSOUT) of the AD998x are selected. Either configuration works, although the HSYNC and VSYNC delay values used for DE generation vary slightly in each case.

PC Port Selection

The jumpers at W1 and W2 must be configured appropriately to use the desired PC port for software control. To select USB, the jumpers must be placed between Pins 2 and 3. To select the printer port, the jumpers should be placed between Pin 1 and Pin 2.

To USB Driver Installation

Follow these steps to install the USB drivers on your PC:

1. Connect the board to the power supply.
2. Connect the USB cable from the PC to the board.
3. Windows sees the new device and asks to install drivers for it.
4. Select Search for Drivers and click Next.
5. Specify a location and browse on the CD-ROM to the USB Drivers\win2k directory.
6. Click Next and follow any remaining instructions.
7. If asked for any files, always browse to the same USB Drivers\win2k (or \win98) folder to find them.

DCLK Selection

The 10-bit display interface board is configured so that the DCLK output of the AD998x drives the generation of PANEL_DCLK and PANEL_DE. This is accomplished through the placement of a jumper between Pins 1 and 2 of Header W3.

EVALUATION BOARD SOFTWARE

The 10-bit display interface board (DIB) registers can be controlled using the 10-bit DIB register map of the DEPL evaluation software. This software is a Visual Basic® program requiring a Windows® 95, or later, operating system. It is on a self-installing CD package included with the evaluation board (in the \DEPL Evaluation Software subdirectory). The 10-bit DIB register map of the DEPL evaluation software should be loaded into the \Program Files\ADI Software directory upon completion of a successful installation.

Note: If a DriverX Install error is encountered during the software installation, rerun the driverxinstall.exe program located in the Program Files\Analog Devices\ DEPL Evaluation Software\DriverX directory.

The 10-bit DIB register map can be accessed two ways. From the menu bar, select **Device > 10Bit DIB**. The 10-bit DIB register map can also be accessed by selection **Tools > 10-Bit Display Interface Board Configuration**. The 10-bit DIB register map is shown in Figure 4. Using this screen, the user can control the features of the 10-bit DIB.

To implement the controls, click **Load**. This is true unless the **Load Register on Change** box is checked or the **Read** button is clicked. In this case, the registers are updated as soon as any change is made in the window.

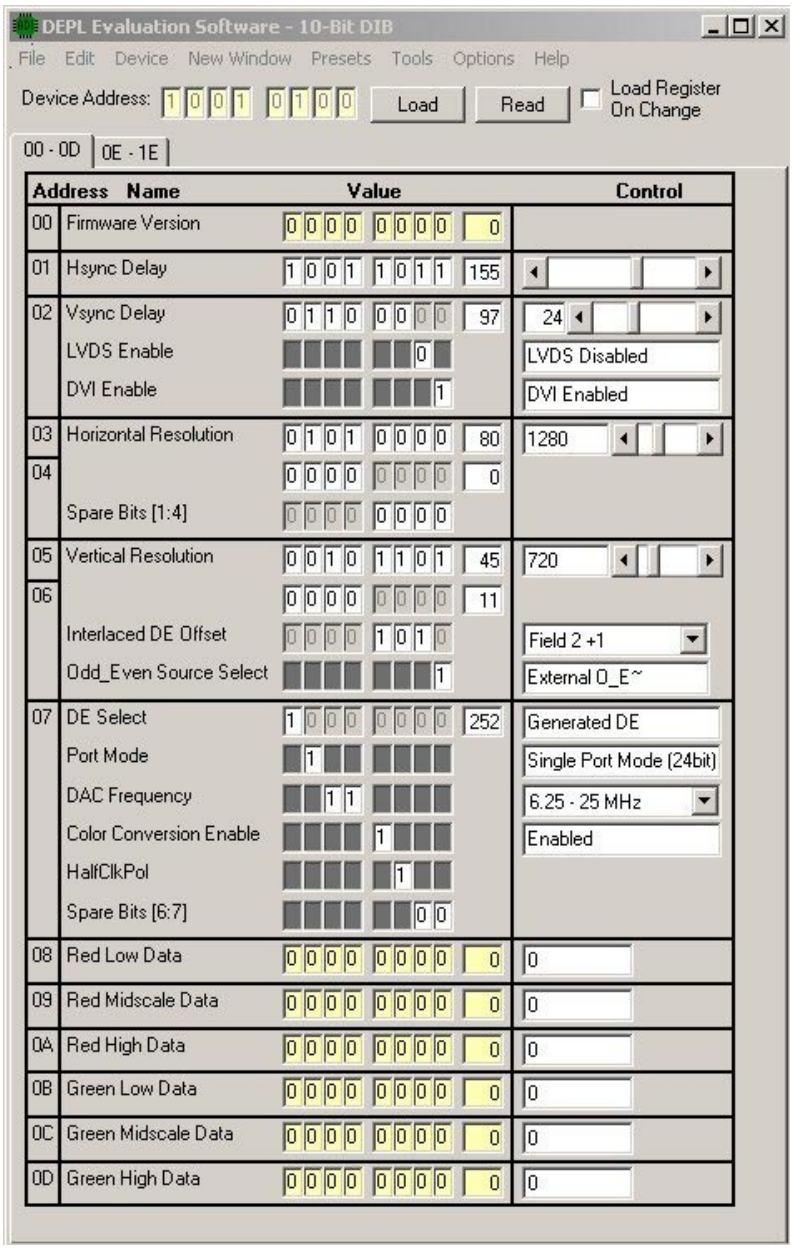

Figure 4. Display Interface Board Configuration Setup Window

10-BIT DIB REGISTER DESCRIPTIONS

Hsync Delay (01–7:0)

Register 01 controls the number of data clock cycles that occur between Hsync and the beginning of DE. This is a decimal number that is written to an 8-bit register. For ease of use, a sliding bar is also included as an alternative method for controlling the Hsync delay. Moving the bar to the right increases the delay and is reflected in the box to the right. Moving the bar left decreases the delay.

If using the DVI output of the 10-bit display interface board, note that an image might not be visible until the Hsync Delay is near the appropriate amount of delay from Hsync to active video.

Vsync Delay (02–7:2)

Bits 7:2 of Register 02 control the number of Hsync periods that occur between Vsync and the beginning of DE. This is a decimal number that is written to a 6-bit register. A sliding bar is also included for Vsync delay control.

LVDS/DVI Interface Enable (02–1:0)

Bits 1:0 of Register 02 serve as enable bits to turn on the LVDS and DVI interface outputs of the 10-bit DIB. It is recommended that these interfaces be powered down when not in use.

Horizontal Resolution (03–7:04–4)

Horizontal resolution must be set using the 12 bits spanning Register 3, Bit 7 (MSB) to Register 4, Bit 4 (LSB). The resolution is set in number of pixels by typing the decimal number directly into the text box on the right or by moving the scroll bar next to it. The maximum value is 4096.

Vertical Resolution (05–7:06–4)

Vertical resolution must be set using the 12 bits spanning Register 5, Bit 7 (MSB) to Register 6, Bit 4 (LSB). The resolution is set in number of lines by typing the decimal number directly into the text box on the right or by moving the scroll bar next to it. The maximum value is 4096.

DE Settings for Interlaced Video (06–3:0)

When generating a data enable (DE) from an interlaced video source, it is necessary to provide for an offset between the odd and even fields. Bits 3:1 of Register 6 allow you to program the amount of offset (in number of lines) between the two fields. Bit 0 allows you to select how the even and odd fields are differentiated from each other. The AD998x devices have an ODD_EVEN~ signal that is routed to the 10-bit DIB's FPGA and can be used to determine the differentiation by setting this bit to a Logic 1. If using a device that does not provide this signal, the FPGA generates its own signal to provide this function. This signal can be selected by setting Bit 0 to Logic 0.

DE Select (07–7)

This bit allows you to select the source for data enable generation. If the analog interface of the AD998x is being used, Generated DE must be selected since the analog interface does not include a DE signal. If the DVI interface of the AD998x is being used, either Generated DE of Digital DE can be used. However, it is recommended that the Digital DE be selected in this case.

Port Mode (07–6)

This bit allows the user to select the operating mode of the AD998x. If the AD998x is operating in single-channel (30-bit) output mode (the AD9981 and the AD9980 have single-channel output only), single port mode must be selected. If the AD998x is operating in dual-channel (60-bit) output mode, Dual Port (60 bit) must be selected.

DAC Frequency (07–5:4)

From the DAC Frequency Range menu, you can select the operating range of the analog output. The 12 MHz to 100 MHz range should be adequate to display all resolutions XGA and above (including 720p and 1080p). For lower speed resolutions, the appropriate range should be selected.

Color Conversion Enable (07–3)

The color conversion enable bit allows you to turn on the 30-bit color space converter in the FPGA.

Half Clock Invert (07–2)

The bit allows the user to route the first pixel of demultiplexed 30-bit data to the even output port of the FPGA rather than the odd output port. The timing relation between data and the data clock (PANEL_CLK_OUT) remain the same. This bit is useful when centering the image using the Hsync delay register.

PC Port Selection

To select between the USB and parallel ports for the software interface click on the Options pull-down menu and click on Device Interface and then select either USB or Parallel. Refer to the PC Port Selection section for further setup instructions.

SCHEMATICS AND LAYOUT

The schematics and layout for this board can also be found on the CD.

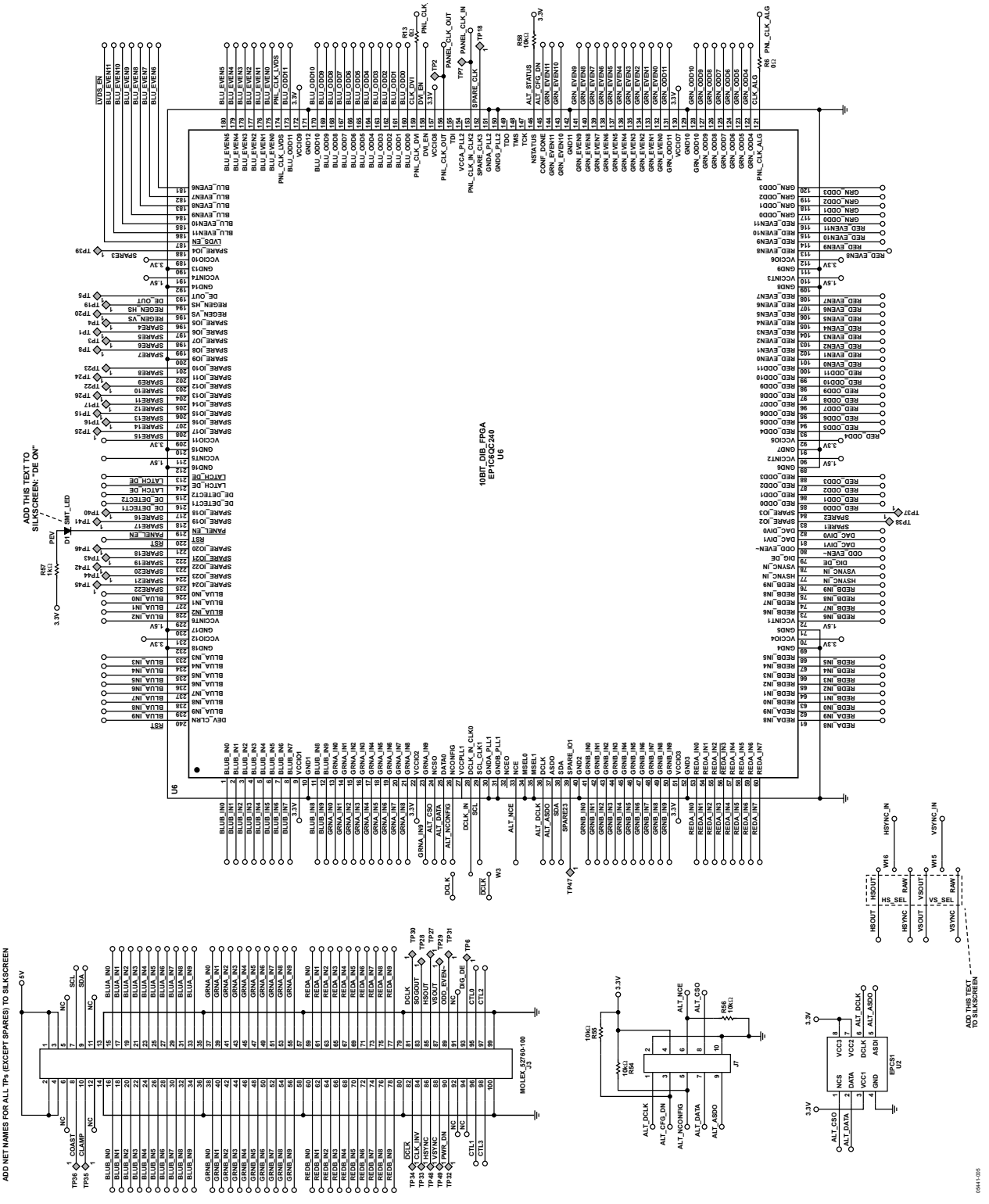

Figure 5.

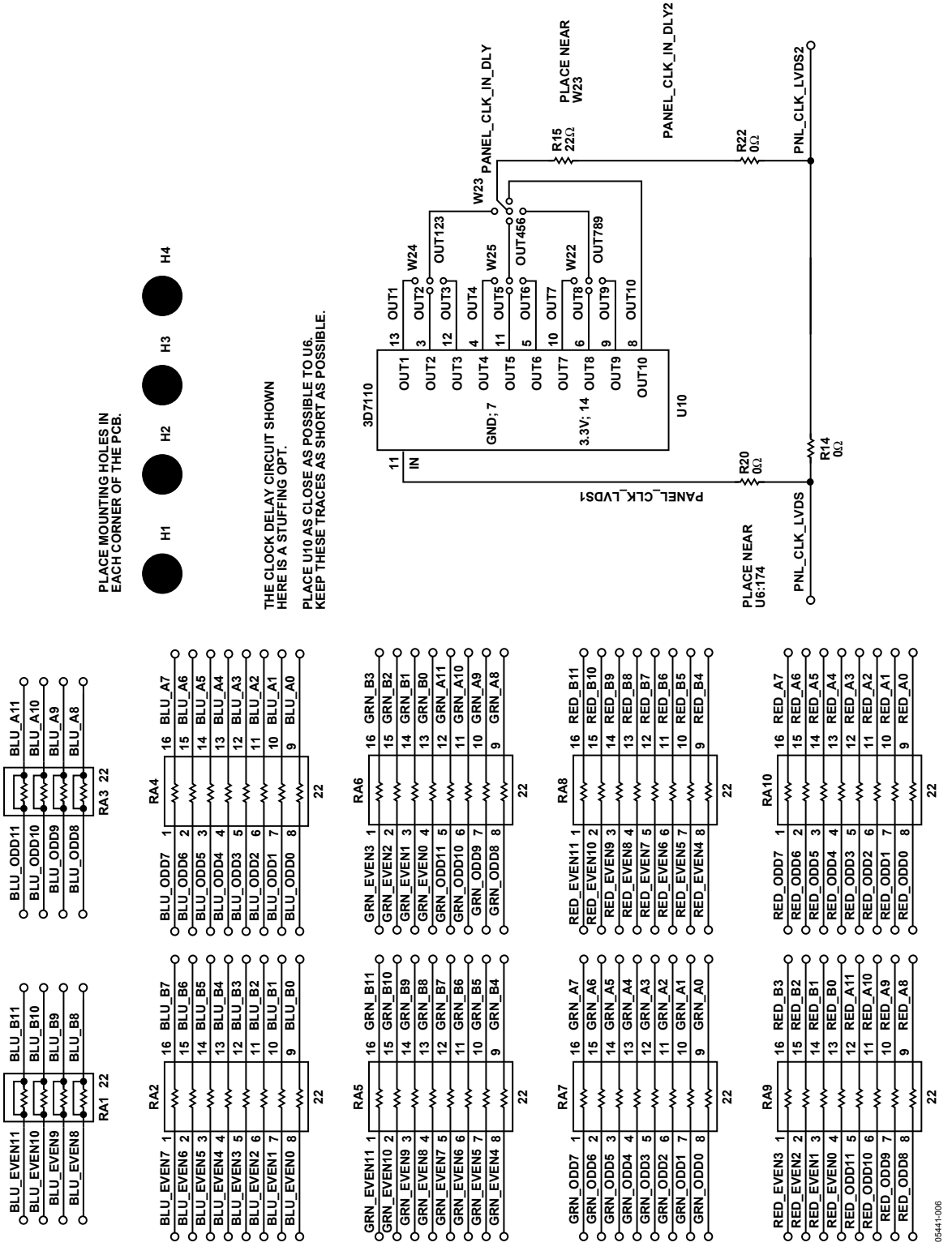
PLACE MOUNTING HOLES IN
EACH CORNER OF THE PCB.
H1
H2
H3
H4
THE CLOCK DELAY CIRCUIT SHOWN
HERE IS A STUFFING OPT.
PLACE U10 AS CLOSE AS POSSIBLE TO U6.
KEEP THESE TRACES AS SHORT AS POSSIBLE.
3D7110
U10
PANEL_CLK_IN_DLY
PLACE NEAR
W23
PANEL_CLK_IN_DLY2
R15
22Ω
R22
0Ω
PNL_CLK_LVDS2
R20
0Ω
R14
0Ω
PANEL_CLK_LVDS1
PLACE NEAR
U6:174
PNL_CLK_LVDS
RA1
RA2
RA3
RA4
RA5
RA6
RA7
RA8
RA9
RA10
05441-006

Figure 6.

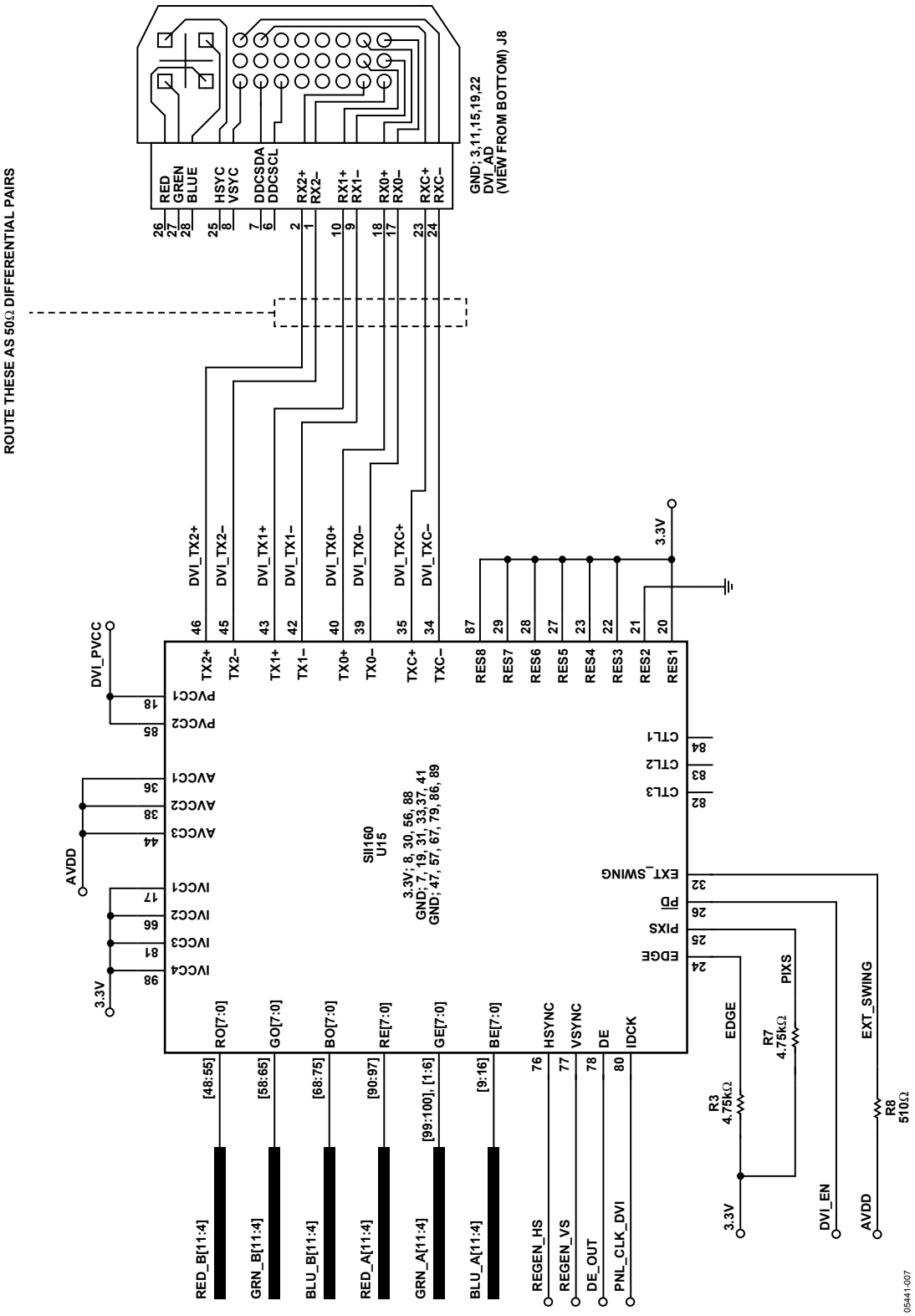
ROUTE THESE AS 50Ω DIFFERENTIAL PAIRS
GND; 3,11,15,19,22
DVI_AD
(VIEW FROM BOTTOM) J8
RED
GREN
BLUE
HSYC
VSYC
DDCSDA
DDCSCL
RX2+
RX2–
RX1+
RX1–
RX0+
RX0–
RXC+
RXC–
SII160
U15
3.3V; 8, 30, 56, 88
GND; 7, 19, 31, 33, 37, 41
GND; 47, 57, 67, 79, 86, 89
DVI_PVCC
AVDD
3.3V
DVI_TX2+
DVI_TX2–
DVI_TX1+
DVI_TX1–
DVI_TX0+
DVI_TX0–
DVI_TXC+
DVI_TXC–
EXT_SWING
PD
PIXS
EDGE
R3
4.75kΩ
R7
4.75kΩ
R8
510Ω
DVI_EN
RED_B[11:4]
GRN_B[11:4]
BLU_B[11:4]
RED_A[11:4]
GRN_A[11:4]
BLU_A[11:4]
REGEN_HS
REGEN_VS
DE_OUT
PNL_CLK_DVI
05441-007

Figure 7.

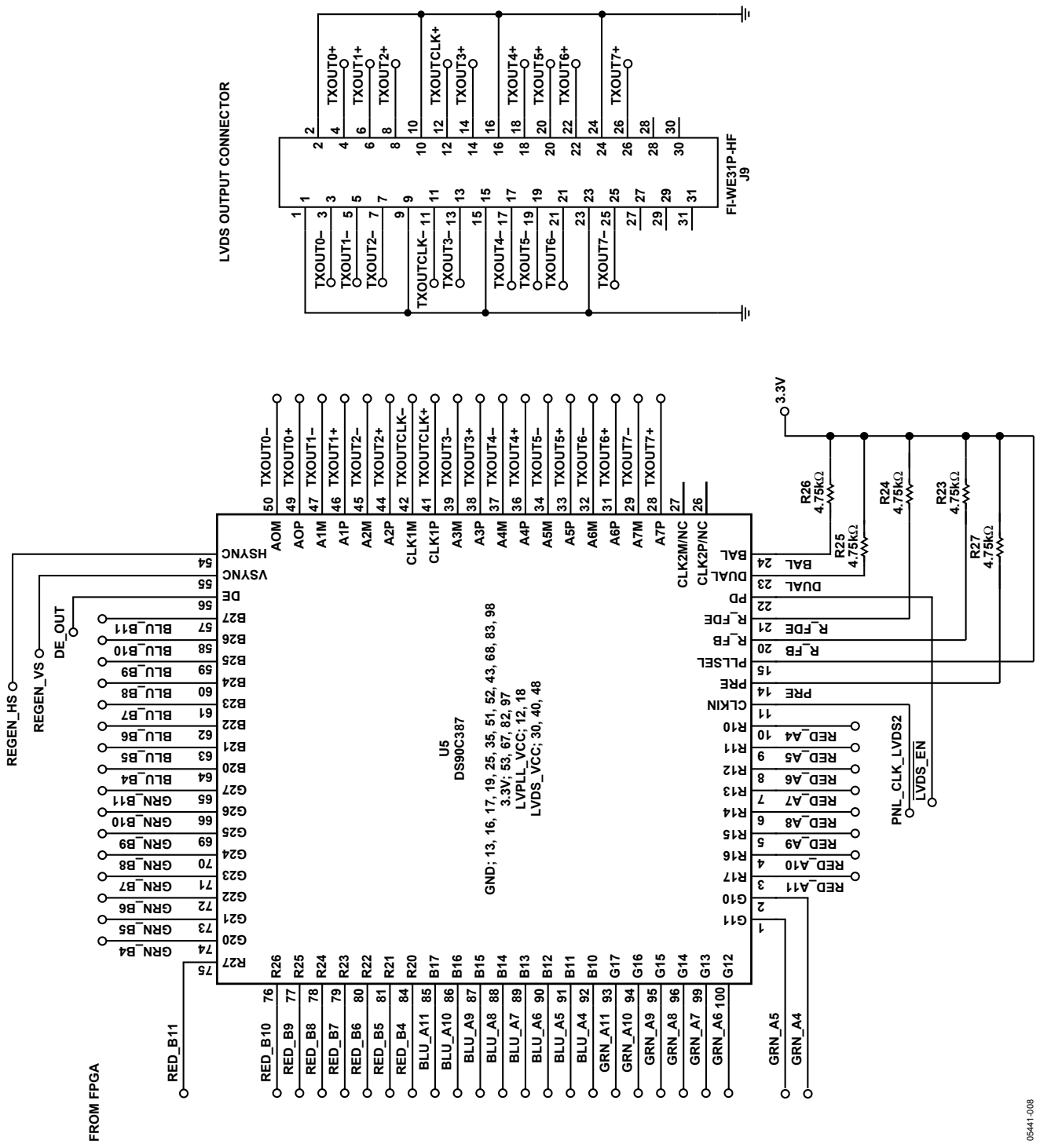
LVDS OUTPUT CONNECTOR
FI-WE31P-HF
J9
TXOUT0–
TXOUT1–
TXOUT2–
TXOUTCLK–
TXOUT3–
TXOUT4–
TXOUT5–
TXOUT6–
TXOUT7–
TXOUT0+
TXOUT1+
TXOUT2+
TXOUTCLK+
TXOUT3+
TXOUT4+
TXOUT5+
TXOUT6+
TXOUT7+
3.3V
R26 4.75kΩ
R25 4.75kΩ
R24 4.75kΩ
R23 4.75kΩ
R27 4.75kΩ
U5
DS90C387
GND; 13, 16, 17, 19, 25, 35, 51, 52, 43, 68, 83, 98
3.3V; 53, 67, 82, 97
LVPLL_VCC; 12, 18
LVDS_VCC; 30, 40, 48
REGEN_HS
REGEN_VS
DE_OUT
FROM FPGA
RED_B11
GRN_A5
GRN_A4
PNL_CLK_LVDS2
LVDS_EN
05441-008

Figure 8.

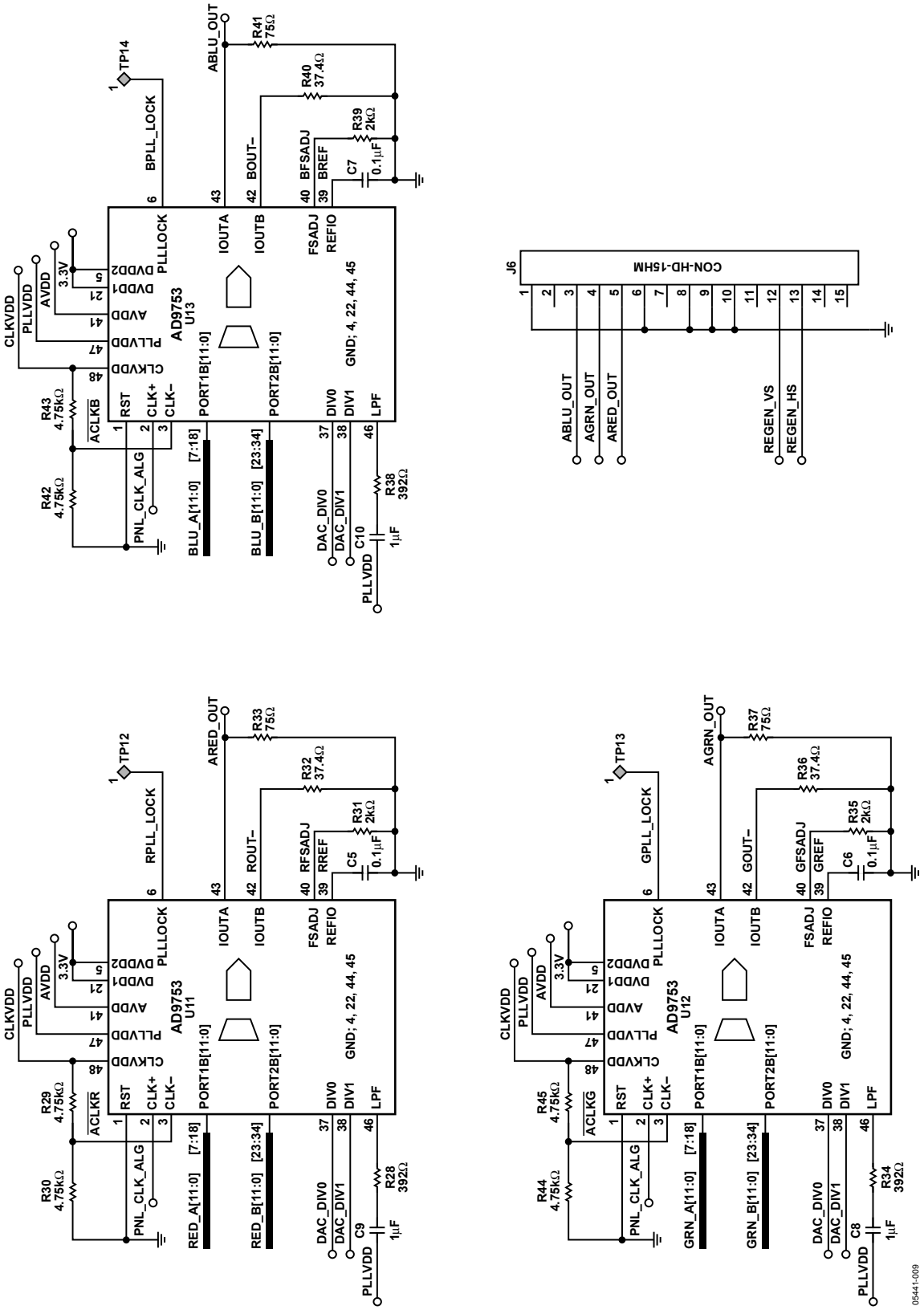
J6
CON-HD-15HM
ABLU_OUT
AGRN_OUT
ARED_OUT
REGEN_VS
REGEN_HS
TP14
BPLL_LOCK
ABLU_OUT
R41 75Ω
R40 37.4Ω
R39 2kΩ
C7 0.1µF
BOUT–
BFSADJ
BREF
IOUTA
IOUTB
FSADJ
REFIO
AD9753 U13
CLKVDD
PLLVDD
AVDD
3.3V
DVDD2
DVDD1
AVDD
PLLVDD
CLKVDD
RST
CLK+
CLK–
ACLKB
R43 4.75kΩ
R42 4.75kΩ
PNL_CLK_ALG
PORT1B[11:0] [7:18]
PORT2B[11:0] [23:34]
BLU_A[11:0]
BLU_B[11:0]
DAC_DIV0
DAC_DIV1
DIV0
DIV1
LPF
GND; 4, 22, 44, 45
C10 1µF
R38 392Ω
PLLVDD
TP12
RPLL_LOCK
ARED_OUT
R33 75Ω
R32 37.4Ω
R31 2kΩ
C5 0.1µF
ROUT–
RFSADJ
RREF
ACLKR
R29 4.75kΩ
R30 4.75kΩ
RED_A[11:0]
RED_B[11:0]
C9 1µF
R28 392Ω
TP13
GPLL_LOCK
AGRN_OUT
R37 75Ω
R36 37.4Ω
R35 2kΩ
C6 0.1µF
GOUT–
GFSADJ
GREF
ACLKG
R45 4.75kΩ
R44 4.75kΩ
GRN_A[11:0]
GRN_B[11:0]
C8 1µF
R34 392Ω
05441-009

Figure 9.

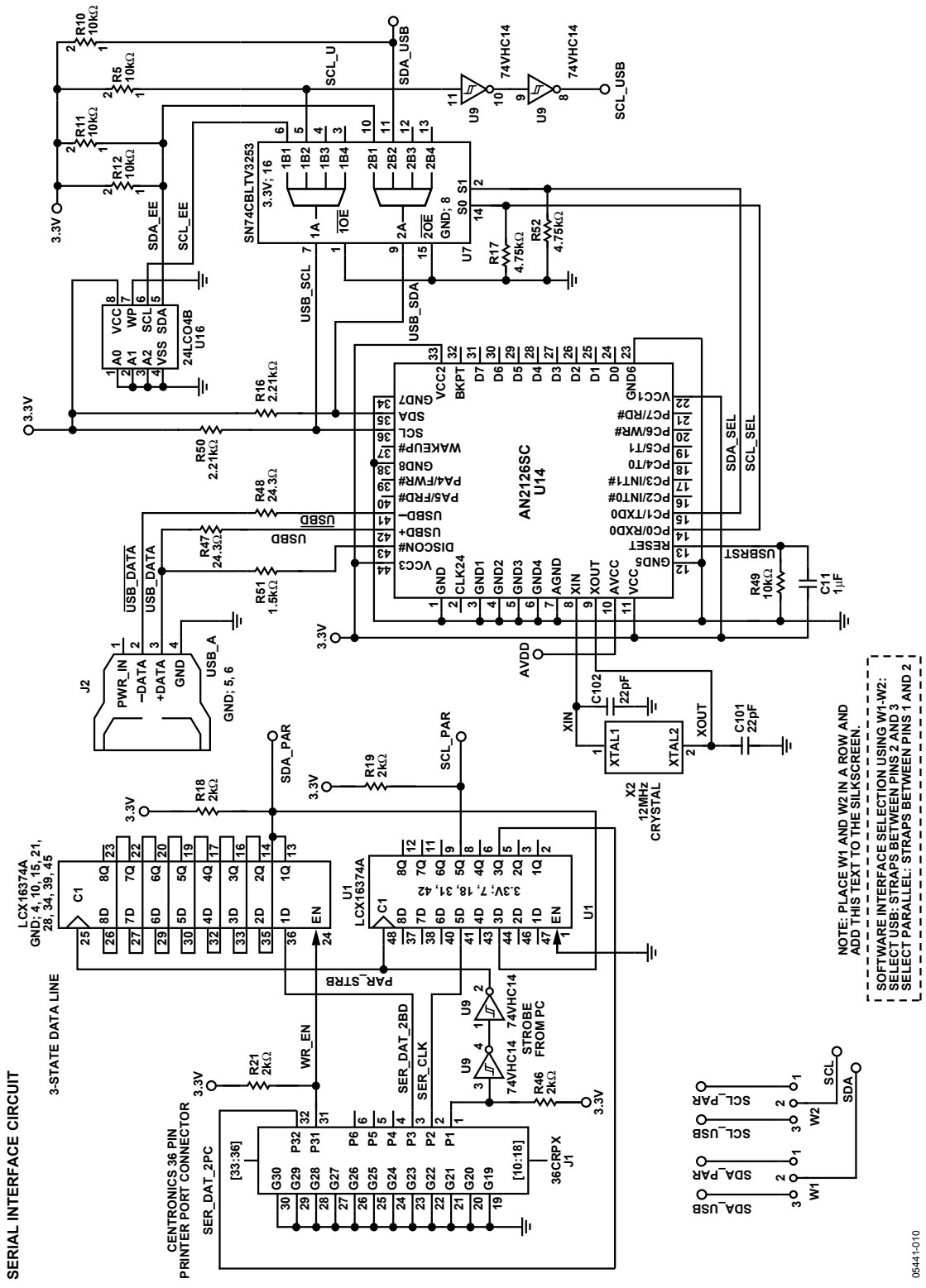
SERIAL INTERFACE CIRCUIT
3-STATE DATA LINE
CENTRONICS 36 PIN PRINTER PORT CONNECTOR
SER_DAT_2PC
36CRPX J1
LCX16374A GND; 4, 10, 15, 21, 28, 34, 39, 45
U1 LCX16374A
3.3V; 7, 18, 31, 42
SN74CBLTV3253 3.3V; 16
GND; 8
24LC04B U16
AN2126SC U14
74VHC14
STROBE FROM PC
PAR_STRB
WR_EN
SER_DAT_2BD
SER_CLK
SDA_PAR
SCL_PAR
SDA_USB
SCL_USB
SCL_U
SDA_EE
SCL_EE
USB_SCL
USB_SDA
USB_DATA
USBD
USBRST
SDA_SEL
SCL_SEL
PWR_IN
–DATA
+DATA
GND
USB_A
GND; 5, 6
XTAL1
XTAL2
X2 12MHz CRYSTAL
XIN
XOUT
AVDD
SOFTWARE INTERFACE SELECTION USING W1-W2:
SELECT USB: STRAPS BETWEEN PINS 2 AND 3
SELECT PARALLEL: STRAPS BETWEEN PINS 1 AND 2
NOTE: PLACE W1 AND W2 IN A ROW AND ADD THIS TEXT TO THE SILKSCREEN.
05441-010

Figure 10.

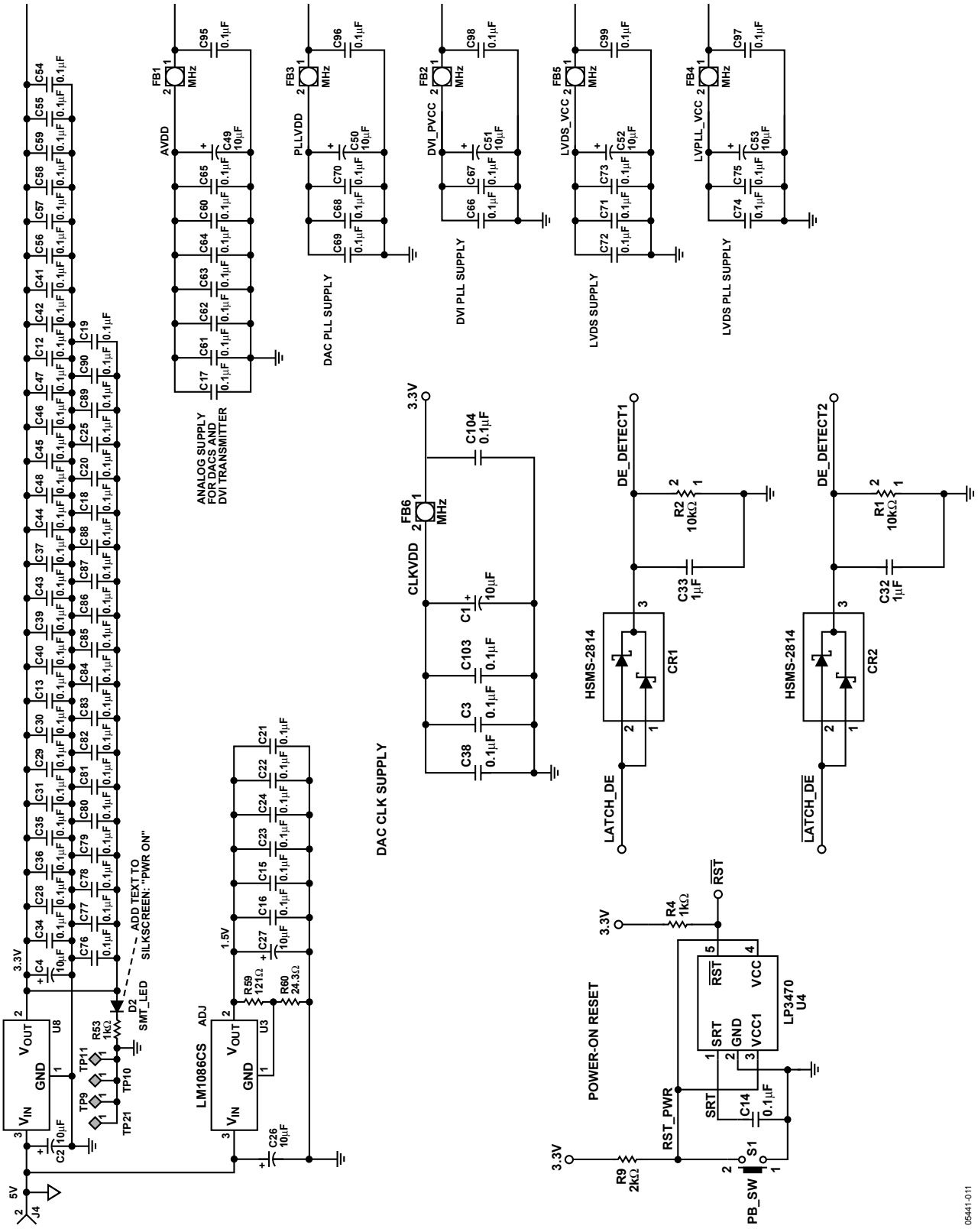
LM1085IT
LM1086CS
ADJ
ADD TEXT TO SILKSCREEN: "PWR ON"
SMT_LED
ANALOG SUPPLY FOR DACS AND DVI TRANSMITTER
DAC PLL SUPPLY
DVI PLL SUPPLY
LVDS SUPPLY
LVDS PLL SUPPLY
DAC CLK SUPPLY
POWER-ON RESET
HSMS-2814
LATCH_DE
DE_DETECT1
DE_DETECT2
LP3470
RST_PWR
PB_SW
AVDD
PLLVDD
DVI_PVCC
LVDS_VCC
LVPLL_VCC
CLKVDD
05441-0-11

Figure 11.

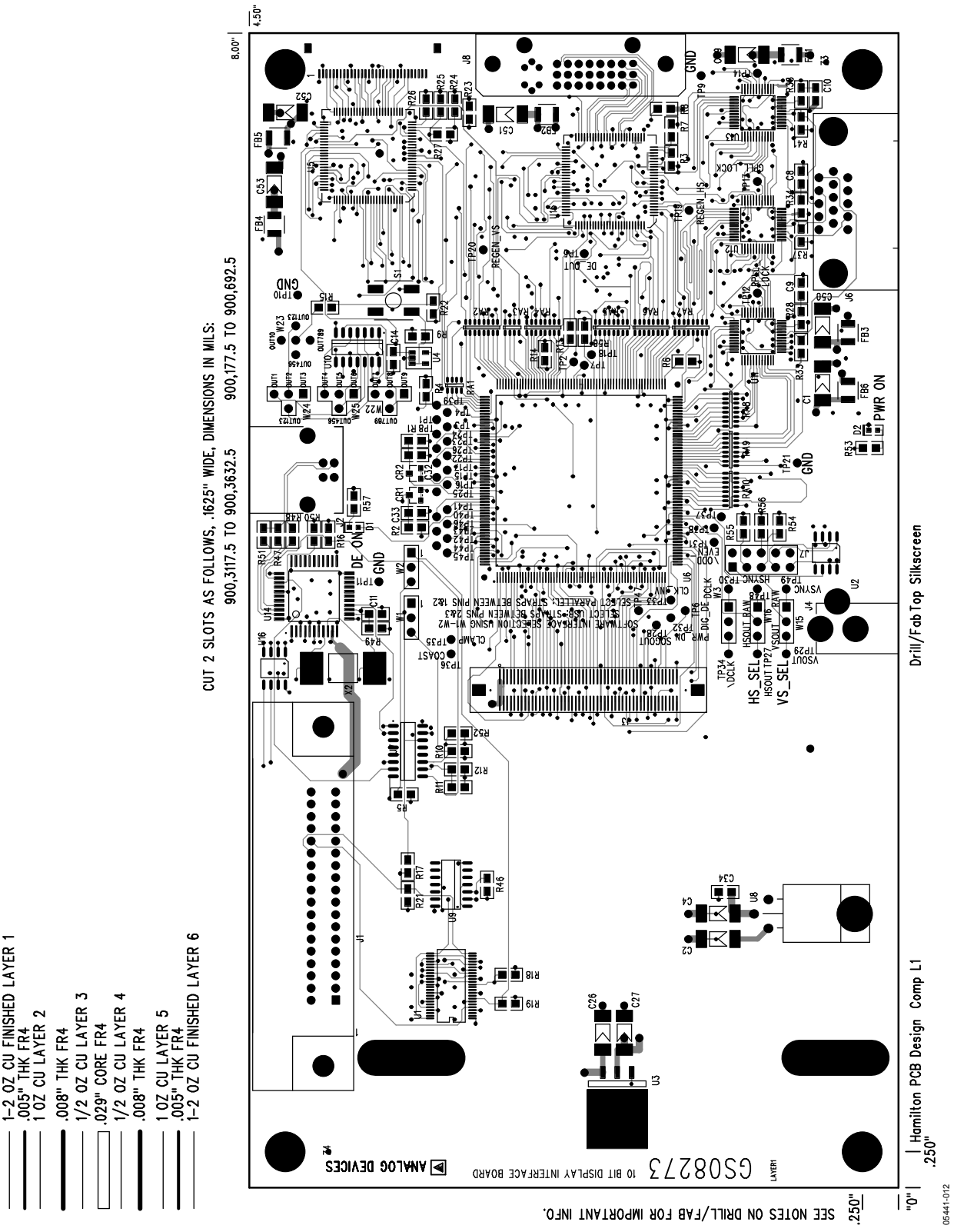
1–2 OZ CU FINISHED LAYER 1
.005" THK FR4
1 OZ CU LAYER 2
.008" THK FR4
1/2 OZ CU LAYER 3
.029" CORE FR4
1/2 OZ CU LAYER 4
.008" THK FR4
1 OZ CU LAYER 5
.005" THK FR4
1–2 OZ CU FINISHED LAYER 6
CUT 2 SLOTS AS FOLLOWS, .1625" WIDE, DIMENSIONS IN MILS:
900,3117.5 TO 900,3632.5
900,177.5 TO 900,692.5
8.00"
4.50"
GS08273
10 BIT DISPLAY INTERFACE BOARD
ANALOG DEVICES
SEE NOTES ON DRILL/FAB FOR IMPORTANT INFO.
Hamilton PCB Design Comp L1
Drill/Fab Top Silkscreen
.250"
"0"
05441-012

Figure 12.

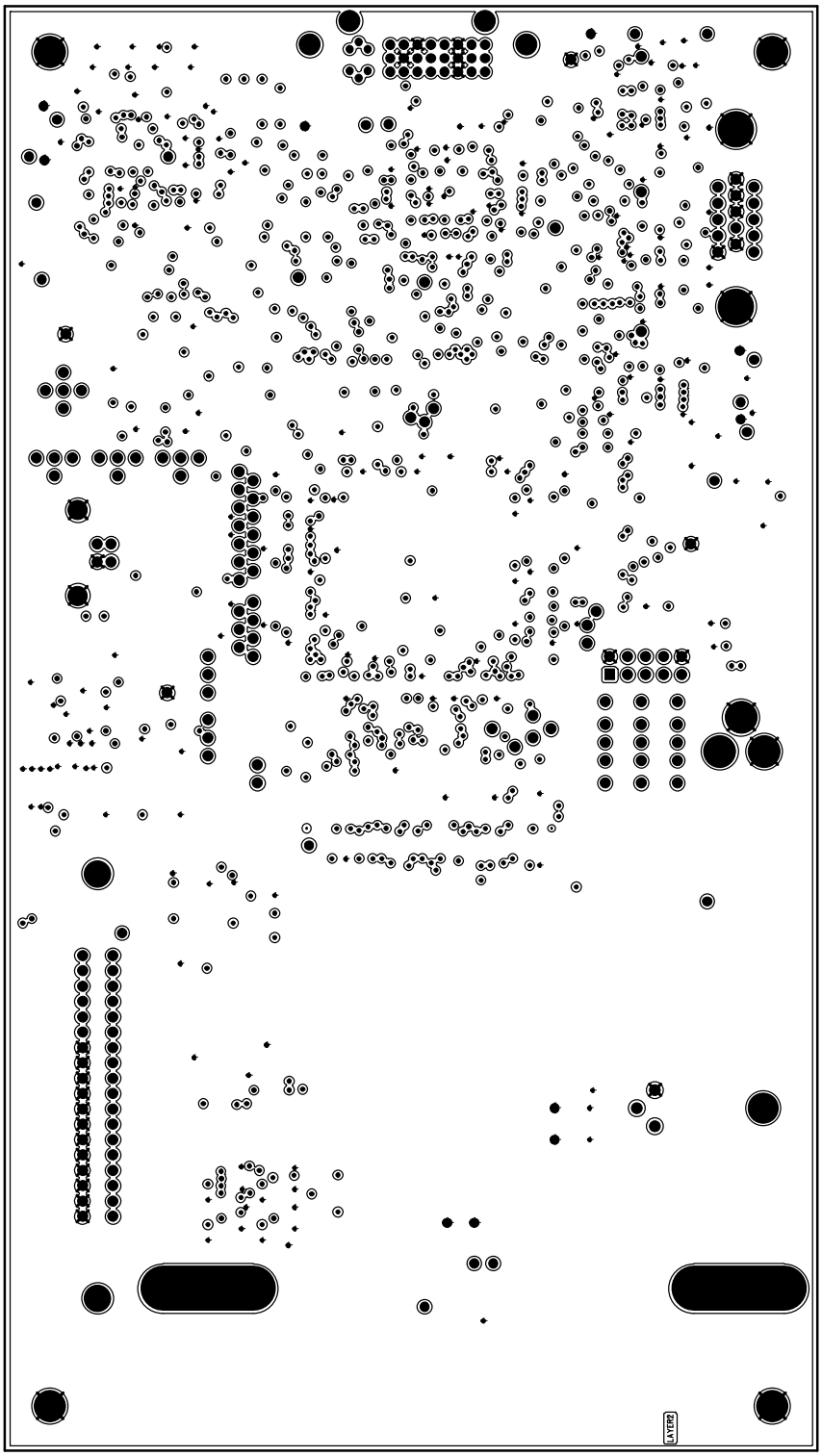
LAYER2
Hamilton PCB Design
Sig L2
SEE NOTES ON DRILL/FAB FOR IMPORTANT INFO.
05441-013

Figure 13.

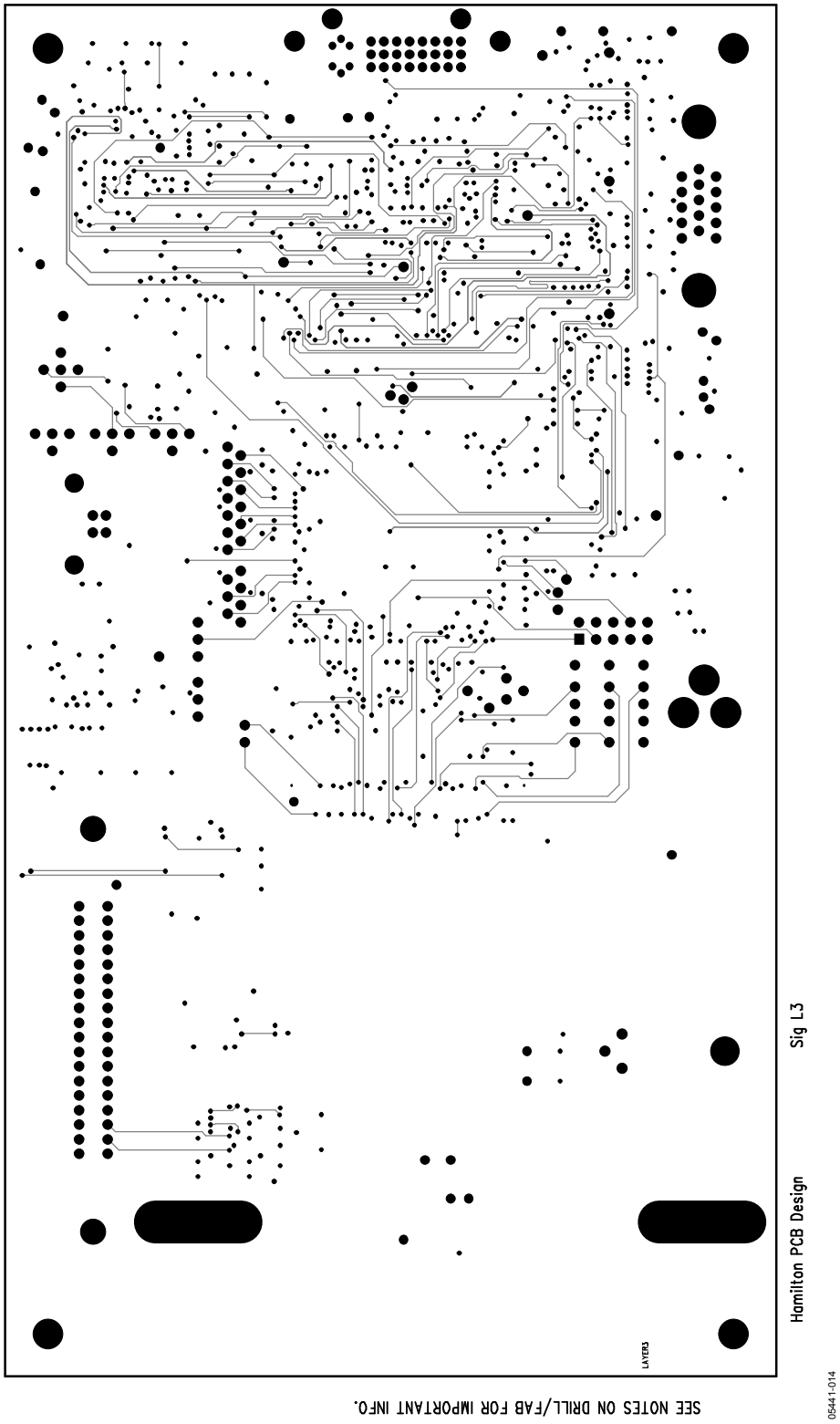
LAYER3
Sig L3
Hamilton PCB Design
SEE NOTES ON DRILL/FAB FOR IMPORTANT INFO.
05441-014

Figure 14.

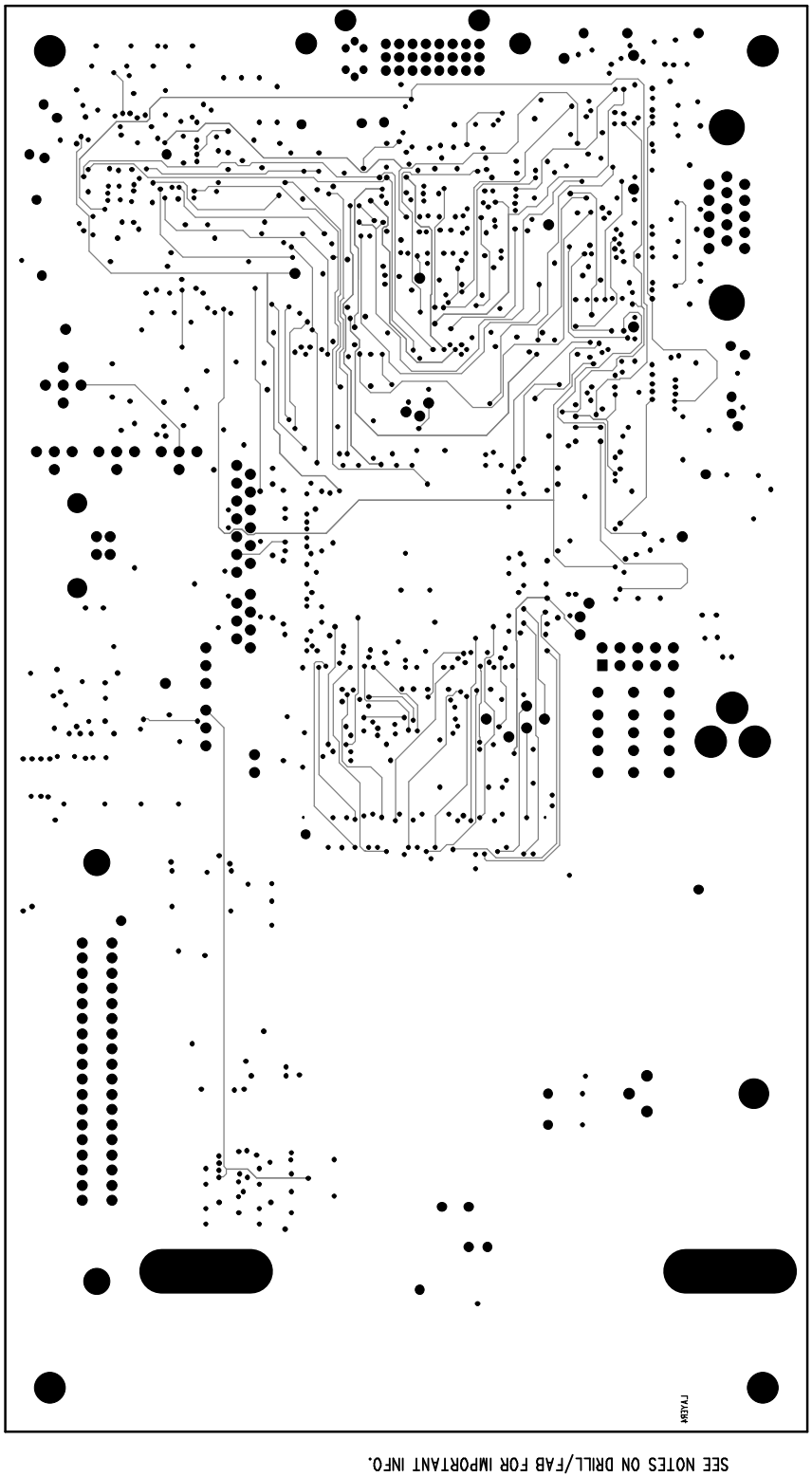
Sig L4
Hamilton PCB Design
05441-015
SEE NOTES ON DRILL/FAB FOR IMPORTANT INFO.

Figure 15.

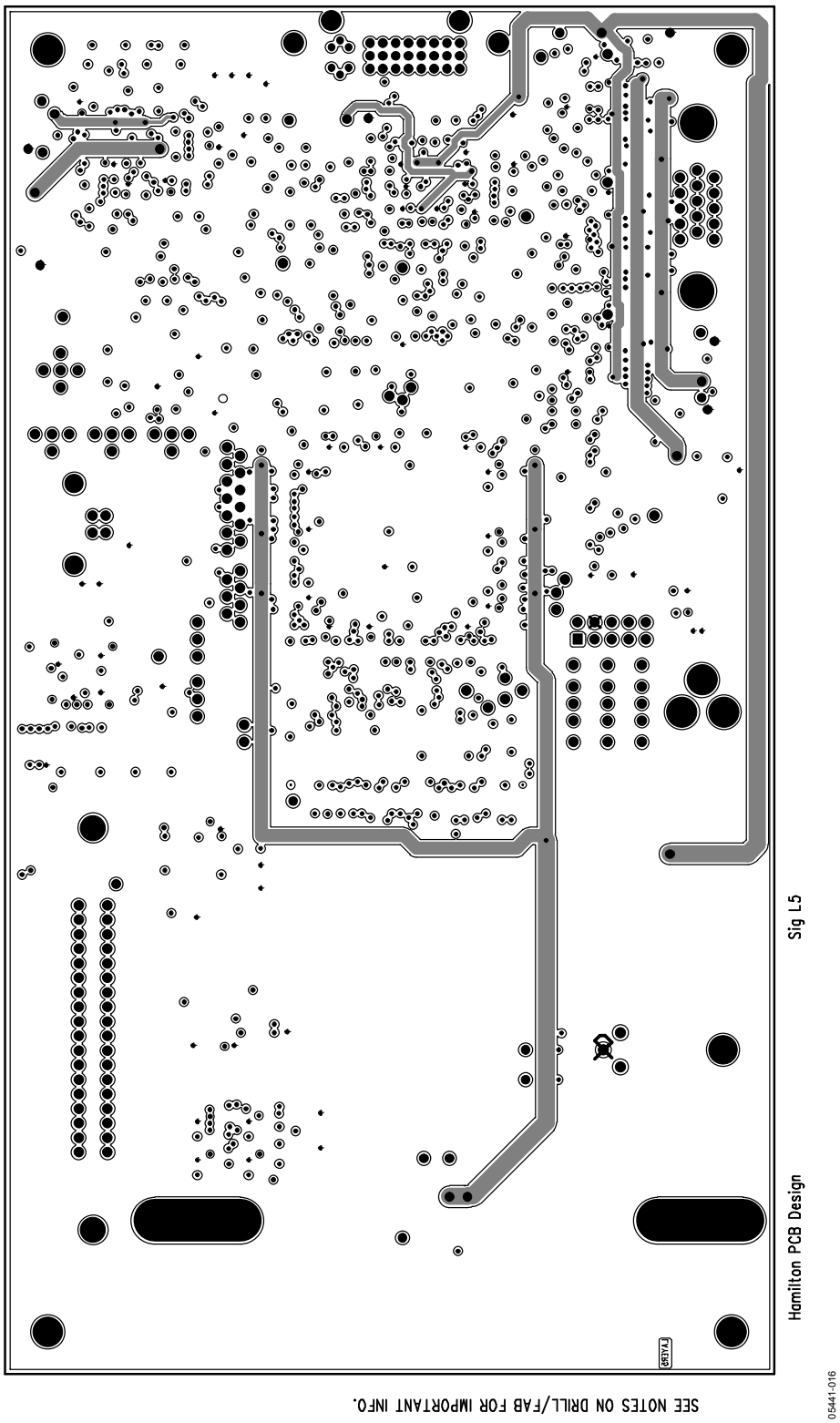
Sig L5
Hamilton PCB Design
SEE NOTES ON DRILL/FAB FOR IMPORTANT INFO.
05441-016

Figure 16.

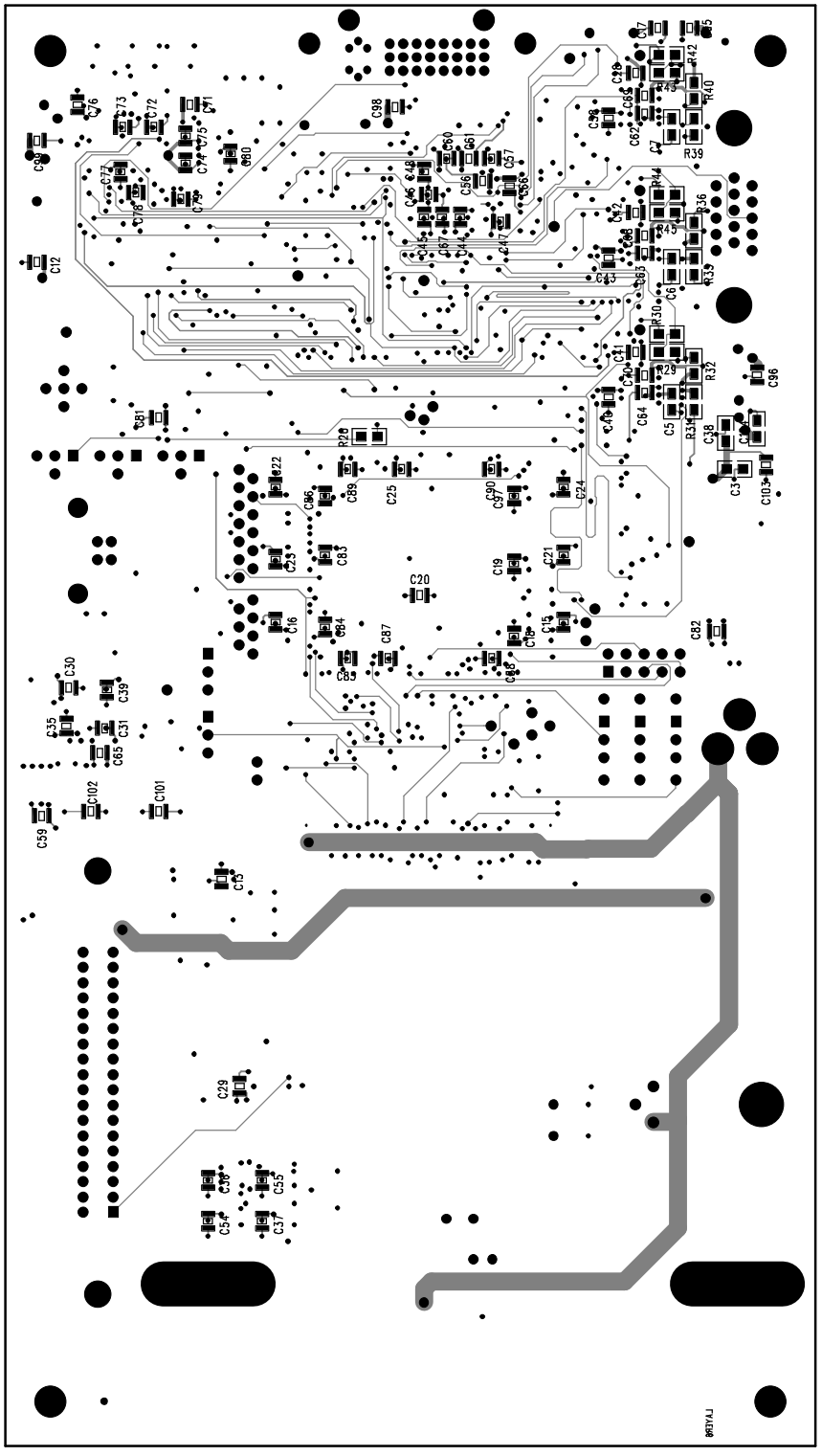
Hamilton PCB Design
Circuit L6
Bottom Silkscreen
SEE NOTES ON DRILL/FAB FOR IMPORTANT INFO.
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Figure 17.

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