

Implementing the Auto-Offset Function on the AD9985

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OVERVIEW

The AD9985 incorporates an auto-offset function. The Auto-Offset works by monitoring the output of each ADC during the clamp period and then calculating the required offset setting to yield a given output code. When auto-offset is enabled (Reg. 0x1D:7 = 1), the settings in the target code registers (0x19 to 0x1B) are used by the auto-offset circuitry as desired clamp codes. The circuit compares the output code during clamp to the target code and adjusts the offset up or down to compensate. In auto-offset mode, the target code is an 8-bit, twos complement word, with Bit 7 of their respective registers being the sign bit.

REGISTER DEFINITIONS

The definition of the offset registers does not change depending on whether the auto-offset function is enabled, or not. The target code and offset adjust registers are independent. The target code registers are disabled when auto-offset is turned off. However, the functionality of the offset registers (0x0B to 0x0D) is slightly different when the auto-offset function is enabled. This change is defined in Table 1.

In addition to the offset registers, the registers defined in Table 2 also support the auto-offset function.

Table 1. Offset Register Definitions

AD9985 Register	Bits	Normal Function (Manual Offset Mode)	Auto-Offset Function (Auto-Offset Mode)
0x0B	7:1	Red Channel Offset (in binary notation)	Red Channel Offset from Target Code (value in twos complement notation)
0x0C	7:1	Green Channel Offset (in binary notation)	Green Channel Offset from Target Code (value in twos complement notation)
0x0D	7:1	Blue Channel Offset (in binary notation)	Blue Channel Offset from Target Code (value in twos complement notation)

Table 2. Auto-Offset Related Register Definitions

Register	Function	Bits	Description	
0x19	Red Target Code	7:0	Sets desired output code for red channel during black reference when auto-offset is enabled	
0x1A	Green Target Code	7:0	Sets desired output code for green channel during black reference when auto-offset is enabled	
0x1B	Blue Target Code	7:0	Sets desired output code for blue channel during black reference when auto-offset is enabled	
0x1C	Test Bits	7:0	Must be set to 0x11 for proper operation	
0x1D	Auto-Offset Control	7	Auto-Offset Enable	1 = Auto-offset enabled 0 = Auto-offset disabled
		6	Hold Auto-Offset	0 = Update auto-offset according to bits 0x1D to 1:0 1 = Hold the current auto-offset value
		5:2	Control Bits	Must be set to 01001 for proper operation
		1:0	Update Mode	00 = Update every clamp 01 = Update every 16 clamps 10 = Update every 64 clamps 11 = Not valid

BRIGHTNESS ADJUSTMENT

If auto-offset is disabled, the offset registers control the absolute offset added to the channel. The offset control provides a +63 LSBs to –64 LSBs of adjustment range (code 128 = 0 offset, code 255 = +63, etc.), with one LSB of offset corresponding to one LSB of output code.

With auto-offset enabled, Registers 0x19 to 0x1B contain target codes for the autclamp feedback circuit. The offset registers (0x0B to 0x0D) are still used to adjust brightness. The difference is, when auto-offset is enabled, the offset register values are in twos complement notation. The effective range for adjusting offset (used for brightness control) is +63 LSBs to –64 LSBs. When developing software to control brightness, this must be taken into consideration.

USING AUTO-OFFSET

To activate the auto-offset mode, set Register 1Dh, Bit 7 to 1. Next, the target code registers (19h through 1Bh) must be programmed. The values programmed into the target code registers should be the output code desired from the AD9985 during the back porch reference time. For example, for RGB signals, all three registers would normally be programmed to a very small code (4 is recommended), while, for YPbPr signals, the green (Y) channel would normally be programmed to a very small code and the blue and red channels (Pb and Pr) would normally be set to 128. Any target code value between 1 and 254 can be set, although the AD9985's offset range may not be

able to reach every value. Intended target code values range from (but are not limited to) 1 to 40 when ground clamping and 90 to 170 when midscale clamping.

The ability to program a target code for each channel gives users a large degree of freedom and flexibility. While, in most cases, all channels will either be set to 4 or 128, the flexibility to select other values allows for the possibility of inserting intentional skews between channels. It also allows for the ADC range to be skewed so that voltages outside of the normal range can be digitized. (For example, setting the target code to 40 would allow the sync tip, which is normally below black level, to be digitized and evaluated.)

Lastly, when in auto-offset mode, the manual offset registers (0Bh to 0Dh) have new functionality. The values in these registers are digitally added to the value of the ADC output. The purpose of doing this is to match a benefit that is present with manual offset adjustment. Adjusting these registers is an easy way to make brightness adjustments. Although some signal range is lost with this method, it has proven to be a very popular function. In order to be able to increase and decrease brightness, the values in these registers in this mode are signed twos complement. The digital adder is only used when in auto-offset mode. Although it cannot be disabled, setting the offset registers to all 0s will effectively disable it by always adding 0.

Table 3. Example Register Settings for Enabling Auto-Offset

Reg.	RGB Auto-Offset Clamping			YPbPr Auto-Offset Clamping		
	Value	Description		Value	Description	
0x0B	0x00	Red offset	Registers used for brightness control: +63 LSBs to –64 LSBs range	0x00	Red offset	Green register only for brightness control: +63 LSBs to –64 LSBs range
0x0C	0x00	Green offset		0x00	Green offset	
0x0D	0x00	Blue offset		0x00	Blue offset	
0x19	0x04	Red target code	Ground-clamped targets = 4	0x80	Red target code	Red, blue targets = 128. Green target = 4
0x1A	0x04	Green target code		0x04	Green target code	
0x1B	0x04	Blue target code		0x80	Blue target code	
0x1C	0x11	Values for proper operation		0x11	Values for proper operation	
0x1D	1*** **	Bit 7 = 1. Enables auto-offset		1*** **	Bit 7 = 1. Enables auto-offset	
0x1D	*0** **	Bit 6 = 0. Continuous update		*0** **	Bit 6 = 0. Continuous update	
0x1D	**10 01**	Bits 5:2 Values for proper operation		**10 01**	Bits 5:2 Values for proper operation	
0x1D	**** **xx	00 – Update auto-offset every clamp 01 – Update every 16 clamps 10 – Update every 64 clamps 11 – Not valid		**** **xx	00 – Update auto-offset every clamp 01 – Update every 16 clamps 10 – Update every 64 clamps 11 – Not valid	