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Software Programmable Evaluation Board for the ADA2200 Synchronous Demodulator

FEATURES

Simple synchronous demodulation development platform
USB powered
Evaluation board compatible with Analog Devices, Inc., system demonstration platform (SDP-S or SDP-B)
SPI or EEPROM programmable
Input and output signal conditioning circuitry
Synchronization signals available for external devices

ADDITIONAL EQUIPMENT

PC running Windows XP or more recent version
SDP-S (EVAL-SDP-CS1Z) or SDP-B (EVAL-SDP-CB1Z) controller board
Function generator
Oscilloscope and/or digital voltmeter

SOFTWARE

ACE software (see the ACE Software User Guide)

GENERAL DESCRIPTION

This user guide describes the SDP-compatible evaluation board for the ADA2200 synchronous demodulator. The ADA2200SDP-EVALZ evaluation board facilitates the evaluation of the ADA2200 by simplifying signal connections to standard test equipment. Inputs, outputs, supplies, and other circuit test points on the board are easily accessed via test clips, differential probes, or standard SMA cables. On-board signal conditioning circuitry offers many options for testing different circuit schemes.

The ADA2200SDP-EVALZ evaluation board mates with the EVAL-SDP-CS1Z SDP-S board or the EVAL-SDP-CB1Z SDP-B controller board. The controller board provides an interface between the ADA2200SDP-EVALZ evaluation board and a PC USB port. The controller board can be purchased separately.

The PC resident ACE software provides an intuitive GUI, allowing all of the ADA2200 modes of operation to be configured over the SPI port. The ACE software also has plug-in modules for many other Analog Devices evaluation boards and CFTL demo boards.

Figure 2 shows the recommended configuration for initial evaluation. See the Quick Start Procedure section for more details.

Full specifications for the ADA2200 are available in the product data sheet, which should be consulted in conjunction with this user guide with using the evaluation board.

EVALUATION BOARD PHOTOGRAPH

Figure 1.

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REVISION HISTORY

12/14—Revision 0: Initial Version

QUICK START PROCEDURE

Figure 2 shows the recommended configuration for initial evaluation. Perform the test procedure in this section to ensure that the bench setup is working properly prior to testing new evaluation configurations.

Set up the ADA2200SDP-EVALZ default test bench by completing the following steps:

1. Install the ACE software on the PC by following the instructions in the ACE Software User Guide. Exit the ACE software program.
2. The ADA2200SDP-EVALZ evaluation board is configured to work with the EVAL-SDP-CS1Z SDP-S controller board by default. To use the EVAL-SDP-CB1Z SDP-B controller board, remove R43.
3. Verify that the jumper configuration on the ADA2200SDP-EVALZ evaluation board matches the settings shown in Table 1.
4. Plug the SDP controller board into P3 of the ADA2200SDP-EVALZ evaluation board.
5. Power the two boards by connecting J2 of the SDP-S controller board to a PC USB port. A green LED lights on each board when power is available.
6. Press S1 momentarily to reset the ADA2200.
7. Apply a 500 kHz clock to the CLKIN input. The input is high input impedance and expects LVCMOS (3.3 V) level inputs.
8. Verify that a square wave (~7.8125 kHz) is present at RCLK_OUT (J3). Connect RCLK_OUT to VINP (J7) with an SMA cable.
9. Use the RCLK signal present on P1 to trigger an oscilloscope. Observethat the demodulated output signals on TP27 and TP28 and the SYNCO signal on TP29 match the waveforms shown in Figure 3.
10. Measure the filtered output across J9 and J10 with a digital multimeter (DMM). The output voltage should read approximately −1.56 V.

Table 1. Default Jumper Settings

Designator	Position	Description
P1	Open	VINP test point
P2	Open	VINN test point
P4	Open	VOP test point
P5	Open	VON test point
P7	2 and 3	INP of ADA2200 connected to +OUT of AD8476 input buffer
P8	2 and 3	INN of ADA2200 connected to –OUT of AD8476 input buffer
P9	1 and 2	VOP connected to U4 LPF
P10	1 and 2	Use external clock oscillator
P12	Open	VIP, VIN test point
JP1	Open	AC-couple RCLK_OUT

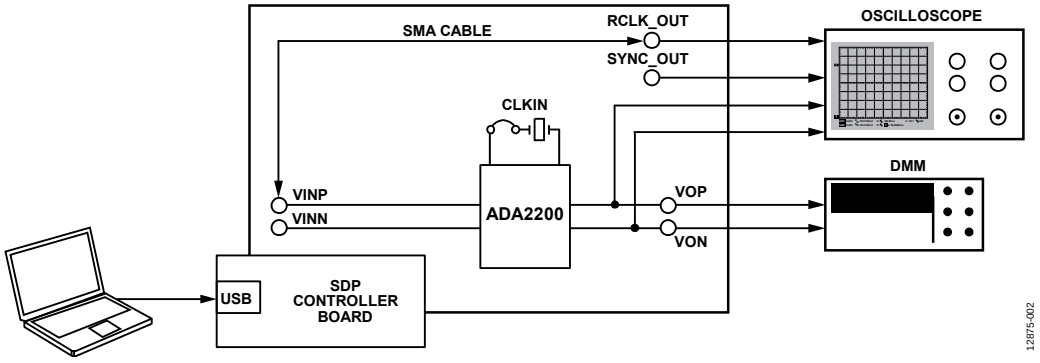

Figure 2. Suggested Configuration for Quick Start, Showing Connections to Standard Test Equipment

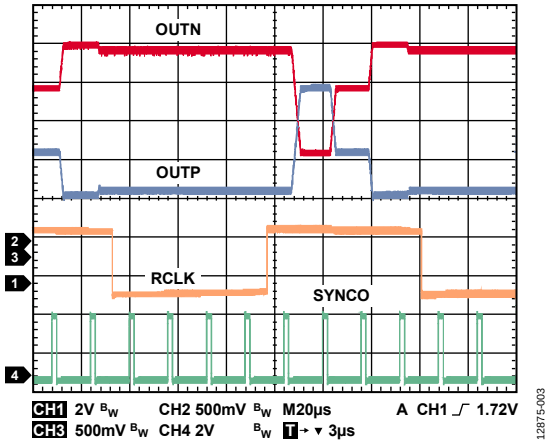

Figure 3. Expected RCLK_OUT, VOP, VON, and SYNC_OUT Waveforms

CONFIGURATION SOFTWARE

The ACE software enables configuration of the ADA2200 over a USB port. This section introduces the key features of the program.

See the ACE Software User Guide for download instructions and a more complete description of the program.

OVERVIEW

With the SDP controller board and the ADA2200SDP-EVALZ evaluation board connected together, plug the USB cable from the PC into the SDP controller board. (Always plug the SDP controller board and the ADA2200SDP-EVALZ evaluation board together before connecting the USB cable to the PC). Start the ACE software. The program opens in the **Start** view tab; this tab shows which boards the program recognizes as connected to your PC. The tab shows the ADA2200SDP-EVALZ evaluation board as attached, as shown in Figure 4.

In the **System** tab, double-clicking the ADA2200SDP-EVALZ evaluation board image opens the **ADA2200 Eval Board** tab, as shown in Figure 5. This tab enables some basic configuration of the ADA2200SDP-EVALZ evaluation board to be performed through the menus available on the left hand side of the screen. To make any changes effective in the hardware, click the **Apply** button.

In the **ADA2200 Eval Board** tab, double-clicking the ADA2200 image opens the **ADA2200** tab. This tab displays the ADA2200 block diagram and allows changes to the device configuration, as shown in Figure 6. This tab also shows the frequencies expected on some of the key clock signals. For the frequencies to match the hardware, enter the actual CLKIN frequency in the **CLKIN** field. The changes are not made to the hardware configuration until the **Apply Changes** button is clicked.

In the **ADA2200** tab, clicking the **Proceed to Memory Map** button on the bottom right hand corner of the window opens the **ADA2200 Memory Map** tab, as shown in Figure 7. This tab allows access to all of the registers of the ADA2200. The changes are not made to the hardware configuration until either the **Apply All** or **Apply Selected** button is clicked.

SOFTWARE TAB VIEWS

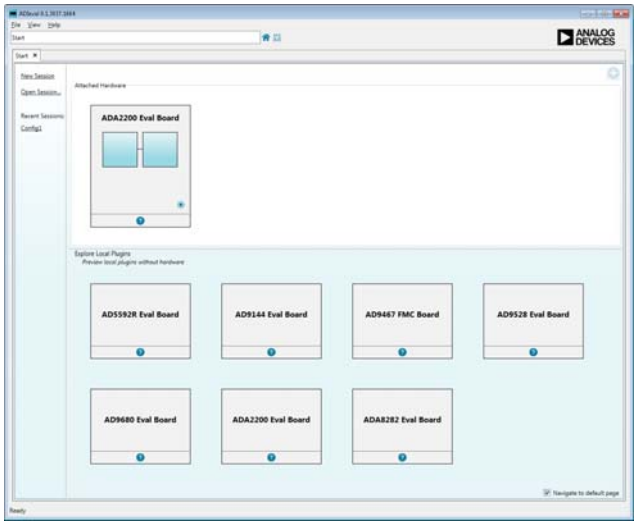

*Figure 4. **Start** Tab View*

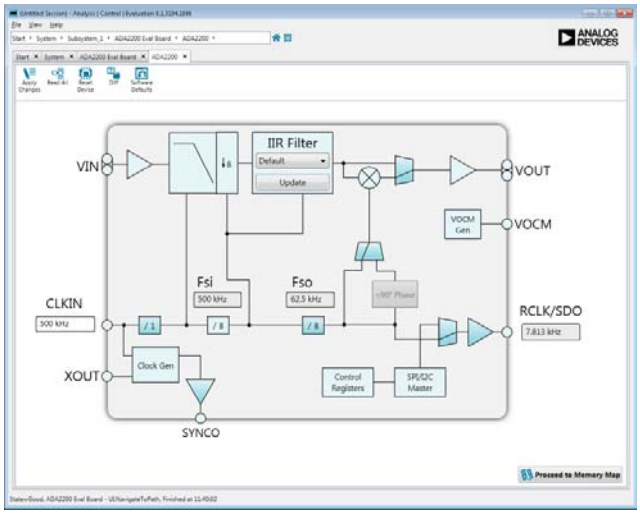

*Figure 6. **ADA2200** Tab View*

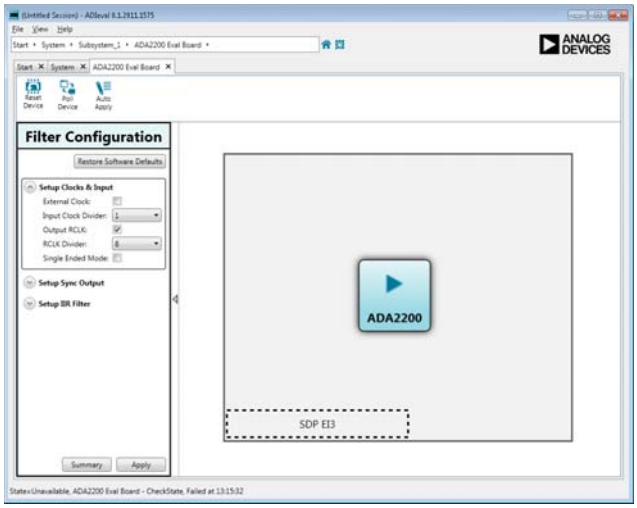

*Figure 5. **ADA2200 Eval Board** Tab View*

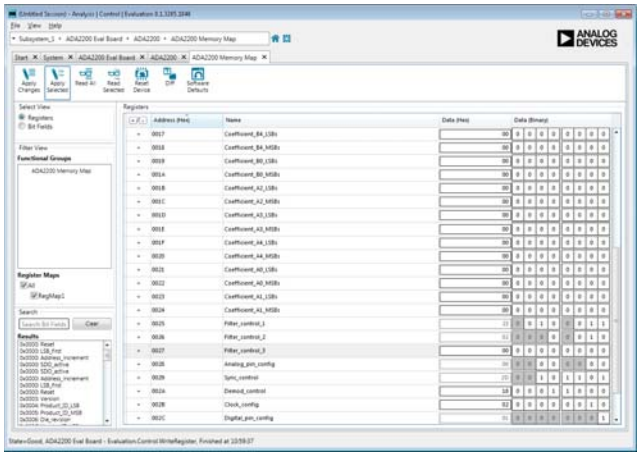

*Figure 7. **ADA2200 Memory Map** Tab View*

DETAILED BOARD DESCRIPTION

This section provides details about the on-board circuitry operation and some of the circuit options that are available.

POWER SUPPLIES

The ADA2200SDP-EVALZ evaluation board accepts +5 V power from the USB_VBUS pin of P3. The ADP151 regulates this supply to +3.3 V and supplies the VIO and 3V3 rails for the board.

To run the board from an external power supply while still using the ADP151 to regulate the power rails, remove E3 and apply power to P6. Use a voltage from 3.6 V to 5.5 V to supply the board through P6.

To run the board by supplying an external power supply to the VIO and 3V3 rails directly, remove R55 and supply power to TP35. Use a voltage from 3.0 V to 3.6 V to supply the board through TP35.

SYSTEM CLOCK

By default, the ADA2200 CLKIN input is generated by the on-board ceramic resonator circuit. This circuit generates a 500 kHz clock. A footprint for a crystal is also provided to facilitate generating frequencies of up to 1 MHz.

To run from an external clock source, install a jumper between Pin 1 and Pin 2 of P10, which connects the clock input (J1) buffer to the ADA2200 CLKIN pin. Note that the R32 of the clock input is uninstalled by default. Signal sources expecting a 50 Ω termination drive twice the expected voltage onto this connector.

INPUT DRIVER

By default, the AD8476 (A2) is configured to receive a single-ended input on the VINP connector and to convert the signal to differential. The differential output of the AD8476 is connected to the INP and INN inputs of the ADA2200. The input impedance of VINP is approximately 10 kΩ. The AD8476 has unity gain; therefore, 1 V applied to VINP results in 1 V differential applied across INP to INN.

To use a differential input (between VINP and VINN) to the AD8476, remove R25 and install a 0 Ω resistor at R57.

To bypass the AD8476, install the shunts of P7 and P8 between Pin 1 and Pin 2. Alternatively, remove the shunts of P7 and P8, and apply the input signal between TP18 and TP19.

Footprints are supplied for a low-pass filter (LPF) before the INP and INN inputs of the ADA2200. For best performance, keep the R30 and R31 series input resistors below 1 kΩ.

OUTPUT FILTER

The OUTP and OUTN from the ADA2200 each have an RC filter on the output, which can be used to set the bandwidth of the demodulated output. By default, the output of the RC filter appears on the VOP and VON connectors.

Reconstruction Filter

There is an optional differential to single-ended reconstruction filter on the evaluation board. To route the ADA2200 outputs through the filter, install R26 and R27. To route the output of the reconstruction filter to the VOP connector, install the shunt of P9 between Pin 2 and Pin 3.

The board component population sets the reconstruction filter corner frequency at 20 kHz. The following equations detail how to redesign the filter for different frequency responses.

Choose the desired values for 3 dB frequency (f_C), quality factor (Q), gain (G), k (a number between 1 and 2 to give convenient capacitor values), and R26 (R). The component values can be calculated as follows:

$$\omega_C = 2 \times \pi \times f_C$$

$$R27 = R$$

$$C15 = k \times Q \times R \times (G + 1)/(2 \times \omega_C \times G \times R2)$$

$$R33 = G \times R$$

$$R47 = R52 = 2 \times R33$$

$$R34 = R35 = R \times R33/(2 \times R \times R33 \times C15 \times (\omega_C/Q) - R - R33)$$

$$C16 = C19 = 1/(2 \times R34 \times R33 \times C15 \times \omega_C^2)$$

An excel spreadsheet that performs these calculations is available on the ADA2200 Evaluation Board Wiki Page.

DIGITAL OUTPUTS

RCLK_OUT and SYNC_OUT

The RCLK signal from the ADA2200 is buffered by U6 and appears on the RCLK_OUT connector (J3).

The SYNCO signal from the ADA2200 appears on the SYNC_OUT connector (J2). It is good practice to disable the SYNCO signal when it is not being used, to minimize any coupling of this signal on the board.

SPI Port Outputs

The SPI port signals are routed to the SDP connector through the A3 and A4 switches. The switches isolate the ADA2200 from the SPI bus during initial boot up to avoid contention with signals on the SDP board.

By default, the ADA2200SDP-EVALZ evaluation board is configured so that the ADA2200 is running in 3-wire SPI mode. To run the ADA2200 in 4-wire mode, install R41.

JUMPERS

Table 2 provides a summary of the jumper configuration options for the ADA2200SDP-EVALZ evaluation board.

Table 2. Jumper Descriptions

Designator	Shunt	Description
P7	1 and 2	VINN (J8) connects to INN of ADA2200
	2 and 3	VINN (J8) connects to AD8476 input driver
P8	1 and 2	VINP (J7) connects to INP of ADA2200
	2 and 3	VINP (J7) connects to AD8476 input driver
P9	1 and 2	VOP (J9) connects to OUTP
	2 and 3	VOP (J9) connects to V_{OUT} of the ADA4841-1 reconstruction filter amplifier
P10	1 and 2	Use external clock for CLKIN
	2 and 3	Use on-board clock for CLKIN
JP1	Open	AC-couple RCLK_OUT
	1 and 2	DC-couple RCLK_OUT

MEASURING SIGNALS

INPUT SIGNAL SYNCHRONIZATION

By default, the ADA2200 filters and demodulates signals located exactly at 1/64 of its clock frequency (f_{CLKIN}). For example, when using the 400 kHz on-board oscillator, the demodulated signal frequency must be 6.25 kHz. The ADA2200 provides the RCLK reference signal to facilitate synchronization of the modulation signal to this internal demodulation clock.

The RCLK signal can be used directly to excite a sensor, or as a trigger for an excitation drive signal, or as a reference clock to a phase-locked loop (PLL) used as the excitation signal clock source.

OUTPUT SIGNAL SYNCHRONIZATION

The SYNCO output synchronization pulse generated by the ADA2200 is available on the SYNC_OUT connector. The ADA2200 generates this pulse every time the output is updated and ready to be sampled. The frequency of this pulse is 1/8 the clock frequency. By default, the pulse polarity is positive, and it is generated 6.5 clock cycles after the last output update.

When the ADA2200 is clocked by the on-board oscillator circuit, the frequency of the SYNCO pulse is 50 kHz; the pulse duration is one clock cycle or 2.5 µs (12.5% duty cycle); and the pulse occurs 16.25 µs after the last output update. The polarity and its occurrence relative to the output update event can be configured for different applications.

Table 3. Default Clock Frequencies Relative to f_{CLKIN}

Signal	Ratio	Description
f_{CLKIN}	1	Master clock
f_{SI}	1	Input sampling rate
f_{SI_NYQ}	1/2	Input sampling Nyquist rate
f_{SO}	1/8	Output sampling rate
f_{SO_NYQ}	1/16	Output sampling Nyquist rate
f_{SYNCO}	1/8	Synchronization pulse frequency
f_{RCLK}	1/64	Reference clock frequency
f_C	1/64	Band-pass filter center frequency
f_M	1/64	Mixer frequency

SIGNAL MEASUREMENTS

The signal present at the output of the ADA2200 depends on the amplitude and relative phase of the signal applied at its inputs. When the amplitude or phase is known and constant, any output variations can be attributed to the modulated parameter. Therefore, when the relative phase of the input is constant, the ADA2200 performs amplitude demodulation. When the amplitude is constant, the ADA2200 performs phase demodulation.

The sampling and demodulation processes introduce additional frequency components onto the output signal. If the output signal of the ADA2200 is used in the analog domain or if it is sampled asynchronously to the ADA2200 sample clock, these high frequency components can be removed by following the ADA2200 with a reconstruction filter.

If the ADA2200 output is sampled by an ADC, synchronizing the ADA2200 CLKIN input to the ADC conversion clock eliminates the need for an analog reconstruction filter. When the ADC samples the ADA2200 output synchronously, the ADC sampling inherently rejects the frequency artifacts created by the ADA2200 output sampling. The demodulation process creates output ripple at the mixing frequency. This output ripple can be removed digitally by performing a cycle mean of the output samples or by a moving average filter.

AMPLITUDE MEASUREMENTS

If the relative phase of the input signal to the ADA2200 remains constant, the output amplitude is directly proportional to the amplitude of the input signal. Note that the signal gain is a function of the relative phase of the input signal. Figure 8 shows the relationship between the cycle mean output and the relative phase.

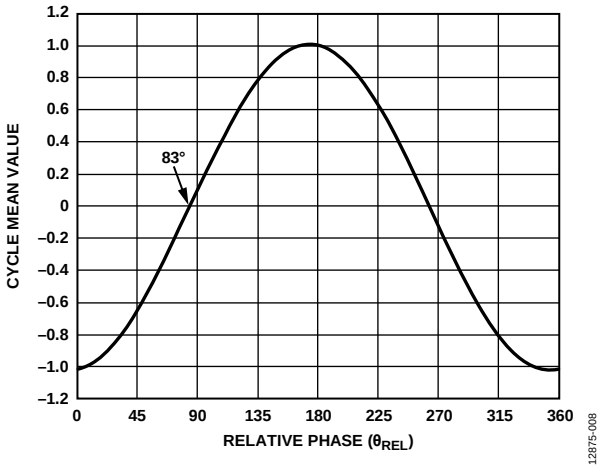

Figure 8. Phase Transfer Function with Phase Delay of 83°, 1 V rms Input

The cycle mean output voltage is

$$V_{CYCLEMEAN} = Conversion\ Gain \times V_{IN(RMS)} \times \sin(\theta_{REL} - \theta_{DEL})$$
$$= 1.05 \times V_{IN(RMS)} \times \sin(\theta_{REL} - \theta_{DEL})$$

Therefore, the highest gain, and thus the largest signal-to-noise ratio measurement, is obtained when operating the ADA2200 with $\theta_{REL} = \theta_{DEL} + 90° = 173°$. This value of θ_{REL} is also the operating point with the lowest sensitivity to changes in the relative phase. Operating with $\theta_{REL} = \theta_{DEL} - 90° = -7°$ offers the same gain and measurement accuracy, but with a sign inversion.

PHASE MEASUREMENTS

If the amplitude of the input signal to the ADA2200 remains constant, the output amplitude is a function of the relative phase of the input signal. The relative phase can be measured as

$$\theta_{REL} = \sin^{-1}(V_{CYCLEMEAN}/(Conversion\ Gain \times V_{IN(RMS)})) + \theta_{DEL}$$
$$= \sin^{-1}(V_{CYCLEMEAN}/(1.05 \times V_{IN(RMS)})) + \theta_{DEL}$$

Note that the output voltage scales directly with the input signal amplitude. A full-scale input signal provides the greatest phase sensitivity (V/°θ_{REL}) and thus the largest signal-to-noise ratio measurement.

The phase sensitivity also varies with relative phase. The sensitivity is at a maximum when θ_{REL} = 83°. Therefore, the optimal measurement range is for input signals with a relative phase equal to the phase delay of ±45°. This range provides the highest gain and thus the largest signal-to-noise ratio measurement. This range is also the operating point with the lowest sensitivity to changes in the relative phase. Operating at a relative phase equal to the phase delay of −135° to −225° offers the same gain and measurement accuracy, but with a sign inversion.

The phase sensitivity with a 4 V p-p differential input operating with a relative phase that is equal to the phase delay results in a phase sensitivity of 36.6 mV/°θ_{REL}.

AMPLITUDE AND PHASE MEASUREMENTS

When both the amplitude and relative phase of the input signals are unknown, it is necessary to obtain two orthogonal components of the signal to determine its amplitude, relative phase, or both. These two signal components are referred to as the in-phase (I) and quadrature (Q) components of the signal.

A signal with two known rectangular components is represented as a vector or phasor with an associated amplitude and phase (see Figure 9).

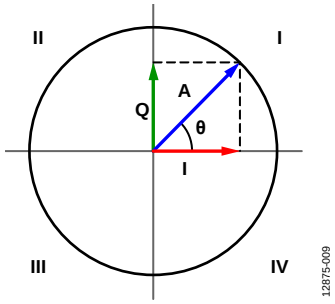

Figure 9. Rectangular and Polar Representation of a Signal

If the signal amplitude remains nearly constant for the duration of the measurement, it is possible to measure both the I and the Q components of the signal by toggling the PHASE90 bit between two consecutive measurements. To measure the I component, set the PHASE90 bit to 0. To measure the Q component, set the PHASE90 bit to 1.

After both the I and Q components have been obtained, it is possible to separate the effects of the amplitude and phase variations. Then, calculate the magnitude and relative phase using the following formulas:

$$A = \sqrt{I^2 + Q^2}$$

$$\theta_{REL} = \cos^{-1}\left[Q/A\right] + \theta_{DEL}$$

Or alternatively,

$$\theta_{REL} = \sin^{-1}\left[I/A\right] + \theta_{DEL}$$

The inverse sine or inverse cosine functions linearize the relationship between the relative phase of the signal and the measured angle. Because the inverse sine and inverse cosine are only defined in two quadrants, the sign of I and Q must be considered to map the result over the entire 360° range of possible relative phase values. The use of the inverse tangent function is not recommended because the phase measurements become extremely sensitive to noise as the calculated phase approaches ±90°.

EVALUATION BOARD SCHEMATIC

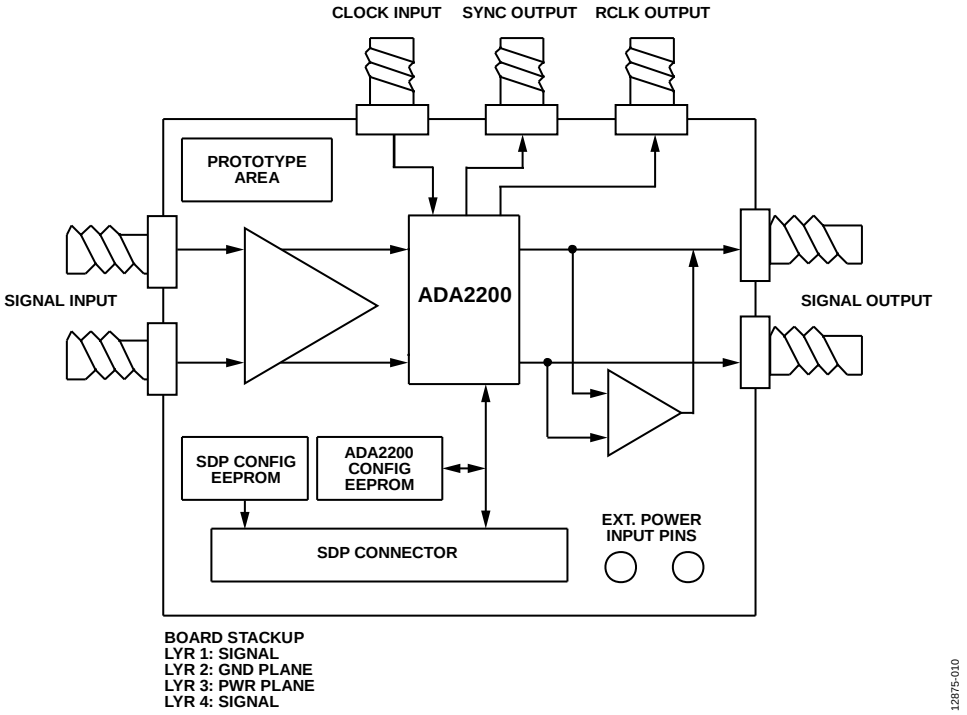

Figure 10. Evaluation Board Block Diagram

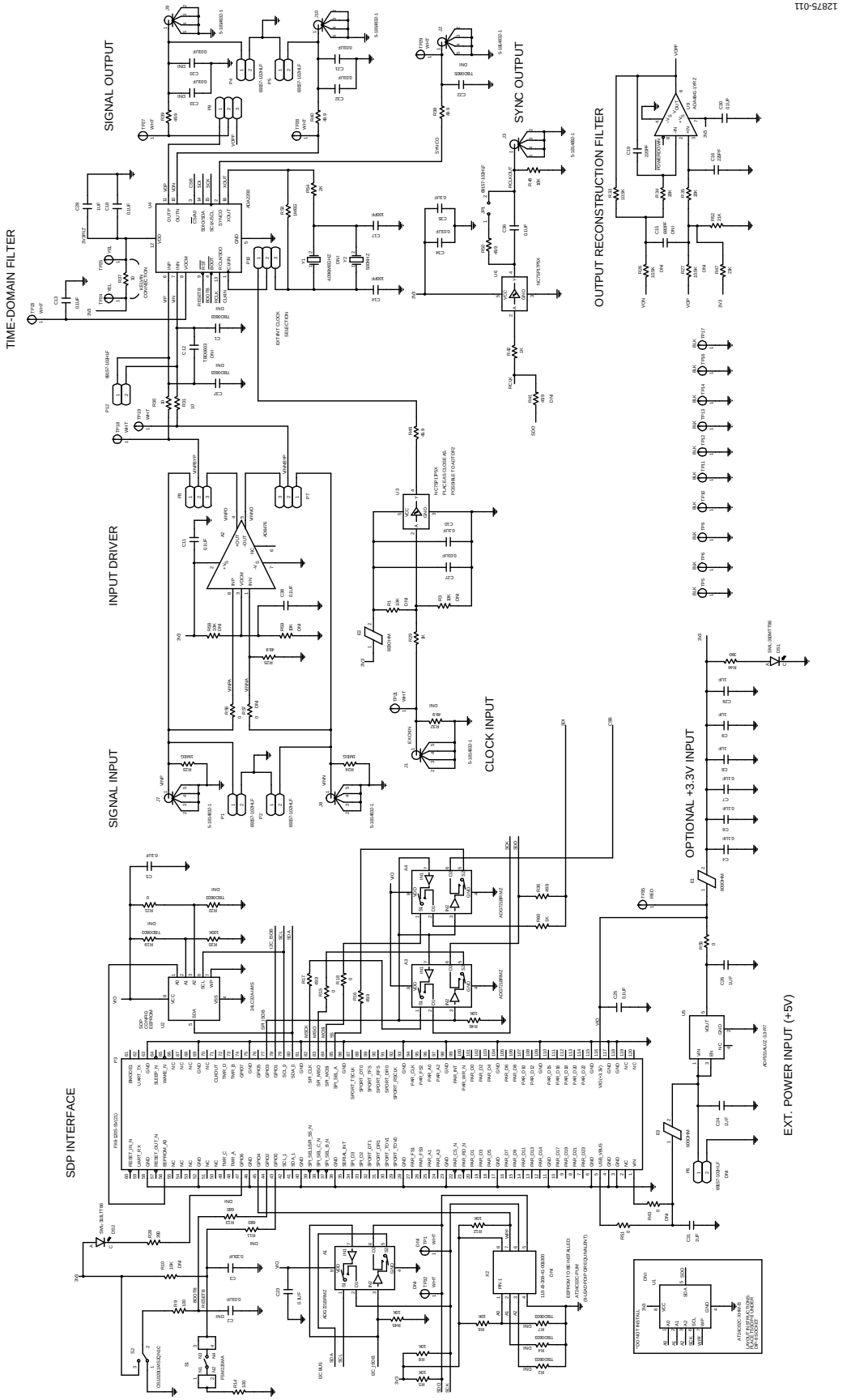

Figure 11. Evaluation Board Schematic

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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