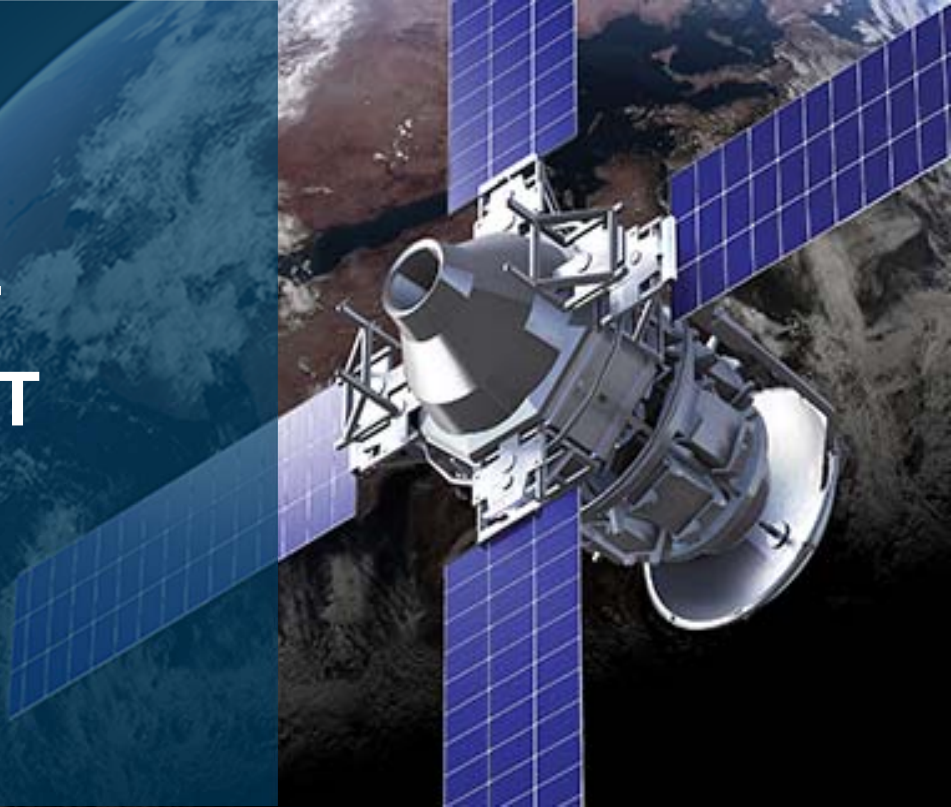


# SINGLE EVENT LATCH-UP TEST REPORT ADA4096-2S

*April 2016*



## Radiation Test Report

Product:	ADA4096-2S
Effective LET:	80.7 MeV-cm <sup>2</sup> /mg
Fluence:	1E7 Ions/cm <sup>2</sup>
Die Type:	ADA4096-2
Facilities:	RADEF, University of Jyvaskyla, Finland
Tested:	September 2015

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**SINGLE EVENT EFFECTS  
TEST REPORT**

Test Type:	Heavy ion
Test facility:	RADEF, University of Jyvaskyla, Finland
Test Date:	September 2015
Part Type:	AD4096-2
Part Description:	Dual 30 V, Micropower, Overvoltage Protection, Rail-to-Rail Input/Output Amplifiers
Part Manufacturer:	Analog Devices

**Analog Devices PO No 45516080 dated 22/06/2015**

<b>Hirex reference :</b>	HRX/SEE/0538	Issue : 01	Date :	October 28, 2015
<b>Written by :</b>	Mehdi Kaddour	Design Engineer		
<b>Authorized by:</b>	F.X. Guerre	Study Manager		

**RESULTS SUMMARY****Facility**

RADEF, University of Jyvaskyla, Finland

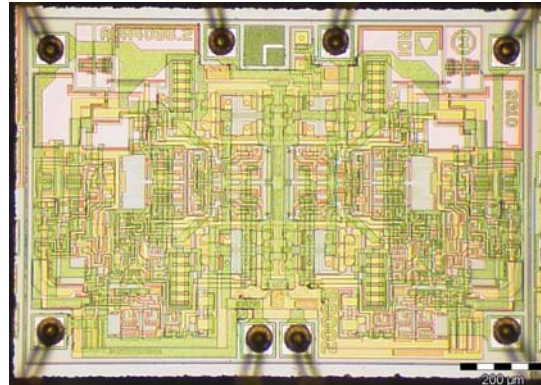
**Test date**

September 2015

**Device description**

Dual Dual 30 V, Micropower, Overvoltage Protection, Rail-to-Rail Input/Output Amplifiers

<b><u>Part type:</u></b>	AD4096-2
<b><u>Manufacturer:</u></b>	Analog Devices
<b><u>Package:</u></b>	MSOP-8
<b><u>Samples used:</u></b>	6
<b><u>Top marking:</u></b>	logo A 2T
<b><u>Bottom marking:</u></b>	#517 7095
<b><u>Date code:</u></b>	1517
<b><u>Die dimensions:</u></b>	1.230 mm X 0.866 mm

**SEL Results**

No SEL neither step current increase has been observed when tested with V+/- set to 5V at any LET value at 125°C with all tested samples.

## DOCUMENTATION CHANGE NOTICE

Issue	Date	Page	Change Item	
01	28/10/2015	All	Original issue	

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## SEE TEST REPORT

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## 1 Introduction

This report presents the results of SEL Heavy Ions test program carried out on Analog Devices AD4096-2. On September 2015, 6 samples were used for heavy ions testing at RADEF, University of Jyväskylä, Finland. This work was performed for Analog Devices, Greensboro under PO n° 45516080 dated 22/06/2015.

## 2 Applicable and Reference Documents

### 2.1 Applicable Documents

AD-1. Datasheet: [http://www.analog.com/media/en/technical-documentation/data-sheets/ADA4096-2\\_4096-4.pdf](http://www.analog.com/media/en/technical-documentation/data-sheets/ADA4096-2_4096-4.pdf)

### 2.2 Reference Documents

RD-1. Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100

### 3 DEVICE INFORMATION

#### 3.1 Device description

AD4096-2 is a dual Dual 30 V, Micropower, Overvoltage Protection, Rail-to-Rail Input/Output Amplifiers.

<u>Part type:</u>	AD4096-2
<u>Part number:</u>	ADA4096 – 2ARMZ
<u>Manufacturer:</u>	Analog Devices
<u>Package:</u>	MSOP-8
<u>Samples used:</u>	6
<u>Top marking:</u>	logo A 2T
<u>Bottom marking:</u>	#517 7095
<u>Date code:</u>	1517
<u>Die dimensions:</u>	1.230 mm X 0.866 mm

#### 3.2 Sample identification

12 AD4096-2 parts were delivered by Analog Devices, Greensboro. Samples were prepared and opened chemically to be tested to heavy ions. 6 samples were verified fully functional before the test campaign, and 6 were tested under irradiation.

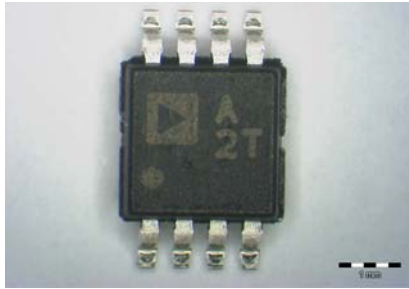


Photo 1 – Device top view

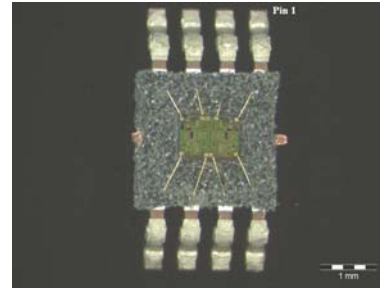


Photo 2 – Device delidded

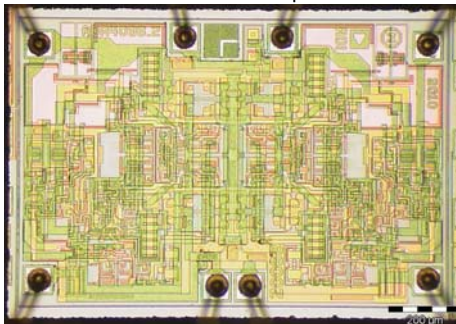


Photo 3 – die, full view

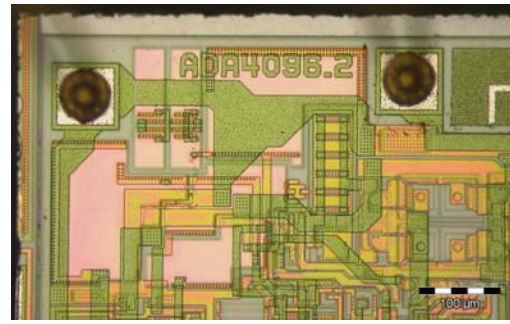


Photo 4 – Die marking #1

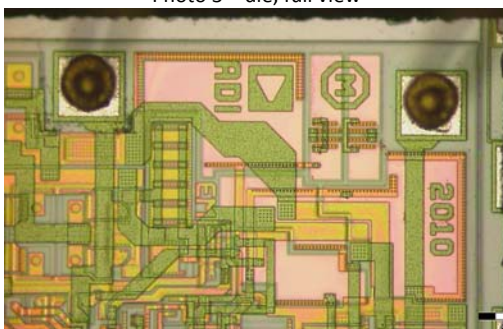


Photo 5 – Die marking #2

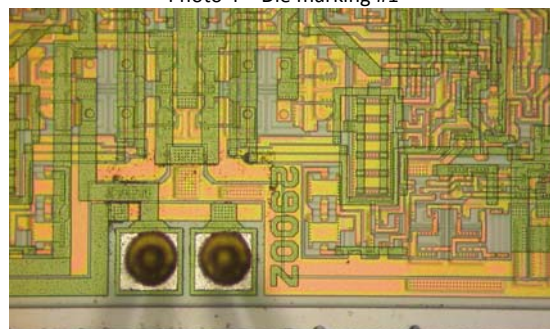


Photo 6 – Die marking #3

**Figure 1 – AD4096-2 device identification**

#### 3.3 Sample preparation and evaluation of dead layer thickness

Samples were opened chemically.

Die micro-section results are given in appendix. Overall dead layer thickness on top of active zone is less or equal to 10 microns of equivalent silicon.



#### 4 **RADEF Facility**

Test at the cyclotron accelerator was performed at University of Jyväskylä (JYFL) (Finland) under HIREX Engineering responsibility.

The facility includes a special beam line dedicated to irradiation studies of semiconductor components and devices. It consists of a vacuum chamber including component movement apparatus and the necessary diagnostic equipment required for the beam quality and intensity analysis.

The cyclotron is a versatile, sector-focused accelerator of beams from hydrogen to xenon equipped with three external ion sources: two electron cyclotron resonance (ECR) ion sources designed for high-charge-state heavy ions, and a multicusp ion source for intense beams of protons. The ECR's are especially valuable in the study of single event effects (SEE) in semiconductor devices. For heavy ions, the maximum energy attainable can be determined using the formula,

$$130 Q^2/M,$$

where Q is the ion charge state and M is the mass in Atomic Mass Units.

##### Test chamber

Irradiation of components is performed in a vacuum chamber with an inside diameter of 75 cm and a height of 81 cm.

The vacuum in the chamber is achieved after 15 minutes of pumping, and the inflation takes only a few minutes. The position of the components installed in the linear movement apparatus inside the chamber can be adjusted in the X, Y and Z directions. The possibility of rotation around the Y-axis is provided by a round table. The free movement area reserved for the components is 25 cm x 25 cm, which allows one to perform several consecutive irradiations for several different components without breaking the vacuum.

The assembly is equipped with a standard mounting fixture. The adapters required to accommodate the special board configurations and the vacuum feed-throughs can also be made in the laboratory's workshops. The chamber has an entrance door, which allows rapid changing of the circuit board or individual components.

A CCD camera with a magnifying telescope is located at the other end of the beam line to determine accurate positioning of the components. The coordinates are stored in the computer's memory allowing fast positioning of various targets during the test.

##### Beam quality control

For measuring beam uniformity at low intensity, a CsI(Tl) scintillator with a PIN-type photodiode readout is fixed in the mounting fixture. The uniformity is measured automatically before component irradiation and the results can be plotted immediately for more detailed analysis.

A set of four collimated PIN-CsI(Tl) detectors is located in front of the beam entrance. The detectors are operated with step motors and are located at 90 degrees with respect to each other. During the irradiation and uniformity scan they are set to the outer edge of the beam in order to monitor the stability of the homogeneity and flux.

Two beam wobblers and/or a 0.5 microns diffusion Gold foil can be used to achieve good beam homogeneity. The foil is placed 3 m in front of the chamber. The wobbler-coils vibrate the beam horizontally and vertically, the proper sweeping area being attained with the adjustable coil-currents.

##### Dosimetry

The flux and intensity dosimeter system contains a Faraday cup, several collimators, a scintillation counter and four PIN-CsI(Tl) detectors. Three collimators of different size and shape are placed 25 cm in front of the device under test. They can be used to limit the beam to the active area to be studied.

At low fluxes a plastic scintillator with a photomultiplier tube is used as an absolute particle counter. It is located behind the vacuum chamber and is used before the irradiation to normalize the count rates of the four PIN-CsI(Tl) detectors.

Ion	LET <sup>SRIM</sup> at surface [MeV.cm <sup>2</sup> .mg <sup>-1</sup> ]	Range [μm]	Beam energy [MeV]
<sup>20</sup> Ne <sup>6+</sup>	3.63	146	186
<sup>40</sup> Ar <sup>12+</sup>	10.2	118	372
<sup>56</sup> Fe <sup>15+</sup>	18.5	97	523
<sup>82</sup> Kr <sup>22+</sup>	32.1	94	768
<sup>131</sup> Xe <sup>35+</sup>	60.0	89	1217

SRIM-2003.26

**Table 1 – Ion beam setting**



## 5 Test Set-up

Test system Figure 2 shows the principle of the Heavy Ion test system.

The test system is based on a Virtex5 FPGA (Xilinx). It runs at 50 MHz. The test board has 168 I/Os which can be configured using several I/O standards.

The test board includes the voltage/current monitoring and the latch-up management of the DUT power supplies up to 24 independent channels.

The communication between the test chamber and the controlling computer is effectively done by a 100 Mbit/s Ethernet link which safely enables high speed data transfer.

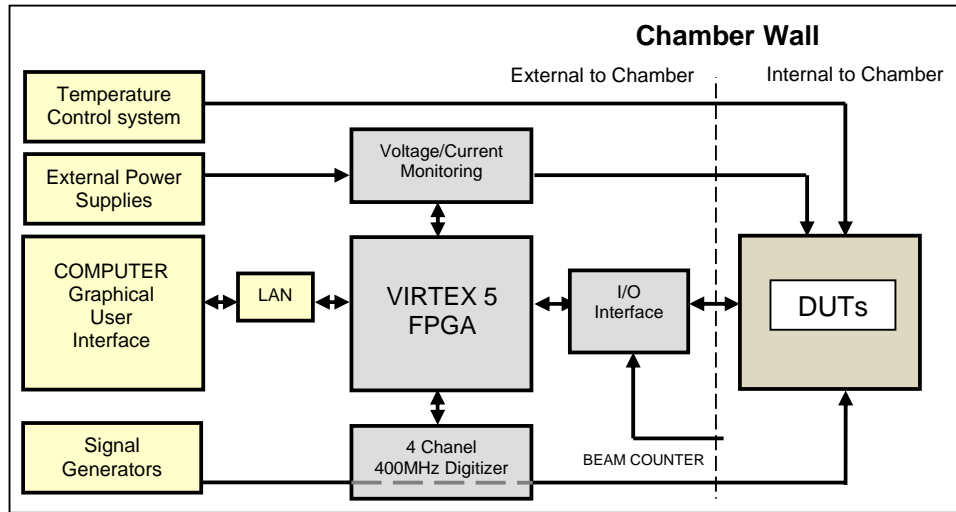


Figure 2 - Heavy ion test set-up

### 5.1 AD4096-2 test principle and conditions

In order to test the AD4096-2, one daughter board was designed. 2 DUTs were mounted on this board (Dut3 and Dut4 positions) and bias conditions are given in Figure 3 and Table 2. Table 3 gives the tester supply channel number used in the tester report.

DUT heating is performed with a thermal resistor in contact with DUTs backside using a thermal conductive paste. The temperature is regulated thanks to a thermocouple sensor put on top of the DUT package.

SEL event is detected when the supply current is over a configurable threshold (in the present case set to 100 mA for V+ and -100mA for V-) and processed (the power supplies are cut off during a configurable wait time, in the present case set to 1s).

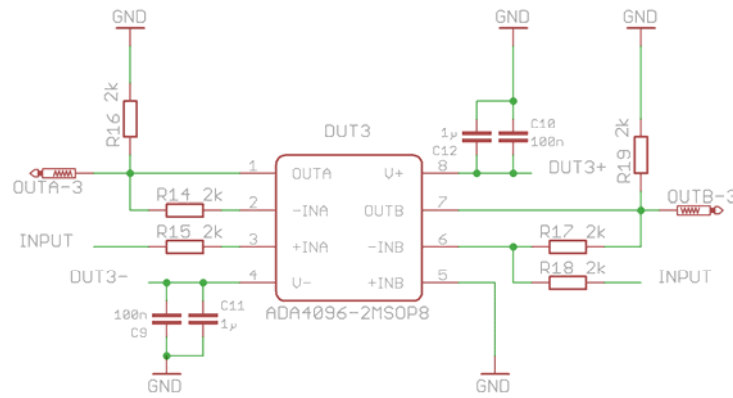
The tester monitors independently the 2 DUTs supplies at the same time. If an SEL is detected on 1 supply channel, the tester system records current/voltage on all channels.

Supply name	voltage
DUT_V+	+5V
DUT_V-	-5V
INPUT	Sine wave $\pm 1V$ at 100 KHz

Table 2 - Voltage bias conditions applied to the 2 DUTs

Supply name	Tester supply channel #
DUT3_V+	5
DUT3_V-	6
DUT4_V+	7
DUT4_V-	8
INPUT	17

Table 3 - Tester supply channel affection



Input: Sine wave  $\pm 1V$  at 100 KHz  
 Supply voltage:  $\pm 5.0V$   
 Load resistance = 2 k $\Omega$   
 Channel A gain set to +1  
 Channel B gain set to -1

Figure 3 – AD4096-2 bias condition

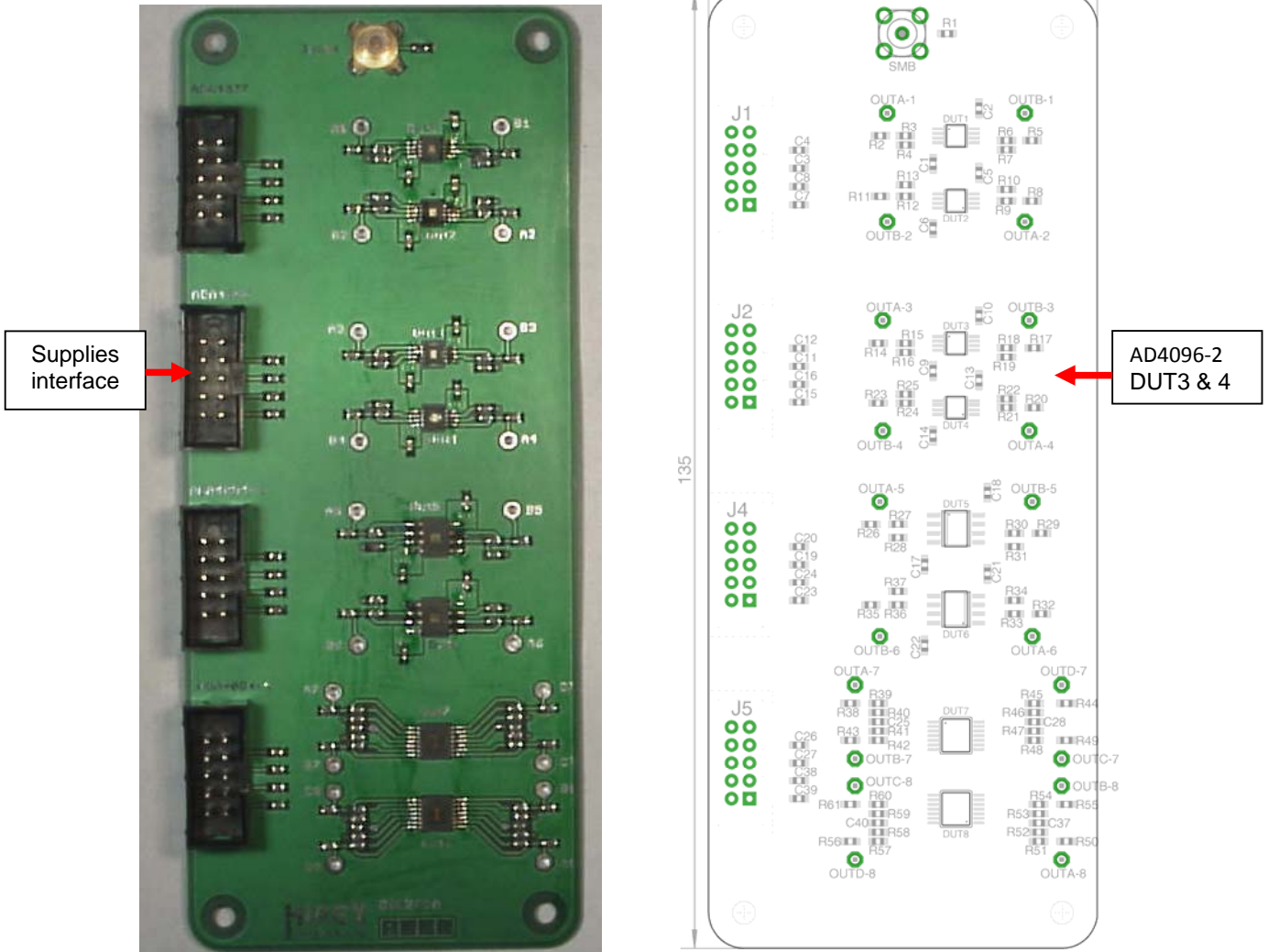


Figure 4 – Photo of test board

## 6 SEE test results

Runs performed are listed in Table 4.

3 boards have been tested with 2 AD4096-2 samples mounted on each board (Dut3 and Dut4 positions).

Upon test completion, all samples were found fully functional

### 6.1 SEL Results

No SEL neither step current increase has been observed when tested with V+/- set to 5V at any LET value at 125°C with all tested samples.

Facility	medium	hirex_run_number	Facility_run_number	board_id	dut_part_number under test	power_config	test_mode	temperature °C	ion	LET MeV/(mg/cm2)	roll	tilt	run_duration s	achieved fluence ions/cm2	eff. LET MeV/(mg/cm2)	dut_comment
RADEF	vacuum	3	3	2	3 & 4	+/-5V	SEL	105	Ar	10.2	0	0	278	1.00E+07	10.2	OK
RADEF	vacuum	6	6	2	3 & 4	+/-5V	SEL	125	Ar	10.2	0	0	333	1.00E+07	10.2	OK
RADEF	vacuum	56	56	3	3 & 4	+/-5V	SEL	125	Xe	60	0	0	497	1.00E+07	60	OK
RADEF	vacuum	57	57	3	3 & 4	+/-5V	SEL	125	Xe	60	0	31	237	1.00E+07	70	OK
RADEF	vacuum	58	58	3	3 & 4	+/-5V	SEL	125	Xe	60	0	42	257	1.00E+07	80.7	OK
RADEF	vacuum	62	62	4	3 & 4	+/-5V	SEL	125	Xe	60	0	42	269	1.00E+07	80.7	OK

**Table 4 - Run table for the AD4096-2, RADEF September 2015**

## 7 Glossary

Most of the definitions here below are from JEDEC standard JESD89A

DUT: Device under test.

Fluence (of particle radiation incident on a surface): The total amount of particle radiant energy incident on a surface in a given period of time, divided by the area of the surface.

In this document, Fluence is expressed in ions per cm<sup>2</sup>.

Flux: The time rate of flow of particle radiant energy incident on a surface, divided by the area of that surface.

In this document, Flux is expressed in ions per cm<sup>2</sup>\*s.

Single-Event Effect (SEE): Any measurable or observable change in state or performance of a microelectronic device, component, subsystem, or system (digital or analog) resulting from a single energetic particle strike. Single-event effects include single-event upset (SEU), multiple-bit upset (MBU), multiple-cell upset (MCU), single-event functional interrupt (SEFI), single-event latch-up (SEL).

Single-Event Transient (SET): A soft error caused by the transient signal induced by a single energetic particle strike.

Single-Event Latch-up (SEL): An abnormal high-current state in a device caused by the passage of a single energetic particle through sensitive regions of the device structure and resulting in the loss of device functionality.

SEL may cause permanent damage to the device. If the device is not permanently damaged, power cycling of the device (off and back on) is necessary to restore normal operation.

An example of SEL in a CMOS device is when the passage of a single particle induces the creation of parasitic bipolar (p-n-p-n) shorting of power to ground.

Single-Event Latch-up (SEL) cross-section: the number of events per unit fluence. For chip SEL cross-section, the dimensions are cm<sup>2</sup> per chip.

Error cross-section: the number of errors per unit fluence. For device error cross-section, the dimensions are cm<sup>2</sup> per device. For bit error cross-section, the dimensions are cm<sup>2</sup> per bit.

Tilt angle: tilt angle, rotation axis of the DUT board is perpendicular to the beam axis; roll angle, board rotation axis is parallel to the beam axis