24-Bit Single Channel Precision µModule Data Acquisition System

Preliminary Technical Data

ADAQ7768-1

FEATURES

- Highly integrated data acquisition solution
- 7 programmable gain options
  - G = 0.325, 0.65, 1.3, 2.6, 5.2, 10.4, 20.8 V/V
- Maximum input range of ±12.6V differential
- Maximum input common mode range of ±12V
- 4th order AAF with maximum flatness and linear phase
- Full aliasing protection with 100dB typical rejection
- Excellent device to device phase matching and drift
- Combined precision ac and dc performance
  - Total system dynamic range up to 130 dB
  - -115 dB typical THD at 0.325 V/V gain
  - 103 dB minimum DC CMRR at 20.8 V/V gain at 25°C
  - 25 pA input bias current
  - ±5 ppm typical INL
  - 5ppm/°C maximum gain drift
  - ±0.2° maximum device phase matching at 20kHz
- Programmable output data rate, filter type and latency
- Linear phase digital filter options:
  - Wideband low ripple FIR filter (110kHz max input BW)
  - Sinc5 FIR Filter (1MSPS output data rate at 208.9KHz BW)
  - Low latency Sinc5 and Sinc3 filter (4us min group delay)
- Integrated LDO
- Built-in supply decoupling capacitors
- Configuration through pin strapping or SPI interface
- Digital interface optimized for isolated applications
- Suite of diagnostic check mechanisms
- Operating temperature range: −40°C to +105°C
- Packaging: 12 mm × 6 mm 84-ball BGA with 0.8mm ball-pitch
  - 10x footprint reduction versus discrete solution

APPLICATIONS

- Universal input measurement platform
- Electrical Test and Measurement
- Sound and Vibration, Acoustic and Material Science R&D
- Control and Hardware in Loop Verification
- Condition monitoring for predictive maintenance
- Audio Test

FUNCTIONAL BLOCK DIAGRAM

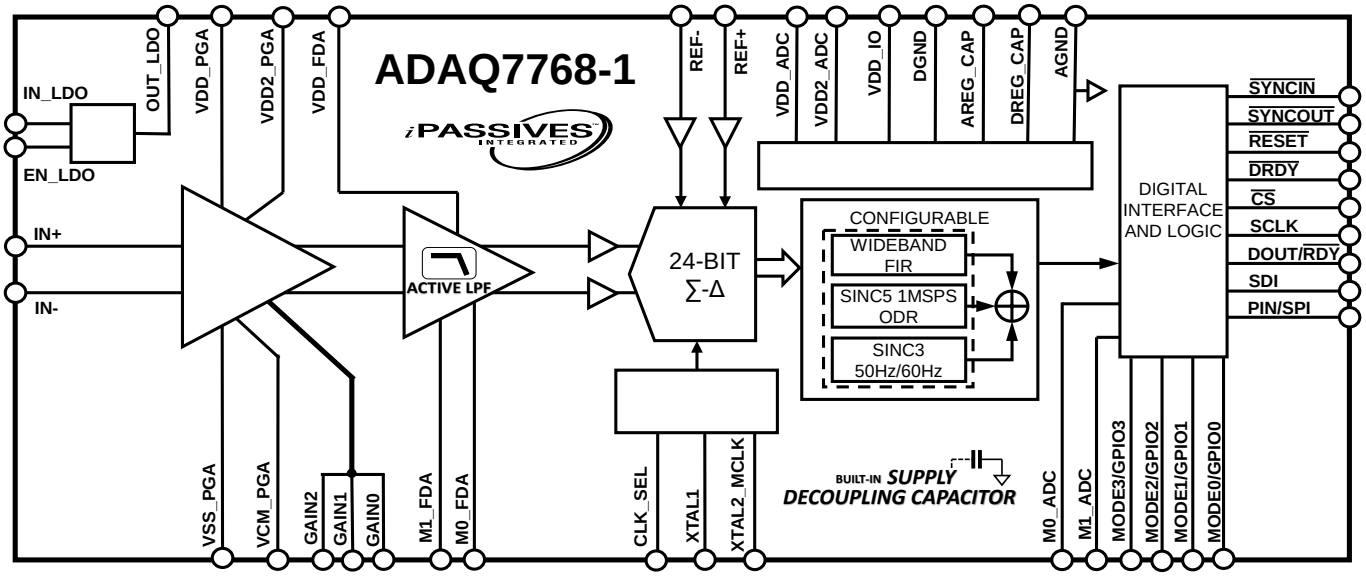

Figure 1. Block Diagram

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support
www.analog.com

TABLE OF CONTENTS

GENERAL DESCRIPTION

The ADAQ7768-1 is a 24-bit precision data acquisition (DAQ) µModule® system that encapsulates signal conditioning, conversion and processing blocks into one system in package (SiP) design that enables rapid development of highly compact, high performance precision DAQ systems.
The ADAQ7768-1 consists of:

- A low noise, low bias current, high bandwidth programmable gain instrumentation amplifier (PGIA) that is also capable of signal amplification and signal attenuation while maintaining high input impedance
- A fourth order, low noise, linear phase anti-aliasing filter
- A low noise, low distortion, high bandwidth ADC driver plus an optional linearity boost buffer
- A high-performance medium bandwidth 24-bit sigma delta ADC with programmable digital filter
- A low noise, low dropout linear regulator
- A reference buffers
- Critical passive components required for the signal chain

The ADAQ7768-1 supports fully differential input signal with a maximum range of ±12.6V. It has an input common mode voltage range of ±12V with excellent common mode rejection ratio (CMRR).

The input signal is fully buffered with very low input bias current of 2 pA typical. This allows easy input impedance matching and enables the ADAQ7768-1 to directly interface to sensors with high output impedance.

The seven pin-configurable gain settings offer additional system dynamic range and improved signal chain noise performance with input signals of lower amplitude.

A 4th order low-pass analog filter combined with the user programmable digital filter ensures the signal chain is fully protected against the high frequency noise and out of band tones presented at the input node from aliasing back into the band of interest. The analog low pass filter is carefully designed to achieve high phase linearity and maximum in-band magnitude response flatness. Constructed with Analog Devices's iPASSIVES™ technology, the resistor network used within the analog low-pass filter possess superior resistance matching in both absolute values and over temperature. As a result, the signal chain performance is maintained with minimum drift over temperature and the ADAQ7768-1 has an excellent device to device phase matching performance.
A high-performance ADC driver amplifier ensures the full settling of the ADC input at the maximum sampling rate. The driver circuit is designed to have minimum additive noise, error and distortion while maintaining stability. The fully differential architecture helps maximizing the signal chain dynamic range.

The analog to digital converter (ADC) inside the ADAQ7768-1 is a high performance, 24-bit precision, single channel Sigma-Delta converter with excellent AC performance and DC precision and the throughput rate of 256 kSPS from a 16.384 MHz MCLK.

An optional linearity boost buffer can further improve the signal chain linearity.

The ADAQ7768-1 is specified with the input reference voltage of 4.096V, but the device can support reference voltages ranging from VDD_ADC down to 1V.

The ADAQ7768-1 has two types of reference buffers. A pre-charge reference buffer to ease the reference input driving requirement or a full reference buffer to provide high impedance reference input. Both buffers are optional and can be turned off through register configuration.
ADAQ7768-1 supports three clock input types: crystal, CMOS or LVDS.

Three types of digital low pass filters are available on the ADAQ7768-1. The wideband filter offers a filter profile similar to an ideal brick wall filter, making it a great fit for doing frequency analysis. The Sinc5 filter offers a low latency path with a smooth step response while maintaining a good level of aliasing rejection. It also supports an output data rate up to 1.024 MHz from a 16.384 MHz MCLK, making the Sinc5 filter ideal for low latency data capturing and time domain analysis. The Sinc3 filter supports a wide decimation ratio and can produce output data rate down to 50 SPS from a 16.384 MHz MCLK. This combined with the simultaneous 50/60Hz rejection post filter makes Sinc3 filter especially useful for precision DC measurement. All the three digital filters on the ADAQ7768-1 are FIR filters with linear phase response. The bandwidth of the filters, which directly corresponds to the bandwidth of the DAQ signal chain are fully programable through register configuration.
The ADAQ7768-1 also supports two device configuration methods. The user has the option to choose to configure the device via register write through its SPI interface, or through a simple hardware pin strapping method to configure the device to operate under a number of pre-defined modes.
A single SPI interface supports both the register access and the sample data readback functions. The ADAQ7768-1 always acts as a SPI slave. Multiple interface modes are supported with a minimum of three IO channels required to communicate with the device.
ADAQ7768-1 also features a suite of internal diagnostic functions that can detect a broad range of errors during operation to help improving the system reliability.
The ADAQ7768-1 device has an operating temperature range of −40°C to +105°C and is available in a 12mm x 6mm, 84-ball BGA package with 0.8mm ball pitch. The ADAQ7768-1 utilizes only 75sq mm of board space, 10 times less than the discrete solution that utilizes 750sq mm.

SPECIFICATIONS

VDD_PGA = 15V, VSS_PGA = -15V, AGND = DGND = 0V, Input common mode voltage = 0V, IN_LDO = 5.1V to 5.5V, VDD_IO = 1.7 to 3.6 V, REF+ = 4.096V, REF-= 0V, MCLK = SCLK[1]=16.384 MHz 50:50 duty cycle, Fmod=MCLK/2, linearity boost buffer on, reference pre-charge buffers on, FDA = Low Power Mode, T_A = - 40°C to 105°C, unless otherwise noted. Typical values are at T_A = 25°C.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG INPUT CHARACTERISTICS					
Input Bias Current	T_A = 25°C		2	25	pA
	−40°C < T_A < +85°C			50	pA
Input Offset Current	T_A = 25°C		2	25	pA
	−40°C < T_A < +85°C			40	pA
Input Voltage Range	Individual pin, IN+ and IN-	-12		12	V
Input Common Mode Range[2]		-12		12	V
Analog Frontend Gain	Gain0 mode		0.325		V/V
	Gain1 mode		0.65		V/V
	Gain2 mode		1.3		V/V
	Gain3 mode		2.6		V/V
	Gain4 mode		5.2		V/V
	Gain5 mode		10.4		V/V
	Gain6 mode		20.8		V/V
Full-Scale Input Range	Differential IN+ to IN-				
	Gain0 mode		±12.603		V
	Gain1 mode		±6.302		V
	Gain2 mode		±3.151		V
	Gain3 mode		±1.575		V
	Gain4 mode		±0.788		V
	Gain5 mode		±0.394		V
	Gain6 mode		±0.197		V
Common-Mode Rejection DC	DC to 60Hz				
Gain0 mode	T_A = 25°C	80	95		dB
	−40°C < T_A < +105°C	75			
Gain1 mode	T_A = 25°C	83	95		dB
	−40°C < T_A < +105°C	80			
Gain2 mode	T_A = 25°C	82	95		dB
	−40°C < T_A < +105°C	80			
Gain3 mode	T_A = 25°C	88	101		dB
	−40°C < T_A < +105°C	86			
Gain4 mode	T_A = 25°C	94	107		dB
	−40°C < T_A < +105°C	92			
Gain5 mode	T_A = 25°C	100	113		dB
	−40°C < T_A < +105°C	98			
Gain6 mode	T_A = 25°C	103	119		dB
	−40°C < T_A < +105°C	98			

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Common-Mode Rejection AC	Referred to input (RTI), DC to 1kHz				
	Gain0 mode		63		dB
	Gain1 mode		65		dB
	Gain2 mode		78		dB
	Gain3 mode		78		dB
	Gain4 mode		90		dB
	Gain5 mode		90		dB
	Gain6 mode		113		dB
Input Current Noise					
Spectral Density	f = 10kHz		1		fA/√Hz
Peak to Peak	f = 0.1Hz to 10Hz		100		fA p-p
Input Resistance	Common mode and differential		5[12]		Ω
Input Capacitance			15		pF
OVERALL SYSTEM DC ACCURACY					
Gain Error	All gain modes, referred to input (RTI)		±0.005	±0.05	%
Gain Error Drift	RTI, Endpoint Method				
	Gain0 mode		±1	±5	ppm/°C
	Gain1 mode		±1	±5	ppm/°C
	Gain2 mode		±1	±5	ppm/°C
	Gain3 mode		±1	±5	ppm/°C
	Gain4 mode		±1	±5	ppm/°C
	Gain5 mode		±1	±5	ppm/°C
	Gain6 mode		±1	±5	ppm/°C
Offset Error	RTI				
	Gain0 mode		±1.13	±15.00	mV
	Gain1 mode		±0.66	±7.59	mV
	Gain2 mode		±0.42	±3.89	mV
	Gain3 mode		±0.30	±2.03	mV
	Gain4 mode		±0.24	±1.11	mV
	Gain5 mode		±0.21	±0.64	mV
	Gain6 mode		±0.19	±0.41	mV
Offset Error Drift[3]	RTI, Box Method				
	Gain0 mode		±17.0	±42	uV/°C
	Gain1 mode		±8.6	±13	uV/°C
	Gain2 mode		±6.0	±13	uV/°C
	Gain3 mode		±5.8	±13	uV/°C
	Gain4 mode		±3.7	±9	uV/°C
	Gain5 mode		±3.0	±9	uV/°C
	Gain6 mode		±1.9	±5	uV/°C
Integral Nonlinearity (INL)	Endpoint method				
Gain0 mode	T_A = 25°C		±5		ppm of FSR
	−40°C < T_A < +85°C[3]			±16	ppm of FSR
	−40°C < T_A < +105°C			±TBD	ppm of FSR
Gain1 mode	T_A = 25°C		±5		ppm of FSR
	−40°C < T_A < +85°C[3]			±11	ppm of FSR
	−40°C < T_A < +105°C			±TBD	ppm of FSR
Gain2 mode	T_A = 25°C		±5		ppm of FSR
	−40°C < T_A < +85°C[3]			±7	ppm of FSR
	−40°C < T_A < +105°C			±TBD	ppm of FSR

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Gain3 mode	T_A = 25°C		±5		ppm of FSR
	−40°C < T_A < +85°C[3]			±11	ppm of FSR
	−40°C < T_A < +105°C			±TBD	ppm of FSR
Gain4 mode	T_A = 25°C		±5		ppm of FSR
	−40°C < T_A < +85°C[3]			±11	ppm of FSR
	−40°C < T_A < +105°C			±TBD	ppm of FSR
Gain5 mode	T_A = 25°C		±5		ppm of FSR
	−40°C < T_A < +85°C[3]			±30	ppm of FSR
	−40°C < T_A < +105°C			±TBD	ppm of FSR
Gain6 mode	T_A = 25°C		±5		ppm of FSR
	−40°C < T_A < +85°C[3]			±32	ppm of FSR
	−40°C < T_A < +105°C			±TBD	ppm of FSR
Low Frequency Noise	ODR= 50 SPS, shorted input, Sinc3 filter, RTI				
	Gain0 mode		1.5		uV rms
	Gain1 mode		0.89		uV rms
	Gain2 mode		0.54		uV rms
	Gain3 mode		0.33		uV rms
	Gain4 mode		0.25		uV rms
	Gain5 mode		0.22		uV rms
	Gain6 mode		0.21		uV rms
OVERALL SYSTEM AC PERFORMANCE	Wideband Low ripple FIR filter, ODR= 256 kSPS, decimation by 32				
DR[4]	shorted input				
	Gain 0 mode	TBD	106.4		dB
	Gain1 mode	TBD	106.1		dB
	Gain2 mode	TBD	105.4		dB
	Gain3 mode	TBD	104.6		dB
	Gain4 mode	TBD	102.6		dB
	Gain5 mode	TBD	98.9		dB
	Gain 6 mode	TBD	93.8		dB
	Total System	TBD	130		dB
Noise Spectral Density	Refer to input, shorted input, at 1kHz				
	Gain0 mode		128.1		nV/√Hz
	Gain1 mode		66.3		nV/√Hz
	Gain2 mode		36.0		nV/√Hz
	Gain3 mode		19.7		nV/√Hz
	Gain4 mode		12.3		nV/√Hz
	Gain5 mode		9.4		nV/√Hz
	Gain 6 mode		8.4		nV/√Hz
Integrated Voltage Noise	Refer to input, shorted input, at 1kHz		42.7		uV rms
	Gain0 mode		22.1		uV rms
	Gain1 mode		12		uV rms
	Gain2 mode		6.5		uV rms
	Gain3 mode		4.1		uV rms
	Gain4 mode		3.1		uV rms
	Gain5 mode		2.8		uV rms
	Gain6 mode				

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SNR	-0.5dBFS, sine input, 1kHz input Tone				
	Gain0 mode	TBD	105.3		dB
	Gain1 mode	TBD	105		dB
	Gain2 mode	TBD	104.4		dB
	Gain3 mode	TBD	103.7		dB
	Gain4 mode	TBD	101.9		dB
	Gain5 mode	TBD	98.3		dB
	Gain6 mode	TBD	93.3		dB
Total Harmonic Distortion (THD)	-0.5dBFS, sine input, 1KHz input Tone, FDA = Full Power Mode				
Gain0 mode	T_A = 25°C			TBD	dB
	−40°C < T_A < +105°C		-115		dB
Gain1 mode	T_A = 25°C			TBD	dB
	−40°C < T_A < +105°C		-115		dB
Gain2 mode	T_A = 25°C			TBD	dB
	−40°C < T_A < +105°C		-115		dB
Gain3 mode	T_A = 25°C			TBD	dB
	−40°C < T_A < +105°C		-115		dB
Gain4 mode	T_A = 25°C			TBD	dB
	−40°C < T_A < +105°C		-115		dB
Gain5 mode	T_A = 25°C			TBD	dB
	−40°C < T_A < +105°C		-114.5		dB
Gain6 mode	T_A = 25°C			TBD	dB
	−40°C < T_A < +105°C		-112.5		dB
SINAD	1kHz, -0.5dBFS, sine input				
	Gain0 mode	TBD	104.9		dB
	Gain1 mode	TBD	104.6		dB
	Gain2 mode	TBD	104		dB
	Gain3 mode	TBD	103.4		dB
	Gain4 mode	TBD	101.7		dB
	Gain5 mode	TBD	98.2		dB
	Gain6 mode	TBD	93.2		dB
SFDR	All gain modes		TBD		dBc
Intermodulation Distortion (IMD)	f_{IN_A} = 19.5kHz, f_{IN_B} = 20.5kHz,				
	Gain0 mode second order		TBD		dB
	Gain0 mode third order		TBD		dB
	Gain2 mode second order		TBD		dB
	Gain2 mode third order		TBD		dB
	Gain6 mode second order		TBD		dB
	Gain6 mode third order		TBD		dB
Analog Group Delay	f_{IN} = 20 kHz, Gain 0 mode		TBD	TBD	us
	f_{IN} = 20 kHz, Gain 6 mode		TBD	TBD	us
Phase Angle Matching Over Gain	Sine Wave, f_{IN} = 20 kHz, Single device, normalized to Gain0				
	Gain0 mode				Degrees
	Gain1 mode			TBD	Degrees
	Gain2 mode			TBD	Degrees
	Gain3 mode			TBD	Degrees
	Gain4 mode			TBD	Degrees
	Gain5 mode			TBD	Degrees
	Gain6 mode			TBD	Degrees

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Phase Angle Drift	f_{IN} = 20 kHz				
	Gain 0 Mode			±TBA	m°/°C
	Gain1 mode			±TBA	m°/°C
	Gain2 mode			±TBA	m°/°C
	Gain3 mode			±TBA	m°/°C
	Gain4 mode			±TBA	m°/°C
	Gain5 mode			±TBA	m°/°C
	Gain6 mode			±TBA	m°/°C
Device to Device Phase Angle Matching	f_{IN} = 20 kHz,				
	Gain 0 Mode	-0.2	TBD	0.2	Degrees
	Gain1 mode		TBD		Degrees
	Gain2 mode		TBD		Degrees
	Gain3 mode		TBD		Degrees
	Gain4 mode		TBD		Degrees
	Gain5 mode		TBD		Degrees
	Gain6 mode		TBD		Degrees
Device to Device Phase Angle Match Drift	f_{IN} = 20 kHz				
	Gain 0 Mode			±TBA	m°/°C
	Gain1 mode			±TBA	m/°C
	Gain2 mode			±TBA	m/°C
	Gain3 mode			±TBA	m/°C
	Gain4 mode			±TBA	m/°C
	Gain5 mode			±TBA	m/°C
	Gain6 mode			±TBA	m/°C
Magnitude Flatness	f_{IN} = 20 kHz		-2.3		mdB
	f_{IN} = 100 kHz		-20		mdB
Alias Rejection	All Gain Mode, -20dBFS input signal				
	at 16.385MHz		100		dB
	at 13.107MHz		100		dB
ADC SPEED AND PERFORMANCE					
Output Data Rate (ODR)[5]					
	Wideband Low Rippler FIR	1		256	kSPS
	Sinc5	1		1024	kSPS
	Sinc3	0.0125		256	kSPS
No Missing codes	Sinc3 Filter, Decimation ratio ≥32	24			Bits
	Sinc5 Filter, Decimation ratio ≥32	24			Bits
	Wideband Low Rippler FIR filter, Decimation ratio ≥64	24			Bits
Data Output Coding		Twos complement, MSB first			
REFERENCE INPUT CHARACTERISTICS					
REFIN voltage	REFIN = (REF+) - (REF-)	1		VDD_ADC-AGND	V
Absolute REFIN voltage Limit	Reference unbuffered	AGND -0.05		VDD_ADC +0.05	V
	Reference buffer on	AGND		VDD_ADC	V
	Reference pre-charge buffer on	AGND		VDD_ADC	V
Average REFIN current	Reference unbuffered		±80		uA/V
	Reference buffer on		±300		nA
	Reference pre-charge buffer on		±20		uA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Average REFIN current drift	Reference unbuffered		±1.7		nA/V/C
	Reference buffer on		125		nA/C
	Reference pre-charge buffer on		4		nA/C
Common mode rejection	Up to 10 MHz		100		dB
DIGITAL FILTER RESPONSE					
Wideband Low Ripple FIR Filter					
Decimation Rate	6 selectable decimation rates	32		1024	
Output Data Rate				256	kSPS
Group Delay	Latency		34/ODR		Sec
Settling time	Complete settling		68/ODR		Sec
Pass band ripple				±0.005	dB
Pass Band	-0.005dB		0.4xODR		Hz
	-0.1dB pass band		0.409xODR		
	-3dB Bandwidth		0.433xODR		Hz
Stop Band frequency	Attenuation >105dB		0.499xODR		Hz
Stop-Band Attenuation		105			dB
Sinc5					
Decimation Rate	8 selectable decimation rates	8		1024	
Output Data Rate				1.024	MSPS
Group Delay	Latency		< 3/ODR		Sec
Settling time	Complete settling		< 6/ODR		Sec
Pass Band	-0.1dB Bandwidth		0.0376 xODR		Hz
	-3dB Bandwidth		0.204 xODR		Hz
Sinc3 Filter					
Decimation Rate	1024 decimation rates	32		185,280	
Output Data Rate				256	kSPS
Group Delay	Latency		TBD		Sec
Settling time	Complete settling to reject 50Hz		60		ms
Pass Band	-0.1dB Bandwidth		0.0483 x ODR		Hz
	-3dB Bandwidth		0.2617 x ODR		Hz
CLOCK					
External Clock MCLK		0.6	16.384	17	MHz
Internal Clock MCLK			16.384		MHz
Input High Voltage	See to logic input parameter				
Duty cycle	16.384 Mhz MCLK	25:75	50:50	25:75	%
MCLK Logic Low Pulse Width		16			ns
MCLK Logic High Pulse Width		16			ns
Crystal Frequency		8	16	17	MHz
Crystal Start-Up Time	Clock output valid		2		ms
ADC RESET					
ADC Start-Up Time after Reset	Time to first DRDY, Decimate x32		1.58	TBC	ms
Minimum RESET low pulse width		2 × tMCLK			
LOGIC INPUTS	Applies to all logic inputs unless specified otherwise, voltage referenced to AGND				
Input High Voltage, V_{INH}	1.7 V ≤ VDD_IO ≤ 1.9 V	0.65 × VDD_IO			V
	2.22 V ≤ VDD_IO ≤ 3.6 V	0.65 × VDD_IO			V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Input Low Voltage, V_{INL}	1.7 V ≤ VDD_IO ≤ 1.9 V			0.35 × VDD_IO	V
	2.22 V ≤ VDD_IO ≤ 3.6 V			0.7	V
Hysteresis	2.22 V ≤ VDD_IO ≤ 3.6 V	0.08		0.25	V
	1.7 V ≤ VDD_IO < 1.9 V	0.04		0.2	V
Leakage Current	Excluding $\overline{\text{RESET}}$ pin	−10	0.05	+10	µA
	$\overline{\text{RESET}}$ pin	TBD		TBD	µA
GAIN0, GAIN1, GAIN2	voltage referenced to AGND				
Input High Voltage		1.4			V
Input Low Voltage				0.6	V
Input Current	Gain0, Gain1, Gain2 = 5V		8	12	µA
M0_FDA, M1_FDA	voltage referenced to AGND				
Input High Voltage		TBD			V
Input Low Voltage				TBD	V
Input Current	TBD		TBD		nA
	TBD		TBD		nA
EN_LDO	voltage referenced to AGND				
Input High Voltage	5.1 V ≤ VIN ≤ 5.5 V	TBD			V
Input Low Voltage	5.1 V ≤ VIN ≤ 5.5 V			TBD	V
Input Current	EN = VIN or GND		0.1		uA
LOGIC OUTPUTS					
Output High Voltage	2.2 V ≤ VDD_IO < 3.6 V, I_{SOURCE} = 500 µA, LV_BOOST_off	0.8 × VDD_IO			V
	1.7 V ≤ VDD_IO < 1.9 V, I_{SOURCE} = 200 µA, LV_BOOST_on	0.8 × VDD_IO			V
Output Low Voltage	2.2 V ≤ VDD_IO < 3.6 V, I_{SINK} = 1 mA, LV_BOOST_off			0.4	V
	1.7 V ≤ VDD_IO < 1.9 V, I_{SINK} = 400 µA, LV_BOOST_on			0.4	V
Leakage Current	Floating state	−10		+10	µA
Output Capacitance	Floating state		10		pF
LDO CHARACTERISTIC					
Input Voltage Range		5.1		5.5	V
IN_LDO Supply Current	LDOOUT load current = 20mA		80		µA
OUT_LDO Voltage		4.9	5	5.075	V
Load Regulation	IOUT = 1 mA to 20 mA		0.0005		%/mA
Dropout Voltage[6]	IOUT = 20 mA		3		mV
Start-Up Time[7]			350		µs
Current Limit Threshold			500		mA
Thermal Shutdown Threshold			150		°C
Thermal Shutdown Hysteresis			15		°C
POWER REQUIREMENTS					
VDD_PGA	Referenced to AGND	4.5		18	V
VSS_PGA	Referenced to AGND	-18		-4.5	V
VDD2_PGA	Referenced to AGND	4.5		5.5	V
VDD_FDA	Referenced to AGND	4.5	5	5.5	V
VDD_ADC	Referenced to AGND	4.5	5	5.5	V
VDD2_ADC	Referenced to AGND	2	2.5	5.5	V
VDD_IO	Referenced to AGND	1.7	1.8	3.6	V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY REJECTION	Referred to output (RTO), DC to 100Hz, V_{STEP}=0.4 Vp-p				
VDD_PGA and VSS_PGA	Gain0 mode		112		dB
	Gain6 mode		130		dB
VDD2_PGA			124		dB
VDD_FDA			116		dB
VDD_ADC			105		dB
VDD2_ADC			124		dB
VDD_IO			104		dB
LDO			124		dB
POWER SUPPLY CURRENT					
VDD_PGA	IN+ = IN- = AGND		3.14		mA
	Full scale 1kHz sine input with common mode = AGND, Gain0 mode		6.02		mA
	Full scale 1kHz sine input with common mode = AGND, Gain6 mode		3.76		mA
	Full scale DC input with common mode = AGND, Gain0 mode		8.18		mA
	Full scale DC input with common mode = AGND, Gain6 mode		4.33		mA
	Standby		230		uA
VDD2_PGA	IN+ = IN- = AGND		0.66		mA
	Full scale 1kHz sine input with common mode = AGND, Gain0 mode		2.09		mA
	Full scale 1kHz sine input with common mode = AGND, Gain6 mode		1.37		mA
	Full scale DC input with common mode = AGND, Gain0 mode		3.56		mA
	Full scale DC input with common mode = AGND, Gain6 mode		2.19		mA
	Standby		1		uA
VSS_PGA	IN+ = IN- = AGND		-6.31		mA
	Full scale 1kHz sine input with common mode = AGND, Gain0 mode		-10.61		mA
	Full scale 1kHz sine input with common mode = AGND, Gain6 mode		-7.63		mA
	Full scale DC input with common mode = AGND, Gain0 mode		-14.24		mA
	Full scale DC input with common mode = AGND, Gain6 mode		-9.024		mA
	Standby		-230		uA
VDD_FDA	Full scale 1kHz sine input with common mode = AGND		3.97		mA
	Full scale DC input with common mode = AGND,		4.37		mA
	IN+ = IN- = AGND		3.74		mA
	Standby		70		uA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
VDD_ADC	Linearity boost buffer on, reference pre-charge buffer on		6.8		mA
	Linearity boost buffer off, reference pre-charge buffers off		2.43		mA
	Standby		210		uA
VDD2_ADC			4.7		mA
	Standby		25		uA
VDD_IO					
Sinc3 filter			2.98		mA
Sinc5 filter			3.32		mA
Wideband filter			9.1		mA
Standby			370		uA
POWER DISSIPATION	External CMOS MCLK, VDD2_ADC=VDD_IO=3.3V				
Full Operating Mode					
Sinc3 Filter	IN+ = IN- = AGND		223		mW
Sinc5 Filter	IN+ = IN- = AGND		224		mW
Wideband Filter	IN+ = IN- = AGND		243	TBA	mW
	Full scale 1kHz sine input with common mode = AGND, Gain0 mode		359	TBA	mW
	Full scale 1kHz sine input with common mode = AGND, Gain6 mode		277	TBA	mW
	Full scale DC input with common mode = AGND, Gain0 mode		455	TBA	mW
	Full scale DC input with common mode = AGND, Gain6 mode		312	TBA	mW
Standby Mode			0.96	TBA	mW

[1] See section MCLK and SCLK Alignment for more information about suggested MLCK and SLK alignment.
[2] The input range is also limited by internal node and is gain dependent. See Common Mode Input Range section for more details.
[3] The preliminary max data came from 3 units tested across temperature on bench
[4] See section Noise Performance and Resolution for Dynamic Rage performance across decimation factor and throughput.
[5] Output data rate (ODR) ranges refer to the programmable decimation rates available on the ADA77680 for a fixed MCLK of 13.1MHz. Varying MCLK allows users a wider variation of ODR. See section ADC Speed and Performance for suggestion on the ODR speed to achieve optimum performance
[6] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. This applies only for output voltages greater than 2.3 V.
[7] Start-up time is defined as the time between the rising edge of EN to VOUT being at 90% of its nominal value.

TIMING SPECIFICATIONS

VDD_ADC = 4.5 V to 5.5 V, VDD2_ADC = 2.0 V to 5.5 V, VDD_IO = 2.2 V to 3.6 V, AGND = DGND = 0 V, Input Logic 0 = 0 V, Input Logic 1 = VDD_IO, and load capacitance (C_{LOAD}) = 20 pF, LV_BOOST bit (Bit 7, INTERFACE_FORMAT register (Register 0x14) disabled, unless otherwise noted.

These specifications were sample tested during the initial release to ensure compliance. All input signals are specified with $t_R = t_F = 5$ ns (10% to 90% of VDD_IO and timed from a voltage level of VDD_IO/2). See Figure 2 to Figure 8 for the timing diagrams.

These specifications are not production tested, but are supported by characterization data at initial product release.

Table 2.

Parameter	Description	Test Conditions/Comments	Min	Typ	Max	Unit
MCLK	Frequency			16.384	17	MHz
t_{MCLK_HIGH}	MCLK high time		16			ns
t_{MCLK_LOW}	MCLK low time		16			ns
f_{MOD}	Modulator frequency	MCLK_DIV[1:0]=11		MCLK/2		Hz
		MCLK_DIV[1:0]=10		MCLK/4		Hz
		MCLK_DIV[1:0]=01		MCLK/8		Hz
		MCLK_DIV[1:0]=00		MCLK/16		Hz
$t_{\overline{DRDY}}$	Conversion period	Rising $\overline{DRDY}$ edge to next rising $\overline{DRDY}$ edge, continuous conversion mode		F_{MOD}/DEC_RATE		Hz
$t_{\overline{DRDY}\_HIGH}$	$\overline{DRDY}$ high time	t_{MCLK} = 1/MCLK	t_{MCLK} − 5	1 × t_{MCLK}		ns
$t_{MCLK\_\overline{DRDY}}$	MCLK to $\overline{DRDY}$	Rising MCLK edge to $\overline{DRDY}$ rising edge	10	13	18	ns
$t_{MCLK\_\overline{RDY}}$	MCLK to $\overline{RDY}$ indicator on the DOUT/$\overline{RDY}$ pin	Rising MCLK edge to $\overline{RDY}$ falling edge	10	13	18	ns
t_{UPDATE}	ADC data update	Time prior to $\overline{DRDY}$ rising edge where the ADC conversion register updates, single conversion read		1 × t_{MCLK}		ns
$t_{\overline{START}}$	$\overline{START}$ pulse width		1.5 × t_{MCLK}			ns
$t_{MCLK\_\overline{SYNC\_OUT}}$	MCLK to $\overline{SYNC\_OUT}$	Falling MCLK to falling $\overline{SYNC\_OUT}$			t_{MCLK} + 16	ns
t_{SCLK}	SCLK period		50			ns
t_1	$\overline{CS}$ falling to SCLK falling		0			ns
t_2	$\overline{CS}$ falling to data output enable				6	ns
t_3	SCLK falling edge to data output valid			10	15	ns
t_4	Data output hold time after SCLK falling edge		4			ns
t_5	SDI setup time before SCLK rising edge		3			ns
t_6	SDI hold time after SCLK rising edge		8			ns
t_7	$\overline{CS}$ high time	4-wire interface	10			ns
t_8	SCLK high time		20			ns
t_9	SCLK low time		20			ns
t_{10}	SCLK rising edge to $\overline{DRDY}$ high	Single conversion read only; time from last SCLK rising edge to $\overline{DRDY}$ high	1 × t_{MCLK}			ns
t_{11}	SCLK rising edge to $\overline{CS}$ rising edge		6			ns
t_{12}	$\overline{CS}$ rising edge to DOUT/$\overline{RDY}$ output disable		4		7	ns
t_{13}	DOUT/$\overline{RDY}$ indicator pulse width	In continuous read mode with $\overline{RDY}$ on, DOUT enabled, with SCLK idling high		1 × t_{MCLK}		ns
t_{14}	$\overline{CS}$ falling edge to SCLK rising edge		2			ns
t_{15}	$\overline{SYNC\_IN}$ setup time before MCLK rising edge		2			ns
t_{16}	$\overline{SYNC\_IN}$ pulse width		1.5 × t_{MCLK}			ns
t_{17}	SCLK rising edge to $\overline{RDY}$ indicator rising edge	In continuous read mode with $\overline{RDY}$ enabled on DOUT	1			ns
t_{18}	$\overline{DRDY}$ rising edge to SCLK falling edge	In continuous read mode with $\overline{RDY}$ enabled on DOUT	8			ns

1.8 V TIMING SPECIFICATIONS

VDD_ADC = 4.5 V to 5.5 V, VDD2_ADC = 2 V to 5.5 V, VDD_IO = 1.7 V to 1.9 V, AGND = DGND = 0 V, Input Logic 0 = 0 V, Input Logic 1 = VDD_IO, and C_{LOAD} = 20 pF, LV_BOOST bit (Bit 7, INTERFACE_FORMAT register (Register 0x14) enabled, unless otherwise noted.

These specifications were sample tested during the initial release to ensure compliance. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of VDD_IO and timed from a voltage level of VDD_IO/2. See Figure 2 to Figure 8 for the timing diagrams.

These specifications are not production tested but are supported by characterization data at initial product release.

Table 3.

Parameter	Description	Test Conditions/Comments	Min	Typ	Max	Unit
MCLK	Frequency			16.384	17	MHz
t_{MCLK_HIGH}	MCLK high time		16			ns
t_{MCLK_LOW}	MCLK low time		16			ns
f_{MOD}	Modulator frequency	MCLK_DIV[1:0]=11		MCLK/2		Hz
		MCLK_DIV[1:0]=10		MCLK/4		Hz
		MCLK_DIV[1:0]=01		MCLK/8		Hz
		MCLK_DIV[1:0]=00		MCLK/16		Hz
$t_{\overline{DRDY}}$	Conversion period	Rising $\overline{DRDY}$ edge to next rising $\overline{DRDY}$ edge, continuous conversion mode		f_{MOD}/DEC_RATE		Hz
$t_{\overline{DRDY}\_HIGH}$	$\overline{DRDY}$ high time	t_{MCLK} = 1/MCLK	$t_{MCLK} - 5$	$1 \times t_{MCLK}$		ns
$t_{MCLK\_\overline{DRDY}}$	MCLK to $\overline{DRDY}$	Rising MCLK edge to $\overline{DRDY}$ rising edge	13	19	25	ns
$t_{MCLK\_\overline{RDY}}$	MCLK to $\overline{RDY}$ indicator on the DOUT/$\overline{RDY}$ pin	Rising MCLK edge to $\overline{RDY}$ falling edge	13	19	25	ns
t_{UPDATE}	ADC data update	Time prior to $\overline{DRDY}$ rising edge where the ADC conversion register updates		$1 \times t_{MCLK}$		ns
$t_{\overline{START}}$	$\overline{START}$ pulse width		$1.5 \times t_{MCLK}$			ns
$t_{MCLK\_\overline{SYNC\_OUT}}$	MCLK to $\overline{SYNC\_OUT}$	Falling MCLK to falling $\overline{SYNC\_OUT}$, see the Synchronization of Multiple ADAQ7768-1 Devices section			$t_{MCLK} + 31$	ns
t_{SCLK}	SCLK period		50			ns
t_1	$\overline{CS}$ falling to SCLK falling		0			ns
t_2	$\overline{CS}$ falling to data output enable				11	ns
t_3	SCLK falling edge to data output valid			14	19	ns
t_4	Data output hold time after SCLK falling edge		7			ns
t_5	SDI setup time before SCLK rising edge		3			ns
t_6	SDI hold time after SCLK rising edge		8			ns
t_7	$\overline{CS}$ high time	4-wire interface	10			ns
t_8	SCLK high time		23			ns
t_9	SCLK low time		23			ns
t_{10}	SCLK rising edge to $\overline{DRDY}$ high	Time from last SCLK rising edge to DRDY high; if this is exceeded, conversion N + 1 is missed; single conversion read	$1 \times t_{MCLK}$			ns
t_{11}	SCLK rising edge to $\overline{CS}$ rising edge		6			ns
t_{12}	$\overline{CS}$ rising edge to DOUT/$\overline{RDY}$ output disable		7.5		13	ns

Parameter	Description	Test Conditions/Comments	Min	Typ	Max	Unit
t_{13}	DOUT/$\overline{RDY}$ indicator pulse width	In continuous read mode with $\overline{RDY}$ on, DOUT enabled, with SCLK idling high		$1 \times t_{MCLK}$		ns
t_{14}	$\overline{CS}$ falling edge to SCLK rising edge		2.5			ns
t_{15}	$\overline{SYNC\_IN}$ setup time before MCLK rising edge		2			ns
t_{16}	$\overline{SYNC\_IN}$ pulse width		$1.5 \times t_{MCLK}$			ns
t_{17}	SCLK rising edge to $\overline{RDY}$ indicator rising edge	In continuous read mode with $\overline{RDY}$ on, DOUT enabled	5.5			ns
t_{18}	$\overline{DRDY}$ rising edge to SCLK falling edge	In continuous read mode with $\overline{RDY}$ on, DOUT enabled	15			ns

Timing Diagrams

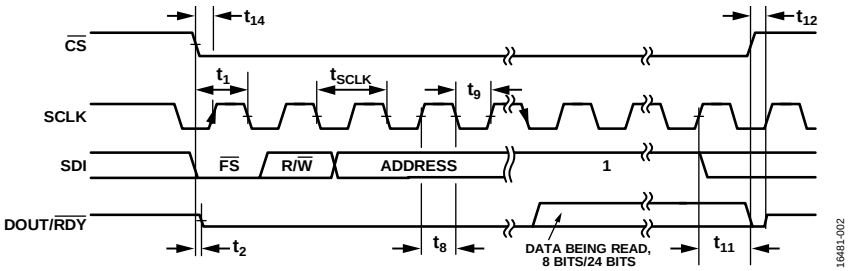

Figure 2. SPI Read Timing Diagram

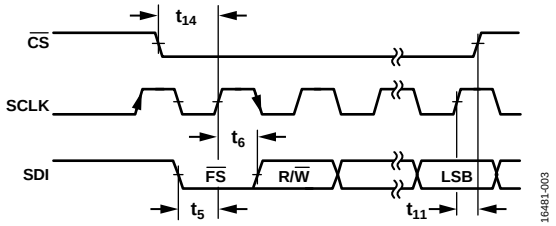

Figure 3. SPI Write Timing Diagram

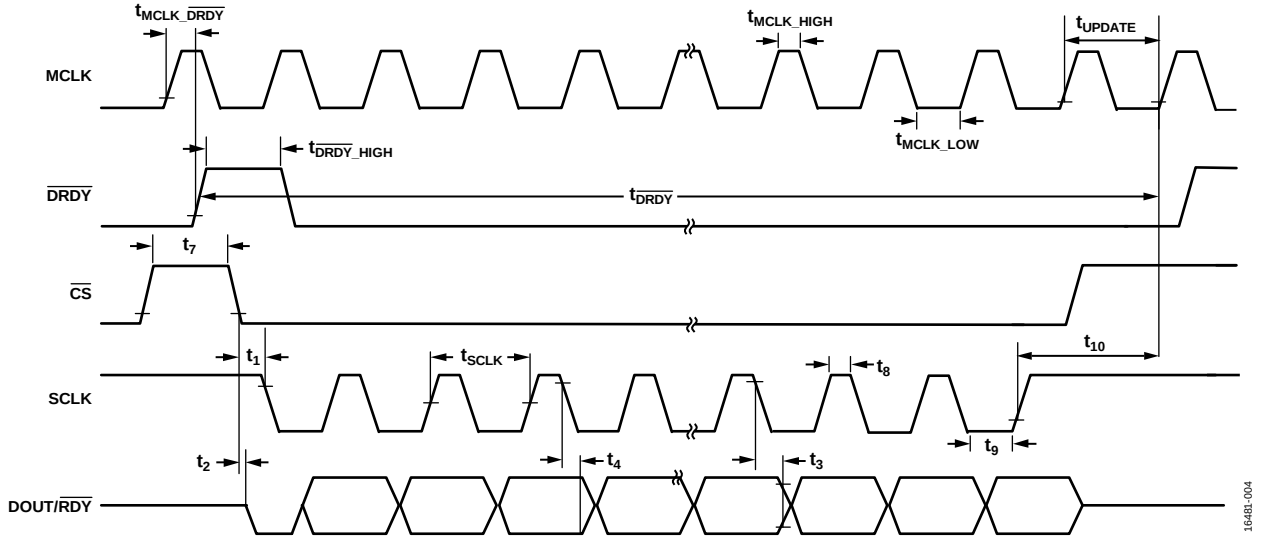

Figure 4. Reading Conversion Result in Continuous Conversion Mode ($\overline{CS}$ Toggling)

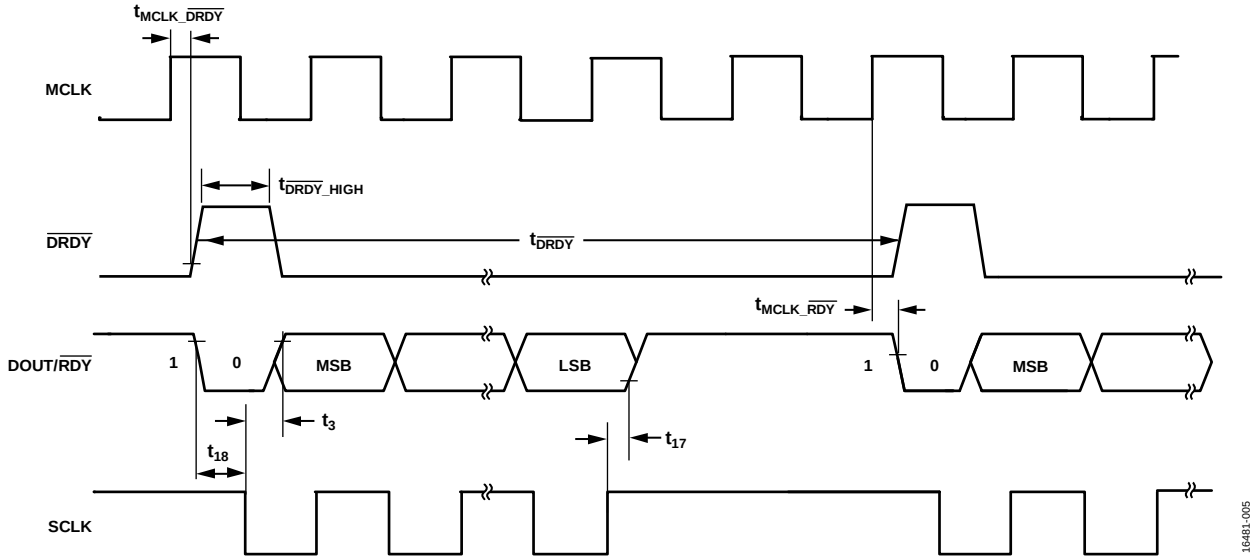

Figure 5. Reading Conversion Result in Continuous Conversion Mode, Continuous Read Mode with $\overline{RDY}$ Enabled ($\overline{CS}$ Held Low)

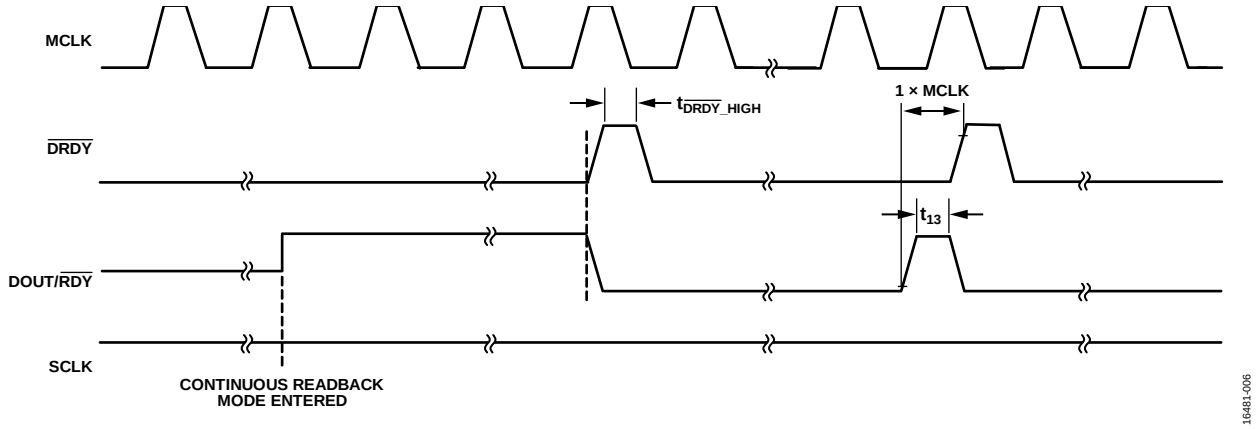

Figure 6. DOUT/$\overline{RDY}$ Behavior Without SCLK Applied

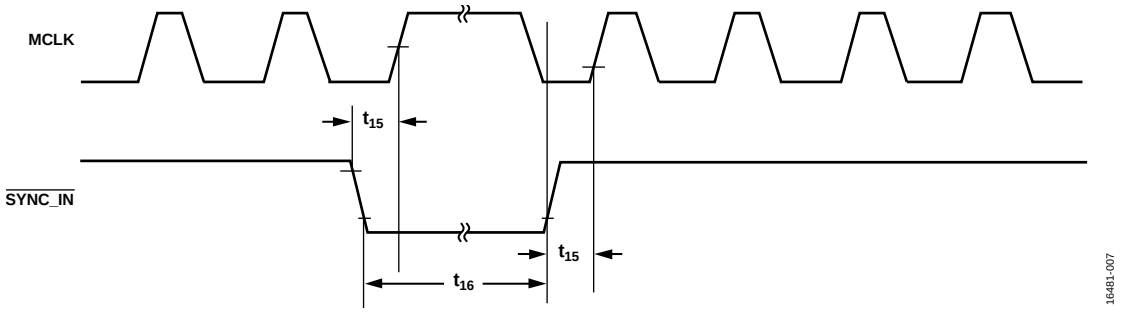

Figure 7. Synchronous $\overline{SYNC\_IN}$ Pulse

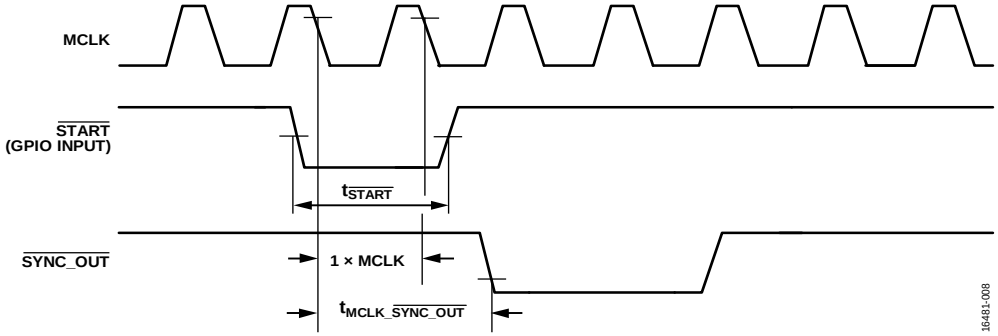

Figure 8. Asynchronous $\overline{START}$ and $\overline{SYNC\_OUT}$

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
VDD_PGA to AGND	+20V
VSS_PGA to AGND	-20V
VDD2_PGA to AGND	+20V
IN+, IN-	VSS_PGA to VDD_PGA
GAIN0, GAIN1, GAIN2	VSS_PGA to VDD_PGA
VCM_PGA	VSS_PGA to VDD2_PGA
VDD_FDA to VDD_ADC	−0.3 V to +0.3V
VDD_FDA to AGND	11V
M0_FDA, M1_FDA to AGND	
IN_LDO to AGND	−0.3 V to +6.5 V
EN_LDO to AGND	−0.3 V to +6.5 V
OUT_LDO to AGND	−0.3 V to IN_LDO
VDD_ADC to AGND	−0.3 V to +6.5 V
VDD2_ADC to AGND	−0.3 V to +6.5 V
VDD_IO to DGND	−0.3 V to +6.5 V
DGND to AGND	−0.3 V to +0.3V
VDD_IO, DREG_CAP to DGND (VDD_IO tied to DREG_CAP for 1.8 V Operation)	−0.3 V to +2.25 V
REF+, REF- to AGND	−0.3 V to VDD_ADC + 0.3 V
Digital Input Voltage to DGND	−0.3 V to VDD_IO + 0.3 V
Digital Output Voltage to DGND	−0.3 V to VDD_IO + 0.3 V
XTAL1 to DGND	−0.3 V to +2.1 V
Operating Temperature Range	-40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Pb-Free Temperature, Soldering Reflow (10 sec to 30 sec)	260°C
Maximum Package Classification Temperature	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface mount packages. Values are calculated based on the standard JEDEC test conditions defined in table 6, unless otherwise specified.

Table 5. Thermal Resistance

Package Type[1]	θ_{JA}	Ψ_{JB}	Unit
			°C/W

Only use θ_{JA} to compare thermal performance of the package of the device with other semiconductor packages when all test conditions listed are similar. One common mistake is to use θ_{JA} to estimate the junction temperature in the system environment. Instead, using Ψ_{JT} is a more appropriate way to estimate the worst-case junction temperature of the device in the system environment. First, take an accurate thermal measurement of the top center of the device (on the mold compound in this case) while the device operates in the system environment. This measurement is known in the following equation as T_{TOP}. This equation can then be used to solve for the worst-case T_J in that given environment as follows:

$$T_J = \Psi_{JT} \times P + T_{TOP}$$

where:
Ψ_{JT} is the junction to top thermal characterization number as specified in data sheet.
P refers to total power dissipation in the chip (W).
T_{TOP} refers to the package top temperature (°C) and is measured at the top center of the package in the environment of the user.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 6. Standard JEDEC Test Conditions

Test Conditions	θ_{JA}	θ_{JC}	θ_{JB}
Main Heat Transfer Mode	Convection	Conduction	Conduction
Board Type	2S2P	1S0P	2S2P
Board Thickness	1.6 mm	1.6 mm	1.6 mm
Board Dimension	If package length is <27 mm, 76.2 mm × 114.3 mm; otherwise, 101.6 mm × 114.3 mm	If package length is <27 mm, 76.2 mm × 114.3 mm; otherwise, 101.6 mm × 114.3 mm	If package length is <27 mm, 76.2 mm × 114.3 mm; otherwise, 101.6 mm × 114.3 mm
Signal Traces Thickness	0.07 mm	0.07 mm	0.07 mm
PWR/GND Traces Thickness	0.035 mm	Not applicable	0.035 mm
Thermal Vias	Use thermal vias with 0.3 mm diameter, 0.025 mm plating, and 1.2 mm pitch whenever a package has an exposed thermal pad; vias numbers are maximized to cover the area of the exposed paddle	Use thermal vias with 0.3 mm diameter, 0.025 mm plating, and 1.2 mm pitch whenever a package has an exposed thermal pad; vias numbers are maximized to cover the area of the exposed paddle	Use thermal vias with 0.3 mm diameter, 0.025 mm plating, and 1.2 mm pitch whenever a package has an exposed thermal pad; vias numbers are maximized to cover the area of the exposed paddle
Cold Plate	Not applicable	Cold plate attaches to either package top or bottom depending on the path of least thermal resistance	Fluid cooled, ring style cold plate that clamps both sides of the test board such that heat flows from package radially in the plane of the test board

TERMINOLOGY

Common-Mode Rejection Ratio (CMRR)
CMRR is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a TBAV p-p sine wave applied to the common-mode voltage of V+ and V- at frequency, f_S.

$$CMRR\ (\text{dB}) = 10 \log(Pf/Pf_S)$$

where:
Pf is the power at frequency, *f*, in the ADC output.
Pf_S is the power at frequency, f_S, in the ADC output.

Differential Nonlinearity (DNL) Error
In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Integral Nonlinearity (INL) Error
Linearity error refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Dynamic Range
Dynamic range is the ratio of the rms value of the full scale to the rms noise measured when input pins are shorted together. The value for dynamic range is expressed in decibels.

Total System Dynamic Range
Total system dynamic range is the ratio of the rms value of the full scale at Gain0 mode to the input refereed rms noise measured when input pins are shorted together in Gain6 mode. The value is expressed in decibels.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa and nfb, where m, n = 0,1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n are equal to 0. For example, the second-order terms include (fa + fb) and (fa − fb), and the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The ADAQ7768-1 is tested using the CCIF standard, where two input frequencies near the top end of the input bandwidth are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves, and the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in decibels.

Gain Error
The first transition (from 100 … 000 to 100 …001) occurs at a level ½ LSB above nominal negative full scale (−4.0959375 V for the ±4.096 V range). The last transition (from 011 … 110 to 011 … 111) occurs for an analog voltage 1½ LSB below the nominal full scale (+4.0959375 V for the ±4.096 V range). The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Gain Error Drift

The ratio of the gain error change due to a temperature change of 1°C and the full-scale range (2^N). It is expressed in parts per million.

Least Significant Bit (LSB)
The least significant bit, or LSB, is the smallest increment that can be represented by a converter. For a fully differential input ADC with N bits of resolution, the LSB expressed in volts is

$$LSB\ (\text{V}) = \frac{V_{INp\text{-}p}}{2^N}$$

Power Supply Rejection Ratio (PSRR)
Variations in power supply affect the full-scale transition but not the linearity of the converter. PSRR is the maximum change in the full-scale transition point due to a change in power supply voltage from the nominal value.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-(Noise + Distortion) Ratio (SINAD)
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels, between the rms amplitude of the input signal and the peak spurious signal (including harmonics).

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Offset Error
Offset error is the difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

Offset Error Drift

Offset error drift is the ratio of the offset error change due to a temperature change of 1°C and the full scale code range (2^N). It is expressed in parts per million.

QUICK START UP GUIDE

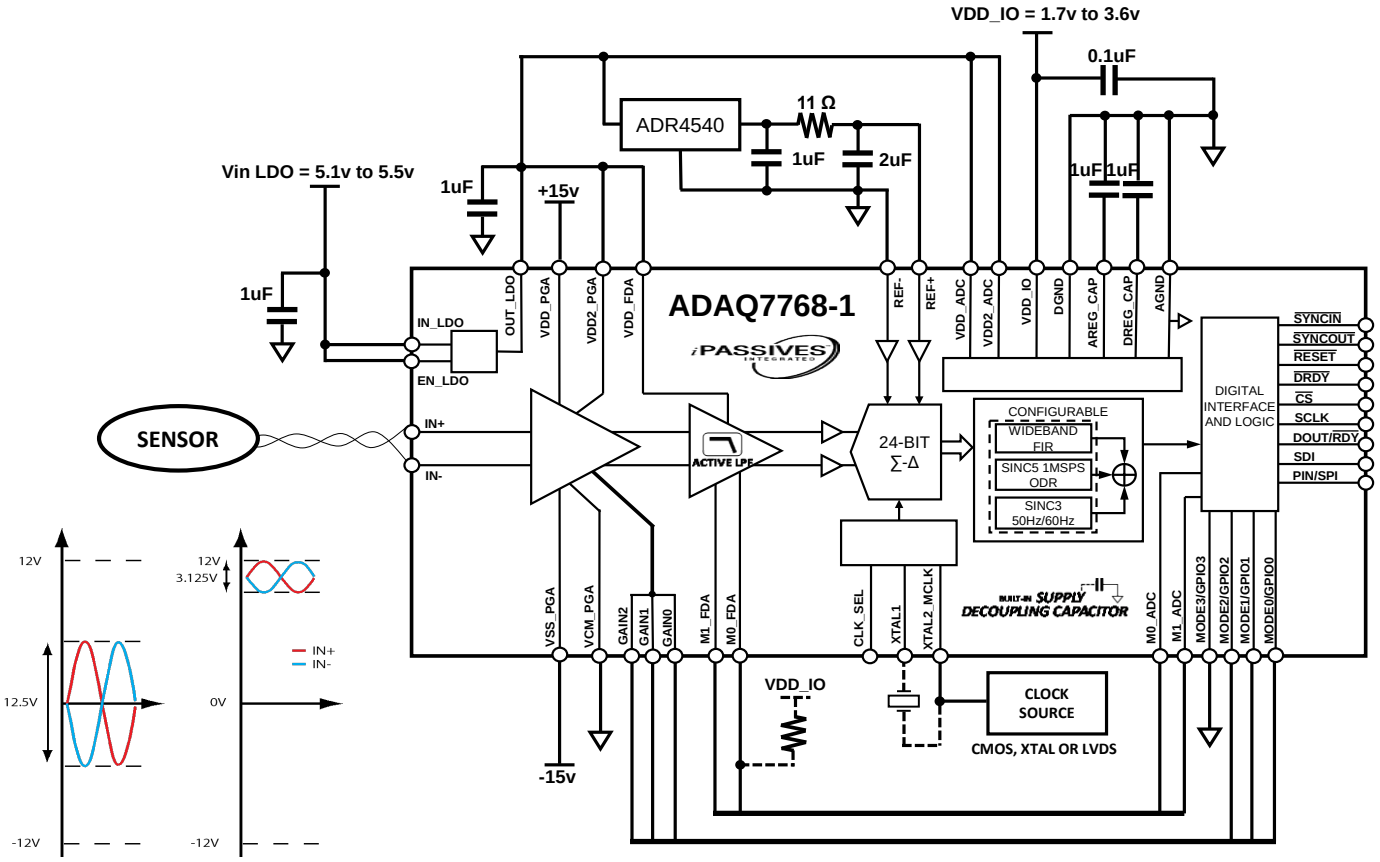

Figure 9. Typical Connection Diagram

POWER SUPPLY CONNECTION

The ADAQ7768-1 has several power supplies to power the analog front end and the ADC, and to simplify the connection, the ADAQ7768-1 have an internal LDO that can be used to supply the voltage of the VDD_ADC, VDD2_PGA, and VDD_FDA. The LDO can also power the ADR4540 reference for the REF+ and REF- pins. The LDO input can handle inputs ranges of 5.1v to 5.5v. For proper operation it is recommended to use 1uF capacitor at the input and output of the LDO. In case the LDO is not used during normal operation, it is recommended to keep all the LDO pins floating.

Depending on the input signal rail the VDD_PGA can be set from 4.5v to 18v, while the VSS_PGA can be set from -4.5v to -18v. The VDD_IO powers the internal regulator needed by the digital logic of the ADC, VDD_IO is referenced to AGND and can vary from 1.7v to 3.6v.

The ADAQ7768-1 has a built-in 0.1uF internal decoupling capacitor on each power supply except for the VDD_IO. For detailed information regarding power supply connection and power supply decoupling refer to Power Supplies and Power Supply Decoupling Sections

DEVICE CONTROL MODE

The ADAQ7768-1 has two options for controlling device functionality. On power-up, the mode is determined by the state of the $\overline{\text{PIN}}$/ SPI pin. The two modes of configuration are

- $\overline{\text{PIN}}$ /SPI = VDD_IO = SPI Control mode: over a 3- or 4-wire SPI interface (complete configurability), suggested control mode.
- $\overline{\text{PIN}}$ /SPI = AGND = Pin Control mode: pin strapped digital logic inputs (a subset of complete configurability, daisy chain is available only at this mode)

The first design decision is setting the ADAQ7768-1 in either the SPI or $\overline{\text{PIN}}$ mode of configuration.

On power-up, the user must apply a soft or hard reset to the device when using either control mode. A $\overline{\text{SYNC\_IN}}$ pulse is also recommended after the reset or after any change to the device configuration. Choose between controlling and configuring over the SPI or via pin connections only.

Detailed discussion on the capability and limitations of the two control mode options can be found in the Device Configuration section.

INPUT RANGE SELECTION

The ADAQ7768-1 input is a low noise, low bias current, high bandwidth Programable Gain Instrumentation Amplifier (PGIA) that is capable of signal attenuation and signal amplification. The PGIA has 6 gain settings that are capable of varying input range from ±0.197v to ±12.603v fully differential input signal.

The PGIA gain can be controlled with Gain0, Gain1 and Gain 2 pins. The gain pin can be set using an external pull-up or pull-down resistor that is connected between AGND and VDD_IO, as shown in Figure 10.

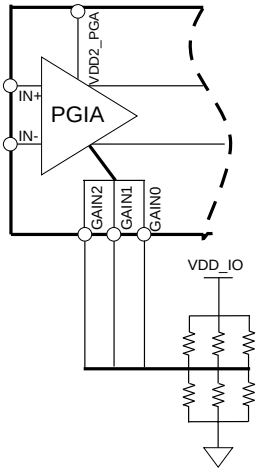

Figure 10. PGIA Gain Control using External Resistors

Error! Reference source not found. Table 11, on Input Range Selection section shows the truth table of the gain pin combinations and the resulting PGIA Gain setting.

The PGIA gain pin can also be connected to GPIO pins of the ADAQ7768-1 as shown in Figure 9. Typical Connection Diagram, this will enable the user to control the PGIA gain over SPI serial interface. When the GPIO pins are used to control the PGIA gain, the user must set the GPIO ports as output, on GPIO_CONTROL register (Register 0x1E). The GPIO_WRITE register (Register 0x1F) will set the desire output logic for GPIO pins.

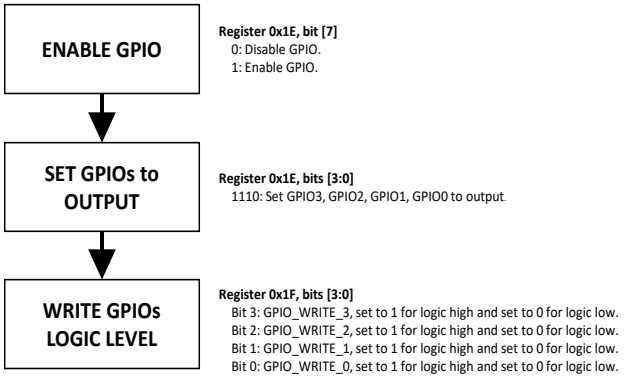

Figure 11. GPIO Gain Control Flow Chart

By writing 111 to GPIOx_OP_EN bits [2:0] of GPIO_CONTROL register (Register 0x1E) will enable GPIO0, GPIO1 and GPIO2. Using the default output logic of GPIO_WRITE register (Register 0x1F) will set the ADAQ7768-1 to system gain of 20.8 V/V capable of input voltage of ± 0.197v.

MCLK DIVIDER AND MCLK SOURCE SELECTION

MCLK Source Selection

The ADAQ7768-1 has an internal oscillator that is used for initial power-up of the device. After the ADAQ7768-1 completes the start-up routine, a clock handover occurs to the external MCLK. The MCLK source can be programmed using the two control mode options, Pin control mode and SPI control mode.

In $\overline{\text{PIN}}$ control mode, the CLK_SEL pin sets the external MCLK source. Three clock options are available in $\overline{\text{PIN}}$ control mode: an internal oscillator, an external CMOS, or a crystal oscillator.

- CLK_SEL = 0 in $\overline{\text{PIN}}$ control mode, the CMOS clock option is selected and must be applied to the MCLK pin. In this case, tie the XTAL1 pin to DGND.
- CLK_SEL = 1 in $\overline{\text{PIN}}$ control mode, the crystal option is selected and must be connected between the XTAL1 and XTAL2 pins.
- On the condition that no external clock is detected, the ADAQ7768-1 will use its internal clock as a default clock source.

In SPI control mode, the following option for MCLK input source are available:

- LVDS
- External crystal
- CMOS input MCLK
- Internal Clock

From the POWER_CLOCK register (Register 0x15), pulling the CLOCK_SEL bits [7:6] low configures the ADAQ7767-1 for a CMOS clock. Pulling the CLOCK_SEL bits high enables the use of an external crystal. Setting CLOCK_SEL bits [7:6] to 10 enables the application of the LVDS clock to the MCLK pin. LVDS clocking is exclusive to SPI mode and requires the register selection for operation.

When switching from one clock source to another, the user must apply soft reset to the device.

For optimum AC performance, it is not recommended to use in the internal clock as MCLK source.

MCLK Divider

The MCLK signal received by the ADAQ7768-1 defines the core ADC's sigma delta modulator clock rate (F_{MOD}) and, in turn, the sampling frequency of the modulator of $2 \times F_{MOD}$. For optimum performance it is recommended to use MCLK = 16.384 MHz and MCLK_DIV = 2. This will set the F_{MOD} = 8.192 MHz, by keeping

the F_{MOD} frequency high it maximizes the out of band tone rejection from the frontend anti-aliasing filter.

$$Fmod = \frac{MCLK}{MCLK\ DIV}$$

The default master clock divider setting for ADAQ7768-1 is MCLK_DIV = 16. To configure the MCLK divider to MCLK = 2, the user must write 11 to MCLK_DIV bits [5:4] of POWER_CLOCK register (Register 0x15) after power up.

Table 20. Control Settings for MODEx Pins shows how to configure MCLK when operating under $\overline{PIN}$ control mode.

MCLK and SCLK Alignment

The ADAQ7768-1 interface is flexible to allow the multiple modes of operation and various data output formats to work across different DSPs and microcontroller units (MCUs). To achieve maximum performance, it is recommended to have a synchronous SCLK to MCLK from same clock source. It is also possible to set SCLK to be multiple of MCLK, detailed discussion about digital interface can be found in Recommended Interface Section.

DIGITAL FILTER SETTING

The ADAQ7768-1 offers three types of digital filters. The digital filters available on the ADAQ7768-1 are

- Wideband Low Ripple FIR filter, −3 dB at 0.433 × ODR (6 rates)
- Sinc5 low latency filter, −3 dB at 0.204 × ODR (8 rates)
- Sinc3 low latency filter, −3 dB at 0.2617 × ODR, widely programmable data rate

Details on the digital filter setting can be found in digital filter section

Decimation Rate and Output Data Rate

The ADAQ7768-1 has programmable decimation rates for the Sinc5, Sinc3 and Wideband Low Ripple FIR digital filters. The decimation rates allow the user to band limit the measurement, which reduces the speed and input bandwidth, but increases the resolution because there is further averaging in the digital filter. Control of the decimation rate on the ADAQ7768-1 when using the SPI control is set in the DIGITAL_FILTER register (Register 0x19) for the Sinc5 and Wideband Low Ripple FIR filters.

The ODR of ADAQ7768-1 can be calculated using the formula:

$$ODR = \frac{MCLK}{MCLK\ DIV \times DEC\ RATE}$$

ADC POWER MODE

The ADC core power mode must match the MCLK_DIV setting, and for optimum performance it is recommended to use MCLK_DIV = 2 this will set the ADAQ7768-1 in high performance mode or fast mode. The user mut be aware that ADAQ7768-1 ADC power mode defaults to eco power mode upon power up. To change the ADC power mode to high performance the user should write 11 to ADC_MODE bits [1:0] of POWER_CLOCK register (Register 0x15).

BASIC REGISTER SETUP

Figure 12, shows the basic flow of register writes for ADAQ7768-1 upon power up.

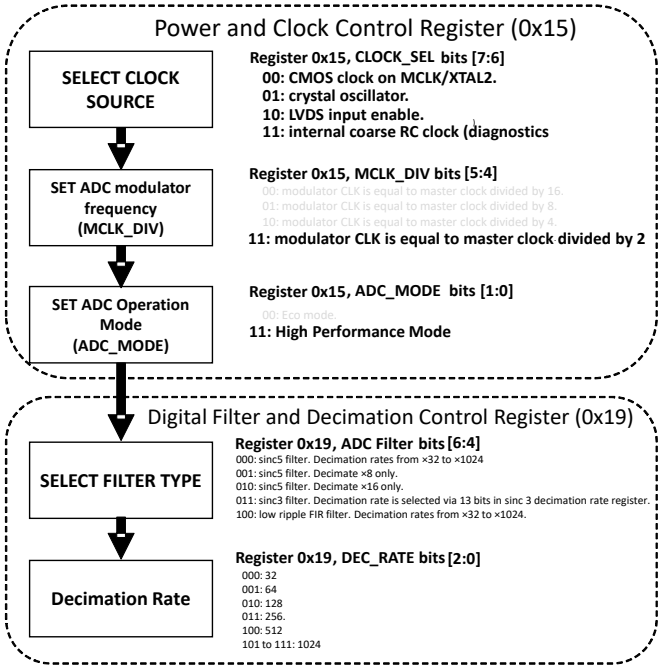

Figure 12. Basic Register Setup for ADAQ7768-1

Subsequent SPI writes needed upon power up to set the ADAQ7768-1 to the following conditions:

- MCLK sourced from CMOS clock
- The MCLK divider should be set to 2 (Recommended)
- ADC Power mode should be set to high performance mode, or fast mode (Recommended)
- Wideband Low Ripple Filter
- Decimation rate to 32

SPI writes:

- Data 0x33 to Register 0x15
- Data 0x40 to Register 0x19

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

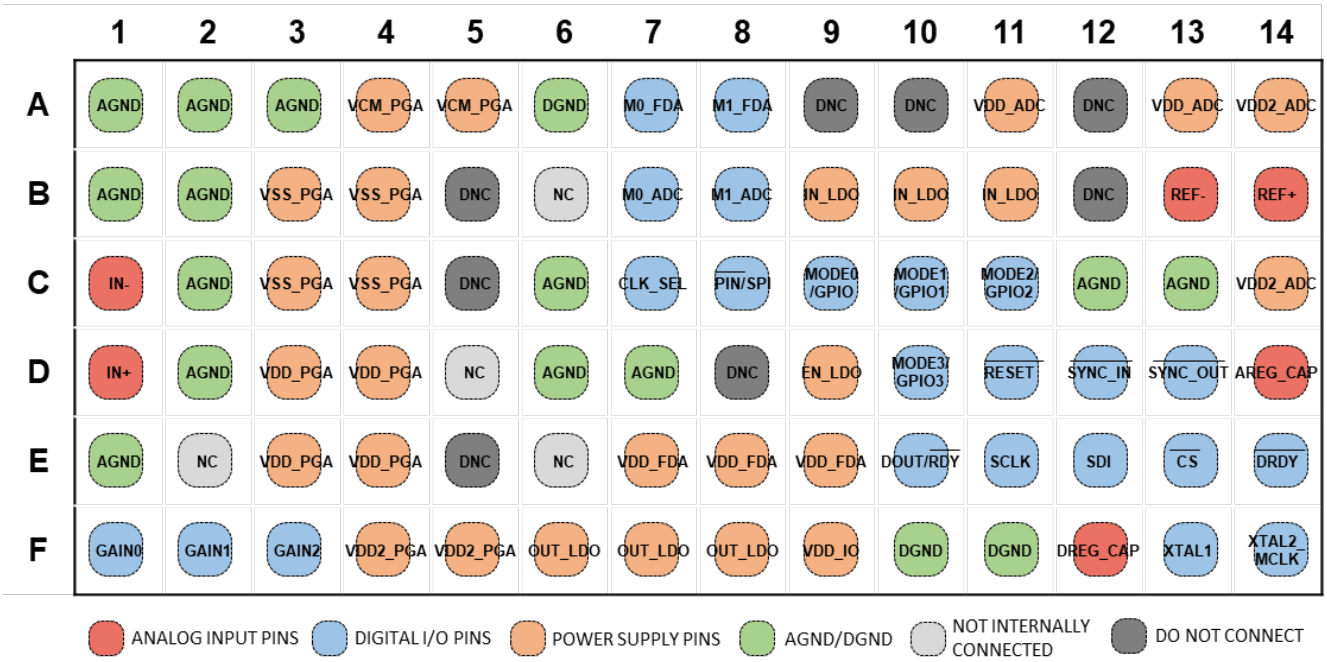

Figure 13. Pin Configuration

Table 7. ADA7768-1 Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
A1,A2,A3	AGND	P	Ground reference for VDD_FDA, IN_LDO, VDD_ADC and AVDD2_ADC supplies. Connect to system ground for normal operation.
A4, A5	VCM_PGA	AI	Output common mode voltage control input of the PGIA. Connect to AGND for normal operation.
A6	DNGD	P	Ground reference for VDD_IO supplies. Connect to system ground for normal operation.
A7	M0_FDA	DI	FDA mode control input 0. Connect to M0_ADC for normal operation.
A8	M1_FDA	DI	FDA mode control input 1. Connect to M1_ADC for normal operation.
A9, A10	DNC		Do not connect.
A11, A13	VDD_ADC	P	ADC analog supply voltage. Referenced to AGND. Connect to OUT_LDO if using on-device LDO, else connect it to a single power source that also supplies the VDD2_PGA and VDD_FDA pins.
A12	DNC		Do not connect.
A14	VDD2_ADC	P	ADC secondary analog supply voltage. Referenced to AGND.

Pin No.	Mnemonic	Type[1]	Description
B1,B2	AGND	P	Ground reference for VDD_FDA, IN_LDO, VDD_ADC and AVDD2_ADC supplies. Connect to system ground for normal operation.
B3, B4	VSS_PGA	P	Programmable gain instrumentation amplifier input and output stage negative supply. Referenced to AGND.
B5	DNC		Do not connect.
B6	NC		Not internally connected. Leave floating or connect to ground reference.
B7	M0_ADC	DO	FDA mode control output 0. Connect to M0_FDA for normal operation.
B8	M1_ADC	DO	FDA mode control output 1. Connect to M1_FDA for normal operation.
B9, B10, B11	IN_LDO	P	On-device LDO supply input. Bypass IN_LDO to AGND with a capacitor of at least 1 µF.
B12	DNC		Do not connect.
B13	REF-	AI	ADC reference input negative node. Connect to AGND for normal operation.
B14	REF+	AI	ADC reference input positive node. Apply an external reference between REF+ and REF- with voltage level ranging from VDD_ADC to AGND +1 V.
C1	IN-	AI	Signal input, inverting.
C2	AGND	P	Ground reference for VDD_FDA, IN_LDO, VDD_ADC and AVDD2_ADC supplies. Connect to system ground for normal operation.
C3, C4	VSS_PGA	P	Programmable gain instrumentation amplifier input and output stage negative supply. Referenced to AGND.
C5	DNC		Do not connect.
C6,	AGND		Connect to system ground for normal operation.
C7	CLK_SEL	DI	ADC clock source selection input. In pin control mode: 0: CMOS clock option. Apply external CMOS clock signal to XTAL2_MCLK pin, tie XTAL1 pin to DGND. 1: Crystal Option. Connect external crystal across the XTAL1 and the XTAL2_MCLK pins. In SPI control mode: Tie CLK_SEL pin to DGND. Select the clock source through register access. The LVDS clock option is available only in SPI control mode.
C8	$\overline{\text{PIN}}$ /SPI	DI	Device mode selection input. 0: Pin mode operation. Control and configure device operation through configuration pin logic. 1: Control and configuration through register over SPI interface.

Pin No.	Mnemonic	Type[1]	Description
C9	MODE0/GPIO0	DI/O	Multi-function pin. In pin control mode: Pin control operating profile selection input 0. In SPI control mode: General purpose I/O pin, with logic level referenced to VDD_IO and DGND pins.
C10	MODE1/GPIO1	DI/O	Multi-function pin. In pin control mode: Pin control operating profile selection input 1. In SPI control mode: General purpose I/O pin, with logic level referenced to VDD_IO and DGND pins.
C11	MODE2/GPIO2	DI/O	Multi-function pin. In pin control mode: Pin control operating profile selection input 2. In SPI control mode: General purpose I/O pin, with logic level referenced to VDD_IO and DGND pins.
C12, C13	AGND	P	Ground reference for VDD_FDA, IN_LDO, VDD_ADC and AVDD2_ADC supplies. Connect to system ground for normal operation.
C14	VDD2_ADC	P	ADC secondary analog supply voltage. Referenced to AGND.
D1	IN+	AI	Signal input, non-inverting.
D2	AGND	P	Ground reference for VDD_FDA, IN_LDO, VDD_ADC and AVDD2_ADC supplies. Connect to system ground for normal operation.
D3, D4,	VDD_PGA	P	Programmable gain instrumentation amplifier positive supply input, Referenced to AGND.
D5	NC		Not internally connected. Leave floating or connect to ground reference.
D6	AGND	P	Connect to system ground for normal operation.
D7	AGND	P	Ground reference for VDD_FDA, IN_LDO, VDD_ADC and AVDD2_ADC supplies. Connect to system ground for normal operation.
D8	DNC	I	Do not connect.
D9	EN_LDO	AI	On-device LDO enable input. Active high.
D10	MODE3/GPIO3	DI/O	Multi-function pin. In pin control mode: Pin control operating profile selection input 3. In SPI control mode: General purpose I/O pin, with logic level referenced to VDD_IO and DGND pins.
D11	$\overline{\text{RESET}}$	DI	ADC Hardware Asynchronous Reset input. After the device is fully powered up it is recommended to do a hardware or software reset.
D12	$\overline{\text{SYNC\_IN}}$	DI	$\overline{\text{SYNC\_IN}}$ receives the synchronization signal from $\overline{\text{SYNC\_OUT}}$ pin or from the main controller. The synchronization signal needs to be synchronous to MCLK. $\overline{\text{SYNC\_IN}}$ enables synchronization and simultaneous sampling of multiple ADAQ7768-1 devices.

Pin No.	Mnemonic	Type[1]	Description
D13	$\overline{\text{SYNC\_OUT}}$	DO	Synchronization pulse output synchronous to MCLK. This pin allows one or multiple ADAQ7768-1 devices to be synchronized through SPI. Send a SYNC command over SPI interface to initiate a $\overline{\text{SYNC\_OUT}}$ output. If used, route $\overline{\text{SYNC\_OUT}}$ signal back to the $\overline{\text{SYNC\_IN}}$ pin of the same device and the $\overline{\text{SYNC\_IN}}$ pins of other ADAQ7768-1 devices for simultaneous sampling.
D14	AREG_CAP	AO	ADC's internal analog LDO regulator output. Decouple this pin to AGND with a 1 µF capacitor. Do not use the voltage output from AREG_CAP in circuits external to the ADAQ7768-1.
E1	AGND	P	Ground reference for VDD_FDA, IN_LDO, VDD_ADC and AVDD2_ADC supplies. Connect to system ground for normal operation.
E2	NC		Not internally connected. Leave floating or connect to ground reference.
E3, E4	VDD_PGA	P	Programmable gain instrumentation amplifier positive supply input, Referenced to AGND.
E5	DNC		Do not connect.
E6	NC		Not internally connected. Leave floating or connect to ground reference.
E7, E8, E9	VDD_FDA	P	ADC driver amplifier positive supply, Referenced to AGND. Connect to OUT_LDO if using on-device LDO, else connect it to a single power source that also supplies the VDD2_PGA and VDD_ADC pins.
E10	DOUT/$\overline{\text{RDY}}$	DO	Serial Interface Data Output and Data Ready signal combined. This output data pin can be configured as either a DOUT pin only, or through the SPI control mode, include the ready signal (RDY). The ability to program the device to provide a combined DOUT/RDY signal can reduce the number of required interface IO lines.
E11	SCLK	DI	Serial interface clock.
E12	SDI	DI	Serial interface data input.
E13	$\overline{\text{CS}}$	DI	Serial interface chip-select input. Active low.
E14	$\overline{\text{DRDY}}$	DO	ADC conversion data ready output. Periodic signal output to signify conversion results are available.
F1	GAIN0	DI	PGIA gain control logic input 0.
F2	GAIN1	DI	PGIA gain control logic input 1.
F3	GAIN2	DI	PGIA gain control logic input 2.
F4, F5	VDD2_PGA	P	PGIA output stage positive power supply. Referenced to AGND. Connect to OUT_LDO if using on-device LDO, else connect it to a single power source that also supplies the VDD_FDA and VDD_ADC pins. Bypass VDD2_PGA to AGND with a decoupling capacitor of 1uF.
F6,F7, F8	OUT_LDO	P	On-device LDO output. Bypass OUT_LDO to AGND with a capacitor of at least 1 µF.

Pin No.	Mnemonic	Type[1]	Description
F9	VDD_IO	P	Digital Supply. The VDD_IO pin sets the logic levels for all interface pins. This pin powers the digital processing via the internal digital LDO. Referenced to DGND. Bypass VDD_IO to DGND with a capacitor of at least 1 µF.
F10, F11	DGND	P	Ground reference for VDD_IO supplies. Connect to system ground for normal operation.
F12	DREG_CAP	AO	ADC's internal digital LDO regulator output. Decouple this pin to DGND with a 1 µF capacitor. For VDD_IO ≤ 1.8 V, use a 10 µF capacitor. Do not use the voltage output from AREG_CAP in circuits external to the ADAQ7768-1.
F13	XTAL1	DI	ADC clock input 1. External Crystal: Connect to one node of the external crystal. LVDS: Connect to one node of the LVDS clock source. CMOS clock: Connect to DGND.
F14	XTAL2_MCLK	DI	ADC clock input 2. External Crystal: Connect to the second node of the external crystal. LVDS: Connect to the second node of the LVDS clock source. CMOS clock: Connect to the CMOS clock source. Logic level referenced to VDD_IO and DGND.

[1] AI is analog input; AO is analog output; DI is digital input; DO is digital output; DI/O is bidirectional digital; P is power or ground.

TYPICAL PERFORMANCE CHARACTERISTICS

VDD_PGA = 15V, VSS_PGA = -15V, AGND = DGND = 0V, Input common mode voltage = 0V, IN_LDO = 5.1V to 5.5, VDD_IO = 3.3 V, REF+ = 4.096V, REF-= 0V, MCLK =16.384 MHz 50:50 duty cycle, FDA = Low Power Mode, Linearity boost buffer on, Reference pre-charge buffer on, Reference buffer off, T_A = 25°C unless otherwise noted.

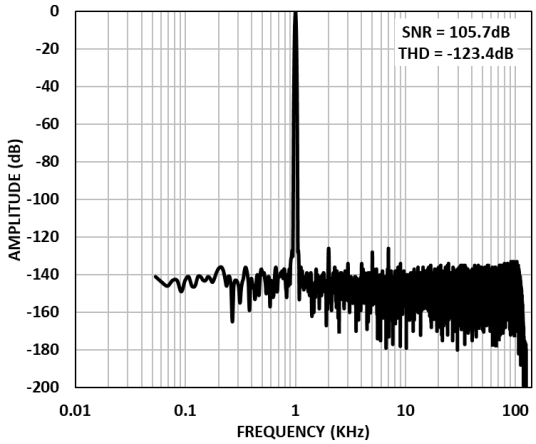

Figure 14. FFT Wideband Low Ripple FIR Filter, Differential Input, -0.5dBFS, Gain = 0.325 V/V, FDA = Full Power.

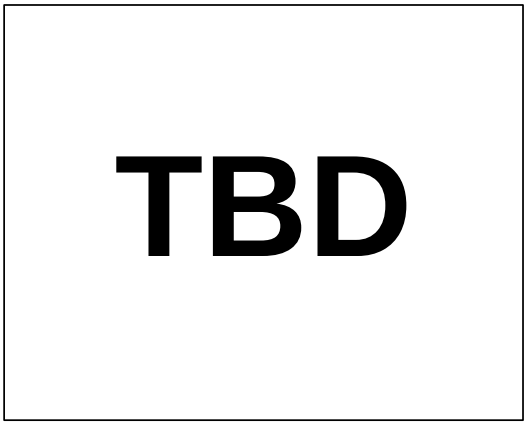

Figure 17. FFT Wideband Low Ripple FIR Filter, Differential Input, -0.5dBFS, Gain = 2.6 V/V, FDA = Full Power.

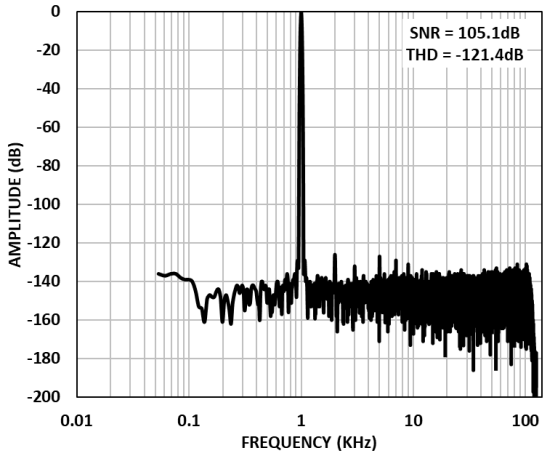

Figure 15. FFT Wideband Low Ripple FIR Filter, Differential Input, -0.5dBFS, Gain = 0.65 V/V, FDA = Full Power.

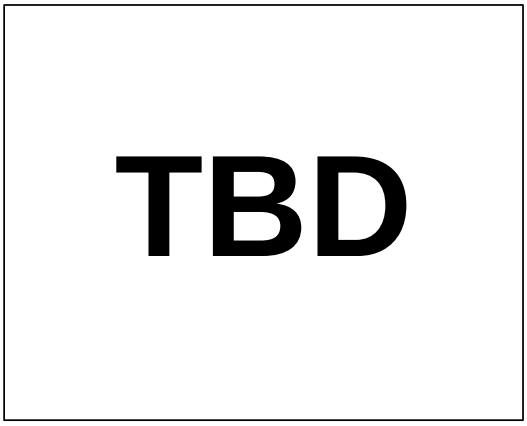

Figure 18. FFT Wideband Low Ripple FIR Filter, Differential Input, -0.5dBFS, Gain = 10.4 V/V, FDA = Full Power.

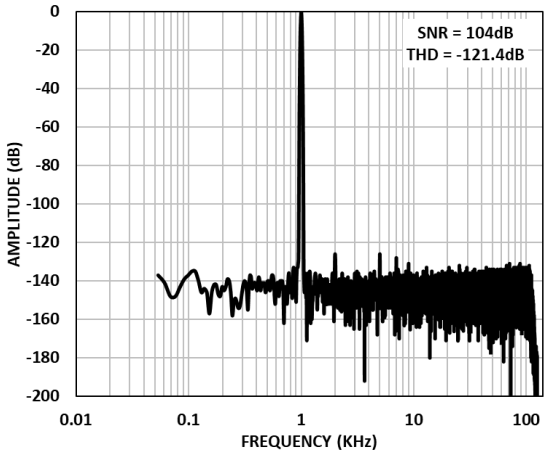

Figure 16. FFT Wideband Low Ripple FIR Filter, Differential Input, -0.5dBFS, Gain = 1.3 V/V, FDA = Full Power.

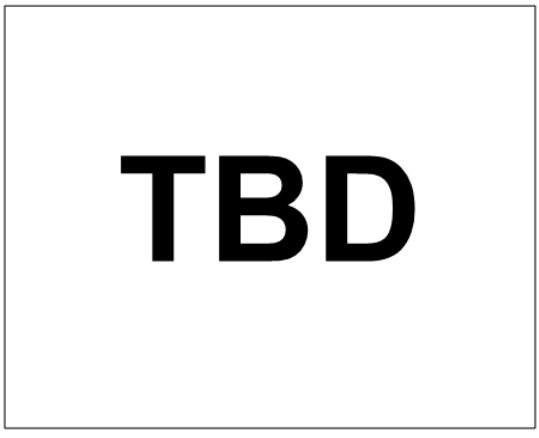

Figure 19. FFT Wideband Low Ripple FIR Filter, Differential Input, -0.5dBFS, Gain = 20.8 V/V, FDA = Full Power.

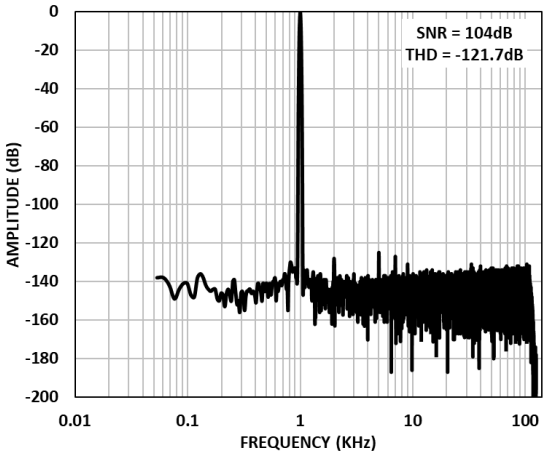

Figure 20. FFT Wideband Low Ripple FIR Filter, Bipolar Single Ended Input, -0.5dBFS, Gain = 1.3 V/V, FDA = Full Power.

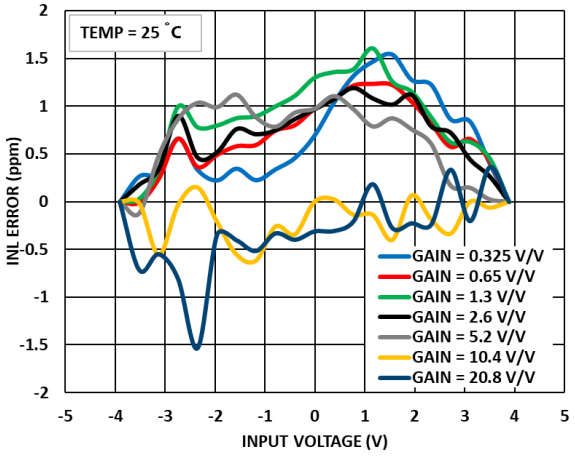

Figure 21. INL Error vs. Input Voltage for Various Gain, Differential Input at 25°C.

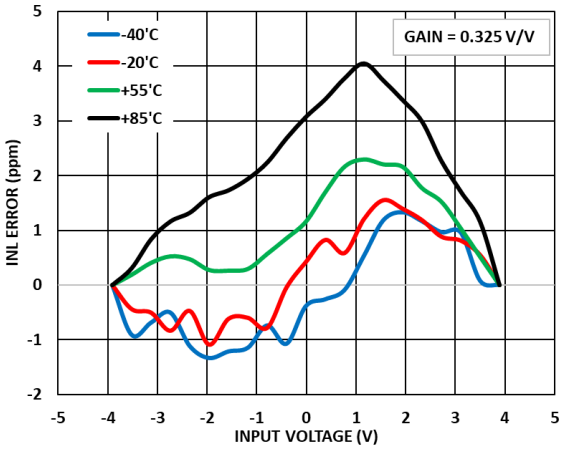

Figure 22. INL Error vs. Input Voltage over Temperature, Differential Input, Gain = 0.325 V/V.

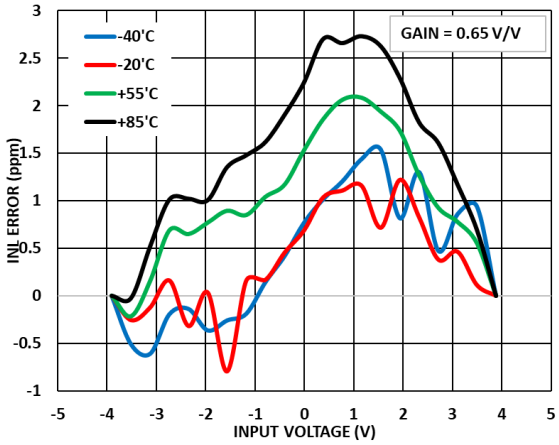

Figure 23. INL Error vs. Input Voltage over Temperature, Differential Input, Gain = 0.65 V/V.

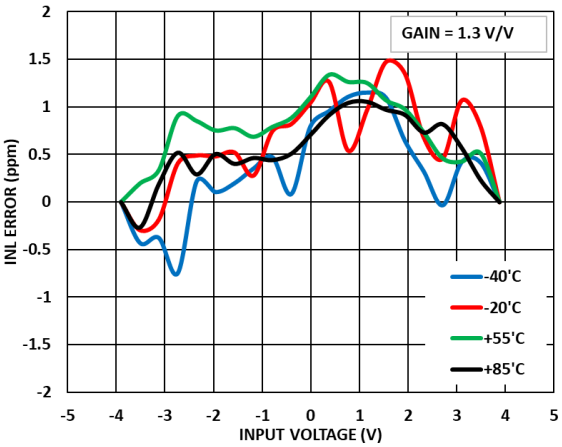

Figure 24. INL Error vs. Input Voltage over Temperature, Differential Input, Gain = 1.3 V/V.

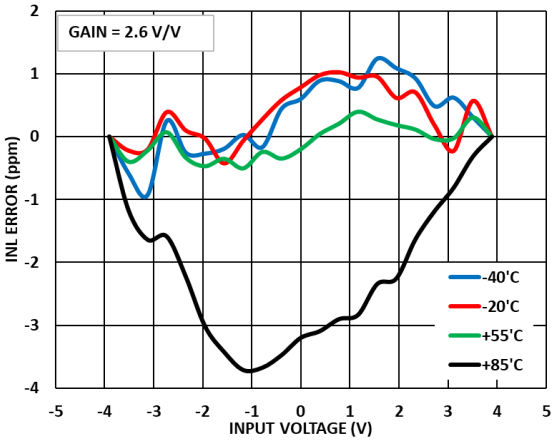

Figure 25. INL Error vs. Input Voltage over Temperature, Differential Input, Gain = 2.6 V/V.

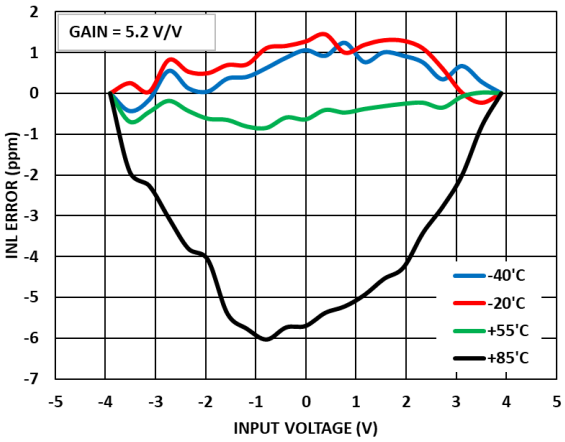

Figure 26. INL Error vs. Input Voltage over Temperature, Differential Input, Gain = 5.2 V/V

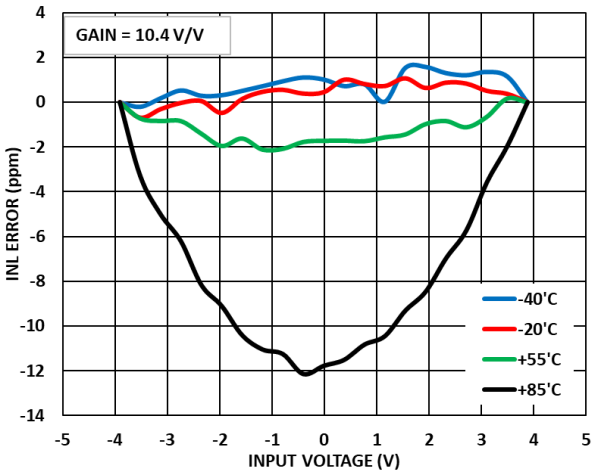

Figure 27. INL Error vs. Input Voltage over Temperature, Differential Input, Gain = 10.4 V/V

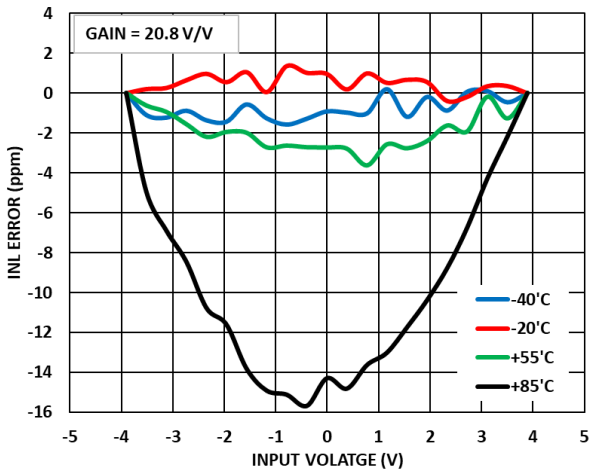

Figure 28. INL Error vs. Input Voltage over Temperature, Differential Input, Gain = 20.8 V/V

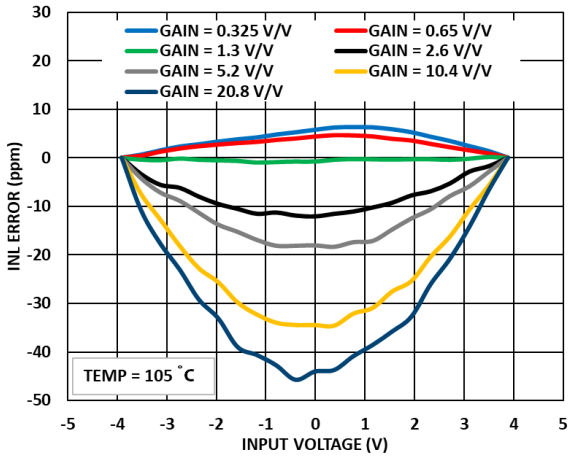

Figure 29. . INL Error vs. Input Voltage for Various Gain, Differential Input at 105 ˚C

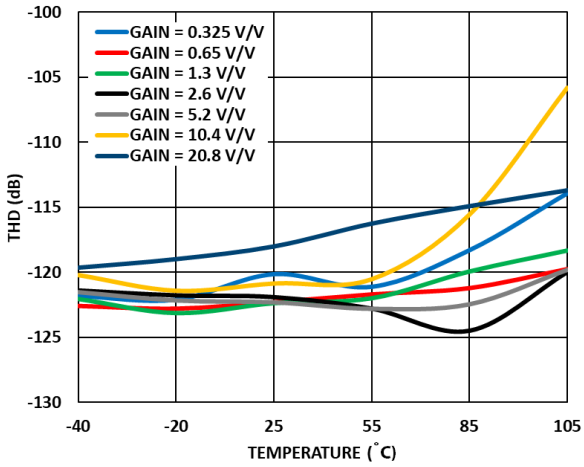

Figure 30. THD across Temperature at Various Gain, -0.5dBFS, 1KHz, FDA = Full Power

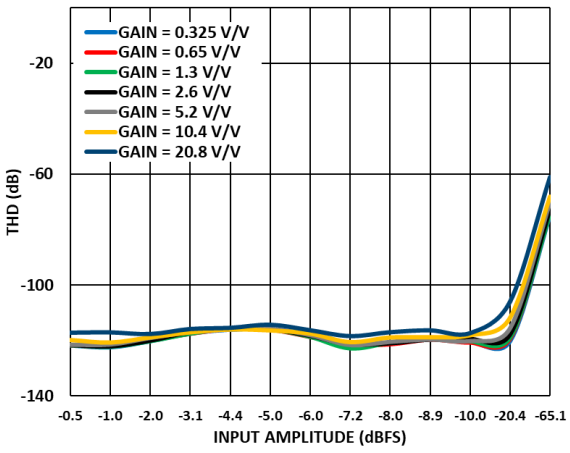

Figure 31. THD across Input Amplitude at Various Gain, 1KHz, FDA = Full Power.

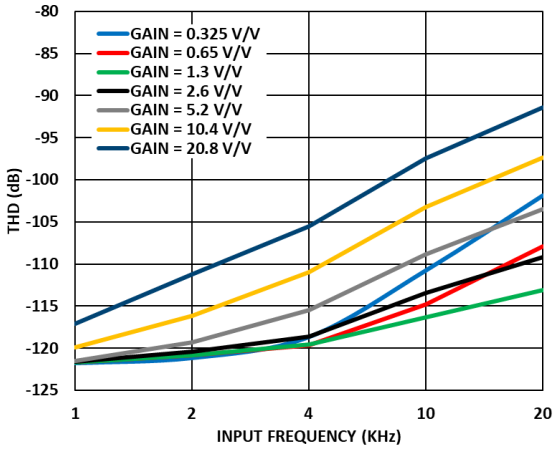

Figure 32. THD vs. Input Frequency for Various Gain, -0.5dBFS, FDA = Full Power.

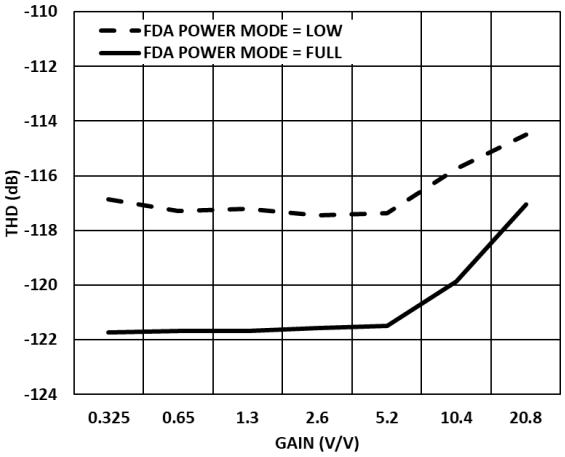

Figure 33. THD vs. Gain over FDA Power Mode, -0.5dBFS, 1kHz.

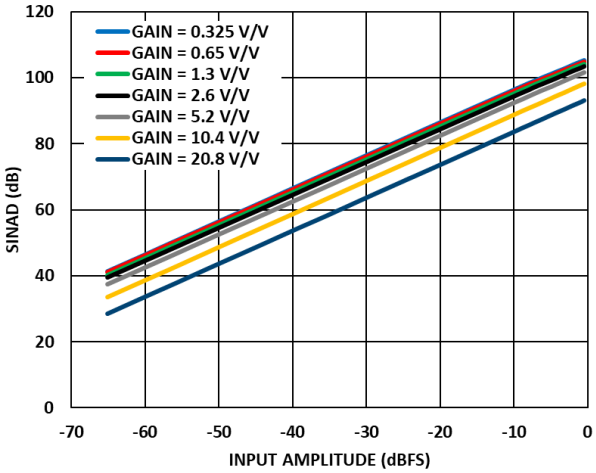

Figure 34. SINAD across Input Amplitude at Various Gain, 1KHz, FDA = Full Power.

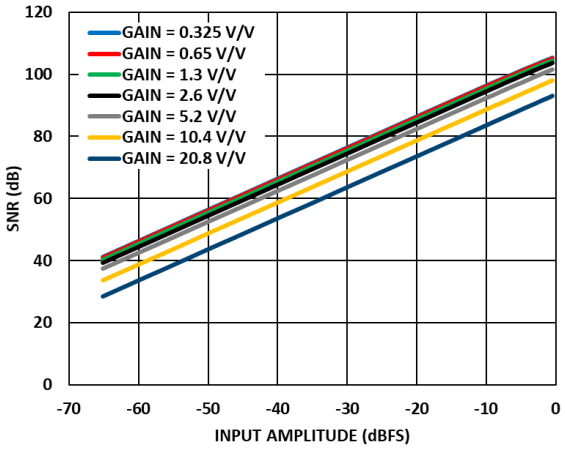

Figure 35. SNR across Input Amplitude at Various Gain, 1KHz.

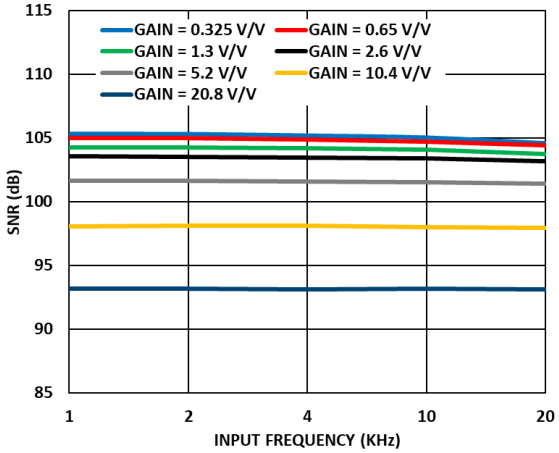

Figure 36. SNR vs. Input Frequency for Various Gain, -0.5dBFS

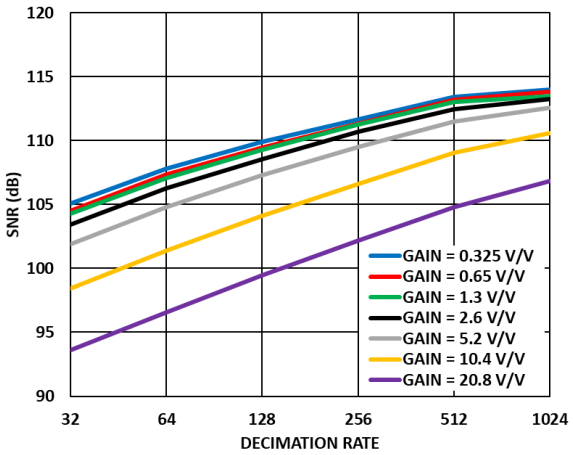

Figure 37. SNR vs Decimation Rate at Various Gain, Wideband Low Ripple FIR Filter, 0.5dBFS, 1KHz.

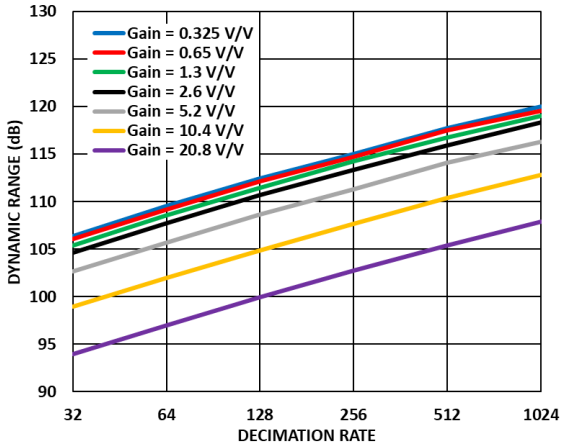

Figure 38. Dynamic Range vs Decimation Rate at Various Gain, Wideband Low Ripple FIR Filter, Shorted Input

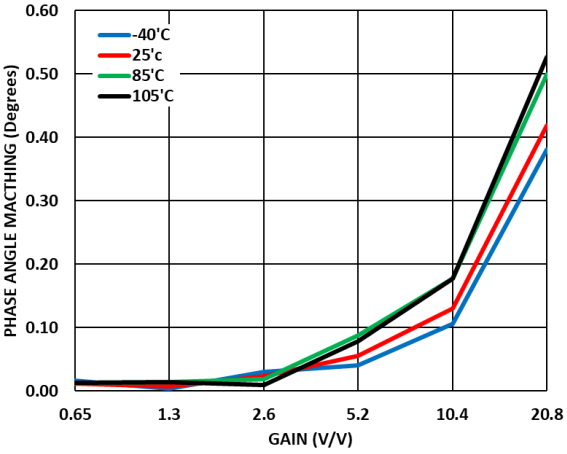

Figure 39. Phase Matching vs PGIA Gain over Temperature, Normalized to Gain = 0.325 V/V

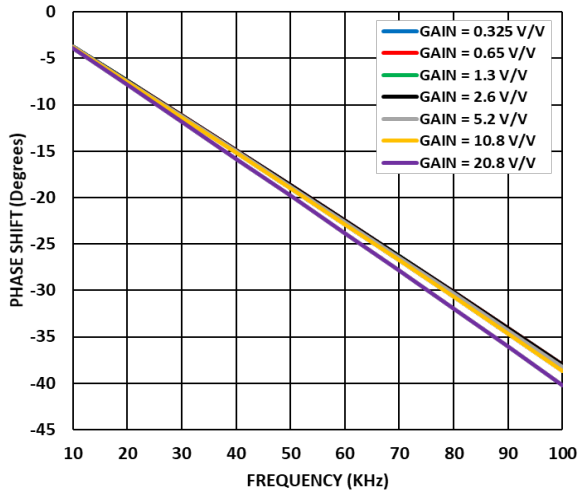

Figure 40. Analog Front End (AFE) Phase Response

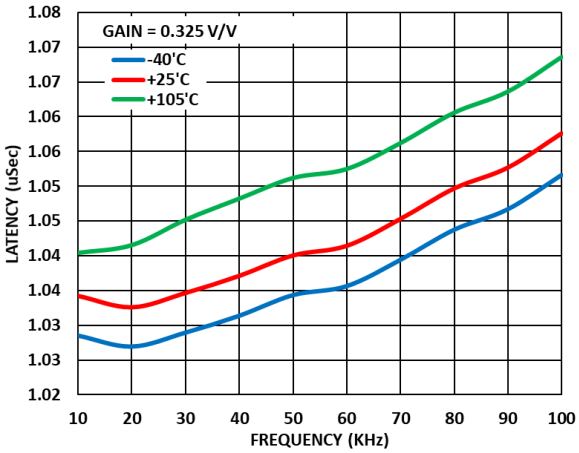

Figure 41. Analog Front End (AFE) Latency vs Frequency across Temperature, Gain = 0.325 V/V

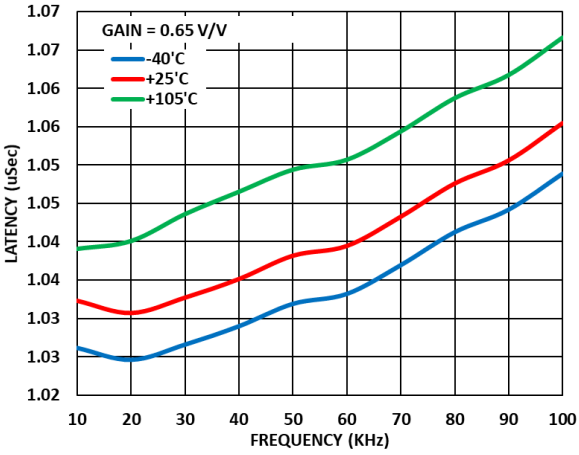

Figure 42. Analog Front End (AFE) Latency vs Frequency across Temperature, Gain = 0.65 V/V

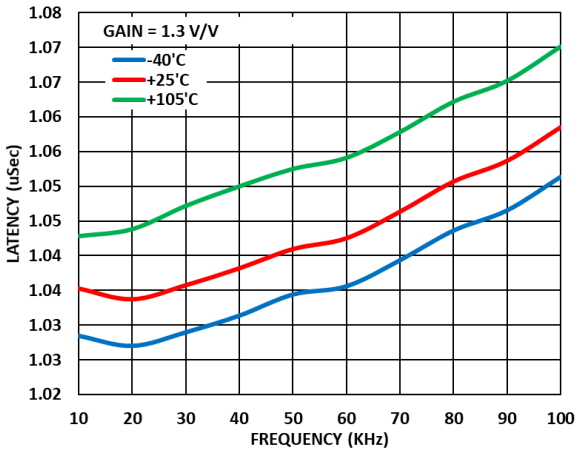

Figure 43. Analog Front End (AFE) Latency vs Frequency across Temperature, Gain = 1.3 V/V

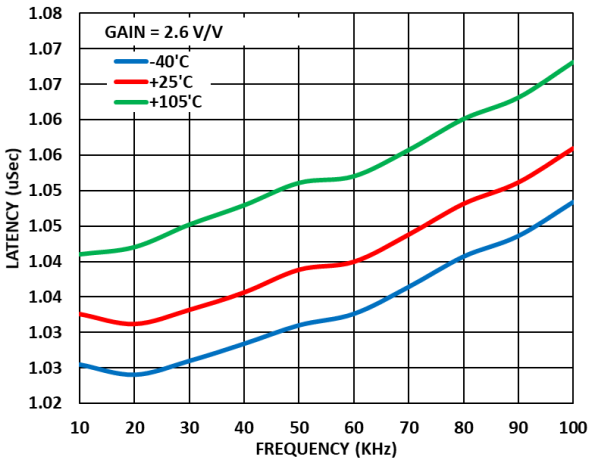

Figure 44. Analog Front End (AFE) Latency vs Frequency across Temperature, Gain = 2.6 V/V

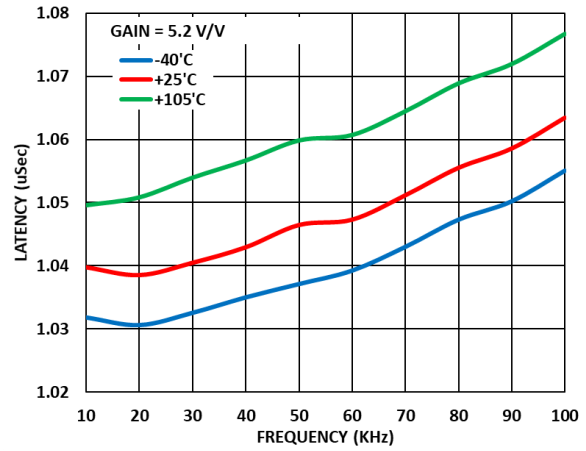

Figure 45. Analog Front End (AFE) Latency vs Frequency across Temperature, Gain = 5.2 V/V

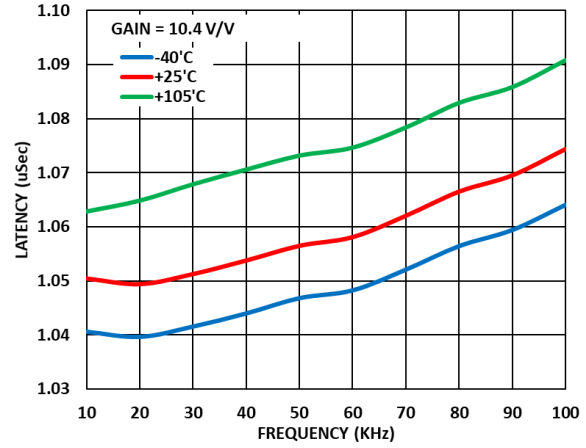

Figure 46. Analog Front End (AFE) Latency vs Frequency across Temperature, Gain = 10.4 V/V

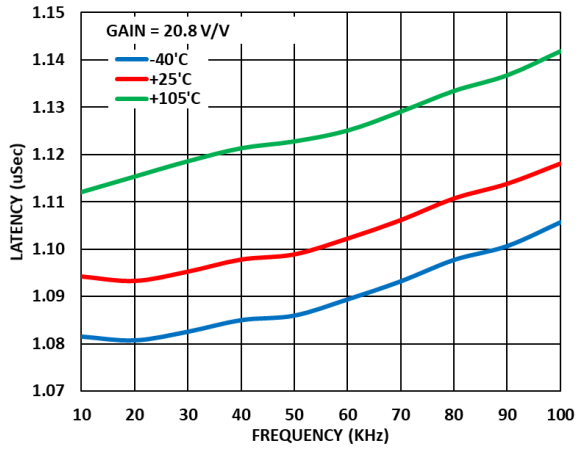

Figure 47. Analog Front End (AFE) Latency vs Frequency across Temperature, Gain = 20.8 V/V

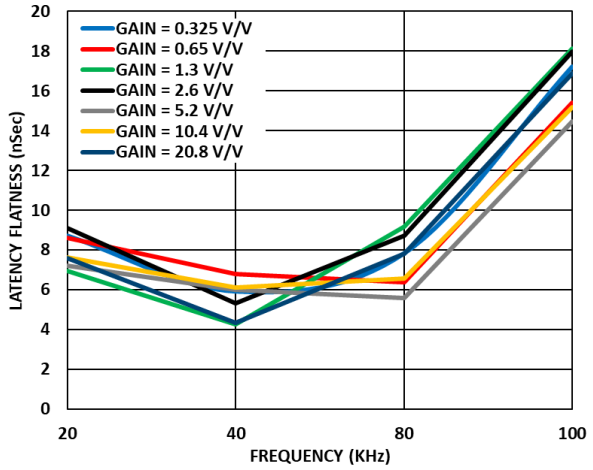

Figure 48. Analog Front End (AFE) Latency Flatness vs Frequency across Gain, Normalized to Latency at 10kHz

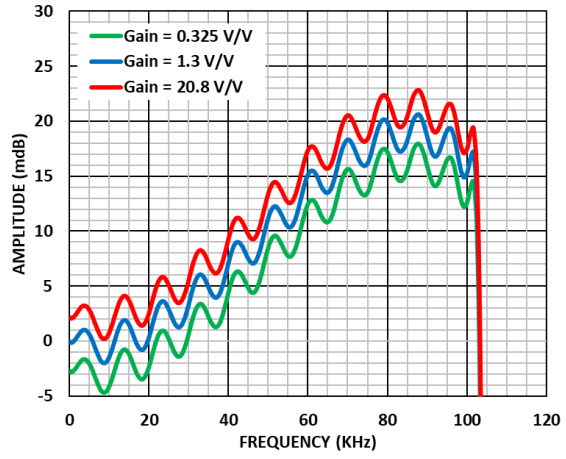

Figure 49. ADAQ7768-1 Wideband Low Ripple FIR Filter Pass-Band Ripple, ODR = 256 kSPS, Normalized to Gain = 1.3 V/V

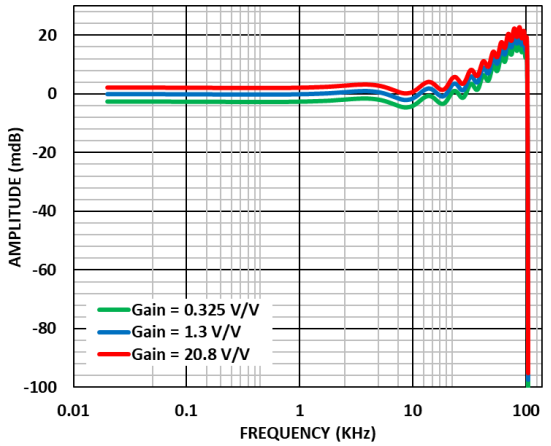

Figure 50. ADAQ7768-1 Magnitude Flatness Response, Wideband Low Ripple FIR Filter, ODR = 256 kSPS, Normalized to Gain = 1.3 V/V

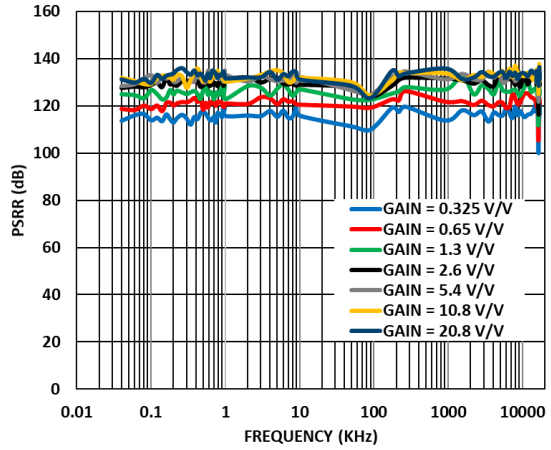

Figure 51. LDO AC PSRR across All Gains, connected to VDD2_PGA, VDD_FDA, VDD_ADC, VDD2_ADC with Internal Supply Decoupling Capacitor

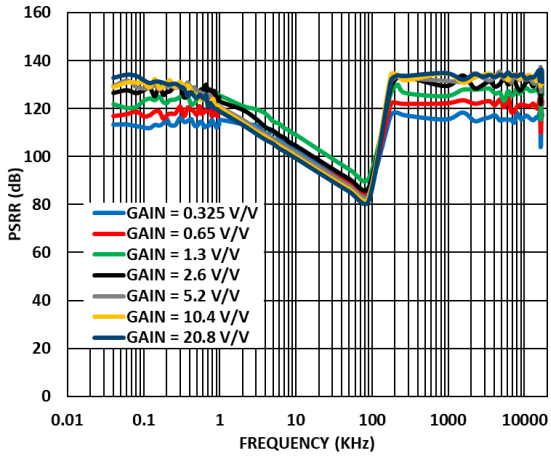

Figure 52. VDD_PGA AC PSSR across All Gains, using the Internal Supply Decoupling Capacitor

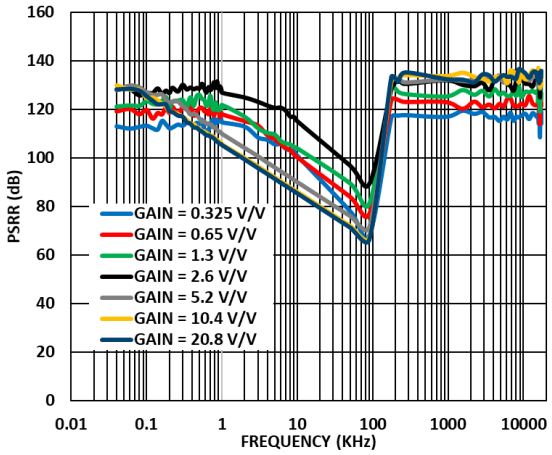

Figure 53. VSS_PGA AC PSSR across All Gains, using the Internal Supply Decoupling Capacitor

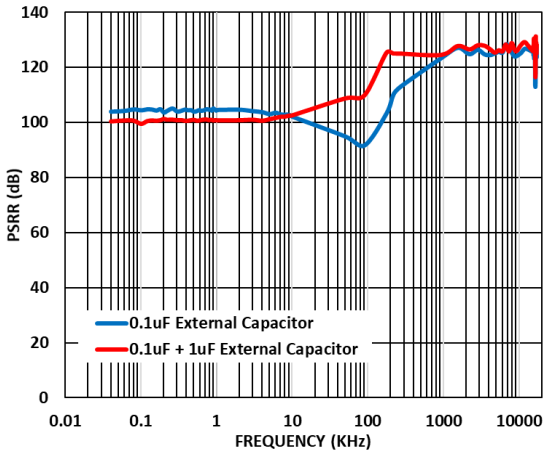

Figure 54. VDD_IO using External Supply Decoupling Capacitor

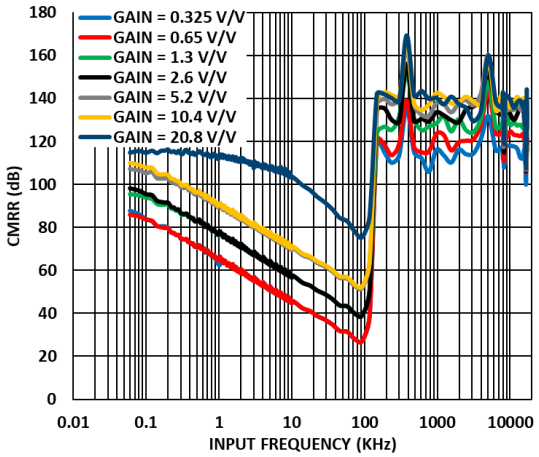

Figure 55. ADAQ7768-1 AC CMRR across all gains

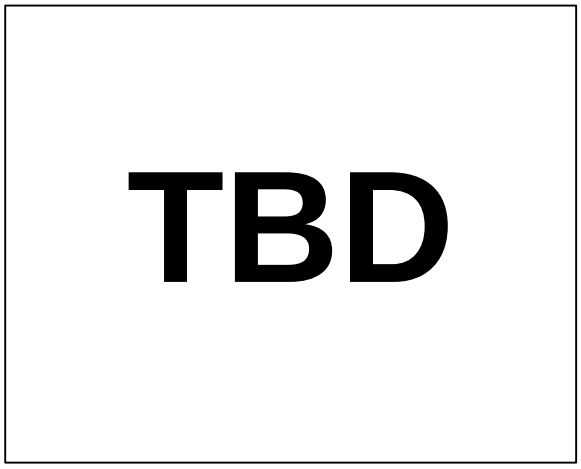

Figure 56

NOISE PERFORMANCE AND RESOLUTION

Table 8, Table 9 and Table 10 show the noise performance for the Wideband Low Ripple FIR, Sinc5 and Sinc3 digital filters of the ADAQ7768-1 for various ODR values and power modes. The specified noise values and dynamic ranges are typical for the bipolar input range with an external 4.096 V reference (V_{REF}). The rms noise is measured with shorted analog inputs to ground reference.

The ratio of the rms shorted input noise to the rms full-scale input signal range calculates the dynamic range.

$$Dynamic\ Range\ (dB) = \frac{V_{REF}}{\sqrt{2}} \div RMS\ Noise$$

$$F_{MOD}(Hz) = \frac{MCLK}{MCLK\ DIV}$$

$$ODR\ (SPS) = \frac{F_{mod}}{DEC\_RATE}$$

MCLK is the ADAQ7768-1 clock frequency
MCLK_DIV = 2
DEC_RATE is the Decimation Rate
F_{mod} Modulator Frequency

Table 8. Wideband Low Ripple FIR Filter Noise for Performance vs. ODR (V_{REF} = 4.096 V, F_{MOD}=MCLK/2)

MCLK (MHz)	Decimation Rate	ODR (kSPS)	–3 dB Bandwidth (kHz)	Gain Mode	Input Range (V)	Shorted Input Dynamic Range (dB)	Input Referred RMS Noise (µV)
16.384	32	256	110.8	Gain0	±12.603	106.4	42.7
16.384	32	256	110.8	Gain1	±6.302	106.1	22.1
16.384	32	256	110.8	Gain2	±3.151	105.4	12.0
16.384	32	256	110.8	Gain3	±1.575	104.6	6.54
16.384	32	256	110.8	Gain4	±0.788	102.6	4.11
16.384	32	256	110.8	Gain5	±0.394	98.9	3.15
16.384	32	256	110.8	Gain6	±0.197	93.9	2.8
16.384	64	128	55.4	Gain0	±12.603	109.5	29.8
16.384	64	128	55.4	Gain1	±6.302	109.2	15.4
16.384	64	128	55.4	Gain2	±3.151	108.6	8.3
16.384	64	128	55.4	Gain3	±1.575	107.7	4.6
16.384	64	128	55.4	Gain4	±0.788	105.7	2.9
16.384	64	128	55.4	Gain5	±0.394	102.0	2.2
16.384	64	128	55.4	Gain6	±0.197	97.7	2.0
16.384	128	64	27.7	Gain0	±12.603	112.4	21.4
16.384	128	64	27.7	Gain1	±6.302	112.1	15.4
16.384	128	64	27.7	Gain2	±3.151	111.4	8.3
16.384	128	64	27.7	Gain3	±1.575	110.7	4.6
16.384	128	64	27.7	Gain4	±0.788	108.6	2.9
16.384	128	64	27.7	Gain5	±0.394	104.9	2.2
16.384	128	64	27.7	Gain6	±0.197	99.9	2.0
16.384	256	32	13.9	Gain0	±12.603	115.0	21.4
16.384	256	32	13.9	Gain1	±6.302	114.7	11.0
16.384	256	32	13.9	Gain2	±3.151	114.3	6.0
16.384	256	32	13.9	Gain3	±1.575	113.4	3.3
16.384	256	32	13.9	Gain4	±0.788	111.3	2.1
16.384	256	32	13.9	Gain5	±0.394	107.7	1.6
16.384	256	32	13.9	Gain6	±0.197	102.7	1.4

MCLK (MHz)	Decimation Rate	ODR (kSPS)	–3 dB Bandwidth (kHz)	Gain Mode	Input Range (V)	Shorted Input Dynamic Range (dB)	Input Referred RMS Noise (µV)
16.384	512	16	6.9	Gain0	±12.603	117.7	15.9
16.384	512	16	6.9	Gain1	±6.302	117.5	8.2
16.384	512	16	6.9	Gain2	±3.151	116.8	4.3
16.384	512	16	6.9	Gain3	±1.575	115.9	2.4
16.384	512	16	6.9	Gain4	±0.788	114.1	1.5
16.384	512	16	6.9	Gain5	±0.394	110.4	1.2
16.384	512	16	6.9	Gain6	±0.197	105.4	1.0
16.384	1024	8	3.5	Gain0	±12.603	120	8.9
16.384	1024	8	3.5	Gain1	±6.302	119.6	4.7
16.384	1024	8	3.5	Gain2	±3.151	119.0	2.5
16.384	1024	8	3.5	Gain3	±1.575	118.3	1.4
16.384	1024	8	3.5	Gain4	±0.788	116.3	0.85
16.384	1024	8	3.5	Gain5	±0.394	112.8	0.64
16.384	1024	8	3.5	Gain6	±0.197	107.9	0.56
13.107	32	204.8	88.7	Gain0	±12.603	106.8	40.8
13.107	32	204.8	88.7	Gain1	±6.302	106.5	21.1
13.107	32	204.8	88.7	Gain2	±3.151	105.8	11.4
13.107	32	204.8	88.7	Gain3	±1.575	105.1	6.22
13.107	32	204.8	88.7	Gain4	±0.788	103.2	3.84
13.107	32	204.8	88.7	Gain5	±0.394	99.7	2.88
13.107	32	204.8	88.7	Gain6	±0.197	94.7	2.55
13.107	64	102.4	44.3	Gain0	±12.603	110.1	28.0
13.107	64	102.4	44.3	Gain1	±6.302	109.8	14.3
13.107	64	102.4	44.3	Gain2	±3.151	109	7.9
13.107	64	102.4	44.3	Gain3	±1.575	108.3	4.3
13.107	64	102.4	44.3	Gain4	±0.788	106.4	2.7
13.107	64	102.4	44.3	Gain5	±0.394	102.8	2.0
13.107	64	102.4	44.3	Gain6	±0.197	97.8	1.8
13.107	128	51.2	22.2	Gain0	±12.603	113.2	19.5
13.107	128	51.2	22.2	Gain1	±6.302	112.9	10.1
13.107	128	51.2	22.2	Gain2	±3.151	112.1	5.5
13.107	128	51.2	22.2	Gain3	±1.575	111.3	3.0
13.107	128	51.2	22.2	Gain4	±0.788	109.4	1.9
13.107	128	51.2	22.2	Gain5	±0.394	105.8	1.4
13.107	128	51.2	22.2	Gain6	±0.197	100.7	1.3
13.107	256	25.6	11.1	Gain0	±12.603	116.2	13.9
13.107	256	25.6	11.1	Gain1	±6.302	115.7	7.3
13.107	256	25.6	11.1	Gain2	±3.151	114.8	4.0
13.107	256	25.6	11.1	Gain3	±1.575	114.1	2.2
13.107	256	25.6	11.1	Gain4	±0.788	112.2	1.37
13.107	256	25.6	11.1	Gain5	±0.394	108.6	1.0
13.107	256	25.6	11.1	Gain6	±0.197	103.2	0.93

Table 9. Sinc5 Filter Noise for Performance vs. ODR (V_{REF} = 4.096 V, F_{MOD}=MCLK/2)

MCLK (MHz)	Decimation Rate	ODR (kSPS)	–3 dB Bandwidth (kHz)	Gain Mode	Input Range (V)	Shorted Input Dynamic Range (dB)	Input Referred RMS Noise (µV)
16.384	8	1024 (16-bit)	208.9	Gain0	±12.603	93.3	192
16.384	8	1024 (16-bit)	208.9	Gain1	±6.302	93.3	96.7
16.384	8	1024 (16-bit)	208.9	Gain2	±3.151	93.2	48.5
16.384	8	1024 (16-bit)	208.9	Gain3	±1.575	93.1	24.7
16.384	8	1024 (16-bit)	208.9	Gain4	±0.788	92.8	12.8

MCLK (MHz)	Decimation Rate	ODR (kSPS)	−3 dB Bandwidth (kHz)	Gain Mode	Input Range (V)	Shorted Input Dynamic Range (dB)	Input Referred RMS Noise (µV)
16.384	8	1024 (16-bit)	208.9	Gain5	±0.394	91.6	7.3
16.384	8	1024 (16-bit)	208.9	Gain6	±0.197	89.1	4.9
16.384	16	512	104.4	Gain0	±12.603	105.8	45.9
16.384	16	512	104.4	Gain1	±6.302	105.5	23.8
16.384	16	512	104.4	Gain2	±3.151	104.8	12.8
16.384	16	512	104.4	Gain3	±1.575	104.0	7.0
16.384	16	512	104.4	Gain4	±0.788	102.1	4.4
16.384	16	512	104.4	Gain5	±0.394	98.6	3.3
16.384	16	512	104.4	Gain6	±0.197	93.7	2.9
16.384	32	256	52.2	Gain0	±12.603	109.8	28.7
16.384	32	256	52.2	Gain1	±6.302	109.5	14.9
16.384	32	256	52.2	Gain2	±3.151	108.7	8.2
16.384	32	256	52.2	Gain3	±1.575	107.9	4.5
16.384	32	256	52.2	Gain4	±0.788	105.8	2.9
16.384	32	256	52.2	Gain5	±0.394	102.1	2.2
16.384	32	256	52.2	Gain6	±0.197	97.0	2.0
16.384	64	128	26.1	Gain0	±12.603	113.0	20.0
16.384	64	128	26.1	Gain1	±6.302	112.7	10.4
16.384	64	128	26.1	Gain2	±3.151	111.8	5.7
16.384	64	128	26.1	Gain3	±1.575	111.0	3.1
16.384	64	128	26.1	Gain4	±0.788	108.9	2.0
16.384	64	128	26.1	Gain5	±0.394	105.1	1.6
16.384	64	128	26.1	Gain6	±0.197	100.0	1.4
16.384	128	64	13.1	Gain0	±12.603	115.9	14.3
16.384	128	64	13.1	Gain1	±6.302	115.6	7.4
16.384	128	64	13.1	Gain2	±3.151	114.9	4.0
16.384	128	64	13.1	Gain3	±1.575	113.9	2.2
16.384	128	64	13.1	Gain4	±0.788	111.8	1.4
16.384	128	64	13.1	Gain5	±0.394	108.0	1.1
16.384	128	64	13.1	Gain6	±0.197	102.9	1.0
16.384	256	32	6.5	Gain0	±12.603	118.8	10.2
16.384	256	32	6.5	Gain1	±6.302	118.6	5.3
16.384	256	32	6.5	Gain2	±3.151	117.7	2.9
16.384	256	32	6.5	Gain3	±1.575	116.8	1.6
16.384	256	32	6.5	Gain4	±0.788	114.6	1.0
16.384	256	32	6.5	Gain5	±0.394	110.8	0.8
16.384	256	32	6.5	Gain6	±0.197	105.6	0.7
13.107	32	204.8	41.8	Gain0	±12.603	110.1	27.8
13.107	32	204.8	41.8	Gain1	±6.302	109.8	14.4
13.107	32	204.8	41.8	Gain2	±3.151	109.1	7.8
13.107	32	204.8	41.8	Gain3	±1.575	108.4	4.2
13.107	32	204.8	41.8	Gain4	±0.788	106.5	2.6
13.107	32	204.8	41.8	Gain5	±0.394	102.9	2.0
13.107	32	204.8	41.8	Gain6	±0.197	97.9	1.8
13.107	64	102.4	20.9	Gain0	±12.603	113.0	19.9
13.107	64	102.4	20.9	Gain1	±6.302	112.9	10.1
13.107	64	102.4	20.9	Gain2	±3.151	112.1	5.5
13.107	64	102.4	20.9	Gain3	±1.575	111.4	3.0
13.107	64	102.4	20.9	Gain4	±0.788	109.5	1.9
13.107	64	102.4	20.9	Gain5	±0.394	105.9	1.4
13.107	64	102.4	20.9	Gain6	±0.197	100.9	1.3

MCLK (MHz)	Decimation Rate	ODR (kSPS)	−3 dB Bandwidth (kHz)	Gain Mode	Input Range (V)	Shorted Input Dynamic Range (dB)	Input Referred RMS Noise (µV)
13.107	128	51.2	51.2	Gain0	±12.603	116.0	14.2
13.107	128	51.2	51.2	Gain1	±6.302	115.7	7.3
13.107	128	51.2	51.2	Gain2	±3.151	115.1	3.9
13.107	128	51.2	51.2	Gain3	±1.575	114.2	2.2
13.107	128	51.2	51.2	Gain4	±0.788	112.3	1.3
13.107	128	51.2	51.2	Gain5	±0.394	108.7	1.0
13.107	128	51.2	51.2	Gain6	±0.197	103.8	0.9
13.107	256	25.6	5.2	Gain0	±12.603	118.7	10.3
13.107	256	25.6	5.2	Gain1	±6.302	118.5	5.3
13.107	256	25.6	5.2	Gain2	±3.151	117.7	2.9
13.107	256	25.6	5.2	Gain3	±1.575	117.0	1.6
13.107	256	25.6	5.2	Gain4	±0.788	115.0	0.99
13.107	256	25.6	5.2	Gain5	±0.394	111.4	0.75
13.107	256	25.6	5.2	Gain6	±0.197	106.4	0.67

Table 10. Sinc3 Filter Noise for Performance vs. ODR (V_{REF} = 4.096 V, F_{MOD}=MCLK/2)

MCLK (MHz)	Decimation Rate	ODR (kSPS)	−3 dB Bandwidth (kHz)	Gain Mode	Input Range (V)	Shorted Input Dynamic Range (dB)	Input Referred RMS Noise (µV)
16.384	32	256	67	Gain0	±12.603	102.9	63.7
16.384	32	256	67	Gain1	±6.302	102.8	32.3
16.384	32	256	67	Gain2	±3.151	102.6	16.6
16.384	32	256	67	Gain3	±1.575	102.3	8.5
16.384	32	256	67	Gain4	±0.788	101.4	4.7
16.384	32	256	67	Gain5	±0.394	99.3	3.0
16.384	32	256	67	Gain6	±0.197	95.2	2.4
16.384	128	64	16.7	Gain0	±12.603	116.5	13.4
16.384	128	64	16.7	Gain1	±6.302	116.3	6.9
16.384	128	64	16.7	Gain2	±3.151	115.6	3.7
16.384	128	64	16.7	Gain3	±1.575	114.8	2.0
16.384	128	64	16.7	Gain4	±0.788	112.1	1.4
16.384	128	64	16.7	Gain5	±0.394	107.9	1.1
16.384	128	64	16.7	Gain6	±0.197	102.6	1.0
16.384	512	16	4.2	Gain0	±12.603	126.1	8.3
16.384	512	16	4.2	Gain1	±6.302	125.4	4.4
16.384	512	16	4.2	Gain2	±3.151	123.8	2.4
16.384	512	16	4.2	Gain3	±1.575	121.3	1.3
16.384	512	16	4.2	Gain4	±0.788	117.3	0.85
16.384	512	16	4.2	Gain5	±0.394	111.6	0.69
16.384	512	16	4.2	Gain6	±0.197	105.8	0.62
16.384	2048	4	1.05	Gain0	±12.603	126.1	4.4
16.384	2048	4	1.05	Gain1	±6.302	125.4	2.4
16.384	2048	4	1.05	Gain2	±3.151	123.8	1.4
16.384	2048	4	1.05	Gain3	±1.575	121.3	0.96
16.384	2048	4	1.05	Gain4	±0.788	117.3	0.76
16.384	2048	4	1.05	Gain5	±0.394	111.6	0.74
16.384	2048	4	1.05	Gain6	±0.197	105.8	0.71
16.384	8192	1	0.26	Gain0	±12.603	128.4	3.4
16.384	8192	1	0.26	Gain1	±6.302	128.0	1.8
16.384	8192	1	0.26	Gain2	±3.151	127.6	0.93
16.384	8192	1	0.26	Gain3	±1.575	126.4	0.53

MCLK (MHz)	Decimation Rate	ODR (kSPS)	−3 dB Bandwidth (kHz)	Gain Mode	Input Range (V)	Shorted Input Dynamic Range (dB)	Input Referred RMS Noise (µV)
16.384	8192	1	0.26	Gain4	±0.788	124.0	0.35
16.384	8192	1	0.26	Gain5	±0.394	119.4	0.30
16.384	8192	1	0.26	Gain6	±0.197	114.3	0.27
16.384	163840	0.05	0.013	Gain0	±12.603	135.5	1.5
16.384	163840	0.05	0.013	Gain1	±6.302	134.0	0.89
16.384	163840	0.05	0.013	Gain2	±3.151	132.3	0.54
16.384	163840	0.05	0.013	Gain3	±1.575	130.6	0.33
16.384	163840	0.05	0.013	Gain4	±0.788	127.0	0.25
16.384	163840	0.05	0.013	Gain5	±0.394	122.0	0.22
16.384	163840	0.05	0.013	Gain6	±0.197	116.4	0.21

THOERY OF OPERATION

ANALOG INPUT

The wide common mode input range and high CMRR of the ADAQ7768-1 allow its IN+ and IN– pins to swing with an arbitrary relationship to each other, allowing the device to accept a wide variety of signal swings, including unipolar and bipolar single ended, pseudo differential and fully differential signals, as shown in Figure 57.

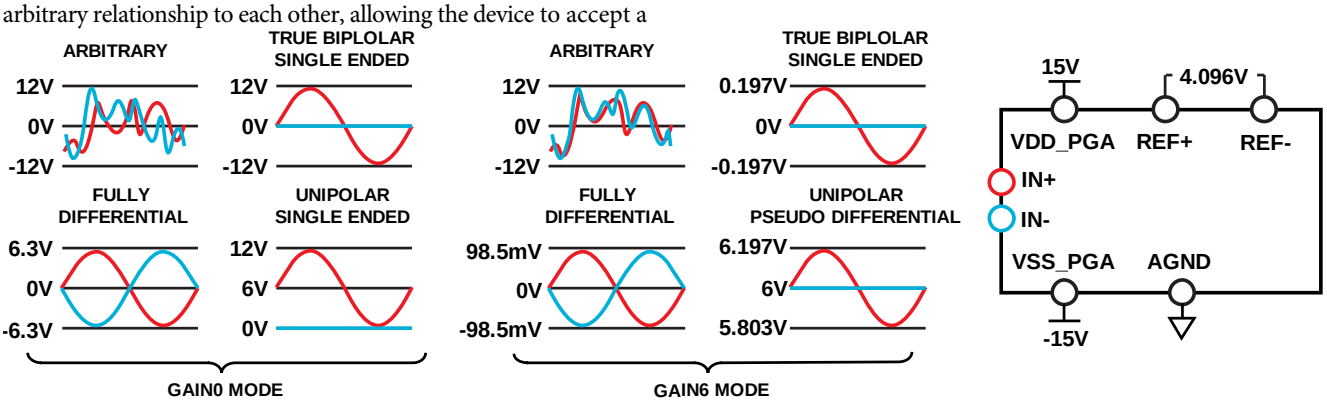

Figure 57. Input Signal Example

Arbitrary Input

The two-tone test shown in Figure TBA demonstrates the arbitrary input drive capability of the ADAQ7768-1. This test simultaneously drives IN+ with a −6dBFS 19.5kHz single-ended sine wave and IN– with a −6dBFS 20.5kHz single-ended sine wave. Together, these signals sweep the analog inputs across a wide range of common mode and differential mode voltage combinations, similar to the more general arbitrary input signal case. They also have a simple spectral representation. An ideal differential converter with no common-mode sensitivity will digitize this signal as two −6dBFS spectral tones, one at each sine wave frequency. The FFT plot in Figure 58 demonstrates the ADAQ7768-1 response approaches this ideal, with TBA dB of SFDR limited by the converter's second harmonic distortion response to the 3.1kHz sine wave on IN–.

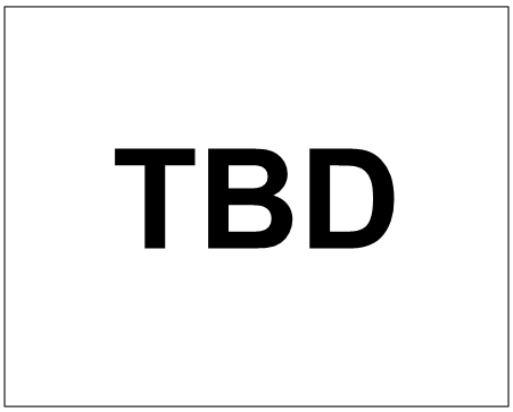

Figure 58. Two-Tone input, IN+ = -6dBFS 19.5kHz Sine, IN– = -6dBFS 20.5kHz Sine, 32k Point FFT, ODR= 256 kSPS, VREF=4.096V, Gain0 Mode.

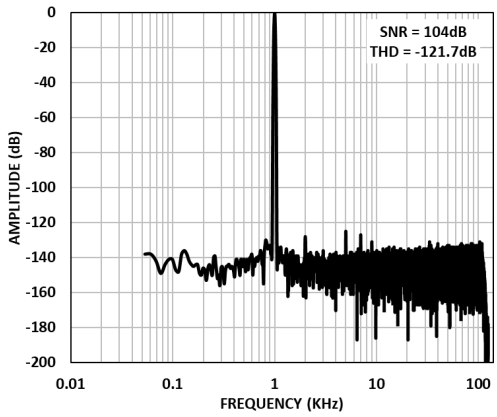

Figure 59. Bipolar Single-ended input, IN+=-0.5dBFS 1kHz Bipolar Sine, IN-=0V, 32k Point FFT, ODR= 256 kSPS, VREF=4.096V, Gain = 0.325V/V.

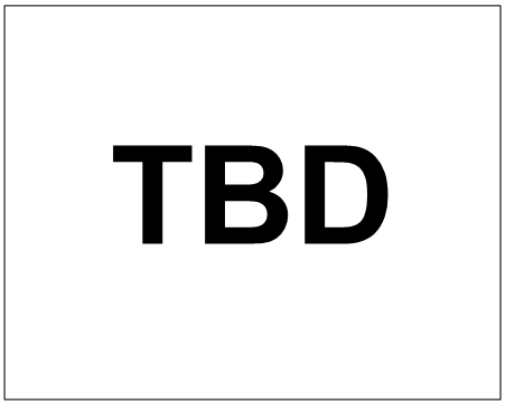

Figure 60. Unipolar Single-ended input, IN+=-0.5dBFS 1kHz Unipolar Sine, IN-=0V, 32k Point FFT, ODR= 256 kSPS, VREF=4.096V, Gain = 0.325V/V.

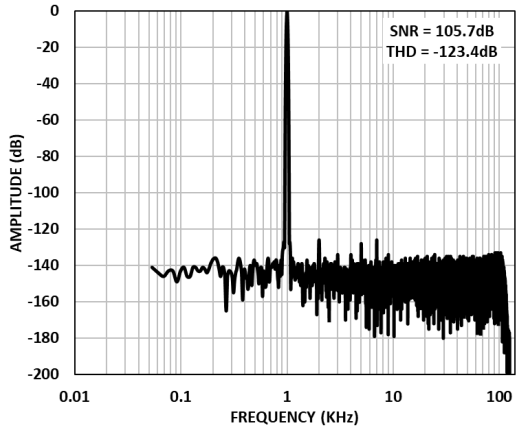

Figure 61. Fully differential input, -0.5dBFS 1kHz Sine, VCM=0V, 32k Point FFT, ODR= 256 kSPS, VREF=4.096V, Gain = 0.325V/V.

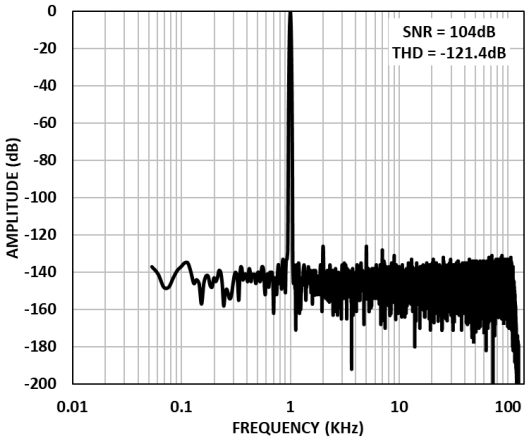

Figure 62. Fully differential input, -0.5dBFS 1kHz Sine, VCM=0V, 32k Point FFT, ODR= 256 kSPS, VREF=4.096V, Gain = 1.3V/V.

TBD

Figure 63. Fully differential input, -0.5dBFS 1kHz Sine, VCM=0V, 32k Point FFT, ODR= 256 kSPS, VREF=4.096V, Gain = 20.8V/V.

ANALOG INPUT RANGE

Absolute Input Range

The absolute voltage on the IN+ and IN- pins are limited to VDD_PGA- TBAV and VSS_PGA+TBAV in all gain mode.

Differential Input Range

The differential signal amplitude depends on the frontend signal gain and the reference voltage level. The maximum differential input voltage can be calculated by:

$$V_{IN+} - V_{IN-} = \pm V_{REF}/GAIN_{AFE}$$

Common Mode Input Range

The input signal common mode range depends on the PGIA supply voltage and the gain mode. Instrumentation amplifiers traditionally specify a valid input common mode range and an output swing range. This however often fails to identify swing limitations associated with internal nodes, as they experience a combination of gained differential signal and common mode signal. The graphs in Figure TBA show the operating region where a valid output is produced for each gain setting of the ADAQ7768-1.

TBD

Figure 64. Input Range Dimond Plot

INPUT RANGE SELECTION

The input range of the ADAQ7768-1 is controlled by its frontend PGIA gain and can be programmed to its desired setting using a digital interface consisting of three parallel gain control pins GAIN0, GAIN1, and GAIN2. The logic threshold for the gain control pins is specified with respect to the AGND pins. Any voltage between AGND and AGND + 0.6V on the gain control pins will generate a logic low (L) state for that pin; any voltage between AGND + 1.4V and VDD_PGA on the gain control pins will generate a logic high (H) state for that pin. The gain of the PGIA and the ADAQ7768-1 input range is programmed according to Table 11. Input Range Selection Truth Table**Error! Reference source not found.**.

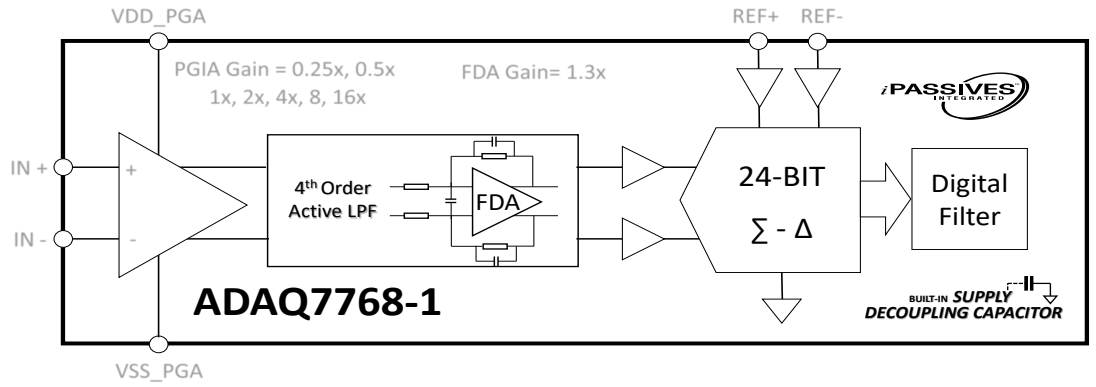

Figure 65. ADAQ7768-1 Top Level Core Signal Chain

Table 11. Input Range Selection Truth Table

Gain mode	GAIN0 pin logic	GAIN1 pin logic	GAIN2 pin logic	PGIA Gain (V/V)	FDA Gain (V/V)	Total Signal Chain Gain (V/V)	Differential Input Range with VREF=4.096V (V)	Common Mode Input Range with Full scale Input Signal VREF=4.096V (V)
Gain0	L	H	H	0.25	1.3	0.325	±12.603	±TBA
Gain1	H	L	H	0.5	1.3	0.65	±6.302	±TBA
Gain2	L	L	H	1	1.3	1.3	±3.151	±TBA
Gain3	H	H	L	2	1.3	2.6	±1.575	±TBA
Gain4	L	H	L	4	1.3	5.2	±0.788	±TBA
Gain5	H	L	L	8	1.3	10.4	±0.394	±TBA
Gain6	L	L	L	16	1.3	20.8	±0.197	±TBA

ANTIALIASING FILTER

The input signal bandwidth of the ADAQ7768-1 is dominated by its digital filter. The user can program the decimation ratio to adjust the digital filter bandwidth. The filter bandwidth can also be fine-tuned through the change of MCLK frequency. For example, with the Wideband Low Ripple FIR filter option and an ODR=256 kSPS, the -3dB bandwidth of the overall signal chain is equal to the digital filter bandwidth of 0.433xODR=110.85 KHz. The same filter has a stop band of 0.499xODR and a minimum stop band attenuation of -105dB. As with any sampled system, the ADAQ7768-1's digital filter does not offer rejection to signals around the signal sampling frequency Fs. As shown in Figure 66, an additional analog anti-aliasing filter is required to reject signals around Fs to prevent out of band signals from folding back to the band of interested.

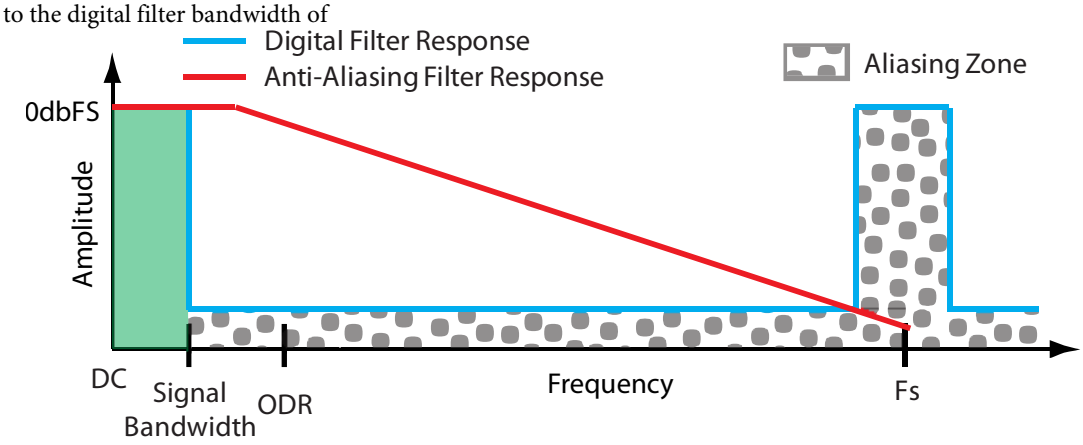

Figure 66. Simplified illustration of the overall frequency response

The digital filter has no rejection to signals within frequency range of Fs+/- F3dB. The ADAQ7768-1's core ADC samples at a frequency of $2xF_{MOD}$. In normal operating mode with $F_{MOD}=F_{MCLK}/2$, the ADC's sampling frequency Fs is equal to F_{MCLK}.

The ADAQ7768-1 features a fourth order analog anti-aliasing filter that is designed to achieve 100dB of rejection at 16.384

MHz. Combining its analog anti-aliasing filter with its Wideband Low Ripple Filter, the ADAQ7768-1 can reject all of the out of band signals by a minimum of 105dB.

Magnitude and Phase Response

The anti-aliasing filter is designed to achieve optimal aliasing rejection level with minimum magnitude and phase distortion to the in-band signal. With the help of ADI's iPASSIVES™ technology, the filter has a highly stable -3dB corner at 330kHz. Its typical magnitude droop is 2.3mdB at 20kHz and 20mdB at 100kHz. The filter's passband phase response in the passband is also highly linear. And the tightly controlled -3dB point of the filter gives the ADAQ7768-1 a superior device to device phase matching performance, as shown in Figure 70. Device to Device Phase Matching Histogram

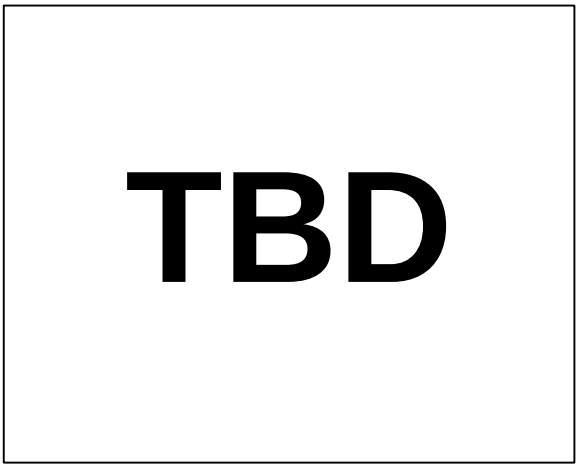

Figure 69. Group Delay vs. Frequency

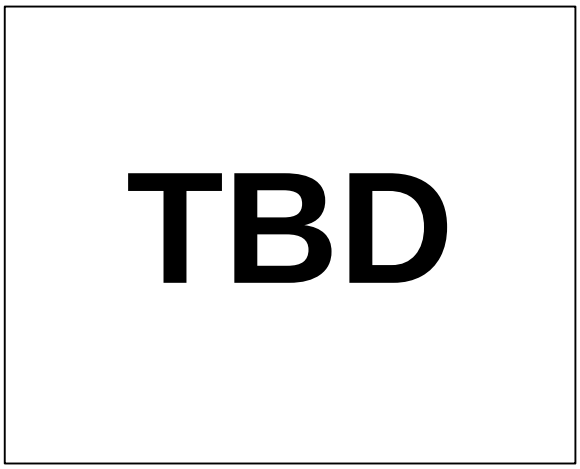

Figure 67. AAF frequency response.

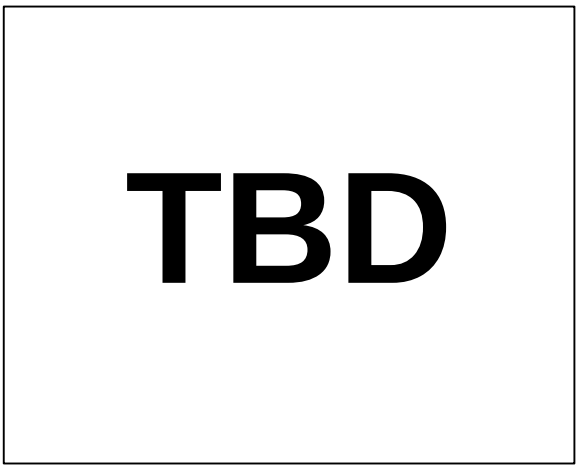

Figure 70. Device to Device Phase Matching Histogram

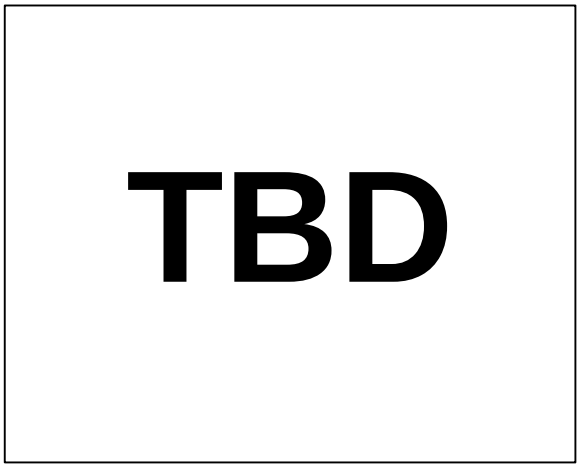

Figure 68. AAF passband droop

FDA POWER MODE

The ADAQ7768-1 Fully Differential Amplifier (FDA) is a low noise, low distortion amplifier that can drive high resolution and high performance Σ - Δ analog-to-digital converters (ADC).

The FDA two selectable power modes are Low Power Mode and High Power Mode. The FDA Low Power Mode is ideal for DC input applications due to its low 1/f noise at low gain settings, 0.325 V/V and 0.65 V/V system gains. The High Power Mode offers better linearity performance at a higher current consumption.

Figure 74, shows the connection between FDA_M0, FDA_M1, and ADC_M0, ADC_M1. The connection sets the FDA to Eco Power Mode. To set the FDA to Full Power Mode, the FDA_M0 needs to be pulled to VDD_IO via a pull up resistor, while keeping the FDA_M1 and ADC_M1 connected as shown on Figure 72.

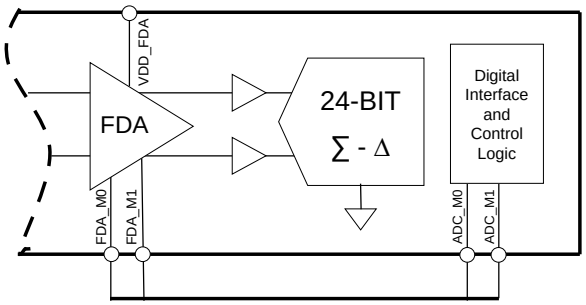

Figure 71. FDA Eco Power Mode Connection

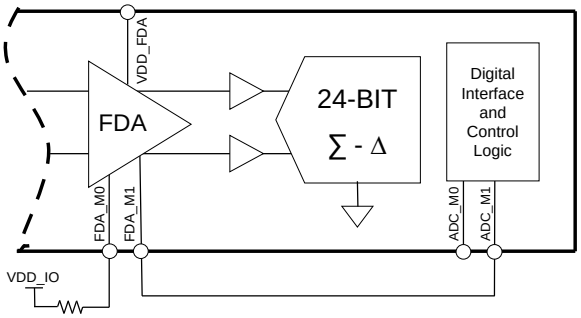

Figure 72. FDA Full Power Mode Connection

LINEARITY BOOST BUFFER

The ADAQ7768-1 has a pair of linearity boost buffer placed in between the driver amplifier and the core ADC. The user has the option to turn them on to boost the linearity performance of the device. The linearity boost buffer adds no noise to the signal chain performance and consumes additional 2mA typical current on the VDD_ADC supply.

The linearity boost buffers are enabled by default. The user can turn them off in SPI control mode by setting the LINEARITY_BOOST_A_OFF and LINEARITY_BOOST_B_OFF (Bits[1:0] in Register 0x16) to zero. The linearity buffers are always enabled in $\overline{\text{PIN}}$control mode.

REFERENCE INPUT AND BUFFERING

The ADAQ7768-1 has differential reference inputs, REF+ and REF−. The absolute input reference voltage range is from 1 V to VDD_ADC − AGND.

The reference inputs can be configured for a fully buffered input on each of the REF+ and REF− pins, a precharge buffered input, or to bypass both buffers.

Use of either the full buffers or the precharge buffers reduces the burden on the external reference when driving large loads or multiple devices. The fully buffered input to the reference pins provides a high impedance input node and enables use of the ADAQ7768-1 in ratiometric applications where the ultralow source impedance of a traditional external reference is not available.

In $\overline{\text{PIN}}$ control mode, the reference precharge buffers are on by default. In SPI mode, the user can choose fully buffered or precharge buffers.

The reference input current scales linearly with the modulator clock rate.

For MCLK = 16.384 MHz in fast mode, the differential input voltage is ~80 µA/V unbuffered and 20 µA/V with the precharge buffers enabled.

With the precharge buffers off, REF+ = 5 V and REF− = 0 V.

$$REF\pm = 5\text{ V} \times 80\ \mu\text{A/V} = +400\ \mu\text{A}$$

With the precharge buffers on, REF+ = 5 V, and REF− = 0 V.

$REF\pm$ = approximately 20 µA

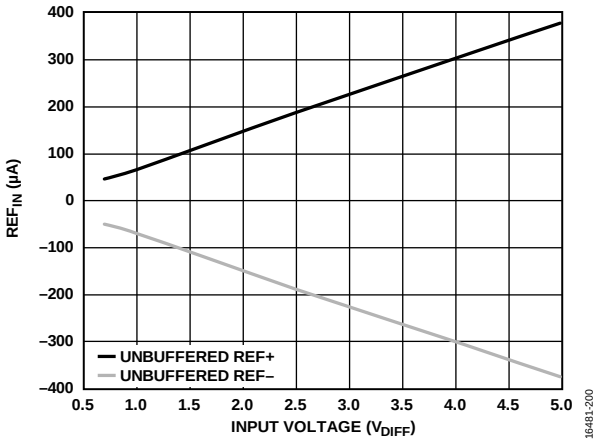

Figure 73. Reference Input Current (REF_{IN}) vs. Input Voltage, Unbuffered REF+ and REF−

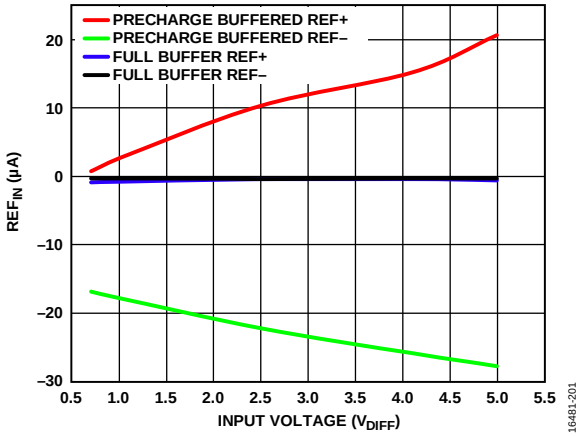

Figure 74. Reference Input Current (REF_{IN}) vs. Input Voltage, Precharge Buffered REF+ and REF− and Full Buffer REF+ and REF−

For the best performance and headroom, use a 4.096 V reference, such as the ADR444 or ADR4540, that can both be supplied by a 5 V rail and shared to the VDD_ADC supply.

A reference detect function is available in SPI control mode. See the Reference Detection section for details.

CORE CONVERTER

The ADAQ7768-1 can use up to a 5 V reference and converts the differential voltage between the analog inputs with the differential input range of +/-V_{REF}/ $GAIN_{AFE}$ to a digital output. The 24-bit conversion result is in MSB first, twos complement

format. Figure 75 shows the ideal transfer functions for the ADAQ7768-1.

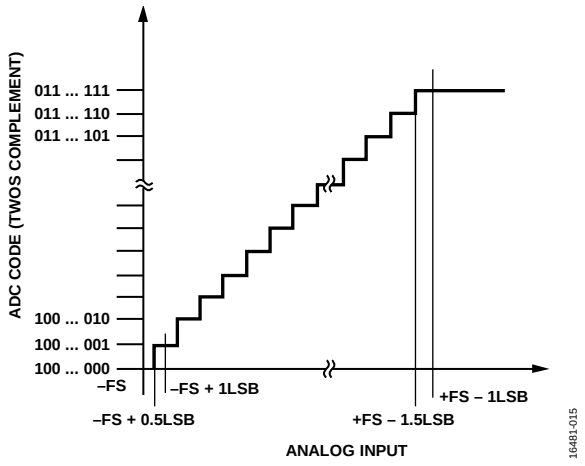

Figure 75. ADC Ideal Transfer Functions (FS is Full-Scale)

Table 12. Output Codes and Ideal Input Voltages

Description	Analog Input (IN+ – IN–) (V)	Digital Output Code, Twos Complement (Hex)
FS – 1 LSB	+VREF/AFE_GAIN	0x7FFFFF
Midscale + 1 LSB	+VREF/AFE_GAIN/2^{23}	0x000001
Midscale	0	0x000000
Midscale – 1 LSB	-VREF/AFE_GAIN /2^{23}	0xFFFFFF
–FS + 1 LSB	-VREF/AFE_GAIN *(1-1/2^{23})	0x800001
–FS	-VREF/AFE_GAIN	0x800000

POWER SUPPLIES

The ADAQ7768-1 has several power supplies to power the analog front end and the ADC, and to simplify the connection, the ADAQ7768-1 have an internal LDO that can be used to supply the voltage of the VDD_ADC, VDD2_PGA, and VDD_FDA. The LDO can also power the ADR4540 reference for the REF+ and REF- pins. The LDO input can handle inputs ranges of 5.1v to 5.5v. For proper operation it is recommended to use 1uF capacitor at the input and output of the LDO. In case the LDO is not used during normal operation, it is recommended to keep all the LDO pins floating.

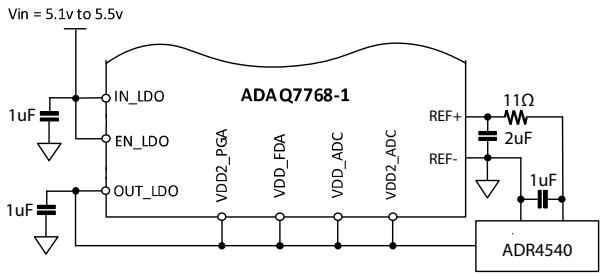

Figure 76. ADAQ7768-1 power supply connection using internal LDO

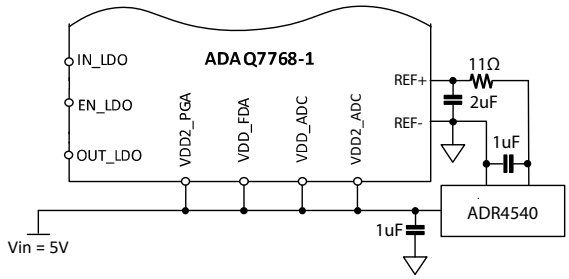

Figure 77. Float IN_LDO and OUT_LDO pins when not used

The VDD_PGA and VSS_PGA supplies power to the frontend amplifiers of the PGIA.

The VDD2_PGA supplies the PGIA output driver with the positive supply. The return current of the output driver flows back through the VSS_PGA.

The VDD_ADC supply powers the linearity boost buffer, core ADC frontend and reference input.

The VDD_FDA supply power to the ADC driver

The VDD2_ADC supply connects to an internal 1.8 V analog LDO regulator. This regulator powers the ADC core. VDD2_ADC – AGND can range from 5.5 V (maximum) to 2.0 V (minimum).

VDD_IO powers the internal 1.8 V digital LDO regulator. This regulator powers the digital logic of the ADC. VDD_IO sets the voltage levels for the SPI interface of the ADC. VDD_IO is referenced to DGND, and VDD_IO – DGND can vary from 3.6 V (maximum) to 1.7 V (minimum).

POWER SUPPLY DECOUPLING

The ADAQ7768-1 has a built-in 0.1uF supply decoupling capacitors on VDD_PGA, VSS_PGA, VDD2_PGA, VDD_FDA, VDD_ADC and VDD2_ADC supply pins. Together with the internal LDO, these features minimize the needed component to operate the ADAQ7768-1.

Figure 78, shows the AC PSRR of the internal LDO while it is connected to VDD2_PGA, VDD_FDA, VDD_ADC with the internal supply decoupling capacitor and the recommended 1uF decoupling capacitor at the OUT_LDO pin, as shown in Figure 76.

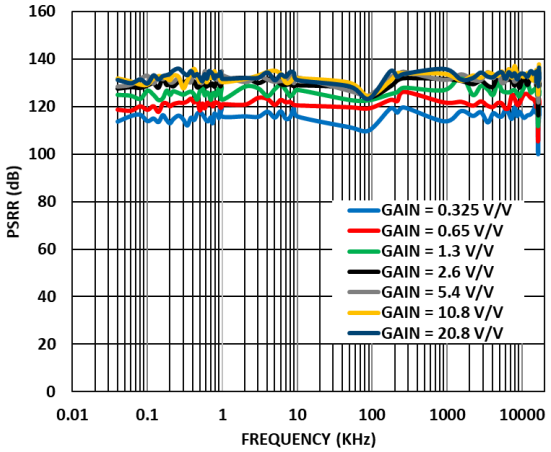

Figure 78. LDO AC PSRR, using internal decoupling capacitor of VDD2_PGA, VDD_FDA, VDD_ADC, VDD2_ADC

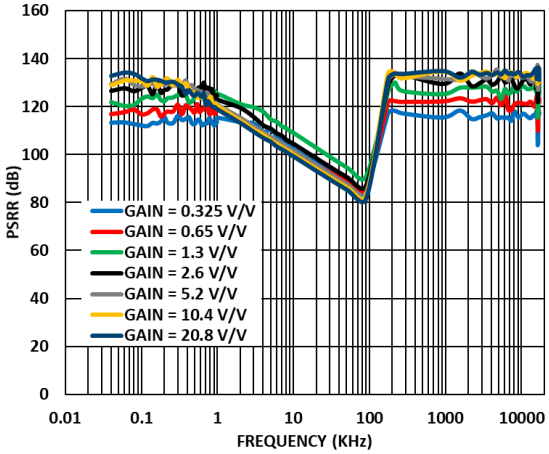

Figure 79. VDD_PGA AC PSSR vs all gains, using the internal 0.1uF supply decoupling capacitor

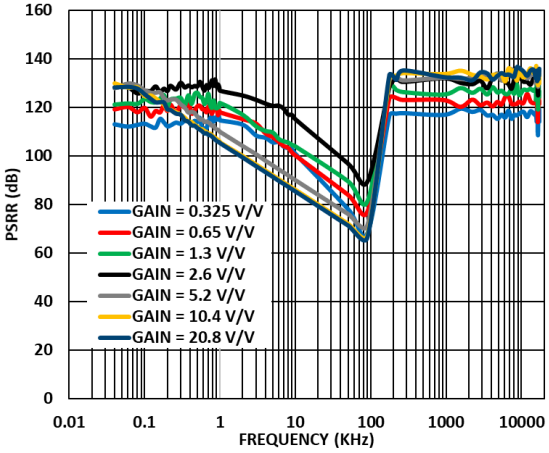

Figure 80. VSS_PGA AC PSSR vs all gains, using the internal 0.1uF supply decoupling capacitor

Only the VDD_IO requires external decoupling capacitor. Figure 81, shows the AC PSRR of the VDD_IO supply pin using 0.1uF external supply decoupling capacitor and the AC PSRR with additional 1uF supply decoupling capacitor.

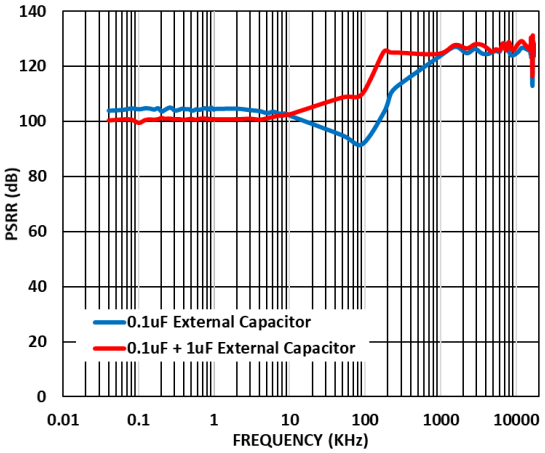

Figure 81. VDD_IO AC PSRR using 0.1uF and additional 1uF supply decoupling capacitor

POWER STANBY

Each functional block of the ADAQ7768-1 can be put into standby mode. The device can achieve TBD W of total power consumption while all functional blocks are put into standby mode.

CLOCKING AND SAMPLING TREE

The ADAQ7768-1 core ADC receives a master clock signal (MCLK). The MCLK signal can be sourced from one of four options: a CMOS clock, a crystal connected between the XTAL1 and XTAL2 pins, an LVDS signal, and the internal clock. The MCLK signal received by the ADAQ7768-1 defines the core ADC's sigma delta modulator clock rate (F_{MOD}) and, in turn, the sampling frequency of the modulator of $2 \times F_{MOD}$.

$$F_{MOD} = \frac{MCLK}{MCLK\ DIV}$$

To determine F_{MOD}, select one of four clock divider settings: MCLK/2, MCLK/4, MCLK/8, or MCLK/16. For example, to maximize the ODR or input bandwidth, an MCLK rate of 16.384 MHz is required. Select an MCLK divider (MCLK_DIV) equal to 2 for a modulator frequency of 8.192 MHz.

Control of the settings for the modulator frequency differ in $\overline{\text{PIN}}$ control mode vs. SPI control mode.

In $\overline{\text{PIN}}$ control mode, the MODEx pins determine the modulator frequency. The MODEx pins are also used to select the filter type and decimation rate. Refer to Table 20. Control Settings for MODEx Pins. For $\overline{\text{PIN}}$ control mode setting for MODEx pins.

It is recommended to keep the F_{MOD} frequency high to maximize the out of band tone rejection from the frontend anti-aliasing filter. Increase the decimation ratio if low input bandwidth is required.

CLOCKING AND CLOCK SELECTION

The ADAQ7768-1 has an internal oscillator that is used for initial power-up of the device. After the ADAQ7768-1 completes the start-up routine, a clock handover occurs to the external MCLK. The ADAQ7768-1 counts the falling edges of the external MCLK over a given number of internal clock cycles to determine if the clock is valid and of a frequency of at least 600 kHz. If there is a fault with the external MCLK, the handover does not occur, the ADAQ7768-1 clock error bit is set, and the ADAQ7768-1 continues to operate from the internal clock.

In SPI control mode, use the clock source bits in POWER_CLOCK register (Register 0x15) to set the external MCLK source. Four clock options are available: internal oscillator, external CMOS, crystal oscillator, or LVDS. If selecting the LVDS clock option, the clock source must be selected using the CLOCK_SEL bits (Bits[7:6] in Register 0x15).

In $\overline{\text{PIN}}$ control mode, the CLK_SEL pin sets the external MCLK source. Three clock options are available in $\overline{\text{PIN}}$ control mode: an internal oscillator, an external CMOS, or a crystal oscillator. The CLK_SEL pin is sampled on power-up.

Set the EN_ERR_EXT_CLK_QUAL bit (Bit 0 in Register 0x29) to turn off the clock qualification. Turning off the clock qualification allows the use of slower external MCLK rates outside the recommended MCLK frequency.

CLK_SEL Pin

If CLK_SEL = 0 in $\overline{\text{PIN}}$ control mode, the CMOS clock option is selected and must be applied to the MCLK pin. In this case, tie the XTAL1 pin to DGND.

If CLK_SEL = 1 in $\overline{\text{PIN}}$ control mode, the crystal option is selected and must be connected between the XTAL1 and XTAL2 pins.

In SPI control mode, the CLK_SEL pin does not determine the MCLK source used and CLK_SEL must be tied to DGND.

Using the Internal Oscillator

In some cases, conversion using an internal clock oscillator may be preferred, such as in isolated applications where dc input voltages must be measured. Converting ac signals with the internal clock is not recommended because using the internal clock can result in degradation of SNR due to jitter.

DIGITAL FILTERING

The ADAQ7768-1 offers three types of digital filters. The digital filters available on the ADAQ7768-1 are

- Wideband Low Ripple FIR filter, −3 dB at 0.433 × ODR (6 rates)
- Sinc5 low latency filter, −3 dB at 0.204 × ODR (8 rates)
- Sinc3 low latency filter, −3 dB at 0.2617 × ODR, widely programmable data rate

Decimation Rate Control

The ADAQ7768-1 has programmable decimation rates for the Sinc3 , Sinc5 and Wideband Low Ripple FIR digital filters. The decimation rates allow the user to band limit the measurement, which reduces the speed and input bandwidth, but increases the resolution because there is further averaging in the digital filter. Control of the decimation rate on the ADAQ7768-1 when using the SPI control is set in the DIGITAL_FILTER register (Register 0x19) for the Sinc5 and Wideband Low Ripple FIR filters.

The decimation rate of the Sinc3 filter is controlled using the SINC3_DEC_RATE_LSB register (Register 0x1A) and the SINC3_DEC_RATE_MSB register (Register 0x1B). These registers combine to provide 13 bits of programmability. The decimation rate is set by incrementing the value in these registers by one and multiplying the value by 32. For example, setting a value of 0x5 in the SINC3_DEC_RATE_LSB register results in a decimation rate of 192 for the Sinc3 filter.

In $\overline{\text{PIN}}$ control mode, the MODE0 pin controls the decimation ratio. Only decimation rates of ×32 and ×64 are available for use with the Sinc5 and wideband filter options. See Table 20 for the full list of options available in $\overline{\text{PIN}}$ control mode.

Table 13. Decimation Rate Options

	Available Decimation Rates	
Filter Option	**SPI Control Mode**	**Pin Control Mode**
Wideband Low Ripple FIR	×32, ×64, ×128, ×256, ×512, ×1024	×32, ×64
Sinc5	×8, ×16, ×32, ×64, ×128, ×256, ×512, ×1024	×8, ×32, ×64
Sinc3	Programmable decimation rate	50 Hz and 60 Hz output only, based on a 16.384 MHz MCLK

Wideband Low Ripple FIR Filter

The FIR filter is a Wideband Low Ripple, input pass-band up to 0.433 × ODR. The Wideband Low Ripple FIR filter has almost full attenuation at 0.5 × ODR (Nyquist), maximizing anti-alias protection. Figure 83 shows the ADAQ7768-1 Wideband Low Ripple FIR filter pass band ripple of 2.3mdB up to 20kHz and 20mdB up to 100kHz. The Wideband Low Ripple FIR filter is a 64-order digital filter. The group delay of the filter is 34/ODR. After a sync pulse, there is an additional delay from the $\overline{\text{SYNC\_IN}}$ rising edge to fully settled data. The time from a $\overline{\text{SYNC\_IN}}$ pulse to both the first $\overline{\text{DRDY}}$ and to fully settled data for various ODR values is shown in Table 14.

The Wideband Low Ripple FIR filter can be selected in one of six different decimation rates, allowing the user to choose the optimal input bandwidth and speed of the conversion vs. the desired resolution.

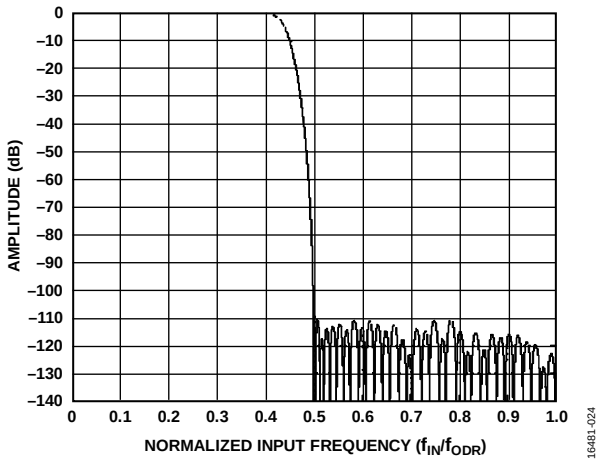

Figure 82. Low Ripple FIR Filter Frequency Response

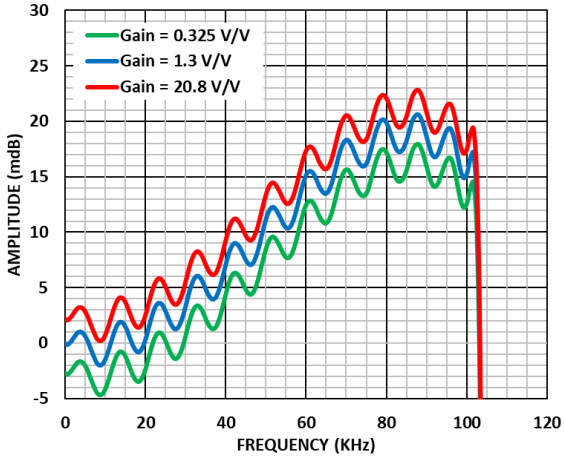

Figure 83. ADAQ7768-1 Wideband Low Ripple FIR Filter Pass-Band Ripple, Normalized to Gain = 1.3 V/V

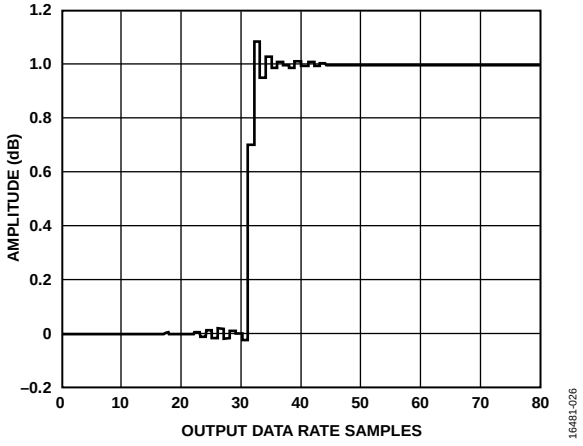

Figure 84. Wideband Low Ripple FIR Filter Step Response

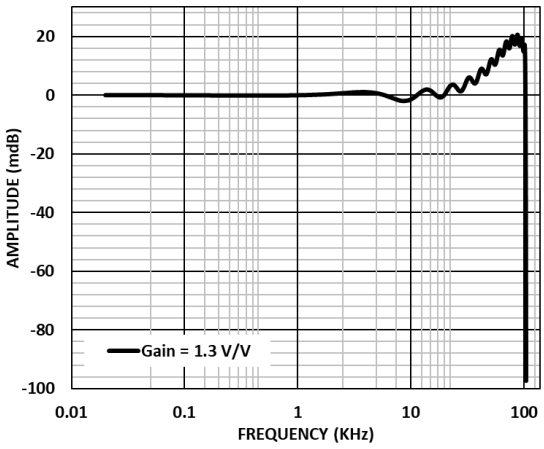

Figure 85. ADAQ7768-1 Wideband Low Ripple FIR Filter Magnitude Flatness, Gain = 1.3 V/V Normalized. 256 kSPS ODR

Figure 85, shows the ADAQ7768-1 magnitude flatness using Wideband Low Ripple FIR filter at 256kSPS ODR. Using the calculation below the Wideband Low Ripple FIR filter offers -0.1dB attenuation up to 104.7KHz as seen in Figure 86.

$$-0.1dB\ Passband = 0.406\ x\ ODR\ =\ 104.7KHz$$

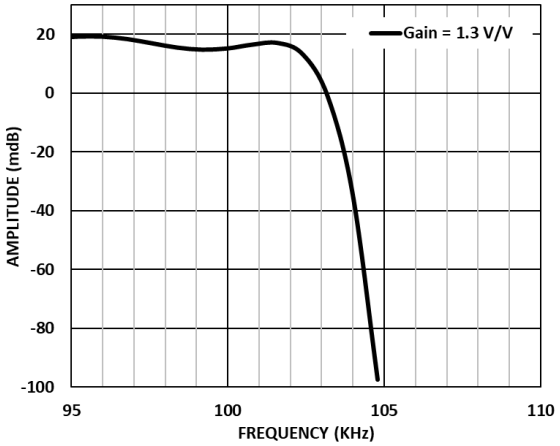

Figure 86. ADAQ7768-1 Wideband Low Ripple FIR Filter, -0.1dB Pass Band

Table 14. Low Ripple FIR Filter $\overline{\text{SYNC\_IN}}$ to Settled Data

MCLK Divide Setting	Decimation Ratio	ODR (kSPS)		MCLK Periods	
		MCLK = 16.384 MHz	MCLK = 13.107 MHz	Delay from First MCLK Rise After $\overline{\text{SYNC\_IN}}$ Rise to First $\overline{\text{DRDY}}$ Rise	Delay from First MCLK Rise After $\overline{\text{SYNC\_IN}}$ Rise to Earliest Settled $\overline{\text{DRDY}}$ Rise
MCLK/2	32	256	204.8	284	4,252
	64	128	102.4	413	8,349
	128	64	51.2	797	16,669
	256	32	25.6	1,565	33,309
	512	16	12.8	3,101	66,589
	1024	8	6.4	6,157	133,133
MCLK/4	32	128	102.4	428	8,364
	64	64	51.2	812	16,684
	128	32	25.6	1,580	33,324
	256	16	12.8	3,116	66,604
	512	8	6.4	6,188	133,164
	1024	4	3.2	12,300	266,252
MCLK/16	32	32	25.6	1,674	33,418
	64	16	12.8	3,202	66,690
	128	8	6.4	6,274	133,250
	256	4	3.2	12,418	266,370
	512	2	1.6	24,706	532,610
	1024	1	0.8	49,154	1,064,962

Sinc5 Filter

The Sinc5 filter offered in the ADAQ7768-1 enables a low latency signal path useful for dc inputs on control loops, or for where user specific post processing is required. The Sinc5 filter has a −3 dB bandwidth of 0.204 × ODR. Table 9 shows the noise performance for the Sinc5 filter across power modes and decimation ratios.

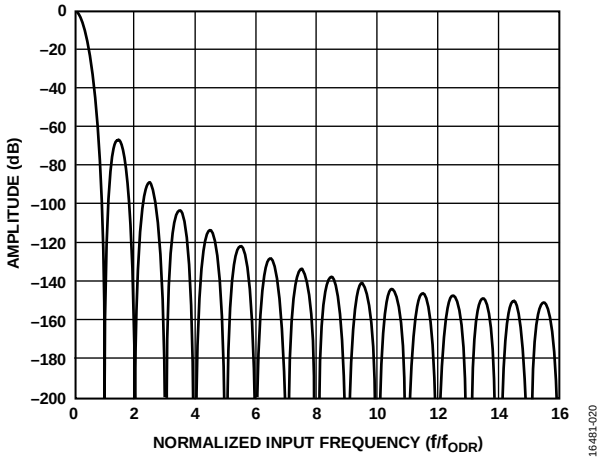

Figure 87. Sinc Filter Frequency Response

The impulse response of the filter is five times the ODR. For 250 kSPS ODR, the time to settle data fully is 20 µs. For the 1 MSPS ODR, the time to settle data fully is 5 µs.

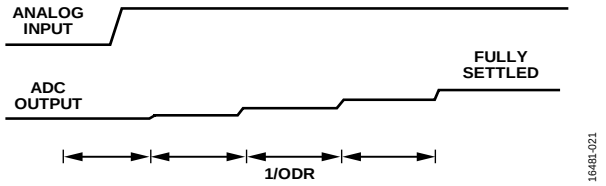

Figure 88. Sinc5 Filter Step Response

The time from a $\overline{\text{SYNC\_IN}}$ pulse to both the first $\overline{\text{DRDY}}$ and to fully settled data for various ODR values for the Sinc5 filter is shown in Table 15.

Table 15. Sinc5 Filter, $\overline{SYNC\_IN}$ to Settled Data

MCLK Divide Setting	Decimation Ratio	ODR (kSPS)		MCLK Periods	
		MCLK = 16.384 MHz	MCLK = 13.107 MHz	Delay from First MCLK Rise After $\overline{SYNC\_IN}$ Rise to First $\overline{DRDY}$ Rise	Delay from First MCLK Rise After $\overline{SYNC\_IN}$ Rise to Earliest Settled $\overline{DRDY}$ Rise
MCLK/2	8	1024	819.2	46	110
	16	512	409.6	62	190
	32	256	204.8	94	350
	64	128	102.4	162	674
	128	64	51.2	295	1,319
	256	32	25.6	561	2,609
	512	16	12.8	1,093	5,189
	1024	8	6.4	2,173	10,365
MCLK/4	8	512	409.6	79	207
	16	256	204.8	111	367
	32	128	102.4	175	687
	64	64	51.2	310	1,334
	128	32	25.6	576	2,624
	256	16	12.8	1,108	5,204
	512	8	6.4	2,172	10,364
	1024	4	3.2	4,332	20,716
MCLK/16	8	128	102.4	278	790
	16	64	51.2	406	1,430
	32	32	25.6	662	2,710
	64	16	12.8	1,194	5,290
	128	8	6.4	2,258	10,450
	256	4	3.2	4,386	20,770
	512	2	1.6	8,642	41,410
	1024	1	0.8	17,282	82,818

Programming for 1.024MSPS Output Data Rate

The Sinc5 FIR filter on ADAQ7768-1 is capable of 1.024MSPS output data rate for 16.384MHz MCLK, this would allow viewing of wider bandwidth with the filter cutoff at 208.9KHz.

To configure the Sinc5 FIR filter for 1.024MSPS output data rate, write 001 to FILTER bits [6:4] of DIGITAL_FILTER register (Register 0x19). The ADAQ7768-1 automatically changes the decimation rate to 8 and output data length is reduced to 16 bits from 24 bits due to the maximum speed limitation of digital serial interface.

For example, to program the ADAQ7768-1 to 1.024MSPS output data rate from power up using 16.384MHz MCLK, while using the CMOS_MCLK as the clock source, the subsequent SPI writes below can be used.

- Data 0x33 to Register 0x15
- Data 0x10 to Register 0x19

Sinc3 Filter

The Sinc3 filter offered in the ADAQ7768-1 enables a low latency signal path useful for dc inputs on control loops, or for eliminating unwanted known interferers at specific frequencies. The Sinc3 filter path incorporates a programmable decimation rate to achieve rejection of known interferers. Decimation rates from 32 to 185,280 are achievable using the Sinc3 filter. The Sinc3 filter has a −3 dB bandwidth of 0.2617 × ODR. Table 16 and Table 17 show the minimum rejection measured at the frequencies of interest with a 50 Hz ODR.

For example, to calculate for a 16.384 MHz MCLK to achieve an ODR of 50 Hz using the Sinc3 filter, use the following equation:

$$ODR = \frac{MCLK}{MCLK\ DIV\ x\ DEC\ RATE}$$

Assuming the ADAQ7768-1 MCLK_DIV = 2

$$DEC\_RATE = \frac{MCLK}{MCLK\ DIV\ x\ ODR} = 163{,}840$$

To program the Sinc3 decimation ratio, the user must first calculate for the equivalent Sinc3 decimation ratio to be written on SINC3_DECIMATION_RATE registers (Register 0x1A and Register 0x1B) using the equation below:

$$Equivalent\ DEC\_RATE = \frac{DEC\_RATE}{32} - 1 = 5119$$

To set the decimation ration to 163,840, write the equivalent binary value of 5119 to SINC3_DECIMATION_RATE registers (Register 0x1A and Register 0x1B) because the value in the register is incremented by 1 and then multiplied by 32 to give the actual decimation rate.

Table 16. Sinc3 Filter 50 Hz Rejection, 50 Hz ODR and Decimate by 163,840

Frequency Band (Hz)	Minimum Measured Rejection (dB)
50 ± 1	101
100 ± 2	102
150 ± 3	102
200 ± 4	102

Table 17. Sinc3 Filter 50 Hz and 60 Hz Rejection, 50 Hz ODR and Decimate by 163,840

Frequency Band (Hz)	Minimum Measured Rejection (dB)
50 ± 1	81
60 ± 1	67
100 ± 2	83
120 ± 2	72
150 ± 3	86
180 ± 3	78
200 ± 4	90
240 ± 4	87

The impulse response of the filter is three times the ODR. For 250 kSPS ODR, the time to settle data fully is 12 µs.

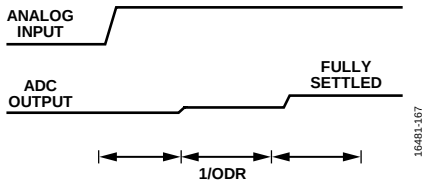

Figure 89. Sinc3 Filter Step Response

Programming for 50 Hz, 60 Hz, and 50 Hz and 60 Hz Rejection

To reject 50 Hz tones, program the ODR of the Sinc3 filter to 50 Hz (see Figure 90). It is also possible to achieve simultaneous rejection of both 50 Hz and 60 Hz by setting Bit 7 in the DIGITAL_FILTER register (Register 0x19). Rejection of both 50 Hz and 60 Hz line frequencies is possible in this configuration (see Figure 90).

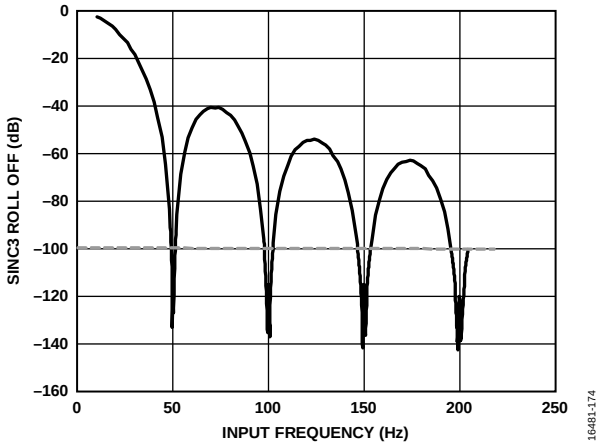

Figure 90. Sinc3 Filter Frequency Response Showing 50 Hz Rejection, 50 Hz ODR, ×163,840 Decimation

Table 18. Sinc3 Filter, $\overline{\text{SYNC\_IN}}$ to Settled Data

MCLK Divide Setting	Decimation Ratio	Equivalent Sinc3 Decimation Ratio	ODR (kSPS)		MCLK Periods	
			MCLK = 16.384 MHz	MCLK = 13.107 MHz	Delay from First MCLK Rise After $\overline{\text{SYNC\_IN}}$ Rise to First $\overline{\text{DRDY}}$ Rise	Delay from First MCLK Rise After $\overline{\text{SYNC\_IN}}$ Rise to Earliest Settled $\overline{\text{DRDY}}$ Rise
MCLK/2	32	0	256	204.8	127	255
	64	1	128	102.4	191	447
	128	3	64	51.2	319	831
	256	7	32	25.6	575	1,599
	512	15	16	12.8	1,087	3,135
	1024	31	8	6.4	2,111	6,207
	163,840	5119	0.05	0.04	327,743	983,103
MCLK/4	32	0	128	102.4	241	497
	64	1	64	51.2	369	881
	128	3	32	25.6	625	1,649
	256	7	16	12.8	1,137	3,185
	512	15	8	6.4	2,161	6,257
	1024	31	4	3.2	4,209	12,401
	81,920	2559	0.05	0.04	327,793	983,153

MCLK Divide Setting	Decimation Ratio	Equivalent Sinc3 Decimation Ratio	ODR (kSPS)		MCLK Periods	
			MCLK = 16.384 MHz	MCLK = 13.107 MHz	Delay from First MCLK Rise After SYNC_IN Rise to First DRDY Rise	Delay from First MCLK Rise After SYNC_IN Rise to Earliest Settled DRDY Rise
MCLK/16	32	0	32	25.6	926	1,950
	64	1	16	12.8	1,438	3,486
	128	3	8	6.4	2,462	6,558
	256	7	4	3.2	4,510	12,702
	512	15	2	1.6	8,606	24,990
	1024	31	1	0.8	16,798	49,566
	20,480	639	0.05	0.04	328,094	983,454

ADC SPEED AND PERFORMANCE

The ADAQ7768-1 offers a wide selection of Output Data Rate (ODR) depending on the digital filter used. This enable the ADAQ7768-1 to offer wide bandwidth selection to the user.

The ADAQ7768-1 is capable of 1 kSPS ODR using Wideband Low Ripple FIR filer and Sinc5 digital filter, while 0.0125 kSPS using Sinc3 filter. This can be achieved by using a high decimation ratio and by operating the modulator at the lowest possible sampling rate. For example, with the Wideband Low Ripple FIR filter option, 1 kSPS ODR can be achieved by using, MCLK = 16.384 MHz, decimation rate = 1024 and F_{MOD} = MCLK / 16.

The user must take note that the ADAQ7768-1 modulator samples on the rising and falling edge of the F_{MOD} and outputs data to the digital filter at a rate of F_{MOD}. There is a zero in the frequency response profile of the modulator centered at the odd multiples of F_{MOD}, which means that there is no foldback from frequencies at F_{MOD} rate and at odd multiple rate. However, the modulator is open to noise for even multiples of F_{MOD}. There is no attenuation at these zones

For optimum performance it is recommended to use MCLK = 16.384 MHz and MCLK_DIV = 2. This will set the F_{MOD} = 8.192 MHz, by keeping the F_{MOD} frequency high it maximizes the out of band tone rejection from the frontend anti-aliasing filter.

The default master clock divider setting for ADAQ7768-1 is MCLK_DIV = 16. To configure the MCLK divider to MCLK = 2, the user must write 11 to MCLK_DIV bits [5:4] of POWER_CLOCK register (Register 0x15) after power up.

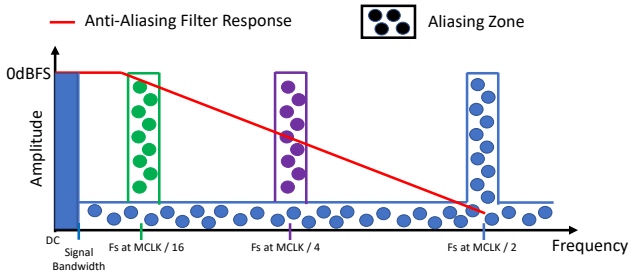

Figure 91. Anti-Alias Filter Response versus MCLK Divider

Figure 91. Anti-Alias Filter Response versus MCLK Divider shows the AAF rejection relative to the sampling frequency. Using higher MCLK divider will result to lower sampling frequency with reduce rejection from the anti-alias filter.

DEVICE CONFIGURATION METHOD

The ADAQ7768-1 has two options for controlling device functionality. On power-up, the mode is determined by the state of the PIN/ SPI pin. The two modes of configuration are

- SPI: over a 3- or 4-wire SPI interface (complete configurability)
- PIN: pin strapped digital logic inputs (a subset of complete configurability)

On power-up, the user must apply a soft or hard reset to the device when using either control mode. A SYNC_IN pulse is also recommended after the reset or after any change to the device configuration. Choose between controlling and configuring over the SPI or via pin connections only.

The first design decision is setting the ADAQ7768-1 in either the SPI or PIN mode of configuration. In either mode, the digital host reads the ADC data over the SPI port lines.

PIN Configuration

An overview of the PIN control mode features is as follows:

- No SPI write access to the device.
- Pins control all functions.
- ADC results read back over the SPI pins.
- ADC result includes an 8-bit status header output after each conversion result.
- SDI pin can be used to create a daisy chain of multiple devices operating in PIN mode.

SPI Control

An overview of the SPI control mode features is as follows:

- Standard SPI Mode 3 interface for register access, where the ADC always behaves as an SPI slave.
- Indication of a new conversion via the DRDY pin output. A second method allows the user to merge the ready signal within the DOUT output stream, which allows a reduction in the number of lines across an isolation barrier.

- Reading back conversions can be performed by writing 8 bits to address the ADC register and reading back the result from the register.
- Continuous readback mode, which is enabled via an SPI write. There is no need to supply the 8 bits to address the ADC_DATA register (Register 0x2C). Data readback occurs on the application of SCLK. The $\overline{\text{DRDY}}$ pin indicates that a conversion result is complete and can be used to trigger a readback of the conversion result.
- In continuous read back mode, there is the option to append either the 8-bit status header or an 8-bit CRC check, or both.

PIN CONTROL MODE OVERVIEW

$\overline{\text{PIN}}$ control mode eliminates the need for SPI communication to set the required mode of operation. For situations where the user requires a single, known configuration, reduce routing signals to the digital host. $\overline{\text{PIN}}$ control mode is useful in digitally isolated applications where minimal configuration is needed. $\overline{\text{PIN}}$ control mode offers a subset of the core functionality and ensures a known state of operation after power-up, reset, or a fault condition on the power supply. In $\overline{\text{PIN}}$ control mode, the linearity boost buffers and the reference input precharge buffers are enabled by default for best performance.

An automatic sync pulse drives out on the $\overline{\text{SYNC\_OUT}}$ pin in $\overline{\text{PIN}}$ control mode when the device is either initially powered up or after a reset. A $\overline{\text{SYNC\_OUT}}$ pulse also occurs when a GPIOx pin toggles, meaning after a change to the $\overline{\text{PIN}}$ control mode settings of the device, the synchronization is automatically performed. For this synchronization to work, tie $\overline{\text{SYNC\_OUT}}$ to $\overline{\text{SYNC\_IN}}$, eliminating the need to provide a synchronous $\overline{\text{SYNC\_IN}}$ pulse. The $\overline{\text{SYNC\_OUT}}$ of one device can also be tied to the $\overline{\text{SYNC\_IN}}$ of many devices when the synchronization of multiple devices is required. If synchronization of multiple devices is required, all devices must share a common MCLK.

Data Output Format

$\overline{\text{PIN}}$ control mode has a set output format for conversion data. The rising $\overline{\text{DRDY}}$ edge indicates that a new conversion is ready. The next 24 serial clock falling edges clock out the 24-bit ADC result. The following eight serial clocks output the status bits of the ADAQ7768-1. The ADC data is output MSB first in twos complement format. If further SCLK falling edges are applied to the ADC after clocking out the status bits, the logic level applied to SDI is clocked out, similar to a daisy-chain scenario. In Figure 92, an extra serial clock edge (33rd falling edge) is shown. If an extra serial clock edge occurs, the logic level of the SDI pin clocks out.

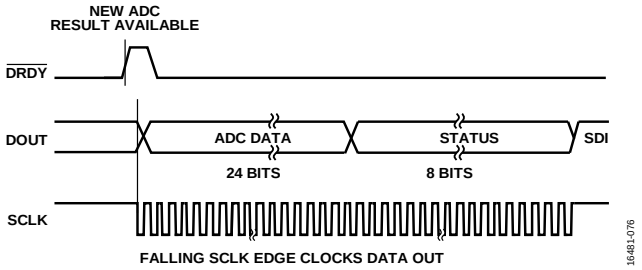

Figure 92. $\overline{\text{PIN}}$ Mode Data Output Format (This Figure Does Not Show the $\overline{\text{CS}}$ Signal)

Table 19. Differences in Control and Interface Pin Functions in $\overline{\text{PIN}}$ Control Mode and SPI Control Mode

	Pin Function	
Mnemonic	**$\overline{\text{PIN}}$ Control Mode**	**SPI Control Mode**
MODE0/GPIO0	MODE0 configuration pin	GPIO0 pin
MODE1/GPIO1	MODE1 configuration pin	GPIO1 pin
MODE2/GPIO2	MODE2 configuration pin	GPIO2 pin
MODE3/GPIO3	MODE3 configuration pin	GPIO3 pin
$\overline{\text{CS}}$	SPI pin for readback of ADC conversion results	SPI interface for full configuration of the ADAQ7768-1 via a register read/write and readback of the ADC conversion results
SCLK	SPI pin for readback of ADC conversion results	SPI interface for full configuration of the ADAQ7768-1 via a register read/write and readback of the ADC conversion results
SDI	SPI pin for readback of ADC conversion results	SPI interface for full configuration of the ADAQ7768-1 via a register read/write and readback of the ADC conversion results
DOUT/$\overline{\text{RDY}}$	SPI pin for readback of ADC conversion results	SPI interface for full configuration of the ADAQ7768-1 via a register read/write and readback of the ADC conversion results

Diagnostics and Status Bits

$\overline{\text{PIN}}$ control mode offers a subset of diagnostics features. Internal errors are reported in the status header output with the data conversion results for each channel.

The status header reports the internal CRC errors, memory map flipped bits, and the undetected external clock, indicating a reset is required. The status header also reports filter settled and filter saturated signals. Users can determine when to ignore data by monitoring these error flags.

If a significant error shows in the status bits, a reset of the ADC using $\overline{\text{RESET}}$ pin is recommended because, like in $\overline{\text{PIN}}$ mode, there is no way to interrogate further for specific errors.

Daisy-Chaining—$\overline{\text{PIN}}$ Control Mode Only

Daisy-chaining devices allows multiple devices to use the same data interface lines by cascading the outputs of multiple ADCs from separate ADAQ7768-1 devices. Daisy-chaining devices is only possible in $\overline{\text{PIN}}$ control mode.

When configured for daisy-chaining, only one ADAQ7768-1 device has its data interface in direct connection with the digital host. For the ADAQ7768-1, cascading the DOUT/$\overline{\text{RDY}}$ pin of the upstream ADAQ7768-1 device to the SDI pin of the next downstream ADAQ7768-1 device in the chain implements this daisy-chaining. The ability to daisy-chain devices and the limit on the number of devices that can be handled by the chain is dependent on the serial clock frequency used and the time available to clock through multiple 32-bit conversion outputs (24-bit conversion + 8-bit status) before the next conversion is complete.

The daisy-chaining feature is useful to reduce component count and to wire connections to the controller.

Figure 93 shows an example of daisy-chaining multiple ADAQ7768-1 devices.

The daisy-chain scheme depends on all devices receiving the same MCLK and SCLK, being synchronized, and being configured with the same decimation rate. The chip select signal ($\overline{\text{CS}}$) gates each conversion chain of data, its rising edge resetting the SPI to a known state after each conversion ripples through. The ADAQ7768-1 device that is furthest from the controller must have its SDI pin tied to VDD_IO, logic high.

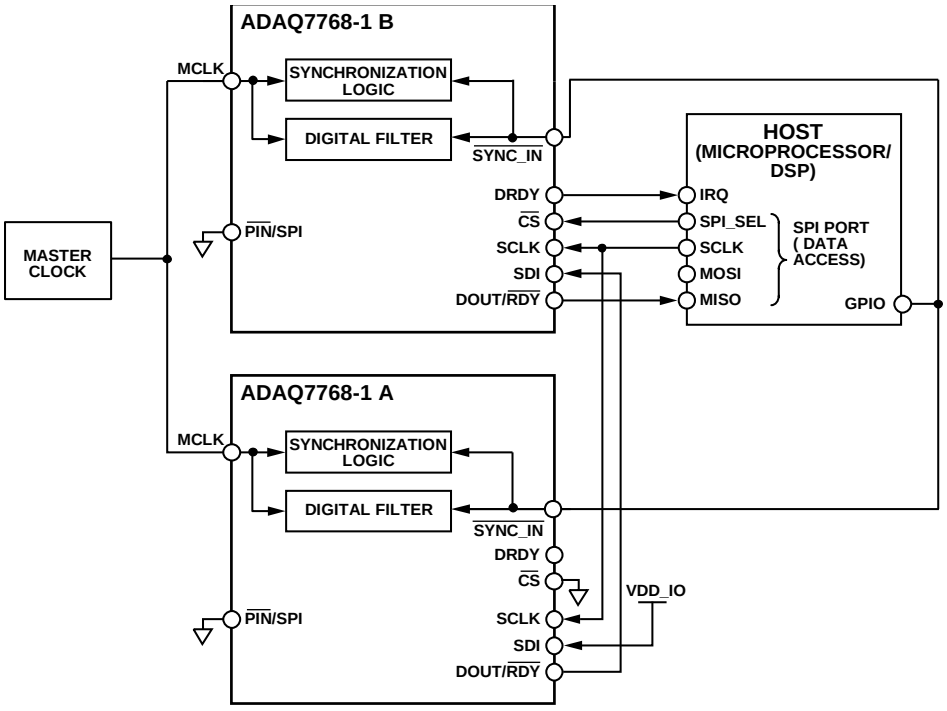

Figure 93. Daisy-Chaining Multiple ADAQ7768-1 Devices

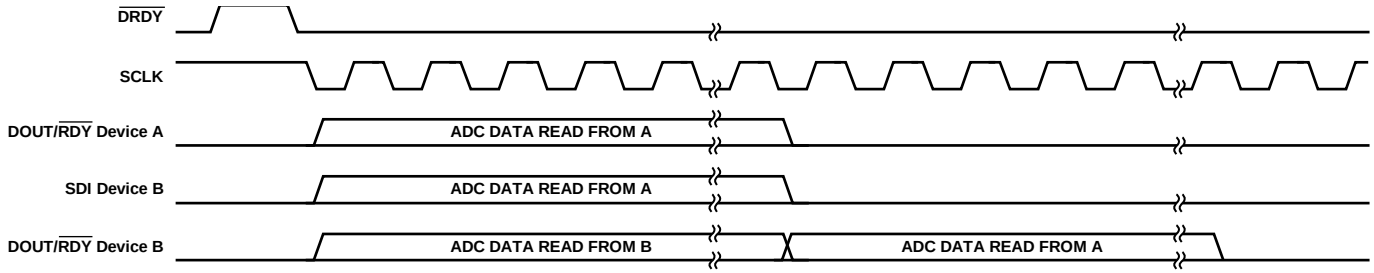

Figure 94. Data Output Format When Devices Daisy-Chained (PIN Control Mode Only)

Table 20. PIN Control Settings for MODEx Pins

MODEx Pin Settings					ADC Configuration			MCLK = 16.384 MHz
MODEx (Hex)	MODE3/ GPIO3	MODE2/ GPIO2	MODE1/ GPIO1	MODE0/ GPIO0	F_{MOD} Frequency	Filter	Decimation	ODR
0	0	0	0	0	MCLK/2	Low ripple FIR	×32	256 kHz
1	0	0	0	1	MCLK/2	Low ripple FIR	×64	128 kHz
2	0	0	1	0	MCLK/2	Sinc5	×32	256 kHz
3	0	0	1	1	MCLK/2	Sinc5	×64	128 kHz
4	0	1	0	0	MCLK/4	Low ripple FIR	×32	128 kHz
5	0	1	0	1	MCLK/4	Low ripple FIR	×64	64 kHz
6	0	1	1	0	MCLK/4	Sinc5	×32	128 kHz
7	0	1	1	1	MCLK/4	Sinc5	×64	64 kHz
8	1	0	0	0	MCLK/16	Low ripple FIR	×32	32 kHz
9	1	0	0	1	MCLK/16	Low ripple FIR	×64	16 kHz
A	1	0	1	0	MCLK/16	Sinc5	×32	32 kHz
B	1	0	1	1	MCLK/16	Sinc5	×64	16 kHz
C	1	1	0	0	MCLK/2	Sinc5	×8	1 MHz
D	1	1	0	1	MCLK/2	Sinc3 50 Hz and 60 Hz rejection[1]	×163,840	50 Hz
E	1	1	1	0	MCLK/16	Sinc3 50 Hz and 60 Hz rejection[1]	×20,480	50 Hz
F	1	1	1	1	ADC Standby			

[1] Sinc3 filter, rejection of 50 Hz and 60 Hz. Rejection of 50 Hz and 60 Hz is possible only if the MCLK applied in PIN control mode is equal to 16.384 MHz. The decimation rate is tuned internally for these pin mode settings so that the Sinc filter notches fall at 50 Hz and 60 Hz.

SPI CONTROL OVERVIEW

SPI control offers a superset of flexibility and diagnostics to the user. The categories described in Table 21 define the major controls, conversion modes, and diagnostic monitoring abilities enabled in SPI control mode.

Table 21. SPI Control Capabilities

SPI Control	Capabilities	Meaning for the User
MCLK Division	MCLK/2 to MCLK/16	The ability to customize clock frequency relating to the bandwidth of interest.
MCLK Source	CMOS, crystal, LVDS, and internal clock	Allows the user a distributed or local clock capability.
Digital Filter Style	Wideband Low Ripple FIR, Sinc5, Sinc3 (programmable)	The ability to customize the latency and frequency response to the measurement target of the user and its bandwidth.
Interface Format	Bit length	The ability to change between a 24-bit and a 16-bit conversion length in continuous read mode.
	Status bits	The ability to view output device status bits with the ADC conversion results.
	CRC	The ability to implement error checking when transmitting data.
	Data streaming	The ability to stream conversion data, eliminating interface write overhead.

SPI Control	Capabilities	Meaning for the User
Analog Buffers	Linearity boost buffer	Boost the linearity performance.
	Reference input precharge	Reduces reference input current, making it easier to filter the reference.
	Reference input full buffer	This full high impedance buffer enables filtering of reference source and enables high impedance sources, that is, reference resistors.
Conversion Modes	Single conversion	The ability to return to standby after one conversion.
	One shot	The ability to perform a conversion similar to a timed successive approximation register (SAR) conversion, in which the ADAQ7768-1 converts on a timed pulse.
	Continuous conversion	Normal operation keeps the modulator continually converting, offering the fastest response to a change on the input.
	Duty-cycled conversion	The ability to save more power for point conversions. Times the rate of conversion and sets the time for the ADC to remain in standby after the conversion completes.
	Calibration	The ability to run a calibration of the system and to save gain calibration or offset calibration results to the system settings of the user by reading back from the gain/offset registers.
Conversion Targets	ADC inputs	The ability to measure the input signal applied at the ADC input.
	Temperature sensor	The ability to measure local temperatures with an on-chip temperature sensor. Used for relative temperature measurement.
	Diagnostic sources	The ability to measure reference inputs and internal voltages for periodic functional safety checking.
GPIO Control	Up to four GPIOx pins	The ability to control other local hardware (such as gain stages),to power down other blocks in the signal chain, or read local status signals over the SPI interface of the ADAQ7768-1.
System Offset and Gain Correction	System calibration routines	The ability to correct offset and/or gain by writing to registers when the environment changes (that is, the temperature increases). Requires characterization of system errors to feed these registers.
Diagnostics	Internal checks and flags	Users can have the highest confidence in the conversion results.

SPI CONTROL MODE

MCLK Source and MCLK Division

MCLK division bits control the divided ratio between the MCLK applied at the input to the ADAQ7768-1 and the clock used by the ADC modulator. Select the division ratio best for configuration of the clocks.

The following options are available as the MCLK input source in SPI mode:

- LVDS
- External crystal
- CMOS input MCLK

Pulling CLOCK_SEL low configures the ADAQ7768-1 for a CMOS clock. Pulling CLOCK_SEL high enables the use of an external crystal.

Pulling CLK_SEL high and setting Bits [7:6] of Register 0x15 enables the application of the LVDS clock to the MCLK pin. LVDS clocking is exclusive to SPI mode and requires the register selection for operation.

ADC Power-Down Mode

All blocks on the core ADC are turned off. A specific code is required to wake the ADC up. All register contents are lost when entering power-down mode. Ensure the FDA is powered down before entering the ADC into power-down mode.

Standby Mode

Core ADC's Analog clocking and power functions are powered down. The digital LDO and register settings are retained when in standby mode. This mode is best used in scenarios where the ADC is not in use, briefly, and the user wants to save power.

SPI Synchronization

The ADAQ7768-1 can be synchronized over the SPI. The final SCLK rising edge of the command is the instance of synchronization. This command initiates the $\overline{\text{SYNC\_OUT}}$ pin to pulse active low and then back active high again. $\overline{\text{SYNC\_OUT}}$ is a signal synchronized internally to the MCLK of the ADC. By connecting the output of $\overline{\text{SYNC\_OUT}}$ to the $\overline{\text{SYNC\_IN}}$ input, the user can synchronize that individual ADC. Routing $\overline{\text{SYNC\_OUT}}$ to other ADAQ7768-1 devices also ensures the devices are synchronized, as long as the devices share a common MCLK source refer to, Figure 95. Basic SPI Synchronization Diagram .

It is recommended to perform synchronization functions directly after the $\overline{\text{DRDY}}$ pulse. If the ADAQ7768-1 $\overline{\text{SYNC\_IN}}$ pulse occurs too close to the upcoming $\overline{\text{DRDY}}$ pulse edge, the

upcoming $\overline{\text{DRDY}}$ pulse may still be output because the $\overline{\text{SYNC\_IN}}$ pulse has not yet propagated through the device.

When using the $\overline{\text{SYNC\_OUT}}$ function with an VDD_IO voltage of 1.8 V, it is recommended to set the $\overline{\text{SYNC_OUT}}$_POS_EDGE bit to a one (Register 0x1D, Bit 6).

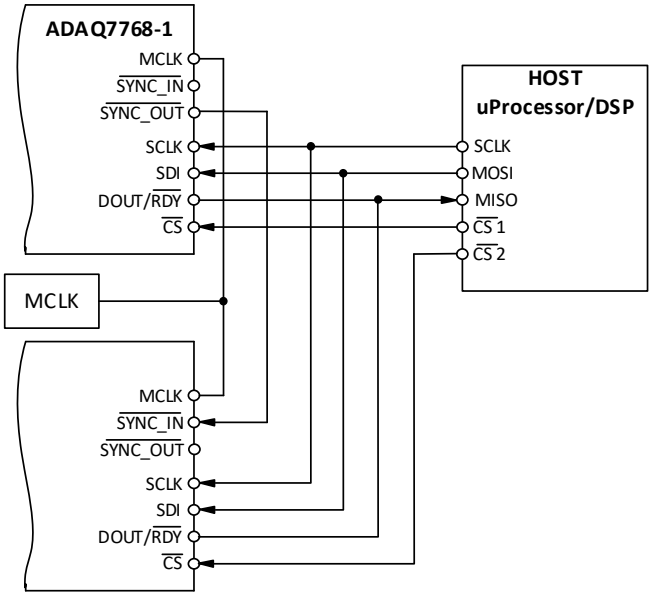

Figure 95. Basic SPI Synchronization Diagram

Offset Calibration

In SPI control mode, the ADAQ7768-1 offers the ability to calibrate offset and gain. The user can alter the gain and offset of the ADAQ7768-1 and its subsystem. These options are available in
SPI control mode only.

The offset correction registers provide 24-bit, signed, twos complement registers for channel offset adjustment. If the channel gain setting is at the ideal nominal value of 0x555555, an LSB of offset register adjustment changes the digital output by −4/3 LSBs. For example, changing the offset register from 0 to 100 changes the digital output by −133 LSBs. As offset calibration occurs before gain calibration, the LSB ratio of −4/3 changes linearly with gain adjustment via the gain correction registers.

Further register information and calibration instructions are available in the Offset Registers section.

Gain Calibration

In SPI control mode, the user can alter the gain and offset of the ADAQ7768-1 and its subsystem. These options are available in SPI control mode only.

The ADC has an associated gain coefficient that is stored for each ADC after factory programming. Nominally, this gain is approximately the 0x555555 value (for an ADC channel). The user can overwrite the gain register setting. However, after a reset or power cycle, the gain register values revert to the hard coded, programmed factory setting.

$$Data = \left[\frac{3 \times V_{IN}}{V_{REF}} \times 2^{21} - (Offset) \right] \times \frac{Gain}{4} \times \frac{4{,}194{,}300}{2^{42}}$$

Further register information and calibration instructions are available in the Gain Registers section.

Reset over SPI Control Interface

The user can issue a reset command to the ADAQ7768-1 by writing to the SPI_RESET bits in the SYNC_RESET register. Two successive writes to these bits are required to initiate the device reset.

Resume from Shutdown

Shutdown mode features the lowest possible current consumption with all blocks on the device turned off, including the standard SPI interface. Therefore, to wake the ADC up from this mode, either a hardware reset on the $\overline{\text{RESET}}$ pin, or a specific code on the SPI SDI input, is required. The specific sequence required on SDI consists of a 1 followed by 63 zeros, clocked in by SCLK while $\overline{\text{CS}}$ is low, which allows the system to wake up the ADAQ7768-1 from shutdown without using the $\overline{\text{RESET}}$ pin. This reset function is useful in isolated applications where the number of pins brought across the isolation barrier must be minimized.

GPIO and $\overline{\text{START}}$ Functions

When operating in SPI mode, the ADAQ7768-1 has additional GPIO functionality. This fully configurable mode allows the device to operate four GPIOs. These pins can be configured as read or write in any order.

GPIO read is a useful feature because it allows a peripheral device to send information to the input GPIO. Then, this information can be read from the SPI interface of the ADAQ7768-1.

The GPIOx pins can be set as inputs or outputs on a per pin basis, and there is an option to configure outputs as open-drain.

In SPI control mode, one of the GPIOx pins can be assigned the function of the $\overline{\text{START}}$ input. The $\overline{\text{START}}$ function allows a signal asynchronous to MCLK to be used to generate the $\overline{\text{SYNC\_OUT}}$ signal to reset the digital filter path of the ADAQ7768-1. The $\overline{\text{START}}$ pin function can be enabled on GPIO3.

SPI Mode Diagnostic Features

The ADAQ7768-1 includes diagnostic coverage across the internal blocks within the core ADC. The diagnostics in the following list allow the user to monitor the ADC and to increase confidence in the fidelity of the data acquired:

- Reference detection
- Clock qualification
- CRC on SPI transaction
- Flags for detection of an illegal register write
- CRC checks

- POR monitor
- MCLK counter

In addition, these diagnostics are useful in situations where instruments require remote checking of power supplies and references during initialization stages.

The diagnostics are selectable by the user via enable registers. The flags for power-on reset (POR) and the clock qualification are on by default. The flags are readable via registers, but also ripple through to the top level status bits that can be output with each ADC conversion, if desired.

Reference Detection

Write 1 to Bit 3 of the ADC_DIAG_ENABLE register (Register 0x29) to enable the reference detection block in SPI control mode. When enabled, the error flags in the ADC_DIAG_STATUS register (Register 0x2F). Any error flags then propagate through to the MASTER_STATUS register (Register 0x2D). The reference error flags when the reference applied on the REF+ pin is below 1/3 of (VDD_ADC − AGND).

Clock Qualification

The clock qualification check attempts to detect when a valid MCLK is detected. When the MCLK applied is greater than 600 kHz, the clock qualification passes. The error flags in both the ADC_DIAG_STATUS register (Register 0x2F) and the MASTER_STATUS register (Register 0x2D). If the clock detected is below the 600 kHz frequency threshold, or if an external MCLK is not detected, the clock qualification error bit is set to 1. To disable the clock qualification check, write 0 to Bit 0 of the ADC_DIAG_ENABLE register (Register 0x29).

CRC on SPI Transaction

See the CRC Check on Serial Interface section for more details.

Flags for Detection of Illegal Register Write

See the SPI Control Interface Error Handling section for more details.

CRC Checks

Enable CRC checks in the DIG_DIAG_ENABLE register (Register 0x2A) to check the state of the memory map of the ADAQ7768-1 and the internal random access memory (RAM) and fuse settings. If any of these errors flag on the device, perform a reset to return the device to a valid state.

POR Monitor

The POR monitor flag appears in both the MASTER_STATUS register and the status bits when output. The POR flag indicates that a reset or a temporary supply brown out occurred.

MCLK Counter

The MCLK_COUNTER register (Register 0x31) updates every 64 MCLKs. The MCLK counter register verifies that the ADAQ7768-1 is still receiving a valid MCLK. Read the MCLK counter register according to the specific MCLK to SCLK ratio to ensure that a valid read occurs. The SCLK applied to read the MCLK_COUNTER register must not be less than 2.1 × MCLK or greater than 4.6 × MCLK. For example, if MCLK = 2 MHz, the SCLK applied cannot be in the 4.2 MHz to 9.2 MHz range. If the MCLK to SCLK ratio is not adhered to, the read may corrupt because the MCLK may update during the read of the register, causing an error.

Product Identification (ID) Number

The ADAQ7768-1 contains ID registers that allow software inter-rogation of the silicon. The class of the product (precision ADC), product ID, device revision, and grade of device can all be read from the registry over the SPI. The vendor ID for Analog Devices, Inc., is also included in the registry for readback. These registers, in addition to a scratch pad that allows free reads from and writes to a specific register address, are methods of verifying the correct operation of the serial control interface.

Table 22. Product Identification Registers

Register Address (Hex)	Name	Bit Fields	
0x03	Chip type	Reserved	Class
0x04	Product ID [7:0]	PRODUCT_ID[7:0]	
0x05	Product ID [15:8]	PRODUCT_ID[15:8]	
0x06	Grade and revision	Grade	DEVICE_REVISION
0x0A	Scratch pad	Value	
0x0C	Vendor ID	VID[7:0]	
0x0D		VID[15:8]	

DIGITAL INTERFACE

The ADAQ7768-1 has a 4-wire SPI interface. The interface operates in SPI Mode 3. In SPI Mode 3, SCLK idles high, the first data is clocked out on the first falling or drive edge of SCLK, and data is clocked in on the rising or sample edge. Figure 97 shows SPI Mode 3 operation where the falling edge of SCLK is driving out the data and the rising edge of SCLK is when the data is sampled.

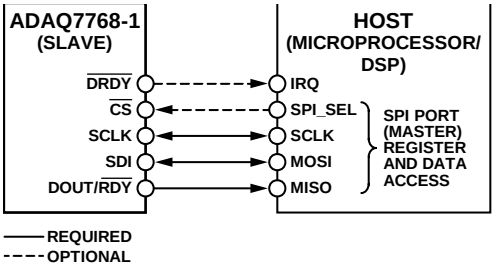

Figure 96. Basic Serial Port Connection Diagram

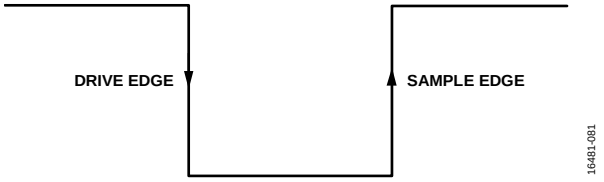

Figure 97. SPI Mode 3

SPI Reading and Writing

To use SPI control mode, set the PIN/SPI pin high. The SPI control operates as a 4-wire interface allowing read and write access. In systems where CS can be tied low, such as those requiring isolation, the ADAQ7768-1 can operate in a 3-wire configuration. Figure 96 shows a typical connection between the ADAQ7768-1 and the digital host. The corresponding 3-wire interface involves tying the CS pin low and using SCLK, SDI, and DOUT/RDY.

The format of the SPI read or write is shown in Figure 98. The MSB is the first bit in both read and write operations. An active low frame start signal (FS) begins the transaction, followed by the R/W bit that determines if the transaction being carried out is to a read (1) or a write (0). The next six bits are used for the address, and the eight bits of data to be written follow. All registers in the ADAQ7768-1 are 8 bits in width, except for the ADC_DATA register (Register 0x2C), which is 24 bits in width. In the case where CS is tied low, the last SCLK rising edge completes the SPI transaction and resets the interface. When reading back data with CS held low, it is recommended that SDI idle high to prevent an accidental reset of the device where SCLK is free running (see the Reset section).

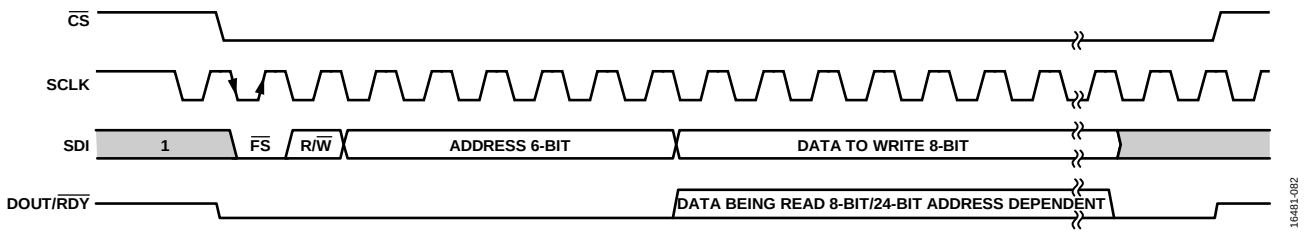

Figure 98. SPI Basic Read/Write Frame

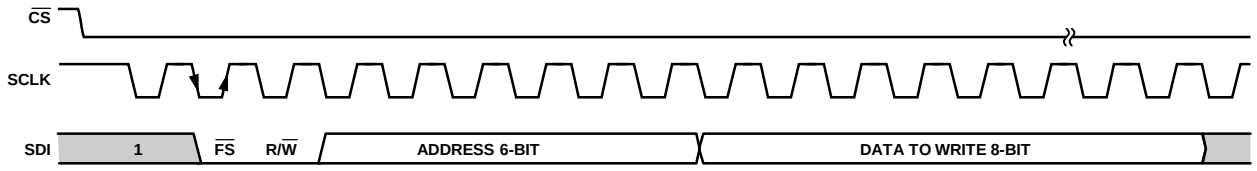

Figure 99. 3-Wire SPI Write Frame (CS = 0)

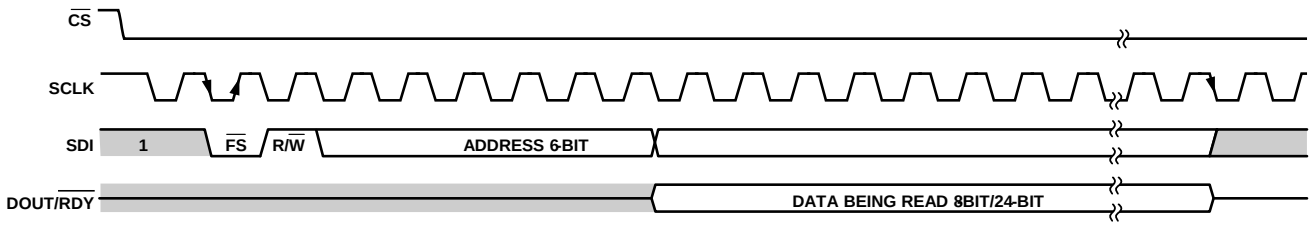

Figure 100. 3-Wire SPI Read Frame (CS = 0)

SPI Control Interface Error Handling

The ADAQ7768-1 SPI control interface detects if an illegal command is received. An illegal command is a write to a read only register, a write to a register address that does not exist, or a read from a register address that does not exist. If any of these illegal commands are received by the ADAQ7768-1, error bits are set in the SPI_DIAG_
STATUS register (Register 0x2E).

Five sources of SPI error can be detected. These detectable error sources must be enabled in the SPI_DIAG_ENABLE register (Register 0x28). Only the EN_ERR_SPI_IGNORE (Bit 4) error is enabled on startup.

The five detectable sources of SPI error are as follows:

- SPI CRC error. This error occurs when the received CRC/XOR does not match the calculated CRC/XOR.
- SPI read error. This error occurs when an incorrect read address is detected (for example, when the user attempts to access a register that does not exist).
- SPI write error. This error occurs when a write to an incorrect address is detected (for example, when the user attempts to write to a register that does not exist).
- SPI clock count error. When the SPI transaction is controlled by $\overline{CS}$, this error flags when the SPI clock count during the frame is not equal to 8, 16, 24, 32, or 40. This error can be detected in both continuous read mode and normal SPI mode.
- SPI ignore error. This error flags when an SPI transaction is attempted before initial power-up completes.

All SPI errors are sticky, meaning they can only be cleared if the user writes a 1 to the corresponding error location.

CRC Check on Serial Interface

The ADAQ7768-1 can deliver up to 40 bits with each conversion result, consisting of 24 bits of data and eight status bits, with the option to add eight further CRC/XOR check bits in SPI mode only.

The status bits default per the description in the Status Header section. The CRC functionality is available only when operating in SPI control mode. When the CRC functionality is in use, the CRC message is calculated internally by the ADAQ7768-1. The CRC is then appended to the conversion data and the optional status bits.

The ADAQ7768-1 uses a CRC polynomial to calculate the CRC message. The 8-bit CRC polynomial used is $x^8 + x^2 + x + 1$.

To generate the checksum, shift the data by eight bits to create a number ending in eight Logic 1s.

The polynomial is aligned such that the MSB is adjacent to the leftmost Logic 1 of the data. Apply an exclusive OR (XOR) function to the data to produce a new, shorter number. The polynomial is again aligned such that the MSB is adjacent to the leftmost Logic 1 of the new result, and the procedure is repeated. This process repeats until the original data is reduced to a value less than the polynomial, which is the 8-bit checksum.

If enabled, the SPI writes always use CRC, regardless of whether the XOR option is selected in the INTERFACE_FORMAT register (Register 0x14). The initial CRC checksum for SPI transactions is 0x00, unless reading back data in continuous read mode, in which case the initial CRC is 0x03.

If using the XOR option in continuous read mode, the initial value is set to 0x6C. The XOR option is only available for SPI reads.

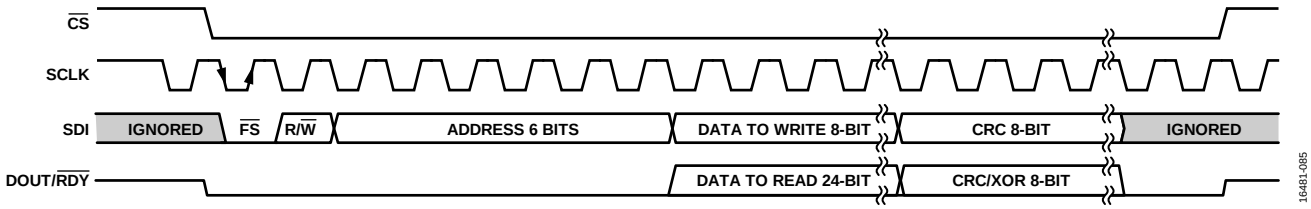

Figure 101. Data Output Format When Using CRC

Conversion Read Modes

The digital interface of the ADAQ7768-1 is a 4-wire SPI implementation operating in Mode 3 SPI. An 8-bit write instruction is needed to access the memory map address space. All registers are eight bits wide, with the exception of the ADC data register. The ADAQ7768-1 operates in a continuously converting mode by default. The user must decide whether to read the data. Two read modes are available to access the ADC conversion results: single-conversion read mode and continuous read mode

Single-read mode is a basic SPI read cycle where the user must write an 8-bit instruction to read the ADC data register. The status register must be read separately, if needed

Write a 1 to the LSB of the INTERFACE_FORMAT register to enter continuous read mode. Subsequent data reads do not require an initial 8-bit write to query the ADC_DATA register. Simply provide the required number of SCLKs for continuous readback of the data. Figure 102 shows an SPI read in continuous read mode.

Key considerations for users on the interface are as follows:

- Conversion data is available for readback after the rising edge of $\overline{\text{DRDY}}$. In continuous read mode, the $\overline{\text{RDY}}$ function can be enabled, and the $\overline{\text{DRDY}}$ function can be ignored. Data is available for readback on the falling edge of $\overline{\text{RDY}}$.
- The ADC conversion data register is updated internally 1 MCLK period prior to the rising $\overline{\text{DRDY}}$ edge.
- MCLK has a maximum frequency of 16.384 MHz.
- SCLK has a maximum frequency of 20 MHz.
- The $\overline{\text{DRDY}}$ high time is $1 \times t_{MCLK}$
- In fast power mode, decimate by 32, the $\overline{\text{DRDY}}$ period is ~4 µs, the fastest conversion can have a $\overline{\text{DRDY}}$ period of 1 µs.
- The $\overline{\text{CS}}$ rising edge resets the serial data interface. If $\overline{\text{CS}}$ is tied low, the final rising SCLK edge of the SPI transaction resets the serial interface. The point at which the interface is reset corresponds to 16 × SCLKs for a normal read operation and up to 40 SCLKs when reading back ADC conversion data, plus the status and CRC headers.

Single-Conversion Read Mode

When using single-conversion read mode, the ADC_DATA register can be accessed in the same way as a normal SPI read transaction. The ADC_DATA register (Register 0x2C), is 24 bits wide. Therefore, 32 SCLKs are required to read a conversion result.

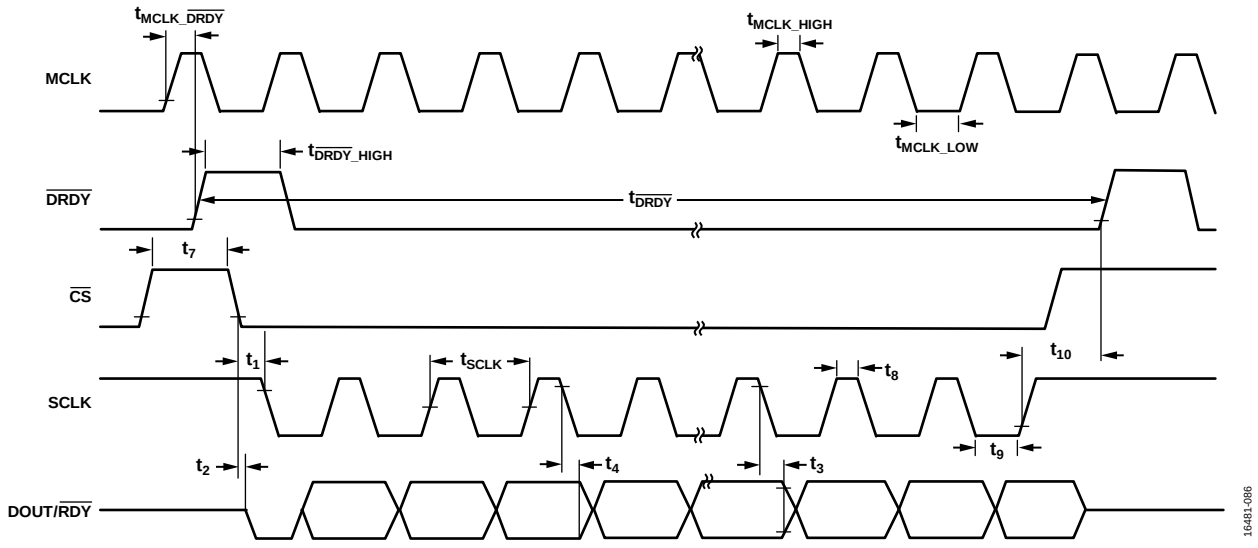

Figure 102. Serial Interface Timing Diagram, Example Reflects Reading an ADC Conversion in Continuous Read Mode

Continuous Read Mode

To eliminate the overhead of needing to write a command to read the ADC data register each time, the user can place the ADC in continuous read mode so that the ADC register can be read directly after the data ready signal is pulsed. In continuous read mode, data is output on the falling edge of the first SCLK received. Therefore, only 24 SCLKs are required to read a conversion. In this continuous read mode, it is also possible to append one or both of the status or CRC headers (eight bits each) to the conversion result. If both the status and CRC headers are enabled, the data format is ADC data + status bits + CRC.

When the $\overline{\text{RDY}}$ function is not used, the ADC conversion result can be read multiple times in the $\overline{\text{DRDY}}$ period, as is shown in Figure 103. When the $\overline{\text{RDY}}$ function is enabled, the DOUT/$\overline{\text{RDY}}$ pin goes high after reading the ADAQ7768-1 conversion result and, therefore, the data cannot be read more than once (see Figure 104).

Continuous readback is the readback mode used in $\overline{\text{PIN}}$ control mode. However, in this mode, the data output format is fixed. There is no option for $\overline{\text{RDY}}$ on the DOUT pin. See the Pin Control Mode Overview section for more details.

When using continuous read mode with the LV_BOOST bit enabled (Bit 7 in the INTERFACE_FORMAT register, Address 0x14), it is necessary to re-enable LV_BOOST each time continuous read mode is exited.

Exiting Continuous Read Mode

To exit continuous read mode, write a key of 0x6C on the SDI, which allows access to the register map one more time and allows further configuration of the device. To comply with a normal SPI write, use the $\overline{\text{CS}}$ signal to reset the SPI interface after this key is entered. If $\overline{\text{CS}}$ cannot be controlled and is permanently held low, 16 SCLKs are needed to complete the transaction so that the SPI interface remains synchronized. For example, when $\overline{\text{CS}}$ is permanently tied low, write 0x006C to exit continuous read mode when using the 3-wire version of the interface. The exit command must be written between $\overline{\text{DRDY}}$ pulses to ensure that the device exits correctly.

A software reset can also be written in this mode in the same way as the exit command, but by writing 0xAD instead of 0x6C.

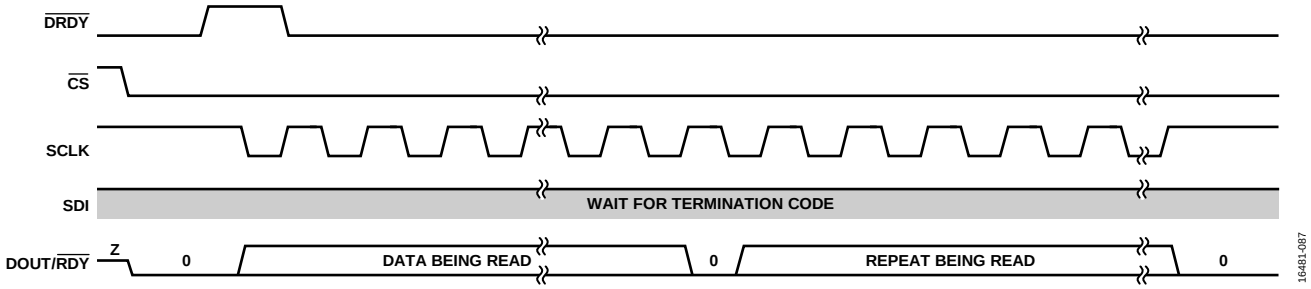

Figure 103. Continuous ADC Read Data Format with $\overline{\text{RDY}}$ Function Disabled

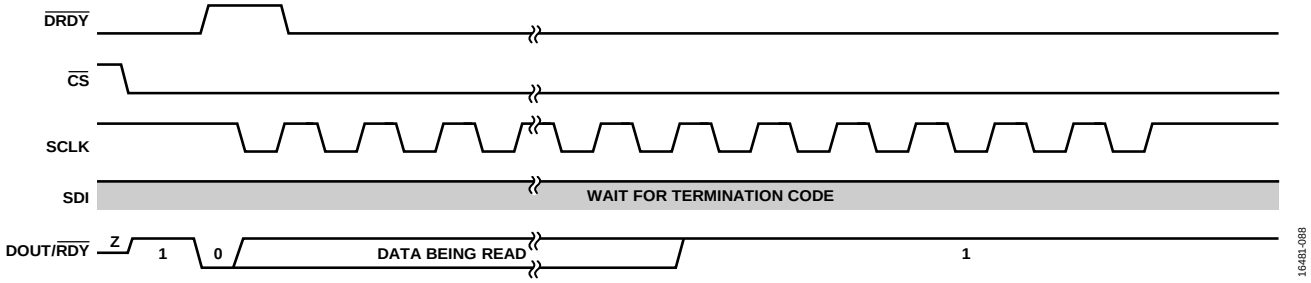

Figure 104. Continuous ADC Read Data Format with $\overline{\text{RDY}}$ Function Enabled on the DOUT/$\overline{\text{RDY}}$ Pin

DATA CONVERSION MODES

The four data conversion modes available in SPI control mode are as follows:

- Continuous conversion
- One shot conversion

The default conversion mode is continuous conversion. A $\overline{\text{SYNC\_IN}}$ pulse must be provided to the ADAQ7768-1 after any change to the configuration of the device, including changing filter settings and data conversion modes.

Continuous Conversion Mode

In continuous conversion mode, the ADC continuously converts and a new ADC result is ready at an interval determined by the ODR, which is the default conversion operation in SPI control mode. This is the only data conversion mode in which the wide-band filter is available. Two methods of data readback are available to the user in SPI control mode and are described in the Conversion Read Modes section.

One Shot Conversion Mode

Figure 105 shows the device operating in one shot conversion mode. In this mode, conversions occur on request by the master device, for example, the DSP or FPGA. The $\overline{\text{SYNC\_IN}}$ pin receives the command initiating the data output.

In one shot conversion mode, the ADC runs continuously. However, the $\overline{\text{SYNC\_IN}}$ pin rising controls the point in time from which data is output.

To receive data, the master device must pulse the $\overline{\text{SYNC\_IN}}$ pin, which resets the filter and forces $\overline{\text{DRDY}}$ low. $\overline{\text{DRDY}}$ subsequently goes high to indicate to the master device that the device has valid settled data available.

When the master asserts $\overline{\text{SYNC\_IN}}$ and the ADAQ7768-1 receives the rising edge of this signal, the digital filter is reset, the full settling time of the filter elapses before the data is settled, and the output is available. The duration of the settling time depends on the filter path and decimation rate. One shot conversion mode is only available for use with the sinc5 or sinc3 filters because these filters feature a minimal settling time. Continuous conversion mode is not available as an option for use with the low ripple FIR filter.

When settled data is available, the $\overline{\text{DRDY}}$ signal pulses. The time from the $\overline{\text{SYNC\_IN}}$ signal until the ADC path settles data (t_{SETTLE}) is shown in Figure 105. After settled data is available, $\overline{\text{DRDY}}$ is asserted high, and the user can read the conversion result. The device then waits for another $\overline{\text{SYNC\_IN}}$ signal before outputting more data.

The settling time is calculated relative to the settling time of the filter used, with some added latency for starting the one shot conversion. This settling time limits the overall throughput achievable in one shot conversion mode.

Because the ADC is sampling continuously, one shot conversion mode affects the sampling theory of the ADAQ7768-1. Periodically sending a $\overline{\text{SYNC\_IN}}$ pulse to the device is a form of subsampling of the ADC output. The bandwidth around this subsampling rate can now alias down to the baseband. Consider keeping the $\overline{\text{SYNC\_IN}}$ pulse synchronous with the master clock to ensure coherent sampling and to reduce the effects of jitter on the frequency response, which otherwise heavily distort the output.

Any SPI configuration of the ADAQ7768-1 required is performed in continuous conversion mode before switching back to one shot conversion mode.

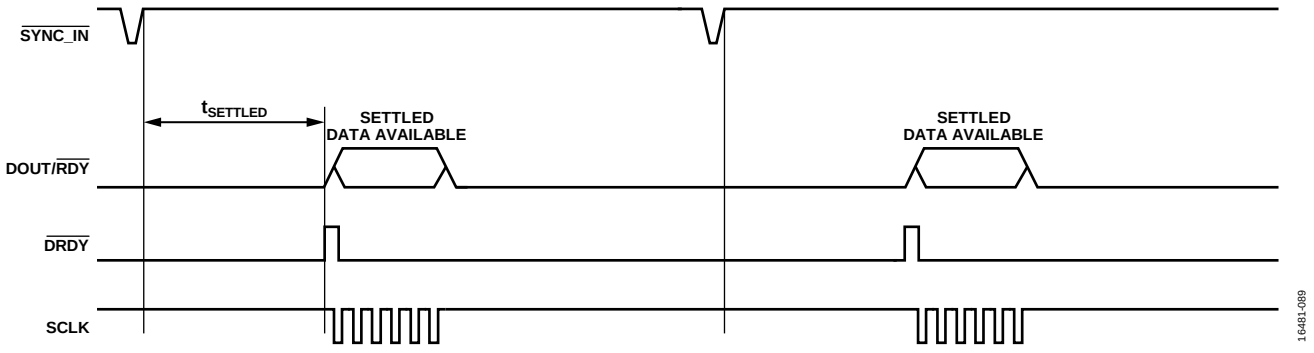

Figure 105. One Shot Conversion Mode, $\overline{\text{SYNC\_IN}}$ Pin Driven with an External Source

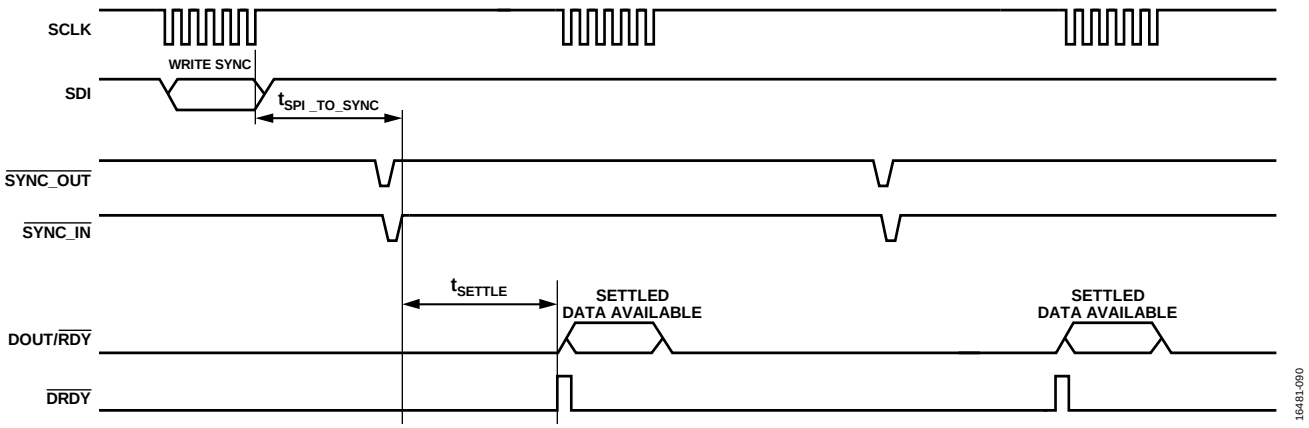

Figure 106. One Shot Conversion Mode, SYNC_IN Pulse Initiated by a Register Write

SYNCHRONIZATION OF MULTIPLE ADAQ7768-1 DEVICES

An important consideration when using multiple ADAQ7768-1 devices in a system is synchronization. The basic provision for synchronizing multiple devices is that each device is clocked with the same base MCLK signal. A SYNC_IN pulse must be provided to the ADAQ7768-1 both after power-up and after any change to the configuration of the device. This pulse serves to flush out the digital filters and ensures that the device is in a known configuration, as well as synchronizing multiple devices in a system.

The ADAQ7768-1 offer three options to ease system synchronization. Choosing between the options depends on the system. However, the most basic consideration is whether the user can supply a synchronization pulse that is truly synchronous with the base MCLK signal.

If a signal that is synchronous to the base MCLK signal cannot be provided, use one of the following methods:

- Configure the GPIOx pin of one of the ADAQ7768-1 devices in the system to be a START input. Apply a START pulse to the configured GPIOx pin. Route the SYNC_OUT pin output to the SYNC_IN input of that same device and all other devices that are to be synchronized.
- The ADAQ7768-1 samples the asynchronous START pulse and generates a SYNC_OUT pulse related to the base MCLK signal for local distribution.
- Use synchronization over SPI (only available in SPI control mode). Write a synchronization command to one predetermined ADC device. Connect the SYNC_OUT pin of this device to its own SYNC_IN pin and to the SYNC_IN pin of any other device locally. Similar to the START pin method, the SPI synchronization is received by one device and, subsequently, the SYNC_OUT signal is routed to local devices to allow synchronization.

If a SYNC_IN signal synchronous to the base MCLK can be provided, apply the SYNC_IN synchronous signal to the SYNC_IN pin from a star point and connect directly to the pin of each ADAQ7768-1 device. The SYNC_IN signal is sampled on the rising MCLK edge and, therefore, setup and hold times are associated with the SYNC_IN input relative to the ADAQ7768-1 MCLK rising edge (see Figure 7).

In this case, SYNC_OUT is redundant and can remain open-circuit or tied to VDD_IO. GPIOx can be used for a different purpose because it is not required for the START function.

Synchronization in channel to channel isolated systems is shown in Figure 107.

It is recommended to perform synchronization functions directly after the DRDY pulse. If the ADAQ7768-1 SYNC_IN pulse occurs too close to the upcoming DRDY pulse edge, the upcoming DRDY pulse may still be output because the SYNC_IN pulse has not yet propagated through the device.

When using the SYNC_OUT function with an VDD_IO voltage of 1.8 V, it is recommended to set the SYNC_OUT_POS_EDGE bit (Register 0x1D, Bit 6) to 1.

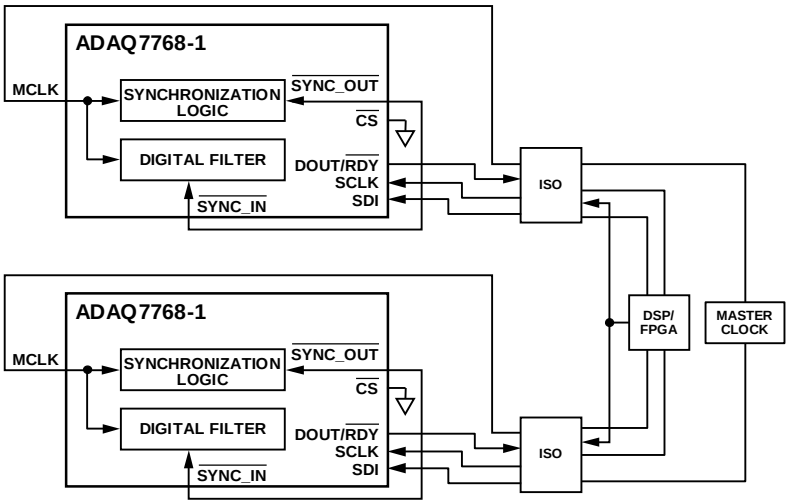

Figure 107. Synchronization in Channel to Channel Isolated Systems

ADDITIONAL FUNCTIONALITY OF THE ADAQ7768-1

Reset

After powering up the device, it is recommended to perform a full reset. There are multiple options available on the ADAQ7768-1 to perform a reset, including

- Using the dedicated RESET pin. See the section Pin Configuration and Function Description.
- When in continuous read mode, the ADAQ7768-1 monitors for the exit command or a reset command of 0xAD. See the Exiting continuous Read ModeExiting Continuous Read Mode section for more details.
- A software reset can be performed by two consecutive writes to the SYNC_RESET register (Register 0x1D).
- When CS is held low, it is possible to provide a reset by clocking in a 1 followed by 63 zeros on SDI, which is the SPI resume command reset function used to exit power-down mode.

The time taken from RESET to an SPI write must be at least 200 µs.

Status Header

In SPI control mode, the status header can be output after the conversion result when operating the ADAQ7768-1 in continuous read back mode. The status header mirrors the MASTER_ STATUS register (Register 0x2D).

In PIN control mode, the status header is output by default after the conversion result. The status header contains the following bits and functions:

- The MASTER_ERROR bit is an OR of all other errors present and can be monitored to provide a quick indication of a problem having occurred.
- The ADC_ERROR bit sets to 1 if any error is present in the ADC_DIAG_STATUS register (Register 0x2F). It is an OR of the error bits in the ADC_DIAG_STATUS register.
- The DIG_ERROR bit sets to 1 if any error is present in the DIG_DIAG_STATUS register (Register 0x30). It is an OR of the error bits in the DIG_DIAG_STATUS register.
- The ADC_ERR_EXT_CLK_QUAL bit sets if a valid clock is not detected (see the Clock Qualification section).
- The ADC_FILT_SATURATED bit sets to 1 if the digital filter is clipped on either positive or negative full scale. The clipping can be caused by the analog input exceeding the analog input range, or by a large step input to the device

that causes a large overshoot in the digital filter. In addition, the filter may saturate if the ADC gain registers are incorrectly set. The combination of a full-scale signal and a large gain saturates the digital filter.

- The ADC_FILT_NOT_SETTLED bit is set to 1 if the output of the digital filter is not settled. The digital filters are cleared following a $\overline{\text{RESET}}$ pulse, or after a $\overline{\text{SYNC\_IN}}$ command is received.

Table 15, Table 14, and Table 18 list the time for $\overline{\text{SYNC\_IN}}$ to settled data for each filter type. When using the Wideband Low Ripple FIR filter, the filter not settled bit takes longer to update and propagate through the device than to read the status header. The filter not settled bit appears set when in fact the data output is settled. The worst case update delay is 128 MCLK cycles for the Wideband Low Ripple, wideband filter, decimate by 1024 setting. In this case, if the readback is delayed by 128 MCLK cycles, the filter not settled bit has time to update, and the time to settled data is equal to the data shown in Table 15, Table 14, and Table 18.

- The SPI_ERROR bit sets to 1 if any error is present in the SPI_DIAG_STATUS register (Register 0x2E). The bit is an OR of the error bits in the SPI_DIAG_STATUS register.
- The POR_FLAG bit detects if a reset or a temporary supply brown out occurred. In $\overline{\text{PIN}}$ control mode, instead of being the POR flag, this bit is always set to 1 and then detects if that the interface is operating correctly.

Diagnostics

Internal diagnostics are available on the ADAQ7768-1 that allow the user to check both the functionality of the ADC and the environment in which the ADC is operating. The internal diagnostics are enabled in the conversion register (Register 0x18). To use the diagnostics, the device must be configured to eco mode, MCLK_DIV = MCLK/16, and the linearity boost buffers must be enabled. The diagnostics available are as follows:

- The temperature sensor is an on-chip temperature sensor that determines the approximate temperature. Temperature changes measured give approximately a 0.6 mV/°C change in the dc converted voltage. For example, at ambient temper-ature, the conversion result is approximately 180 mV. A 50°C increase in temperature reads back as approximately 210 mV, signaling, for example, a potential fault or the need to calibrate the system.
- The analog input short disconnects the core ADC's input pins from the external input and creates an internal short across the analog input pins that can detect a fault.
- The voltage converted is V_{REF+} for positive full scale, if selected.
- The voltage converted is V_{REF-} for negative full scale, if selected.

APPLICATIONS INFORMATION

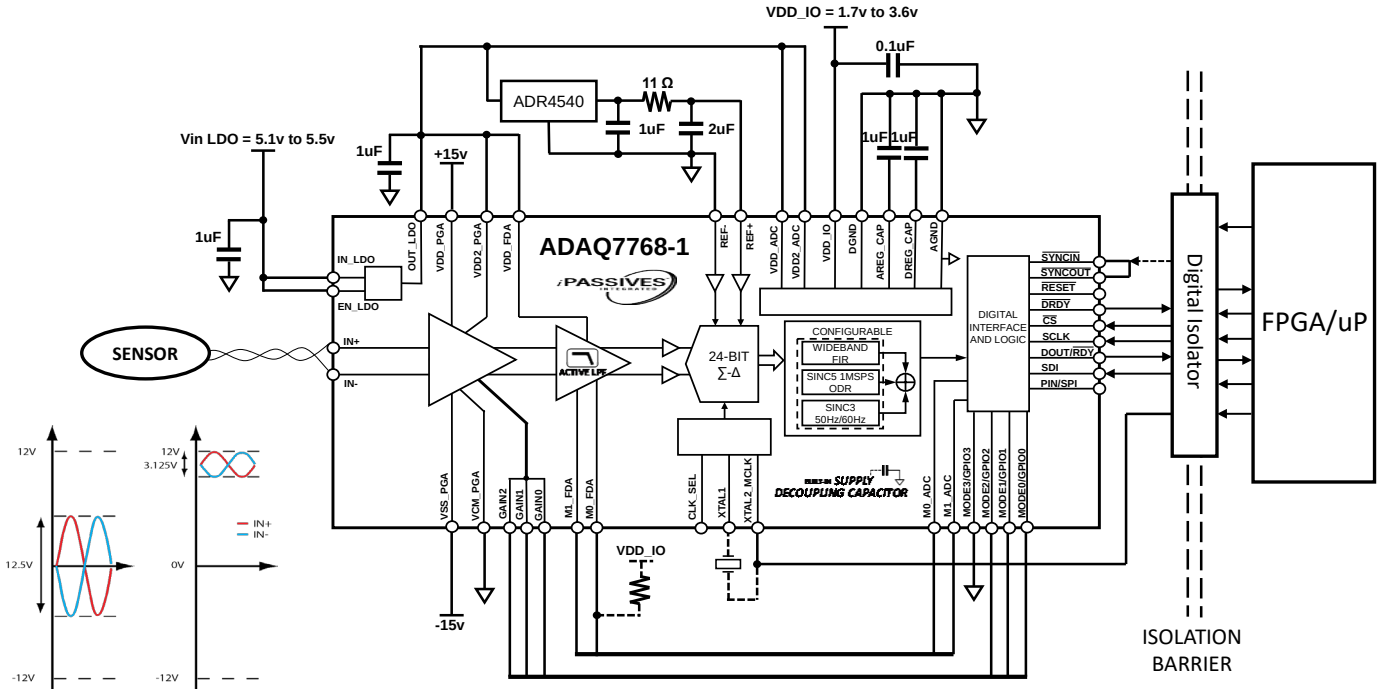

Figure 108. Typical applications diagram of a per channel isolated DAQ system

SENSOR INTERFACING

TBD

POWER CHAIN

TBD

POWER SUPPLY DECOUPLING

The value of build in decoupling capacitors and the requirement of external

POWER SUPPLY SEQUENCING

TBD

ISOLATION

TBD

GAIN CONTROL USING GPIO

TBD

REFERENCE AND BUFFER

TBD

RECOMMENDED INTERFACE

The ADAQ7768-1 interface is flexible to allow the many modes of operation and for data output formats to work across different DSPs and microcontroller units (MCUs). To achieve maximum performance, the recommended interface configuration for reading conversion results is shown in Figure 109. This recommended implementation uses a synchronous SCLK to MCLK relationship.

Configure the interface as follows to achieve the recommended operation:

1. Tie the $\overline{CS}$ signal low during the conversion readback.
2. Enter continuous readback mode to avoid needing to provide the address bits for the ADC_DATA register. Continuous readback mode is the default readback mode in $\overline{PIN}$ mode.
3. 32 bits of data are clocked out, consisting of the 24-bit conversion result plus eight bits that can be selected to be either the status or CRC bits. In $\overline{PIN}$ mode, this is always the conversion result plus the eight status bits.
4. Provide an SCLK that is a divided down version of MCLK. For example, SCLK = MCLK/2 in a case where decimate by 32 is selected.
5. Clocking 32 bits ensures that the data readback operation fills the entire $\overline{DRDY}$ period when SCLK = MCLK/2. SCLK runs continuously. The readback spans the full $\overline{DRDY}$ period, thus spreading the dynamic current needed on VDD_IO across the full ODR period.
6. The $\overline{DRDY}$ signal can synchronize the data being read into the host controller.

Figure 109 shows how the recommended interface operates. The data read back spans the entire length of the $\overline{DRDY}$ period

and the LSB remains until $\overline{\text{DRDY}}$ goes high for the next conversion.

Initializing the Recommended Interface

To configure the recommended interface, take the following steps:

1. Configure the device settings, such as power mode, decimation ratio, filter type, and so on.
2. Enter continuous readback mode.
3. Issue a synchronization pulse to apply the changes to the digital domain and to reset the digital filter. Issue the pulse immediately after $\overline{\text{DRDY}}$ goes high.

Recommended Interface for Reading Data

The recommended interface for reading data is as follows:

4. Synchronize the host controller with the $\overline{\text{DRDY}}$ or $\overline{\text{RDY}}$ pulse. See Figure 6 for details on the $\overline{\text{RDY}}$ behavior before data is clocked out.
5. Generate SCLK based on the $\overline{\text{DRDY}}$ or $\overline{\text{RDY}}$ timing. SCLK is high when the $\overline{\text{DRDY}}$ signal goes high and transitions on the MCLK falling edges (see Figure 109) to ensure that the LSB can be read correctly as the DOUT/$\overline{\text{RDY}}$ output is reset on the $\overline{\text{DRDY}}$ rising edge. However, SCLK rising occurs before this transition.
6. The MSB is clocked out on the next falling edge of SCLK.
7. In $\overline{\text{PIN}}$ control mode, the LSB of the conversion output is the last bit of the status output. In $\overline{\text{PIN}}$ control mode, this bit is always 1 and, therefore, does not need to be read.

Resynchronization of the Recommended Interface

Because the full ODR period is for clocking data, the $\overline{\text{RDY}}$ signal no longer flags after each LSB outputs. This signal only flags if the ADAQ7768-1 is in continuous readback mode, or if the ADAQ7768-1 does not count 32 SCLKs within 1 × t_{MCLK} before $\overline{\text{DRDY}}$, as is shown in Figure 109.

The $\overline{\text{RDY}}$ function is only available in continuous readback mode. In normal readback, where the ADC_DATA register must be addressed each time, the DOUT line is reset 1 × t_{MCLK} before $\overline{\text{DRDY}}$, as per t_{10} in the Timing Specifications section. If $\overline{\text{DRDY}}$ is used, the device operates as normal, and conversion readback is timed from the $\overline{\text{DRDY}}$ pulse. In the case where $\overline{\text{RDY}}$ detects the beginning of each sample, and where the data readback loses synchronization, the SCLK timing can be recovered by one of the following two methods:

- Using $\overline{\text{CS}}$ to reset the interface and to observe the $\overline{\text{RDY}}$ transition.
- Stopping SCLK toggling until the $\overline{\text{RDY}}$ transition is detected one more time.

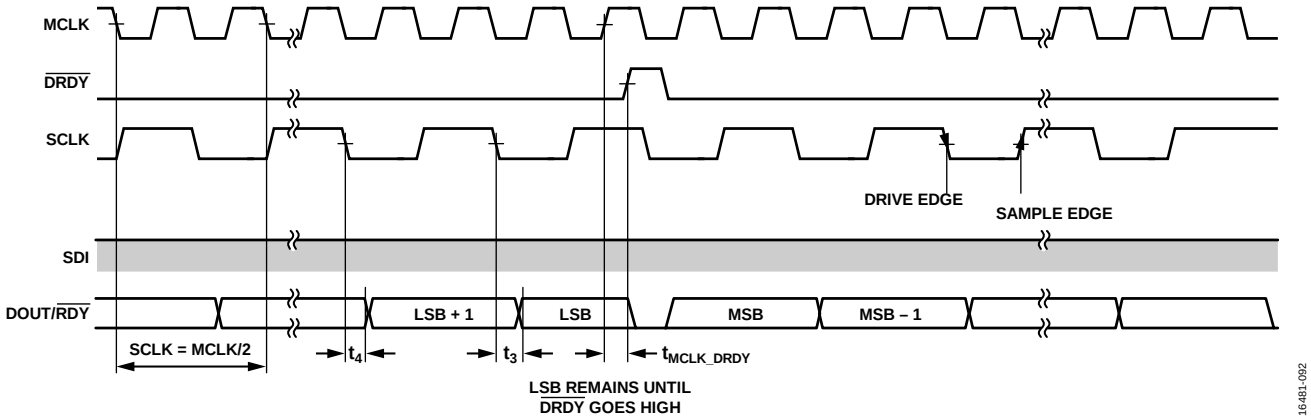

Figure 109. Recommended Interface for Reading Conversions, SPI Control, Continuous Readback Mode

PROGRAMMABLE DIGITAL FILTER

If there are additional filter requirements outside of the digital filters offered by default on the ADAQ7768-1, there is the added option of designing and uploading a custom digital filter to memory. This upload overwrites the default Wideband Low Ripple FIR filter coefficients to be replaced by a set of user defined coefficients.

The ADAQ7768-1 filter path has three separate stages:

- Initial Sinc filter
- Sinc compensation filter
- Wideband Low Ripple FIR filter

The user cannot change the first two stages. The only programmable stage is the third stage, where the default Wideband Low Ripple FIR filter coefficients can be replaced by a set of user-defined coefficients.

The data rate into the third stage is double the final ODR due to a fixed decimation by two that occurs after the final stage of filtering. Therefore, the programmable FIR stage receives data at a rate that is decimated from F_{MOD} by rates of 16, 32, 64, 128, 256, and 512.

After the final decimation by 2, the overall decimation values are given and are in the range of decimate by 32 to decimate by 1024. The data rates into the final FIR stage are listed in Table 23. Table 23 describes the data rate into the final filter stage for each power mode, assuming the correct MCLK_DIV setting is selected for the corresponding power mode.

Filter Coefficients

The ADAQ7768-1 Wideband Low Ripple FIR filter uses a set of 112 coefficients. By writing the appropriate key to the ADAQ7768-1, these coefficients can be overwritten. Then, the customized filter coefficients can upload and lock into memory. If the ADAQ7768-1 is reset, these coefficients must be rewritten.

The coefficients uploaded are subject to the following required conditions:

- The number of coefficients in a full set is 112, which is made up of 56 coefficients that are mirrored to make the total coefficients sum 112. Therefore, only 56 coefficients are written to during any one filter upload.
- Coefficients written must be in integer form. The format used is twos complement.
- The coefficient data register to be written is 24 bits wide, which is the only 24-bit register write used on the ADAQ7768-1. Only 23 bits are used for the coefficients. The remaining MSB is a control bit, detailed in the Register 0x33.
- Filter coefficients are scaled such that the 56 coefficients must sum to 2^{22}. The total (112) coefficients, therefore, sum to 2^{23}.

For example, if the filter coefficient to be written to is −0.0123, this value is scaled to $-0.0123 \times 2^{22} = -51{,}590$. In twos complement format, this value is represented by 0x7F367A.

Each filter coefficient is written by first selecting the coefficient address. Then, a separate write of the data occurs, which is repeated for all 56 coefficients from Address 0 to Address 55.

Because the FIR size cannot be changed, the filter group delay remains fixed at 34/ODR when using the programmable filter option. If a shorter number of coefficients are required, padding the end coefficients with zeros can achieved this requirement. The group delay of the uploaded filter must always be equal to the group delay of the default ADAQ7768-1 FIR filter that equals approximately 34/ODR.

Each time either the coefficient address register or the coefficient data register (COEFF_CONTROL or COEFF_DATA) are accessed, the user must wait a period before performing another read or write. The following equation determines the wait time:

$$t_{WAIT} = 512/MCLK$$

This wait time allows time for the register contents to update. Then, the coefficients are written to memory.

Table 23. Data Rates into the Final FIR Input Stage

	Input to Third Stage, Programmable FIR (MCLK = 16.384 MHz)								
Power Mode	**512 kHz**	**256 kHz**	**128 kHz**	**64 kHz**	**32 kHz**	**16 kHz**	**8 kHz**	**4 kHz**	**2 kHz**
High Performance (Fast)	Yes	Yes	Yes	Yes	Yes	Yes		Not applicable	Not applicable
Eco Mode	Not applicable	Not applicable	Not applicable	Yes	Yes	Yes	Yes	Yes	Yes

Upload Sequence

To program a user defined set of filter coefficients, perform the following sequence:

8. Write 0x4 to the filter bits in the DIGITAL_FILTER register (Register 0x19, Bits[6:4]).
9. The following key must be written to access the filter upload. First, write 0xAC to the ACCESS_KEY register (Register 0x34). Second, write 0x45 to the ACCESS_KEY register. Bit 0 (the key bit) of the ACCESS_KEY register can be read back to check if the key is entered correctly.
10. Write 0xC0 to the COEFF_CONTROL register (Register 0x32). Wait for t_{WAIT} sec to perform the following actions:
    a. Set the coefficient address to Address 0.
    b. Enable the access to memory (COEFFACCESSEN = 1).
    c. Allow a write to the coefficient memory (COEFFWRITEEN = 1).
11. The address of the first coefficient is selected. Write the required coefficient to the COEFF_DATA register (Register 0x33), and then wait for t_{WAIT} sec. Always wait t_{WAIT} sec between writes to Register 0x32 and Register 0x33.
12. Repeat Step 4 and Step 5 for each of the 56 coefficients. For example, write 0xC1 to COEFF_CONTROL to select coefficient Address 1. After waiting t_{WAIT} sec, enter the coefficient data. Increment the data until Coefficient 55 is reached. (Coefficient 55 is a write of 0xF7 to COEFF_CONTROL.)
13. Disable writing to the coefficients by first writing 0x80 to COEFF_CONTROL. Then, wait t_{WAIT} sec. Then, write 0x00 to COEFF_CONTROL to disable coefficient access.
14. Set USERCOEFFEN = 1 by writing 0x800 to COEFF_DATA to allow the user to toggle the synchronization pulse and to begin reading data.
15. Exit the filter upload by writing 0x55 to the ACCESS_KEY register (Register 0x34).
16. Send a synchronization pulse to the ADAQ7768-1. One way of sending this pulse is by writing to the SYNC_RESET register (Register 0x1D). The filter upload is now complete.

The RAM CRC error check fails when the digital filter uploads. To disable this check, use the DIG_DIAG_ENABLE register (Register 0x2A).

See the Register Details Section for further details on the register bits.

Example Filter Upload

The following sequence programs a sinc1 filter. The coefficients in Address 0 to Address 23 = 0. The coefficients from Address 24 to Address 55 = 131,072 ($2^{22}/32$). When MCLK = 16.384 MHz and ODR = 256 kHz, the filter notch appears at 8 kHz and multiples of 8 kHz. This filter provides low noise and is recognizable by the distinctive filter profile shown in Figure 110.

To program the filter, take the following steps:

17. Write 0x4 to the filter bits in the DIGITAL_FILTER register (Register 0x19, Bits[6:4]).
18. Enter the key by writing to the ACCESS_KEY register (Register 0x34).
19. Write 0xC0 to the COEFF_CONTROL register, Register 0x32, (COEFFADDR = 0, COEFFACCESSEN = 1, and COEFFWRITEEN = 1). Wait t_{WAIT} sec.
20. Write 0x000000 to COEFF_DATA (Register 0x33). Wait t_{WAIT} sec.
21. Write 0xC1 to the COEFF_CONTROL register (COEFFADDR = 1). Wait t_{WAIT} sec. In this case, the coefficient in Address 0 is equal to Address 1 and, therefore, the value in COEFF_DATA does not change.
22. Write 0xC2 to the COEFF_CONTROL register (COEFFADDR = 2). Wait t_{WAIT} sec.
23. Increment the address of the COEFF_CONTROL register (COEFFADDR = 23) until the write of 0xD7. Continue to wait t_{WAIT} sec.
24. Write 0xD8 to COEFF_CONTROL (COEFFADDR = 24).
25. Write 0x010000 to COEFF_DATA. Wait t_{WAIT} sec.
26. Write 0xD9 to COEFF_CONTROL (COEFFADDR = 25). Wait t_{WAIT} sec.
27. Write 0xDA to COEFF_CONTROL (COEFFADDR = 26) Wait t_{WAIT} sec.
28. Increment the address of the COEFF_CONTROL register (COEFFADDR = 55) until the write 0xF7. Wait t_{WAIT} sec.
29. Disable write and access by first writing 0x80 to the COEFF_CONTROL register. Wait t_{WAIT} sec. Then, write 0x00 to the COEFF_CONTROL register.
30. Set USERCOEFFEN = 1 to allow the user to toggle synchronization without reloading the default coefficients. (Write 0x800000 to COEFF_DATA.)
31. Exit the write by writing 0x55 to the ACCESS_KEY register.
32. Toggle synchronization.
33. Gather data. The resulting filter profile is shown in Figure 110.

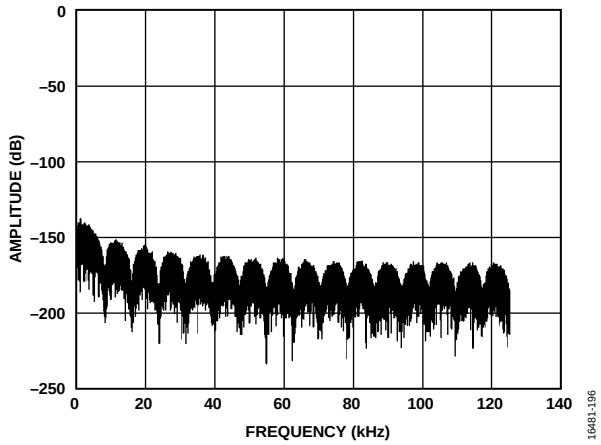

Figure 110. Example Filter Profile Upload

Filter Upload Verification

To check that the filter coefficients are uploaded correctly, it is possible to read back the values written to the COEFF_DATA register. This read can be performed after an upload by taking the following steps:

34. Enter the key by writing to the ACCESS_KEY register (Register 0x34). First, write 0xAC to the ACCESS_KEY register, and then write 0x45 to the ACCESS_KEY register.
35. Write 0x80 to the COEFF_CONTROL register, Register 0x32, (COEFFADDR = 0, COEFFACCESSEN = 1, COEFFWRITEEN = 0). Wait t_{WAIT} sec.
36. Read back the contents of the 24-bit COEFF_DATA register (Register 0x33). Check that the coefficient matches the uploaded value.
37. Write 0x81 to the COEFF_CONTROL register (COEFFADDR = 1). Wait t_{WAIT} sec.
38. Read the 24-bit COEFF_DATA register for Address 1. Increment and continue to read back the data. Continue to wait t_{WAIT} sec between updates to the COEFF_CONTROL register.
39. Disable the coefficient access by writing 0x00 to the COEFF_CONTROL register.
40. Exit the readback process by writing 0x55 to the ACCESS_KEY register.

ELECTROMAGNETIC COMPATIBILITY (EMC) TESTING

TBD

REGISTER SUMMARY

Table 24. ADAQ7768-1 Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x03	CHIP_TYPE	[7:0]	RESERVED				CLASS				0x07	R
0x04	PRODUCT_ID_L	[7:0]	PRODUCT_ID[7:0]								0x01	R
0x05	PRODUCT_ID_H	[7:0]	PRODUCT_ID[15:8]								0x00	R
0x06	CHIP_GRADE	[7:0]	GRADE				DEVICE_REVISION				0x00	R
0x0A	SCRATCH_PAD	[7:0]	VALUE								0x00	R/W
0x0C	VENDOR_L	[7:0]	VID[7:0]								0x56	R
0x0D	VENDOR_H	[7:0]	VID[15:8]								0x04	R
0x14	INTERFACE_FORMAT	[7:0]	SPI_PAD_LVBOOST	EN_SPI_CRC	CRC_TYPE	STATUS_EN	CONVLEN	EN_RDY_DOUT	RESERVED	EN_CONT_READ	0x00	R/W
0x15	POWER_CLOCK	[7:0]	CLOCK_SEL		MCLK_DIV		ADC POWER DOWN	RESERVED	ADC_MODE		0x00	R/W
0x16	ANALOG	[7:0]	REF_BUF_POS		REF_BUF_NEG		RESERVED		LINEARITY_BOOST_A_OFF	LINEARITY_BOOST_B_OFF	0x00	R/W
0x18	CONVERSION	[7:0]	DIAG_MUX_SELECT				CONV_DIAG_SELECT	CONV_MODE			0x00	R/W
0x19	DIGITAL_FILTER	[7:0]	EN_60HZ_REJ	FILTER			RESERVED	DEC_RATE			0x00	R/W
0x1A	SINC3_DEC_RATE_MSB	[7:0]	RESERVED			SINC3_DEC[12:8]					0x00	R/W
0x1B	SINC3_DEC_RATE_LSB	[7:0]	SINC3_DEC[7:0]								0x00	R/W
0x1C	DUTY_CYCLE_RATIO	[7:0]	IDLE_TIME								0x00	R/W
0x1D	SYNC_RESET	[7:0]	SPI_STARTB	SYNCOUT_POS_EDGE	RESERVED		EN_GPIO_START	RESERVED	SPI_RESET		0x80	R/W
0x1E	GPIO_CONTROL	[7:0]	UGPIO_EN	GPIO2_OPEN_DRAIN_EN	GPIO1_OPEN_DRAIN_EN	GPIO0_OPEN_DRAIN_EN	GPIO3_OP_EN	GPIO2_OP_EN	GPIO1_OP_EN	GPIO0_OP_EN	0x00	R/W
0x1F	GPIO_WRITE	[7:0]	RESERVED				GPIO_WRITE_3	GPIO_WRITE_2	GPIO_WRITE_1	GPIO_WRITE_0	0x00	R/W
0x20	GPIO_READ	[7:0]	RESERVED				GPIO_READ_3	GPIO_READ_2	GPIO_READ_1	GPIO_READ_0	0x00	R
0x21	OFFSET_HI	[7:0]	OFFSET[23:16]								0x00	R/W
0x22	OFFSET_MID	[7:0]	OFFSET[15:8]								0x00	R/W
0x23	OFFSET_LO	[7:0]	OFFSET[7:0]								0x00	R/W
0x24	GAIN_HI	[7:0]	GAIN[23:16]								0x00	R/W
0x25	GAIN_MID	[7:0]	GAIN[15:8]								0x00	R/W
0x26	GAIN_LO	[7:0]	GAIN[7:0]								0x00	R/W
0x27	BIST_CONTROL	[7:0]	RESERVED			BIST_COMPLETE	RESERVED			RUN_BIST	0x10	R/W
0x28	SPI_DIAG_ENABLE	[7:0]	RESERVED			EN_ERR_SPI_IGNORE	EN_ERR_SPI_CLK_CNT	EN_ERR_SPI_RD	EN_ERR_SPI_WR	RESERVED	0x10	R/W
0x29	ADC_DIAG_ENABLE	[7:0]	RESERVED		EN_ERR_DLDO_PSM	EN_ERR_ALDO_PSM	EN_ERR_REF_DET	EN_ERR_FILTER_SATURATED	EN_ERR_FILTER_NOT_SETTLED	EN_ERR_EXT_CLK_QUAL	0x07	R/W
0x2A	DIG_DIAG_ENABLE	[7:0]	RESERVED			EN_ERR_MEMMAP_CRC	EN_ERR_RAM_CRC	EN_ERR_FUSE_CRC	EN_ERR_RAM_BIST	EN_FREQ_COUNT	0x0D	R/W
0x2C	ADC_DATA	[31:24]	ADC_READ_DATA[31:24]								0x00000000	R
		[23:16]	ADC_READ_DATA[23:16]									
		[15:8]	ADC_READ_DATA[15:8]									
		[7:0]	ADC_READ_DATA[7:0]									

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x2D	MASTER_STATUS	[7:0]	MASTER_ERROR	ADC_ERROR	DIG_ERROR	ERR_EXT_CLK_QUAL	FILT_SATURATED	FILT_NOT_SETTLED	SPI_ERROR	POR_FLAG	0x00	R
0x2E	SPI_DIAG_STATUS	[7:0]	RESERVED			ERR_SPI_IGNORE	ERR_SPI_CLK_CNT	ERR_SPI_RD	ERR_SPI_WR	ERR_SPI_CRC	0x00	R/W
0x2F	ADC_DIAG_STATUS	[7:0]	RESERVED		ERR_DLDO_PSM	ERR_ALDO_PSM	ERR_REF_DET	FILT_SATURATED	FILT_NOT_SETTLED	ERR_EXT_CLK_QUAL	0x00	R
0x30	DIG_DIAG_STATUS	[7:0]	RESERVED			ERR_MEMMAP_CRC	ERR_RAM_CRC	ERR_FUSE_CRC	ERR_RAM_BIST	RESERVED	0x00	R
0x31	MCLK_COUNTER	[7:0]	MCLK_COUNTER								0x00	R
0x32	COEFF_CONTROL	[7:0]	COEFFACCESSEN	COEFFWRITEEN		COEFFADDR					0x00	R/W
0x33		[23:16]	USERCOEFFEN	COEFFDATA[22:16]							0x000000	R/W
		[15:8]	COEFFDATA[15:8]									
		[7:0]	COEFFDATA[7:0]									
0x34	ACCESS_KEY	[7:0]	RESERVED							KEY	0x00	R

REGISTER DETAILS

COMPONENT TYPE REGISTER

Register: 0x03, Reset: 0x07, Name: CHIP_TYPE

Table 25. Bit Descriptions for CHIP_TYPE

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	CLASS	Chip Type 111: Analog to digital converter.	0x7	R

UNIQUE PRODUCT ID REGISTER

Register: 0x04, Reset: 0x01, Name: PRODUCT_ID_L

Table 26. Bit Descriptions for PRODUCT_ID_L

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[7:0]	Product ID	0x1	R

UNIQUE PRODUCT ID REGISTER

Register: 0x05, Reset: 0x00, Name: PRODUCT_ID_H

Table 27. Bit Descriptions for PRODUCT_ID_H

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[15:8]	Product ID	0x0	R

DEVICE GRADE AND REVISION REGISTER

Register: 0x06, Reset: 0x00, Name: CHIP_GRADE

Table 28. Bit Descriptions for CHIP_GRADE

Bits	Bit Name	Description	Reset	Access
[7:4]	GRADE	Device Grade	0x0	R
[3:0]	DEVICE_REVISION	Device Revision ID	0x0	R

USER SCRATCHPAD REGISTER

Register: 0x0A, Reset: 0x00, Name: SCRATCH_PAD

Table 29. Bit Descriptions for SCRATCH_PAD

Bits	Bit Name	Description	Reset	Access
[7:0]	VALUE	Scratch PAD - Read/Write aread communciation/POR check	0x0	R/W

DEVICE VENDOR ID REGISTER

Register: 0x0C, Reset: 0x56, Name: VENDOR_L

Table 30. Bit Descriptions for VENDOR_L

Bits	Bit Name	Description	Reset	Access
[7:0]	VID[7:0]	Vendor ID	0x56	R

DEVICE VENDOR ID REGISTER

Register: 0x0D, Reset: 0x04, Name: VENDOR_H

Table 31. Bit Descriptions for VENDOR_H

Bits	Bit Name	Description	Reset	Access
[7:0]	VID[15:8]	Vendor ID	0x4	R

INTERFACE FORMAT CONTROL REGISTER

Register: 0x14, Reset: 0x00, Name: INTERFACE_FORMAT

Table 32. Bit Descriptions for INTERFACE_FORMAT

Bits	Bit Name	Description	Reset	Access
7	SPI_PAD_LVBOOST	Boosts drive strength of SPI pads 0: 1:	0x0	R/W
6	EN_SPI_CRC	Activates CRC on all SPI transactions 0: Disable CRC function on all SPI transfers. 1: Enable CRC function on all SPI transfers.	0x0	R/W
5	CRC_TYPE	Selects CRC method as XOR or 8-bit polynomial 1: XOR instead of CRC (applied to READ transactions only). 0: CRC bits are based on CRC-8 Polynomial.	0x0	R/W
4	STATUS_EN	Enables Status bits output. In SPI control mode with continuous read mode enabled the status bits are output prior to the ADC conversion result. In pin control mode the status bits are output after the ADC conversion result. 0: Disable outputting STATUS bits after ADC result in continuous read mode. 1: Output STATUS bits after ADC result in continuous read mode.	0x0	R/W
3	CONVLEN	Conversion Result Output Length 0: Full 24 BIT. 1: Output only 16 MSB of the ADC result.	0x0	R/W
2	EN_RDY_DOUT	Enables RDY signal on DOUT/RDY pin. Enables RDY indicator on DOUT/RDY pin in continuous read mode. By default the DOUT/RDY pin does not signal when new ADC conversion data is ready. Setting this bit will cause DOUT/RDY to signal the availability of ADC conversion data. 0: Enables RDY function on SDO in continuous read mode after result has been clocked out. 1: Disables RDY function on SDO in continuous read mode after result has been clocked out.	0x0	R/W
1	RESERVED	Reserved.	0x0	R
0	EN_CONT_READ	Continuous read enable bit 0: Disable Continuous Read Mode. 1: Enable Continuous Read Mode.	0x0	R/W

POWER AND CLOCK CONTROL REGISTER

Register: 0x15, Reset: 0x00, Name: POWER_CLOCK

Table 33. Bit Descriptions for POWER_CLOCK

Bits	Bit Name	Description	Reset	Access
[7:6]	CLOCK_SEL	Options for setting the clock used by the device 0: CMOS clock on mclk/xtal2. 1: Crystal oscillator. 10: LVDS INPUT ENABLE. 11: INTERNAL COARSE RC CLOCK (DIAGNOSTICS).	0x0	R/W

Bits	Bit Name	Description	Reset	Access
[5:4]	MCLK_DIV	Sets the division of the MCLK to create the ADC modulator frequency FMOD. 0: Modulator CLK is equal to Master clock divided by 16. 1: Modulator CLK is equal to Master clock divided by 8. 10: Modulator CLK is equal to Master clock divided by 4. 11: Modulator CLK is equal to Master clock divided by 2.	0x0	R/W
3	ADC POWER DOWN	Places ADC into a power down state. All blocks including the SPI are powered down. The standard SPI is not active in this state. Power-down is the lowest power consumption mode. To enter power-down mode, write 0x08 to this register. If the user attempts to set Bit 3 while also setting other bits in this register, the SPI write command is ignored, the device does not enter power-down, and the other bits are not set. Power-down mode can be exited in three ways: by a reset using the /RESET pin, by issuing the SPI resume command over SDI and SCLK, or by using the power cycle of the device.	0x0	R/W
2	RESERVED	Reserved.	0x0	R/W
[1:0]	ADC_MODE	Sets the operation mode of the ADC core. This setting in conjunction with MCLK_DIV create the conditions for the power scaling the ADC versus input bandwidth/throughput. 0: Eco Mode. 11: High Performance Mode.	0x0	R/W

ANALOG BUFFER CONTROL REGISTER

Register: 0x16, Reset: 0x00, Name: ANALOG

Used to turn on or off front end buffering.

Table 34. Bit Descriptions for ANALOG

Bits	Bit Name	Description	Reset	Access
[7:6]	REF_BUF_POS	Buffering options for the reference positive input. 0: Precharge reference buffer on. 1: Unbuffered reference input. 10: Full reference buffer on.	0x0	R/W
[5:4]	REF_BUF_NEG	Buffering options for the reference negative input. 0: Precharge Reference buffer on. 1: Unbuffered input. 10: Full Reference buffer on.	0x0	R/W
[3:2]	RESERVED	Reserved.	0x0	R
1	LINEARITY_BOOST_A_OFF	Linearity boost buffer A disable control. Setting this bit will disable the linearity boost buffer A. Use in conjunction with LINEARITY_BOOST_B_OFF. 0: Linearity boost buffer A enable. 1: Linearity boost buffer A disable.	0x0	R/W
0	LINEARITY_BOOST_B_OFF	Linearity boost buffer B disable control. Setting this bit will disable the linearity boost buffer B. Use in conjunction with LINEARITY_BOOST_A_OFF. 0: Linearity boost buffer B enable. 1: Linearity boost buffer B disable.	0x0	R/W

CONVERSION SOURCE SELECT AND MODE CONTROL REGISTER

Register: 0x18, Reset: 0x00, Name: CONVERSION

Table 35. Bit Descriptions for CONVERSION

Bits	Bit Name	Description	Reset	Access
[7:4]	DIAG_MUX_SELECT	Selects which signal to route through diagnostic mux 0: Temperature sensor. 1000: ADC input short (zero check). 1001: Positive full scale. 1010: Negative full scale.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
3	CONV_DIAG_SELECT	Select the ADC's input for conversion as normal or diagnostic mux 0: Converting signal through the normal signal chain. 1: ADC converting (and turning on) diagnostic subblocks.	0x0	R/W
[2:0]	CONV_MODE	Sets the conversion mode of the ADC. 000: Continuous conversion. 001: Continuous one shot. 010: Single conversion standby. 011: Periodic conversion standby. 100: Standby. 101: 110: 111:	0x0	R/W

DIGITAL FILTER AND DECIMATION CONTROL REGISTER

Register: 0x19, Reset: 0x00, Name: DIGITAL_FILTER

Table 36. Bit Descriptions for DIGITAL_FILTER

Bits	Bit Name	Description	Reset	Access
7	EN_60HZ_REJ	For use with Sinc 3 filter only. Firstly program the Sinc 3 filter to output at 50Hz. By subsequently selecting Rej60 bit allows one zero of the Sinc filter to fall at 60Hz. This bit will only enable rejection of both 50 and 60Hz if it is set in combination with programming Sinc 3 filter for 50Hz data rate. 0: Sinc 3 Filter optimized for single frequency rejection - 50Hz or 60Hz. 1: Filter operation is modified to allow both 50Hz and 60Hz Rejection.	0x0	R/W
[6:4]	FILTER	Selects the style of filter for use 000: Sinc 5 filter. Decimate x32 to x1024. Use DEC_RATE bits to select one of six available decimation rates from x32 to x1024. 001: Sinc5 filter. Decimate x8 only. Enables a maximum data rate of 1MHz. This path allows viewing of wider bandwidth, however it is quantization noise limited so output data is reduced to 16-bits. 010: Sinc5 filter. Decimate x16 only. Enables a maximum data rate of 512 kHz. This path allows viewing of wider bandwidths, however it is quantization noise limited so output data is reduced to 16-bits. 011: Sinc3 filter. Programmable decimation rate. Decimation rate is selected via SINC3_DEC bits in Sinc 3 decimation rate MSB and LSB registers. The Sinc3 filter can be tuned to reject 50 or 60Hz and with EN_60HZ_REJ bit set can allow rejection of both 50 and 60Hz when used with a 16.384 MHz MCLK. 100: Wideband Low Ripple FIR filter. FIR filter with Wideband low ripple passband and sharp transition band. Use DEC_RATE bits to select one of six available decimation rates from x32 to x1024.	0x0	R/W
3	RESERVED	Reserved.	0x0	R
[2:0]	DEC_RATE	Selects the Decimation rate for the Sinc 5 filter and the Brick Wall low pass FIR filter. 0: Decimate x32. 1: Decimate x64. 10: Decimate x128. 11: Decimate x256. 100: Decimate x512. 101: Decimate x1024. 110: Decimate x1024. 111: Decimate x1024.	0x0	R/W

SINC3 DECIMATION RATE (MSB) REGISTER

Register: 0x1A, Reset: 0x00, Name: SINC3_DEC_RATE_MSB

Table 37. Bit Descriptions for SINC3_DEC_RATE_MSB

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	SINC3_DEC[12:8]	Determines the decimation rate of used with the Sinc 3 filter. Value entered is incremented by 1 and multiplied by 32 to give actual dec rate	0x0	R/W

SINC3 DECIMATION RATE (LSB) REGISTER

Register: 0x1B, Reset: 0x00, Name: SINC3_DEC_RATE_LSB

Table 38. Bit Descriptions for SINC3_DEC_RATE_LSB

Bits	Bit Name	Description	Reset	Access
[7:0]	SINC3_DEC[7:0]	Determines the decimation rate of used with the Sinc 3 filter. Value entered is incremented by 1 and multiplied by 32 to give actual dec rate	0x0	R/W

PERIODIC CONVERSION RATE CONTROL REGISTER

Register: 0x1C, Reset: 0x00, Name: DUTY_CYCLE_RATIO

Table 39. Bit Descriptions for DUTY_CYCLE_RATIO

Bits	Bit Name	Description	Reset	Access
[7:0]	IDLE_TIME	Sets idle time for periodic conversion when in standby. 1 in this registers corresponds to time for one output from filter selected. The value in this register is incremented by one and doubled.	0x0	R/W

SYNCHRONISATION MODES AND RESET TRIGGERING REGISTER

Register: 0x1D, Reset: 0x80, Name: SYNC_RESET

Table 40. Bit Descriptions for SYNC_RESET

Bits	Bit Name	Description	Reset	Access
7	SPI_STARTB	Trigger STARTb signal. Allows user to initiate a SYNC_OUT pulse over SPI. Setting this bit LO drives a low pulse through SYNC_OUT which can be used as SYNC_IN signal to the same device and other ADAQ7768-1 devices where synchronised sampling is required. This bit clears itself after use.	0x1	R
6	SYNCOUT_POS_EDGE	SYNCOUT drive edge select. Setting this bit will cause SYNCOUT to be driven low by the positive edge of MCLK. Device default is that SYNCOUT is driven low on the negative edge of MCLK.	0x0	R/W
[5:4]	RESERVED	Reserved.	0x0	R
3	EN_GPIO_START	Enable STARTb function on GPIO input. Allows the user to use one of the GPIO pins as a STARTb input pin. When enabled, a low pulse on the STARTb input generates a low pulse through SYNC_OUT which can be used as SYNC_IN signal to the same device and other ADAQ7768-1 devices where synchronised sampling is required. When enabled on the LFCSP package, GPIO3 becomes the STARTb input. On the TSSOP package GPIO1 becomes the STARTb input. While the STARTb function is enabled the relevant GPIO pin cannot be used for general purpose IO reading and writing.	0x0	R/W
2	RESERVED	Reserved.	0x0	R
[1:0]	SPI_RESET	Enables device reset over SPI. Two writes to these bits are required to initiate the reset. The user must first set the bits to 11, then set the bits to 10. Once this sequence is detected on these two bits the reset will occur. It is not dependent on other bits in this register being set or cleared.	0x0	R/W

GPIO PORT CONTROL REGISTER

Register: 0x1E, Reset: 0x00, Name: GPIO_CONTROL

Table 41. Bit Descriptions for GPIO_CONTROL

Bits	Bit Name	Description	Reset	Access
7	UGPIO_EN	Universal enabling of GPIO pins. This bit must be set HI to change GPIO settings.	0x0	R/W
6	GPIO2_OPEN_DRAIN_EN	Change GPIO2 output from strong driver to open drain	0x0	R/W
5	GPIO1_OPEN_DRAIN_EN	Change GPIO1 output from strong driver to open drain	0x0	R/W
4	GPIO0_OPEN_DRAIN_EN	Change GPIO0 output from strong driver to open drain	0x0	R/W
3	GPIO3_OP_EN	Output Enable for GPIO pin. 0 -> input, 1-> output	0x0	R/W
2	GPIO2_OP_EN	Output Enable for GPIO pin. 0 -> input, 1-> output	0x0	R/W
1	GPIO1_OP_EN	Output Enable for GPIO pin. 0 -> input, 1-> output	0x0	R/W
0	GPIO0_OP_EN	Output Enable for GPIO pin. 0 -> input, 1-> output	0x0	R/W

GPIO OUTPUT CONTROL REGISTER

Register: 0x1F, Reset: 0x00, Name: GPIO_WRITE

Table 42. Bit Descriptions for GPIO_WRITE

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
3	GPIO_WRITE_3	Write to this bit to set GPIO[3] HI	0x0	R/W
2	GPIO_WRITE_2	Write to this bit to set GPIO[2] HI	0x0	R/W
1	GPIO_WRITE_1	Write to this bit to set GPIO[1] HI	0x0	R/W
0	GPIO_WRITE_0	Write to this bit to set GPIO[0] HI	0x0	R/W

GPIO INPUT READ REGISTER

Register: 0x20, Reset: 0x00, Name: GPIO_READ

Table 43. Bit Descriptions for GPIO_READ

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
3	GPIO_READ_3	Read the value from GPIO[3]	0x0	R
2	GPIO_READ_2	Read the value from GPIO[2]	0x0	R
1	GPIO_READ_1	Read the value from GPIO[1]	0x0	R
0	GPIO_READ_0	Read the value from GPIO[0]	0x0	R

OFFSET CALIBRATION MSB REGISTER

Register: 0x21, Reset: 0x00, Name: OFFSET_HI

Table 44. Bit Descriptions for OFFSET_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	OFFSET[23:16]	User offset calibration coefficient. The offset correction registers provide 24-bit, signed, twos-complement registers for channel offset adjustment. If the channel gain setting is at its ideal nominal value of 0x555555, an LSB of offset register adjustment changes the digital output by −4/3 LSBs. For example, changing the offset register from 0 to 100 changes the digital output by −133 LSBs. The user offset calibration coefficient correction is applied to the digital filter output data before the gain calibration correction, so the ratio above changes linearly with any gain adjustment applied via the gain calibration registers.	0x0	R/W

OFFSET CALIBRATION MID REGISTER

Register: 0x22, Reset: 0x00, Name: OFFSET_MID

Table 45. Bit Descriptions for OFFSET_MID

Bits	Bit Name	Description	Reset	Access
[7:0]	OFFSET[15:8]	User offset calibration coefficient. The offset correction registers provide 24-bit, signed, twos-complement registers for channel offset adjustment. If the channel gain setting is at its ideal nominal value of 0x555555, an LSB of offset register adjustment changes the digital output by −4/3 LSBs. For example, changing the offset register from 0 to 100 changes the digital output by −133 LSBs. The user offset calibration coefficient correction is applied to the digital filter output data before the gain calibration correction, so the ratio above changes linearly with any gain adjustment applied via the gain calibration registers.	0x0	R/W

OFFSET CALIBRATION LSB REGISTER

Register: 0x23, Reset: 0x00, Name: OFFSET_LO

Table 46. Bit Descriptions for OFFSET_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	OFFSET[7:0]	User offset calibration coefficient. The offset correction registers provide 24-bit, signed, twos-complement registers for channel offset adjustment. If the channel gain setting is at its ideal nominal value of 0x555555, an LSB of offset register adjustment changes the digital output by −4/3 LSBs. For example, changing the offset register from 0 to 100 changes the digital output by −133 LSBs. The user offset calibration coefficient correction is applied to the digital filter output data before the gain calibration correction, so the ratio above changes linearly with any gain adjustment applied via the gain calibration registers.	0x0	R/W

GAIN CALIBRATION MSB REGISTER

Register: 0x24, Reset: 0x00, Name: GAIN_HI

Table 47. Bit Descriptions for GAIN_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	GAIN[23:16]	User gain calibration coefficient. The ADC has an associated factory programmed gain calibration coefficient. The coefficient is stored in the ADC during factory programming and the nominal value is around 0x555555. The user cannot read back the factory programmed value, but may overwrite the gain register setting to apply their own calibration coefficient. The user offset calibration coefficient correction is applied to the digital filter output data before the gain calibration correction.	0x0	R/W

GAIN CALIBRATION MID REGISTER

Register: 0x25, Reset: 0x00, Name: GAIN_MID

Table 48. Bit Descriptions for GAIN_MID

Bits	Bit Name	Description	Reset	Access
[7:0]	GAIN[15:8]	User gain calibration coefficient. The ADC has an associated factory programmed gain calibration coefficient. The coefficient is stored in the ADC during factory programming and the nominal value is around 0x555555. The user cannot read back the factory programmed value, but may overwrite the gain register setting to apply their own calibration coefficient. The user offset calibration coefficient correction is applied to the digital filter output data before the gain calibration correction.	0x0	R/W

GAIN CALIBRATION LSB REGISTER

Register: 0x26, Reset: 0x00, Name: GAIN_LO

Table 49. Bit Descriptions for GAIN_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	GAIN[7:0]	User gain calibration coefficient. The ADC has an associated factory programmed gain calibration coefficient. The coefficient is stored in the ADC during factory programming and the nominal value is around 0x555555. The user cannot read back the factory programmed value, but may overwrite the gain register setting to apply their own calibration coefficient. The user offset calibration coefficient correction is applied to the digital filter output data before the gain calibration correction.	0x0	R/W

DIGITAL SELF TEST TRIGGER AND STATUS REGISTER

Register: 0x27, Reset: 0x10, Name: BIST_CONTROL

Table 50. Bit Descriptions for BIST_CONTROL

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
4	BIST_COMPLETE	Indicates BIST testing is complete	0x1	R
[3:1]	RESERVED	Reserved.	0x0	R
0	RUN_BIST	Starts BIST testing on internal memory devices	0x0	R/W

SPI INTERFACE DIAGNOSTIC CONTROL REGISTER

Register: 0x28, Reset: 0x10, Name: SPI_DIAG_ENABLE

Table 51. Bit Descriptions for SPI_DIAG_ENABLE

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
4	EN_ERR_SPI_IGNORE	SPI Ignore Error Enable	0x1	R/W
3	EN_ERR_SPI_CLK_CNT	SPI Clock Count Error Enable	0x0	R/W
2	EN_ERR_SPI_RD	SPI Read Error Enable	0x0	R/W
1	EN_ERR_SPI_WR	SPI Write Error Enable	0x0	R/W
0	RESERVED	Reserved.	0x0	R

ADC DIAGNOSTIC FEATURE CONTROL REGISTER

Register: 0x29, Reset: 0x07, Name: ADC_DIAG_ENABLE

Table 52. Bit Descriptions for ADC_DIAG_ENABLE

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	EN_ERR_DLDO_PSM	DLDO PSM Error Enable	0x0	R/W
4	EN_ERR_ALDO_PSM	ALDO PSM Error Enable	0x0	R/W
3	EN_ERR_REF_DET	REF DET Error Enable	0x0	R/W
2	EN_ERR_FILTER_SATURATED	Filter Saturated Error Enable	0x1	R/W
1	EN_ERR_FILTER_NOT_SETTLED	Filter Not Settled Error Enable	0x1	R/W
0	EN_ERR_EXT_CLK_QUAL	Enable qualification check on external clock	0x1	R/W

DIGITAL DIAGNOSTIC FEATURE CONTROL REGISTER

Register: 0x2A, Reset: 0x0D, Name: DIG_DIAG_ENABLE

Table 53. Bit Descriptions for DIG_DIAG_ENABLE

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
4	EN_ERR_MEMMAP_CRC	Memmap CRC Error Enable	0x0	R/W
3	EN_ERR_RAM_CRC	RAM CRC Error Enable	0x1	R/W
2	EN_ERR_FUSE_CRC	Fuse CRC Error Enable	0x1	R/W
1	EN_ERR_RAM_BIST	RAM BIST Error Enable	0x0	R/W
0	EN_FREQ_COUNT	Enable MCLK counter	0x1	R/W

CONVERSION RESULT REGISTER

Register: 0x2C, Reset: 0x00000000, Name: ADC_DATA

Table 54. Bit Descriptions for ADC_DATA

Bits	Bit Name	Description	Reset	Access
[31:0]	ADC_READ_DATA	ADC Read Data	0x0	R

DEVICE ERROR FLAGS MASTER REGISTER

Register: 0x2D, Reset: 0x00, Name: MASTER_STATUS

Table 55. Bit Descriptions for MASTER_STATUS

Bits	Bit Name	Description	Reset	Access
7	MASTER_ERROR	Master Error	0x0	R
6	ADC_ERROR	Any ADC Error (OR)	0x0	R
5	DIG_ERROR	Any Digital Error (OR)	0x0	R
4	ERR_EXT_CLK_QUAL	No Clock Error - Applied to Master Status Register Only	0x0	R
3	FILT_SATURATED	Filter Saturated	0x0	R
2	FILT_NOT_SETTLED	Filter Not Settled	0x0	R
1	SPI_ERROR	Any SPI Error (OR)	0x0	R
0	POR_FLAG	POR Flag	0x0	R

SPI INTERFACE ERROR REGISTER

Register: 0x2E, Reset: 0x00, Name: SPI_DIAG_STATUS

Table 56. Bit Descriptions for SPI_DIAG_STATUS

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
4	ERR_SPI_IGNORE	SPI Ignore Error	0x0	R/W1C
3	ERR_SPI_CLK_CNT	SPI Clock Count Error	0x0	R
2	ERR_SPI_RD	SPI Read Error	0x0	R/W1C
1	ERR_SPI_WR	SPI Write Error	0x0	R/W1C
0	ERR_SPI_CRC	SPI CRC Error	0x0	R/W1C

ADC DIAGNOSTICS OUTPUT REGISTER

Register: 0x2F, Reset: 0x00, Name: ADC_DIAG_STATUS

Table 57. Bit Descriptions for ADC_DIAG_STATUS

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	ERR_DLDO_PSM	DLDO PSM Error	0x0	R
4	ERR_ALDO_PSM	ALDO PSM Error	0x0	R
3	ERR_REF_DET	REF DET Error	0x0	R
2	FILT_SATURATED	Filter Saturated	0x0	R
1	FILT_NOT_SETTLED	Filter Not Settled	0x0	R
0	ERR_EXT_CLK_QUAL	No Clock Error - Applied to Master Status Register Only	0x0	R

DIGITAL DIAGNOSTICS OUTPUT REGISTER

Register: 0x30, Reset: 0x00, Name: DIG_DIAG_STATUS

Table 58. Bit Descriptions for DIG_DIAG_STATUS

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
4	ERR_MEMMAP_CRC	Memmap CRC Error	0x0	R
3	ERR_RAM_CRC	RAM CRC Error	0x0	R
2	ERR_FUSE_CRC	Fuse CRC Error	0x0	R
1	ERR_RAM_BIST	RAM BIST Error	0x0	R
0	RESERVED	Reserved.	0x0	R

MCLK DIAGNOSTIC OUTPUT REGISTER

Register: 0x31, Reset: 0x00, Name: MCLK_COUNTER

Table 59. Bit Descriptions for MCLK_COUNTER

Bits	Bit Name	Description	Reset	Access
[7:0]	MCLK_COUNTER	MCLK Counter. This register increments after every 64 MCLKs.	0x0	R

COEFFICIENT CONTROL REGISTER

Register: 0x32, Reset: 0x00, Name: COEFF_CONTROL

Table 60. Bit Descriptions for COEFF_CONTROL

Bits	Bit Name	Description	Reset	Access
7	COEFFACCESSEN	Setting this bit to a 1 allows access to the coefficient memory.	0x0	R/W
6	COEFFWRITEEN	Enables write to the coefficient memory. Write a 1 to enable.	0x0	R/W
[5:0]	COEFFADDR	Address to be accessed for the coefficient memory. The address ranges from 0 to 55 for 56 coefficients that form one symmetrical half of the 112 coefficients.	0x00	R/W

COEFFICIENT DATA REGISTER

Register: 0x33, Reset: 0x00, Name: COEFF_DATA

Table 61. Bit Descriptions for COEFF_DATA

Bits	Bit Name	Description	Reset	Access
23	USERCOEFFEN	Setting this bit to a 1 prevents the coefficients from ROM over writing the user defined coefficients after a sync toggle. A sync pulse is required after every change to the AD7767-1 digital filter configuration, including a customized filter upload.	0x0	R/W
[22:0]	COEFFDATA	Filter coefficients written to memory are written to these bits. These bits are 23 bits wide.	0x000000	R/W

ACCESS KEY REGISTER

Register: 0x34, Reset: 0x00, Name: ACCESS_KEY

Table 62. Bit Descriptions for ACCESS_KEY

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.		
0	Key	A specific key must be written to the ACCESS_KEY register prior to any filter upload. If written correctly, the key bit reads back as 1.	0x0	R/W

OUTLINE DIMENSIONS

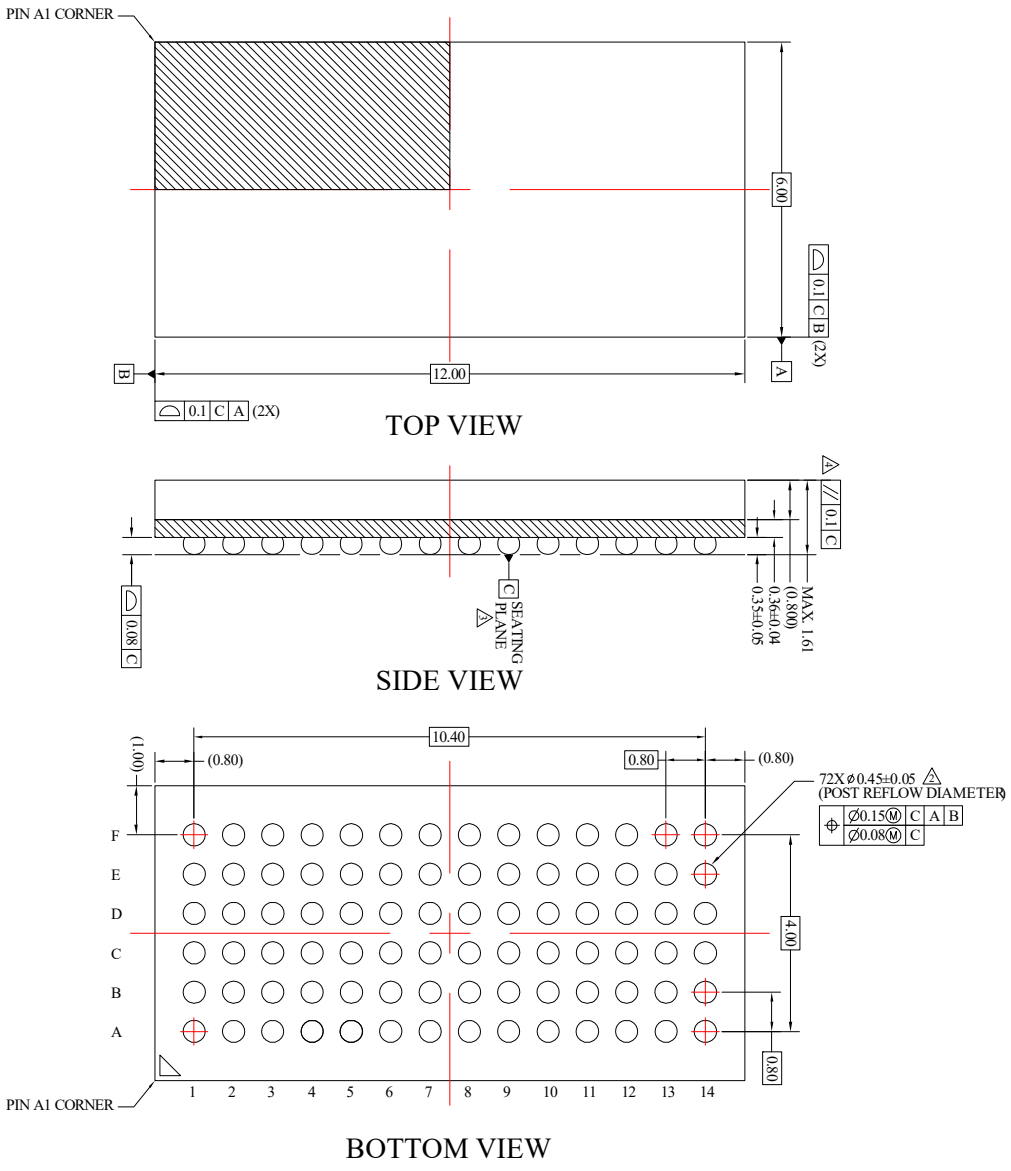

Figure 111. Package Drawings

PR21932-10/20(PrH)