ANALOG DEVICES

EVAL-ADAU1452REVBZ User Guide
UG-1662

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Evaluating the ADAU1452 SigmaDSP Audio Processor

FEATURES

On-board AD1938 codec with 4 analog inputs and 8 analog outputs
Stereo S/PDIF input and output
Self boot EEPROM memory

EVALUATION KIT CONTENTS

EVAL-ADAU1452REVBZ evaluation board
EVAL-ADUSB2EBZ communications adapter (USBi)
USB cable with mini-B plug
AC to 6 V dc power supply

EQUIPMENT REQUIRED

PC running Windows XP, Windows Vista, or Windows 7 OS
Analog, stereo audio source with an output cable terminated with a 3.5 mm (1/8 inch) plug (for analog input)
Headphones, desktop speakers, or audio input with a cable terminated with a 3.5 mm (1/8 inch) plug (for analog output)
S/PDIF audio source and receiver, each with optical cables terminated with TOSLINK connectors (for digital input/output)
Audio cables

DOCUMENTS NEEDED

ADAU1452 data sheet
AD1938 data sheet
AN-1006 Application Note

SOFTWARE REQUIRED

SigmaStudio software, available for download from the SigmaStudio product page

GENERAL DESCRIPTION

This user guide describes the design, setup, and operation of the EVAL-ADAU1452REVBZ evaluation board. This board evaluates and develops the software for the ADAU1452 and ADAU1462 SigmaDSP® processors. The ADAU1452 and the ADAU1462 are functionally identical, except that the ADAU1462 has more program and data memory. Selecting this component in the software instructs the compiler to limit the amount of allocated memory to match the ADAU1462.

All other procedures and instructions in this user guide are applicable to both the ADAU1462 and ADAU1452.

The EVAL-ADAU1452REVBZ evaluation board provides access to the digital serial audio ports of the ADAU1452 and some of the general-purpose input/outputs (GPIOs). An analog input and output is provided by the AD1938 codec included in the evaluation kit.

The ADAU1452 core is programmed using the Analog Devices, Inc., SigmaStudio® software, which interfaces to the evaluation board via the universal serial bus interface (USBi). The on-board electronically erasable programmable read-only memory (EEPROM) can be programmed for self boot mode.

The evaluation board is powered by a 6 V dc supply, which is regulated to the voltages required on the board. The printed circuit board (PCB) is a 4-layer design with a ground plane and a power plane on the inner layers. The evaluation board includes connectors for external analog inputs and outputs and optical Sony/Philips digital interface (S/PDIF) interfaces. The integrated oscillator circuit and the on-board, 12.288 MHz passive crystal (Y1) provides the master clock.

For full details, see the ADAU1452 and AD1938 data sheets, which must be used in conjunction with this user guide when using the EVAL-ADAU1452REVBZ evaluation board.

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REVISION HISTORY

10/2019—Revision 0: Initial Version

EVALUATION BOARD PHOTOGRAPH

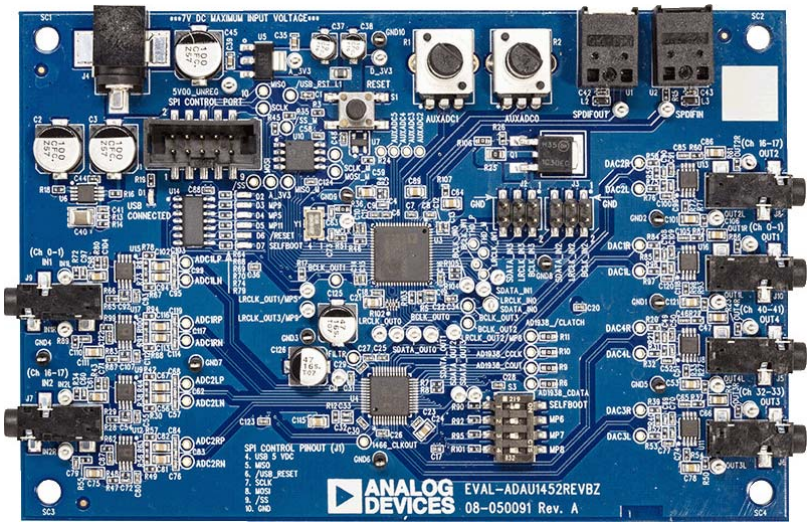


Figure 1.

SETTING UP THE EVALUATION BOARD

Using the EVAL-ADAU1452REVBZ evaluation board requires a PC running a Windows® XP operating system (OS) or later with a USB interface, the USBi, and an internet connection. The PC communicates with the evaluation board using the included USBi.

The software tool chain used with the ADAU1452 is SigmaStudio, a fully graphical user interface (GUI)-based programming environment. No digital signal processing (DSP) programming is required. A full version of SigmaStudio, which includes a library of DSP building blocks and the required USBi drivers, can be downloaded from the SigmaStudio software page on the Analog Devices website at www.analog.com/SigmaStudio.

INSTALLING THE SigmaStudio SOFTWARE

To download the latest version of SigmaStudio, take the following steps:

1. Go to the SigmaStudio software page on the Analog Devices website and select the latest version of the SigmaStudio software from the **Downloads and Related Software** section.
2. Determine whether the software must be installed on a 32-bit or 64-bit version of Windows and locate the latest, corresponding release version of SigmaStudio.
3. Download the installer and run the executable file. Follow the prompts in the program and accept the license agreement to install the software.

INSTALLING THE EVAL-ADUSB2EBZ (USBi) DRIVERS

To use the USBi, install SigmaStudio first (see the Installing the SigmaStudio Software section). After installing the SigmaStudio, take the following steps:

1. Connect the USBi to an available USB 2.0 port using the USB cable included in the evaluation board kit. The USBi does not function properly with a USB 3.0 port.
2. Install the driver software (see the Using Windows XP section or the Using Windows 7 or Windows Vista section for more information).

Using Windows XP

After connecting the USBi to the USB 2.0 port, Windows recognizes the device (see Figure 2) and prompts the user to install the required drivers. To install these drivers, take the following steps:

*Figure 2. **Found New Hardware** Notification*

1. From the **Found New Hardware Wizard** window, select the **Install from a list or specific location (Advanced)** radio button and click **Next >** (see Figure 3).

*Figure 3. **Found New Hardware Wizard**—Installation*

2. In the next window, select the **Search for the best driver in these locations** radio button, select the **Include this location in the search:** checkbox, and click **Browse** to find the USB drivers subdirectory within the SigmaStudio directory (see Figure 4).

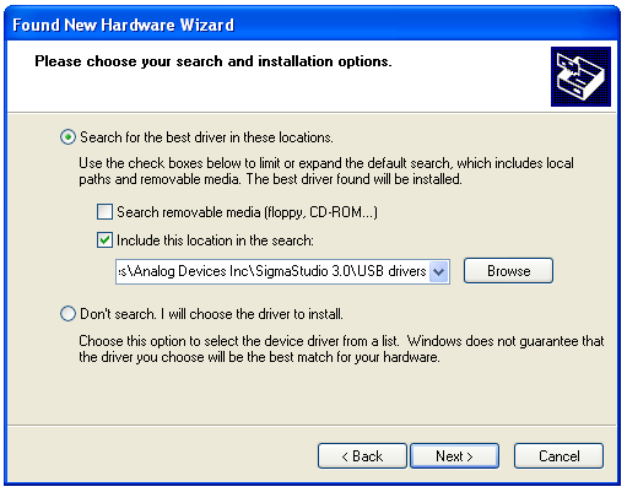


*Figure 4. **Found New Hardware Wizard**—Search and Installation Options*

3. When the warning about Windows logo testing appears, click **Continue Anyway** (see Figure 5).

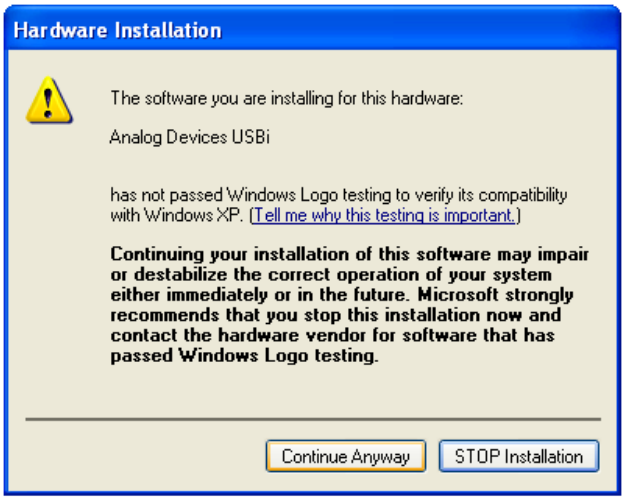


*Figure 5. **Hardware Installation**—Windows Logo Testing Warning*

The USBi drivers are now installed. Leave the USBi connected to the PC.

Using Windows 7 or Windows Vista

After connecting the USBi to the USB 2.0 port, Windows 7 or Windows Vista recognizes the device and installs the drivers automatically (see Figure 6). After the installation is complete, leave the USBi connected to the PC.

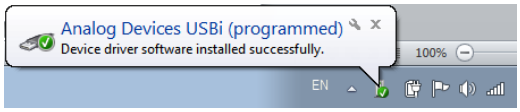


Figure 6. USBi Driver Installed Correctly Notification

Confirming Proper Installation of the USBi Drivers

To confirm that the USBi drivers are properly installed, take the following steps:

1. With the USBi still connected to the computer, check that both the yellow I²C LED and the red power indicator (D4) LED are illuminated (see Figure 7).
2. In the Windows **Device Manager** under the **Universal Serial Bus controllers** section (see Figure 8), check that **Analog Devices USBi (programmed)** is displayed.

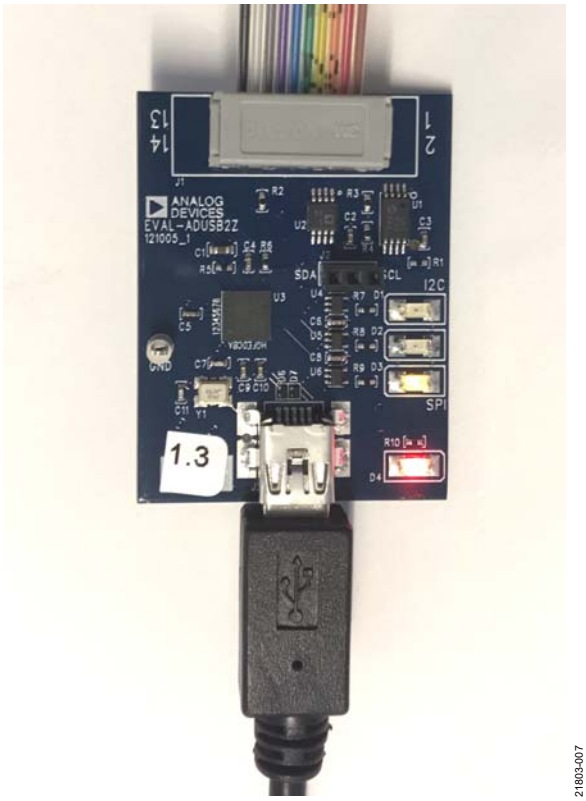


Figure 7. USBi Status LEDs After Driver Installation

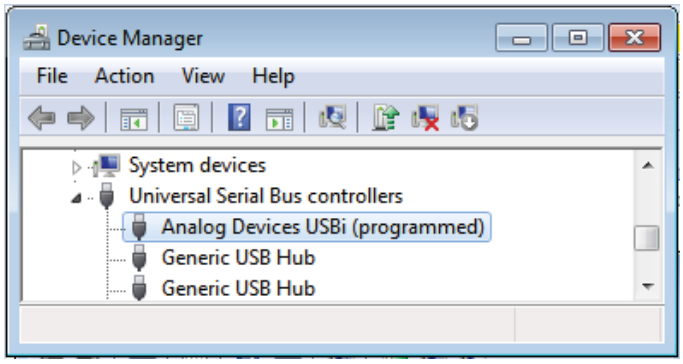


*Figure 8. Confirming Driver Installation with the **Device Manager***

DISABLING THE SELF BOOT SWITCH

When setting up the EVAL-ADAU1452REVBZ evaluation board, ensure that the first switch of the four-position, dual, inline package (DIP) switches, S3, is in the off position, meaning the switch is pointed away from the **SELFBOOT** label on the evaluation board (see Figure 67).

When the default S3 switch position is in the off (disabled) position, the ADAU1452 is prevented from executing a self boot operation at power-up. When the switch is in the on position, LED D7 (see Figure 76) illuminates and a self boot operation executes. Self boot also causes the ADAU1452 to attempt to load code from an EEPROM when the device powers up or comes out of reset.

POWERING UP THE EVALUATION BOARD

To power up the evaluation board, take the following steps:

1. Connect the included 6 V dc power supply to the wall outlet (100 V to 240 V, ac 50 Hz to 60 Hz).
2. Connect the female plug of the power supply to the J4 male connector on the EVAL-ADAU1452REVBZ board, as shown in Figure 9.

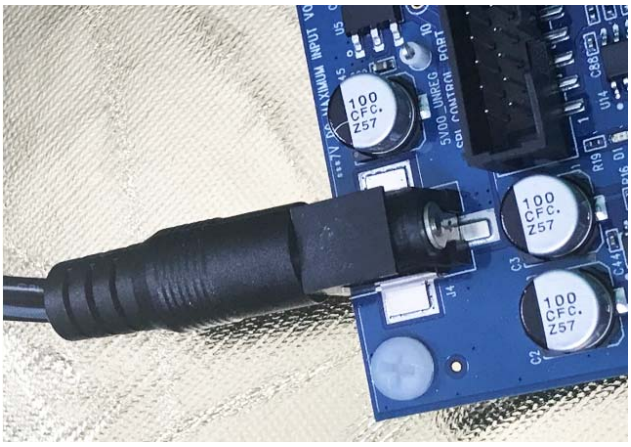


Figure 9. Connecting the Power Supply

3. After the power supply is connected, the D2 (A_3V3) status LED illuminates (see Figure 76).
4. Connect the ribbon cable of the USBi to the control port of the EVAL-ADAU1452REVBZ (see Figure 10). The USBi must already be connected to the USB 2.0 port of the computer.

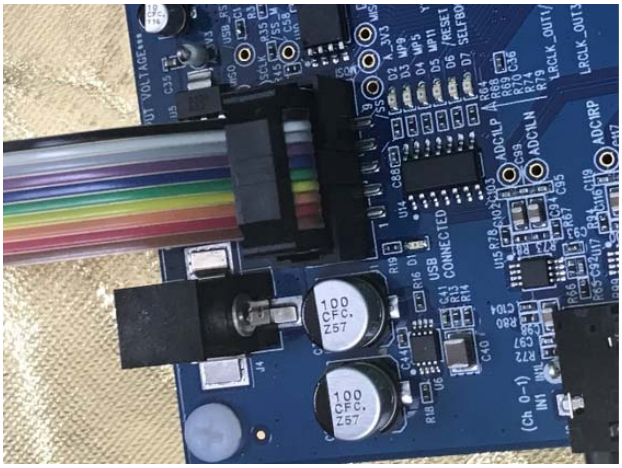


Figure 10. Connecting the USBi to the Serial Peripheral Interface (SPI) Control Port Header

CONNECTING THE AUDIO CABLES

To connect the audio cables to the evaluation board, take the following steps:

1. Connect an analog stereo audio source to J9 (IN1) with a standard 3.5 mm (1/8 inch) stereo tip, ring, and sleeve (TRS) audio cable (see Figure 11). The audio signals must be single-ended and line level with a maximum voltage of 2.8 V p-p. The tip of the plug is the left channel analog audio, the ring is the right channel analog audio, and the sleeve is the common or ground.
2. Connect headphones or powered speakers to J10 (OUT1) (see Figure 12).

Figure 11 shows the input source connection and Figure 12 shows the output connection. Figure 13 shows the location of the input and output connectors on the evaluation board.

Figure 11. Analog Stereo Input Source Connection at J9 (IN1)

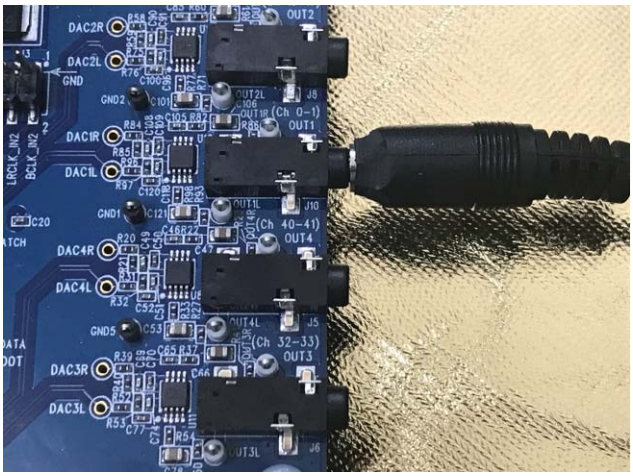


Figure 12. Analog Stereo Output Connection at J10 (OUT1)

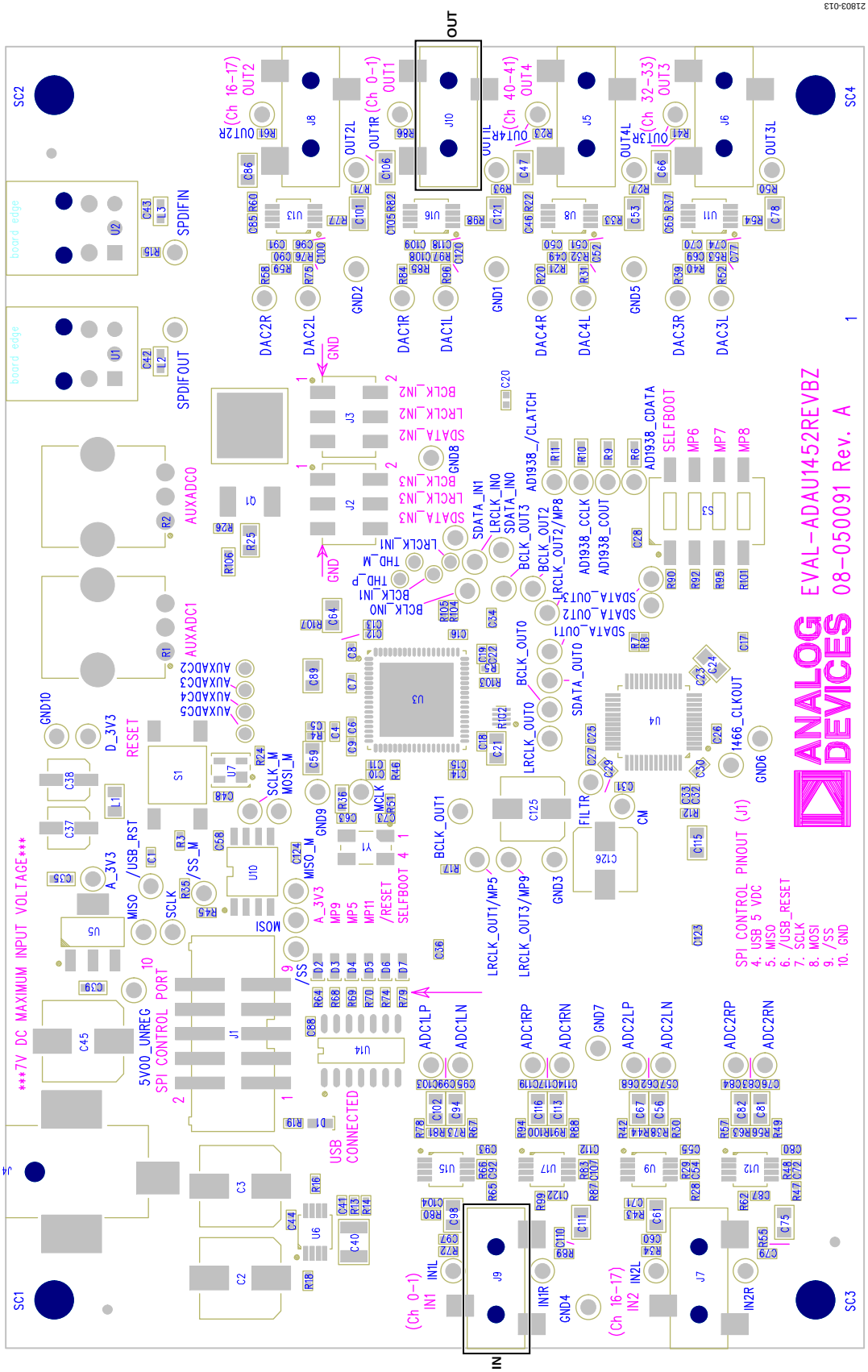


Figure 13. Location of J10 (OUT1) and J9 (IN1), Schematic Rotated 90°

SETTING UP COMMUNICATIONS IN SigmaStudio

When using the EVAL-ADAU1452REVBZ board to evaluate the ADAU1462, select the ADAU1462 block rather than the ADAU1452, as shown in Figure 15.

To set up communications with the EVAL-ADAU1452REVBZ board in SigmaStudio, take the following steps:

1. Start the SigmaStudio software either by double-clicking the desktop shortcut or by finding and running the executable file in **File Explorer**.
2. To create a new SigmaStudio project, select **New Project** from the **File** menu or by pressing the **Ctrl** + **N** keys. The **Hardware Configuration** tab is the default view of the new project.
3. In the **Hardware Configuration** tab, add the appropriate components to the project space by clicking and dragging them from the left **Tree ToolBox** panel to the empty white project space on the right of the window. The user can change the names of the component blocks as desired.
4. Add a **USB Interface** block (the USBi) to the project by clicking **USBi** from the **Communication Channels** subsection of the **Tree ToolBox** (see Figure 14), and then dragging it to the project space.

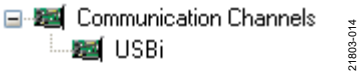


*Figure 14. Adding a **USBi** Component From **Communication Channels***

5. Add an **IC 1** block to the project by clicking the **ADAU1452** component from the **Processors (ICs/DSPs)** subsection (see Figure 15), and then dragging it into the project space.

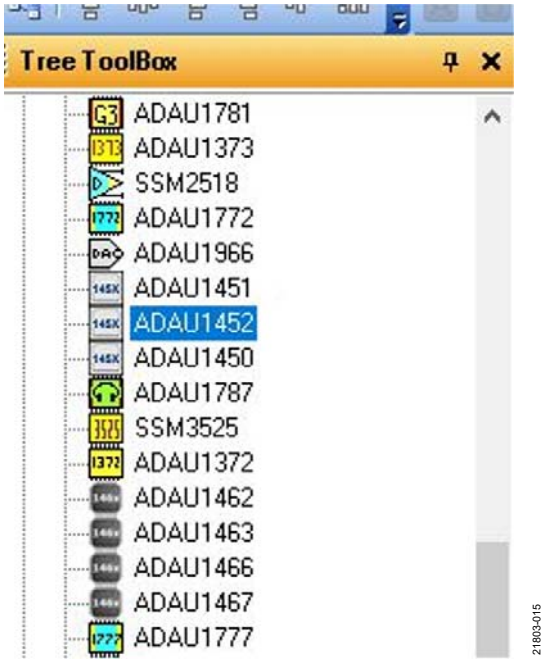


*Figure 15. Adding an **ADAU1452** Component*

6. Ensure that SigmaStudio can detect the USBi on the USB port of the PC by checking if the background of the **USB** label is green in the **USB Interface** block (see Figure 16).

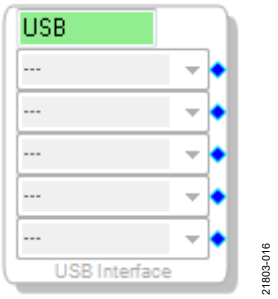


Figure 16. USBi Detected by SigmaStudio

7. When SigmaStudio cannot detect the USBi connected to the PC USB port, the background of the **USB** label is red (see Figure 17). This error can occur either when the USBi is not connected to the port or when the drivers are installed incorrectly.

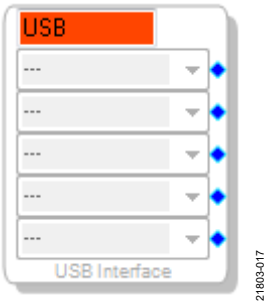


Figure 17. USBi Not Detected by SigmaStudio

8. To connect the **USB Interface** block to the **IC 1** block, the ADAU1452, click and drag a line representing a wire between the blue pin of the **USB Interface** block and the green pin of the **IC1** block (see Figure 18). This connection allows the USBi to communicate with the ADAU1452. The corresponding drop-down field of the **USB Interface** block automatically fills with the default mode and channel for the connected **IC1** block. With the ADAU1452, the default communications mode is SPI, the default slave select line is 1, and the default address is 0.

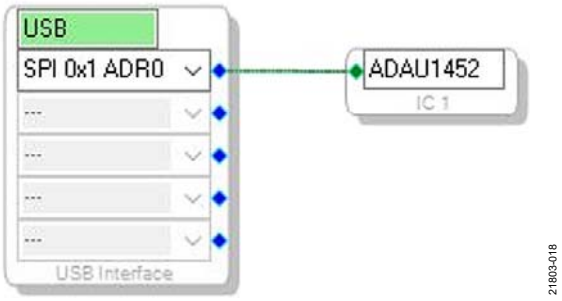


*Figure 18. Connecting the **USB Interface** Block to the **IC 1** Block in the **Hardware Configuration** Tab*

CREATING A BASIC SIGNAL FLOW

To create a signal processing flow, take the following steps:

1. Click the **Schematic** tab near the top of the window (see Figure 19).

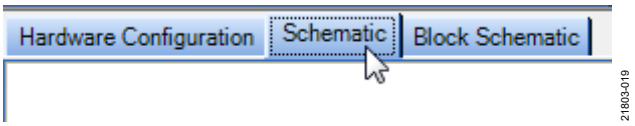


*Figure 19. **Schematic** Tab*

2. To add the appropriate elements to the project space, click and drag the elements from the **Tree ToolBox** to the empty white project space on the right of the window. The **Tree ToolBox** contains all the algorithms that can run in SigmaDSP.
3. Add an **Input1** block by clicking the **Input** component from the **(IC 1) ADAU1452** > **IO** > **Input** > **sdata 0-15** folder (see Figure 20), and then dragging it into the empty project space. The **Input1** block, which represents an input channel, then appears as shown in Figure 21. By default, Channel 0 and Channel 1 are selected and this configuration matches the analog audio source hardware connections shown in Figure 11 and Figure 12. Therefore, no modifications are needed.

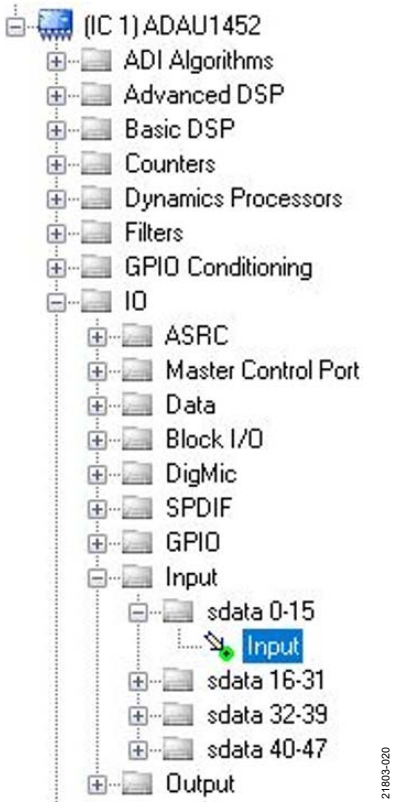


*Figure 20. Adding an **Input** Component*

*Figure 21. **Input1** Block in the Project Space*

4. Add two output blocks, **Output1 and Output2**, by clicking the **Output** component from the **(IC 1) ADAU1452** > **IO** > **Output** folder (see Figure 22), and then dragging it into the project space. Ensure that these blocks, which represent output channels, are assigned to Channel 0 and Channel 1.

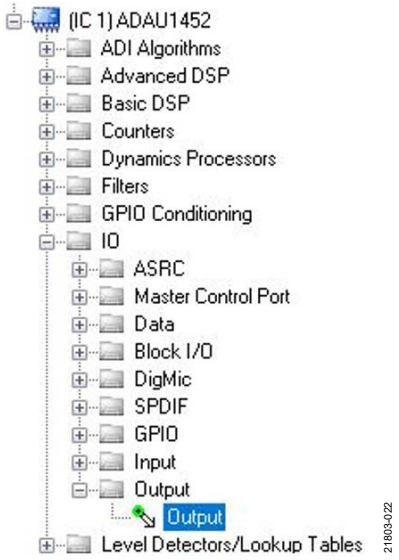


*Figure 22. Adding an **Output** Component*

5. Repeat Step 4 to add another output (see Figure 23).

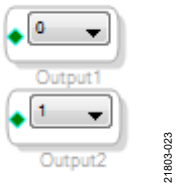


*Figure 23. **Output1** and **Output2** Blocks in the Project Space*

6. To connect each **Input1** channel to the corresponding output block, click and drag a line representing a wire between the blue pin of the **Input1** block and the green pin of the corresponding output block (see Figure 24). **Input1** Channel 0 connects to **Output1** Channel 0 and **Input1** Channel 1 connects to **Output2** Channel 1.

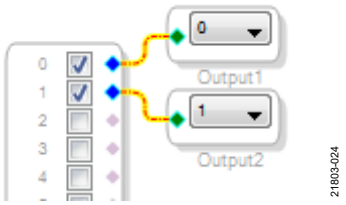


Figure 24. Signal Flow with Two Analog Inputs and Two Analog Outputs Connected

The default register settings in SigmaStudio are configured to match the EVAL-ADAU1452REVBZ board hardware, including the signal routing between the ADAU1452 and the AD1938 codec.

When these steps are complete, the basic signal flow is complete and the stereo analog input source passes directly through the SigmaDSP and connects to the stereo analog output.

Add Volume Control

To add volume control functionality to the project, take the following steps:

1. Add a **Single1** block (volume control) by clicking the **Single Volume** component from the **Volume Controls** > **Adjustable Gain** > **Clickless HW Slew** folder (see Figure 25), and then dragging it to the project space.

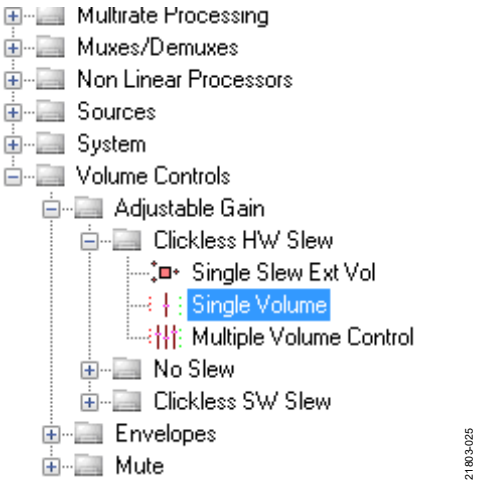


*Figure 25. Adding a **Single Volume** Component*

2. By default, the **Single1** block has one input and one output, meaning it is a single channel. To add another channel, right-click the empty white space of the **Single1** block and from the drop-down menu that appears, select the **Grow Algorithm** > **1. Gain (HW slew)** > **1** option (see Figure 26).
3. To delete the existing yellow connection wires, the connections added in Step 6 of the Creating a Basic Signal Flow section, click the connection wires and then press the **Delete** key.

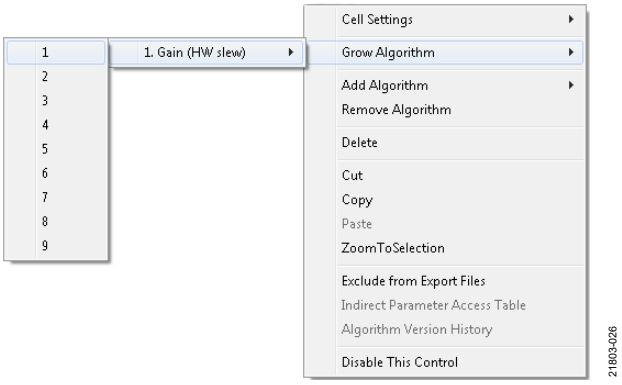


*Figure 26. Adding a Channel to the **Single1** Block*

4. Connect the blocks as shown in Figure 27.

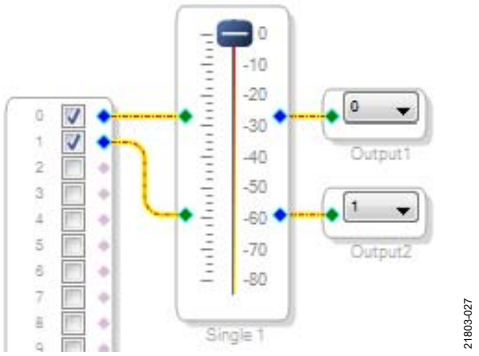


Figure 27. Completed Signal Flow with Volume Control

After performing these steps, the schematic of the completed signal flow (see Figure 27) is ready to be compiled and downloaded to the evaluation board.

DOWNLOADING THE PROGRAM TO THE DSP

After the signal is completed, compile and download the DSP code to the DSP either by clicking the **Link/Compile/Download** button in the main toolbar of SigmaStudio (see Figure 28) or by pressing the **F7** key.

*Figure 28. **Link/Compile/Download** Button*

After the code is downloaded to the DSP, the following events occur almost simultaneously:

- If the compiler finishes compiling the project, the compiled data downloads from SigmaStudio via the USBi to the ADAU1452, and the SigmaDSP starts running.
- The status bar in the lower right corner of the SigmaStudio window (see Figure 29) turns from blue to green and the text changes from **Design Mode** to **Active: Downloaded** (see Figure 29 and Figure 30). Until this point, SigmaStudio is in design mode, as noted by the blue status bar and the **Design Mode** text in the lower right corner of the SigmaStudio window (see Figure 29).

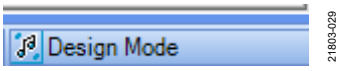


*Figure 29. **Design Mode** and Blue Status Bar*

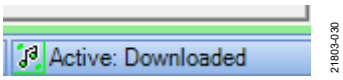


*Figure 30. **Active: Downloaded** Text and Green Status Bar*

- The signal flow runs on the EVAL-ADAU1452REVBZ board and the audio passes from the analog input to the analog output. To change the volume in real time, click and drag the volume control slider in the **Single1** block in the **Schematic** tab (see Figure 27).
- The **Output** window shown in Figure 31 is open by default at the time of compilation and displays a compiler output log. Open or close the **Output** window by using the keyboard shortcut, **Ctrl** + **4**. The **Output** window shows the compiler output log only if it is open when the **Link/Compile/Download** button is clicked.

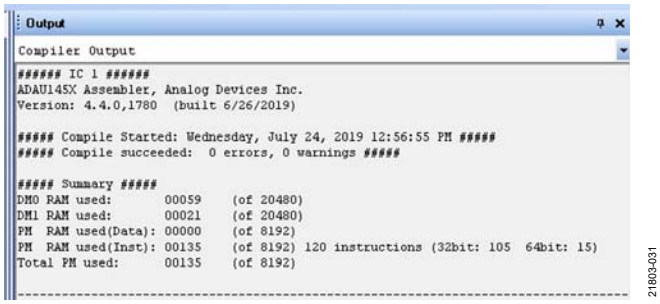


Figure 31. Compiler Output Window

ADDING S/PDIF INPUT AND OUTPUT TO THE PROJECT

The EVAL-ADAU1452REVBZ evaluation board has two optical S/PDIF interfaces. One interface is an optical input that converts the optical signal to an electrical signal that is sent to the ADAU1452 S/PDIF receiver (the SPDIFIN pin). The other interface is an optical output that takes the electrical output from the ADAU1452 S/PDIF transmitter (the SPDIFOUT pin) and converts it to an optical signal.

Figure 32 shows the location of the optical input connector and the optical output connector. The connectors are located on the underside of the PCB.

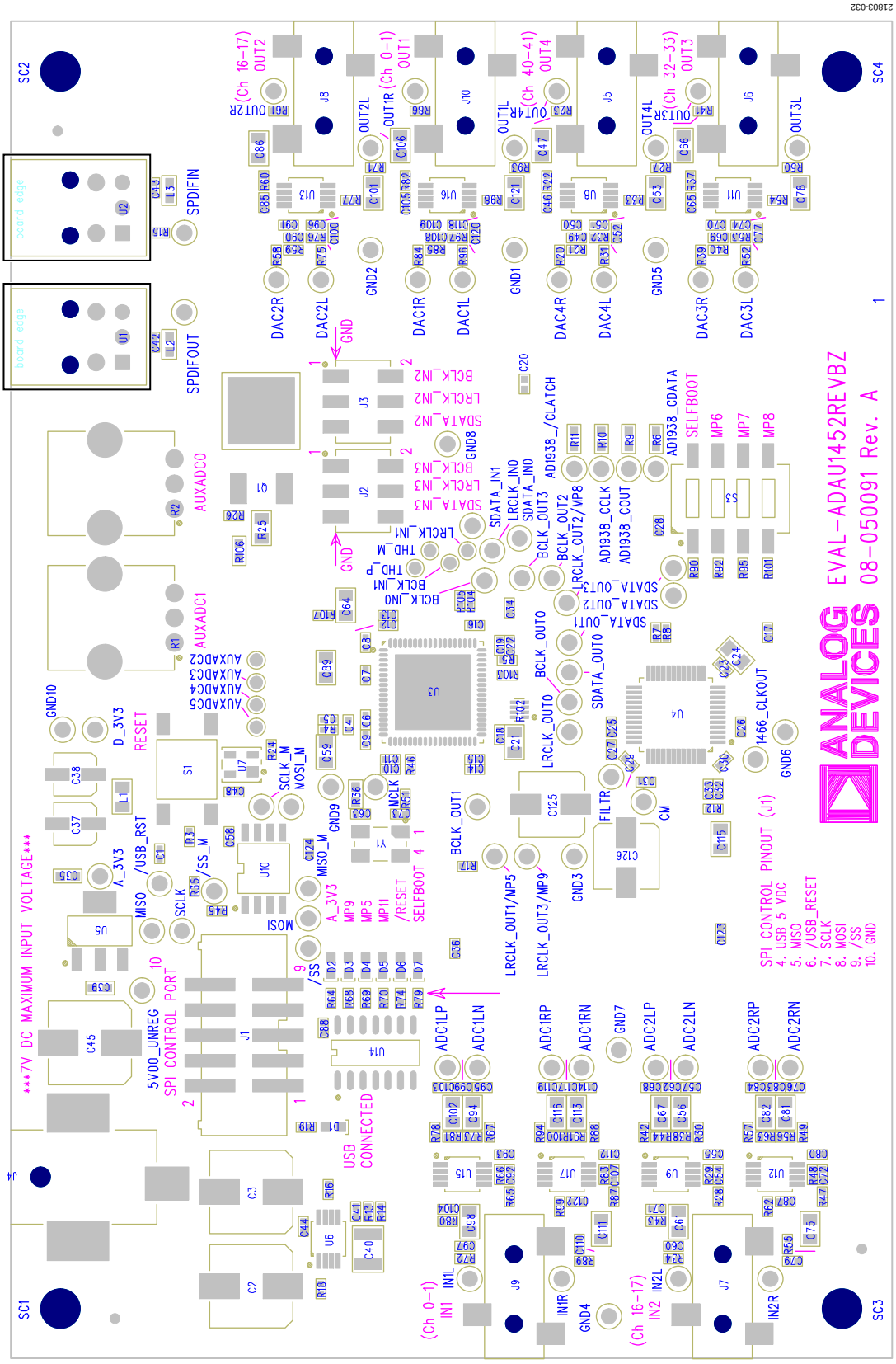


Figure 32. Location of S/PDIF Optical Input (J5) and S/PDIF Optical Output (J6), Schematic Rotated 90°

To add a stereo S/PDIF input and output to the project in SigmaStudio, take the following steps:

1. Connect an S/PDIF source to the EVAL-ADAU1452REVBZ board by connecting a standard TOSLINK® optical cable to the S/PDIF receiver connector, U2 (see Figure 33).

Figure 33. Optical S/PDIF Input Connection

2. Configure the S/PDIF input and output by modifying the ADAU1452 registers with the following steps in order:

   - Click the **Hardware Configuration** tab, then click the **IC 1 – ADAU145x Register Controls** tab at the bottom of the window (see Figure 34).

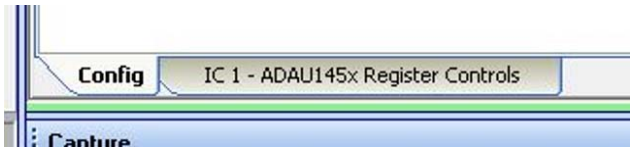


*Figure 34. Selecting the **IC 1 - ADAU145x Register Controls** Tab*

   - Next, click the **SPDIF_RX** tab (see Figure 35).

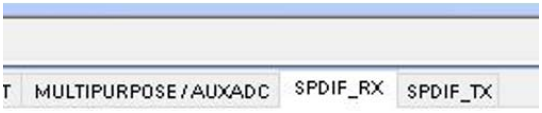


*Figure 35. Selecting the **SPDIF_RX** Tab*

   - Enable the SPDIF_RESTART register by clicking the **Do not automatically restart the audio on relock** button (see Figure 36). After clicking this button, the text displayed on the button changes to **Restarts the audio automatically on relock** and the color changes from red to green (see Figure 37).

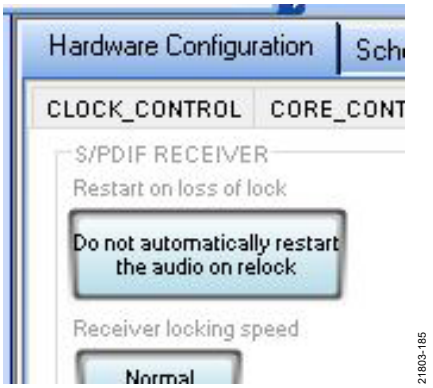


Figure 36. Activating the SPDIF_RESTART Register, Initial Button

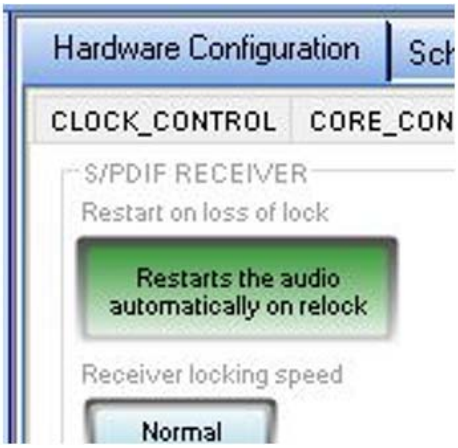


Figure 37. Activating the SPDIF_RESTART Register, Changed Button

   - To enable the S/PDIF interface, click the **Disabled** button in the **SPDIF TX EN** section. When this button is clicked, the text displayed on the button changes to **Enabled** and the button color changes from red to green (see Figure 38).

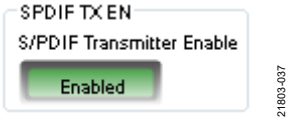


Figure 38. Enabling the SPDIF_TX_EN Register

3. Click the **ROUTING_MATRIX** tab in the register controls tab shown in Figure 34 to allow users to configure the routing matrix (see Figure 39).

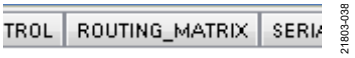


*Figure 39. Selecting the **ROUTING_MATRIX** Tab*

4. To configure the S/PDIF receiver signal routing, click the first asynchronous sample rate converter (ASRC) button, **ASRC 0** (see Figure 40), in the **ROUTING_MATRIX** tab to open the window in Figure 41. Configure the **ASRC 0** routing matrix registers using the drop-down menus until the menus match Figure 41. This configuration routes the S/PDIF receiver signal through an ASRC before the signal is accessed in the DSP core. It is necessary to route the signal through the ASRC because the clock recovered from the S/PDIF source is not synchronous to the ADAU1452.

*Figure 40. **ASRC 0** Control Button*

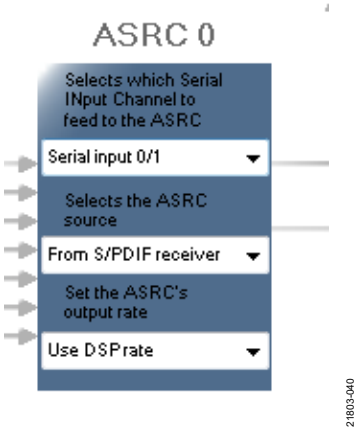


*Figure 41. Configuring the **ASRC 0** Routing Matrix Registers*

5. To configure the S/PDIF transmitter signal routing, begin by clicking the **S/PDIF TX** box (see Figure 42).

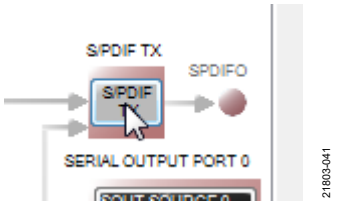


Figure 42. Configuring the S/PDIF Transmitter Routing Matrix Register

6. From the drop-down menu that appears, select the **From DSP** option to choose the signal coming from the DSP core to route the DSP core outputs to the S/PDIF transmitter (see Figure 43).

Figure 43. Routing the DSP Core Outputs to the S/PDIF Transmitter

7. Close the **SPDIFTX INPUT** dialog box shown in Figure 43.
8. Confirm the DSP core outputs are routed to the S/PDIF transmitter by verifying that the color of the **S/PDIF TX** box changes from gray to black (see Figure 44). If the color of the box changes to black, the DSP core is successively routed to the S/PDIF transmitter, allowing the output of **ASRC 0** to be used in the DSP program.

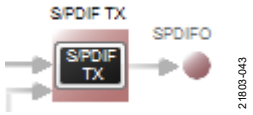


Figure 44. Confirming the DSP Core Outputs Are Routed to the S/PDIF Transmitter

9. Click the **Schematic** tab at the top of the window to return to the schematic design view.
10. Add an **Asrcin1** block (the S/PDIF input) to the project by clicking the **Asrc Input** component from the **IO** > **ASRC** > **From ASRC** folder (see Figure 45), and dragging it to the project space where it appears as shown in Figure 46.

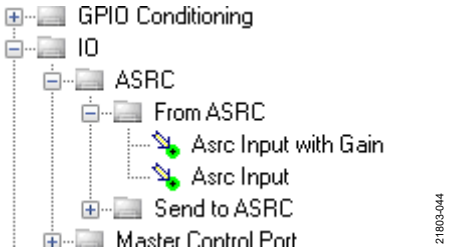


*Figure 45. Adding an **Asrc Input** Component*

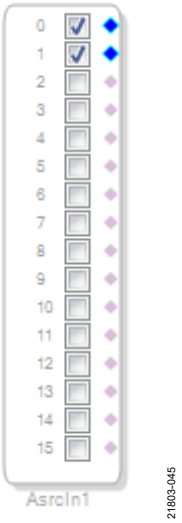


*Figure 46. **Asrcin1** Block in Project Space*

Because the left and right signals of the S/PDIF receiver pass through the **ASRC 0**, the input to the DSP program is the **Asrcin1** block in SigmaStudio. The naming convention for the input and output blocks is such that all blocks in SigmaStudio are named from the perspective of the DSP core. Therefore, the **Asrcin1** block in SigmaStudio represents the input to the DSP from the ASRC outputs. The inputs to the ASRCs themselves are defined in the register window (see Figure 41).

By default, Channel 0 and Channel 1 are active when the corresponding checkboxes are selected. Because the **ASRC 0** outputs correspond to Channel 0 and Channel 1, use the default configuration shown in Figure 46. For reference, Table 1 provides a mapping of the ASRC outputs to the corresponding channels on the **Asrcin1** block in the DSP schematic.

Table 1. ASRC Output to SigmaStudio Input Channel Mapping

ASRC Output	Corresponding Channels on ASRC Input Block in SigmaStudio
ASRC 0	Channel 0 and Channel 1
ASRC 1	Channel 2 and Channel 3
ASRC 2	Channel 4 and Channel 5
ASRC 3	Channel 6 and Channel 7
ASRC 4	Channel 8 and Channel 9
ASRC 5	Channel 10 and Channel 11
ASRC 6	Channel 12 and Channel 13
ASRC 7	Channel 14 and Channel 15

11. Add two S/PDIF output blocks, **SpdifOut1** and **SpdifOut2**, to the project by clicking the **Spdif Output** component (see Figure 47), and then dragging it to the project space.

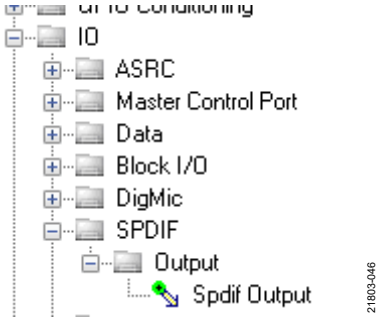


*Figure 47. Adding a **Spdif Output** Component*

12. Repeat the previous step to add another S/PDIF output block.
13. Connect the signals from the **Asrcin1** block to the **SpdifOut1** and **SpdifOut2** blocks with wires so that the resulting signal flow resembles Figure 48.
14. Click the **Link/Compile/Download** button (see Figure 28) or press the **F7** key. The signal flow then compiles and downloads to the hardware.
15. Confirm the S/PDIF inputs, outputs, and ASRCs are properly oriented by checking that any signal input to the S/PDIF optical receiver is copied and output on the S/PDIF optical transmitter.

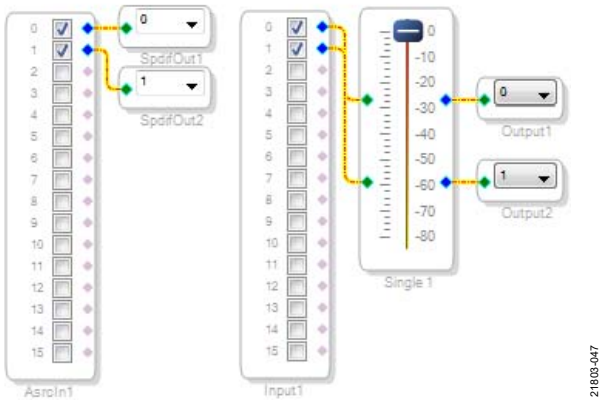


Figure 48. Signal Flow Including the S/PDIF Input (via the ASRC) Connected to the S/PDIF Output

Add a Filter

To add a filter, take the following steps:

1. Add a **MidFilter1** block by clicking the **Medium-Size Eq** component from the **Filters** > **Second Order** > **Double Precision** folder (see Figure 49), and then dragging it to the project space.

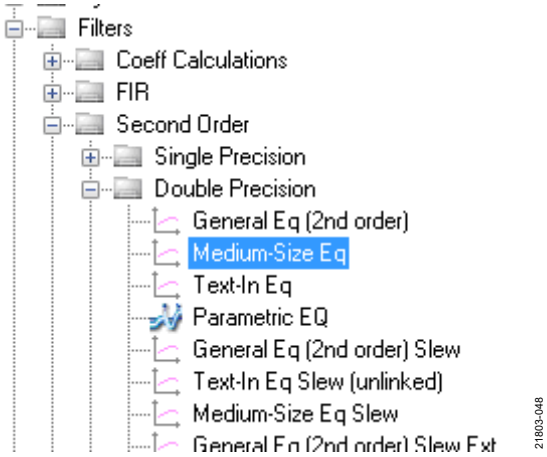


*Figure 49. Adding a **Medium-Size Eq** Component*

2. By default, the block has one input and one output (single channel). To add another channel, right-click the empty white space of the **MidFilter1** block, then select **Grow Algorithm** > **1. Multi-Channel – Double Precision: Grow Channels** > **1** option from the drop-down menu that appears (see Figure 50).

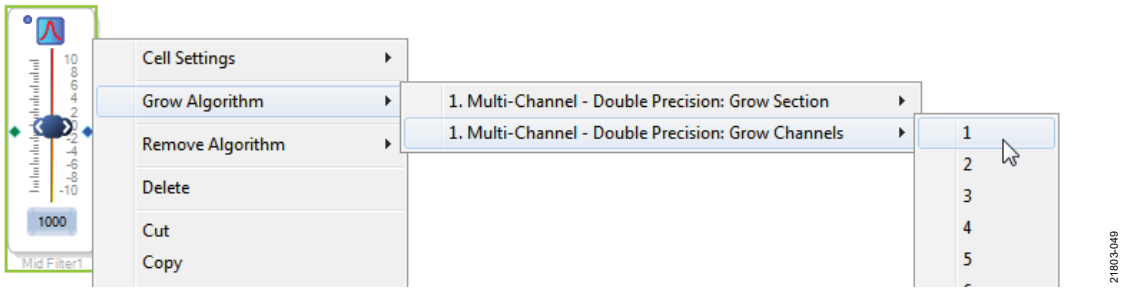


Figure 50. Adding a Channel to the Filter

3. Connect the filter in series between the **Asrcin1** block and the **SpdifOut1** and **SpdifOut2** blocks to apply the filter to the signals passing through the DSP. The completed signal flow resembles Figure 51.

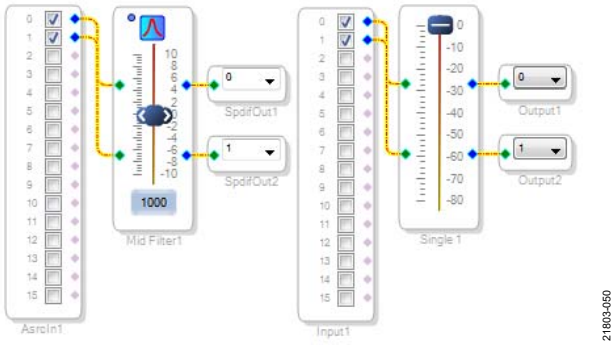


Figure 51. Completed Signal Flow

4. Click the **Link/Compile/Download** button (see Figure 28) or press the **F7** key to compile the signal flow and download it to the evaluation board hardware. The audio signal passes from the S/PDIF receiver through the ASRCs, into the DSP and the filter, and then out on the S/PDIF transmitter.
5. To change the settings of the filter, click the blue icon at the top left of the **Mid Filter1** block (see Figure 51). To change the filter gain in real time while the project is running, drag the control slider in the **MidFilter 1** block.

CONTROLLING VOLUME WITH A POTENTIOMETER

The 10-bit auxiliary analog-to-digital converter (ADC) (AUXADC) on the ADAU1452 eliminates the need for a microcontroller in many applications by using analog control signals as user interface devices. For example, the EVAL-ADAU1452REVBZ board includes two 10 kΩ linear potentiometers, R1 and R2 (see Figure 66), connected to Channel AUXADC0 and Channel AUXADC1. These potentiometers can be used as an inexpensive, versatile, and physical way to control parameters such as gain, filter corner frequency, slew rate, and compression level. The following steps demonstrate how to configure a potentiometer as a stereo volume control:

1. Create a new project in SigmaStudio, and use the **Hardware Configuration** tab to use an ADAU1452 as described in the Setting up Communications in SigmaStudio section.
2. Add an **Input1** block and two output blocks as described in the Creating a Basic Signal Flow section.
3. Add an **ADC In1** block by clicking the **Auxiliary ADC Input** component from the **IO** > **GPIO** > **Input** folder (see Figure 52), and then dragging it to the project space.

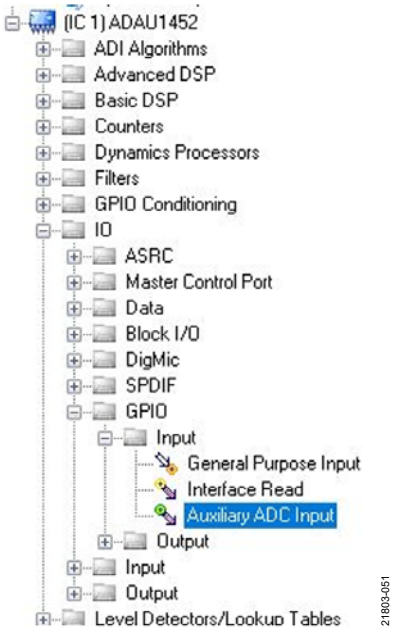


*Figure 52. Adding an **Auxiliary ADC Input** Component*

4. Add a **Shift1** block by clicking the **Arithmetic Shift** component from the **Basic DSP** > **Arithmetic Operations** folder (see Figure 53), and then dragging it to the project space.

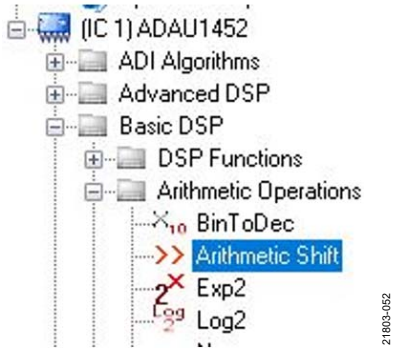


*Figure 53. Adding an **Arithmetic Shift** Component*

5. The **Shift1** block performs a bitwise shift to the right or to the left. Click the blue button in the **Shift1** block in Figure 58 to select the direction of the shift. Ensure the block is performing a left shift for a multiplication function. The **Shift1** block appears as shown in Figure 58.
6. To set the number of bits the **ADC In1** block is shifted by to 14, click and type in the yellow text box in the **Shift1** block in Figure 58.
7. Add two **DSP Readback** blocks to the project space by clicking the **DSP Readback** component from the **Basic DSP** > **DSP Functions** folder (see Figure 54), and then dragging it to the project space.

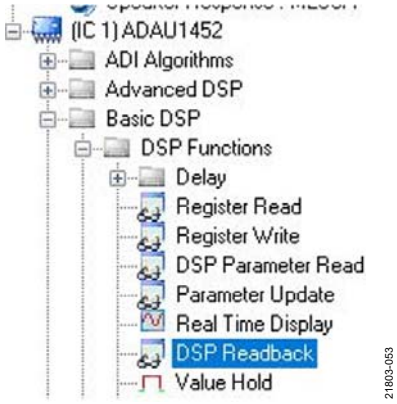


*Figure 54. Adding the **DSP Readback** Component*

8. Repeat Step 7 to add another **DSP Readback** block.
9. The **DSP Readback** block uses the USBi to read a signal value from the memory of the DSP core as the algorithm is executing. The block passes the signal (unchanged) through from the **Input1** block to the output blocks.
10. Click the **Read** button in the **DSP Readback** block (see Figure 55) to fetch the instantaneous value of the signal passing through the block.
11. It is possible to set the **DSP Readback** block to poll the current sample value repeatedly. This polling feature is useful for debugging but substantially increases the amount of computer processing time, USB communication, and screen refreshes performed by SigmaStudio. Avoid setting a large number of **DSP Readback** blocks to read continuously because this action can cause the PC to run slowly. Note that this action does not affect the real-time processing on the SigmaDSP core.
12. On each **DSP Readback** block, click the blue dot to the left of the **Read** button to read both blocks continuously (see Figure 55).

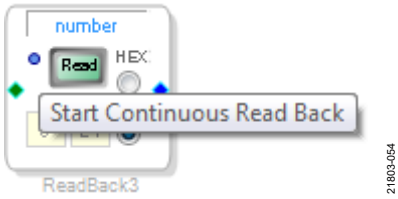


Figure 55. Activating Continuous Readback

13. For one of the **DSP Readback** blocks, change the numeric format used to decode and display the signal value to 32.0 by inputting 32 in the left format box and then pressing the **Tab** key. SigmaDSP uses a numeric format of 8.24 for audio signals. See Figure 58 for more details.
14. Add an externally controlled volume control with slew (to prevent zipper noise), the **Slew vol 1** block, by clicking the **Single Slew Ext Volume** component from the **Volume Controls** > **Adjustable Gain** > **Clickless HW Slew** folder (see Figure 56), and then dragging it to the project space.

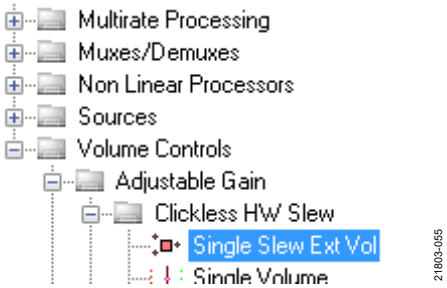


*Figure 56. Adding a **Single Slew Ext Vol** Component*

15. By default, the **Slew vol 1** block has one audio signal input. To add another channel, right-click the empty white space of the **Slew vol 1** block and select the **Grow Algorithm > 1. Gain (HW slew) > 1** option from the drop-down menu that appears (see Figure 57).

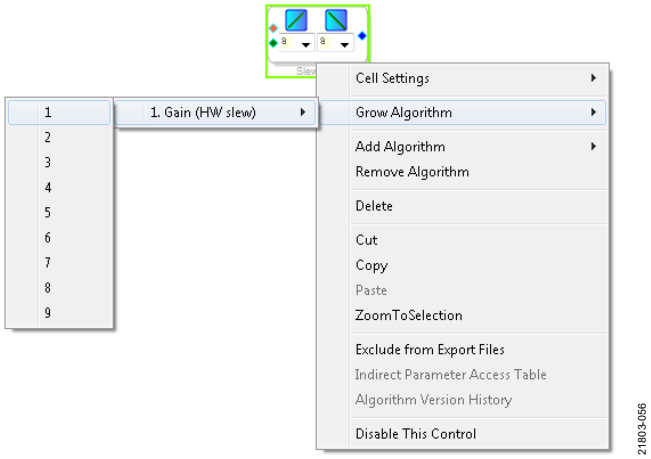


*Figure 57. Adding a Channel to the **Slew vol 1** Block*

16. Wire the blocks together as shown in Figure 58. The position of blocks in the diagram does not matter.
17. Click the **Link/Compile/Download** button (see Figure 28) or press the **F7** key to compile the signal flow and download it to the evaluation board hardware. The audio signal passes from the S/PDIF receiver through the ASRCs into the DSP and the filter, and then out on the S/PDIF transmitter. To change the settings of the filter, click the blue icon at the top of the **Mid Filter1** block (see Figure 51). Drag the control slider in the **Mid Filter1** block to change the filter gain in real time while the project is running.

The schematic (see Figure 58) shows audio from input Channel 0 and input Channel 1 connected to the input of a **Slew vol 1** block. The volume is controlled by the **AUX_ADC_1** value of the **ADC In1** block, which is controlled by the left potentiometer, R1.

The output of the AUXADC on the ADAU1452 is a 10-bit integer value in a 32 bit register. The first **DSP Readback** block before the left shift displays the output of the ADC in 32.0 format, which can be interpreted as 32 integer bits and 0 fractional bits. When the potentiometer is turned fully counterclockwise, this block reads back the minimum ADC output value of 0. When the potentiometer is turned fully clockwise, this block reads back the maximum ADC output value of 1023 (within the range of the component tolerance).

The native audio format of the ADAU1452 is 8.24. In this example, the volume control multiplies the input signal by a fractional value ranging from 0 (silence) to 1 (unity gain). Therefore, the control signal from the ADC must be shifted left 14 bits to scale the maximum value appropriately.

The second **DSP Readback** block after the left shift displays the output of the ADC in 8.24 format, which can be interpreted as eight integer bits and 24 fractional bits. When the potentiometer is turned fully counterclockwise, this **DSP Readback** block reads back the minimum ADC output value of 0. When the potentiometer is turned fully clockwise, this block reads back the maximum ADC output value of 1 (within the range of the component tolerance).

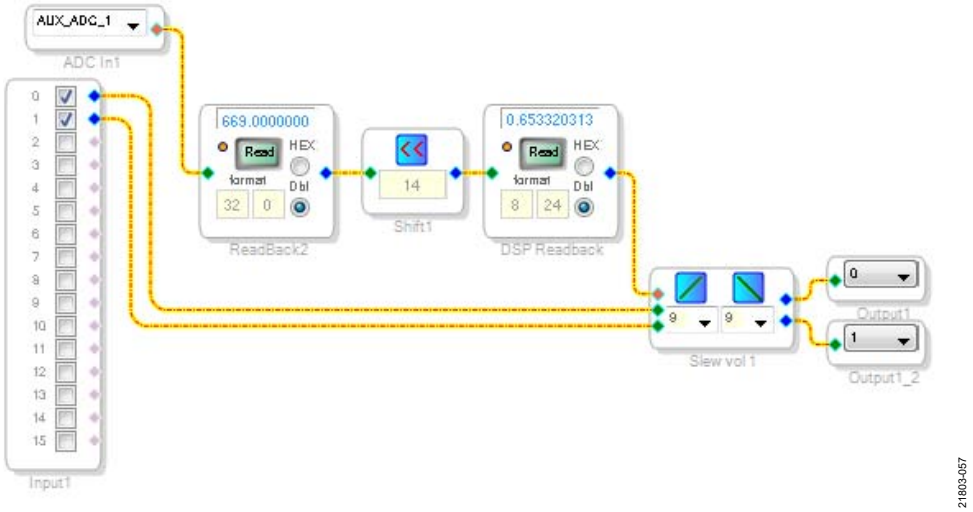


Figure 58. Completed Signal Flow with DSP Readback

USING THE EVALUATION BOARD

POWER SUPPLY

Power is supplied to the evaluation board using a dc power supply with a female positive center plug. The plug has a 2.1 mm inner diameter, a 5.5 mm outer diameter, and a 9.5 mm length (see Figure 59). The output must range between 5 V and 7 V and must be able to source at least 1.5 A of current. Connect the power supply to Connector J4 (see Figure 9). The unregulated supply powers the operational amplifiers used in the active audio filters for the analog audio inputs and outputs.

An on-board linear regulator (U5) generates the 3.3 V dc supply required for the ADAU1452 and AD1938, as well as other supporting ICs. When the power supply is connected properly, LED D2 (A_3V3) illuminates (see Figure 76).

Figure 59. DC Power Supply Plug and Cable

INPUTS AND OUTPUTS

The EVAL-ADAU1452REVBZ board provides access to the serial ports, S/PDIF interfaces, multipurpose (MPx) pins, and AUXADCs of the ADAU1452.

AD1938 Codec

Two of the four serial input ports are connected to the ADCs of the AD1938. All four serial output ports are connected to the digital-to-analog converters (DACs) of the AD1938 for a total of four analog audio input channels and eight analog audio output channels.

The AD1938 is hardwired in standalone mode and the serial ports are configured as clock slaves. Therefore, the corresponding serial ports on the ADAU1452 must be set as clock masters. By default, all serial ports on the ADAU1452 are set as clock masters when a new project is created in SigmaStudio.

Standalone mode eliminates the need and ability to configure the AD1938 registers via the SPI port. This mode fixes the sample rate of the AD1938 at either 44.1 kHz or 48 kHz. It is not possible to change this setting. Even though the ADAU1452 is flexible and can run at any sample rate up to 192 kHz, the analog audio inputs and outputs on the EVAL-ADAU1452REVBZ board can be distorted or silent if a sample rate other than 44.1 kHz or 48 kHz is used for the ADAU1452 serial ports.

Stereo Line Inputs

Two stereo input jacks allow four, single-ended, line level analog input signals. The AD1938 ADC inputs are configured such that the full-scale signal is 2.8 V p-p, which is approximately 1 V rms for a sine wave. Any signal that exceeds 2.8 V p-p at the audio jack is clipped, which creates distortion. The signals are fed to active, low-pass filters and converted to differential pairs before reaching the ADCs of the AD1938. The filters are designed for a system sample rate of 44.1 kHz or 48 kHz.

The stereo input jacks accept standard stereo TRS 3.5 mm (1/8 inch) mini plugs. The tip is connected to left audio, the ring is connected to the right audio, the sleeve is connected to the common left and right audio grounds with two channels of audio (see Figure 60).

Figure 60. Standard Stereo TRS 1/8 Inch Mini Audio Plug and Cable

The signals pass through the AD1938 ADCs and are then sent to the ADAU1452 serial input ports in I²S format. Table 2 maps the input signals to input channels in SigmaDSP and SigmaStudio.

Table 2. Mapping of Stereo Analog Input Signals to SigmaStudio Channels

Input Jack	Plug Contact	AD1938 ADC Pins	ADAU1452 Serial Input Pins	Input Channel in SigmaStudio
J9	Left (tip)	ADC1LN, ADC1LP	SDATA_IN0	0
J9	Right (ring)	ADC1RN, ADC1RP	SDATA_IN0	1
J7	Left (tip)	ADC2LN, ADC2LP	SDATA_IN1	16
J7	Right (ring)	ADC2RN, ADC2RP	SDATA_IN1	17

Stereo Line Outputs

Four stereo output jacks allow eight, line level analog output signals. The AD1938 DAC outputs are configured such that a full-scale signal is 2.8 V p-p at the jack, which is approximately 1 V rms for a sine wave. The signals output from the DACs are fed to active low-pass filters and then ac-coupled before reaching the output jacks. The filters are designed for a system sample rate of 44.1 kHz or 48 kHz.

The output filters are designed to drive high impedance loads, such as loads from active speakers. Some low impedance loads, such as loads from headphones, can also be driven by these filters. However, very low (< 64 Ω) impedance loads, such as loads from passive speakers, cannot be driven by these output filters.

The stereo output jacks accept standard stereo TRS 1/8 inch mini plugs. The tip is connected to left audio, the ring is connected to the right audio, the sleeve is connected to the common left and right audio grounds with two channels of audio (see Figure 60).

The signals first pass from the ADAU1452 serial outputs in I²S format to the AD1938 DACs, where they are converted to analog signals and sent through the output filters to the output jacks. Table 3 shows the mapping among the SigmaStudio output channels, output serial ports, and output jacks.

S/PDIF Optical Transmitter and Receiver

The ADAU1452 S/PDIF interfaces are connected directly to optical transmitter and receiver connectors that convert the electrical signals to and from optical signals, respectively. The connectors accept standard TOSLINK connectors and optical fiber cables (see Figure 61).

Figure 61. TOSLINK Connector and Optical Fiber Cable for S/PDIF Input and Output

The ADAU1452 S/PDIF receiver accepts signals with sample rates between 18 kHz and 192 kHz. Because the incoming signal is asynchronous to the system sample rate, use an ASRC to convert the sample rate of the incoming signal. Optionally, configure the SigmaDSP core to start processing audio samples based on the sample rate of the incoming S/PDIF receiver signal, negating the need for an ASRC. However, users are strongly recommended to use an ASRC for performance and reliability reasons.

The ADAU1452 S/PDIF transmitter typically transmits signals from the DSP core so the sample rate of the audio coming out of the S/PDIF transmitter on the EVAL-ADAU1452REVBZ board is typically 44.1 kHz or 48 kHz. Optionally, configure the S/PDIF transmitter in a pass through mode, where the transmitter simply transmits a copy of the signal directly from the receiver.

Both the S/PDIF receiver and transmitter carry two channels of uncompressed audio.

Serial Audio Interface

Two of the four ADAU1452 serial input ports are connected to the AD1938. Because the AD1938 is in standalone mode, the device always drives the SDATA_IN0 and SDATA_IN1 pins of the ADAU1452. As a result, external data signals cannot be input to either of the SDATA_IN0 or SDATA_IN1 pins.

However, the remaining two serial input ports (Serial Input 2 and Serial Input 3) are composed of the SDATA_IN2 pin and the SDATA_IN3 pin grouped with the corresponding clock pins, BCLK_IN2, LRCLK_IN2/MP12, BCLK_IN3, and LRCLK_IN3/MP13. The serial port signals are directly accessible via the J2 and J3 headers (see Figure 62).

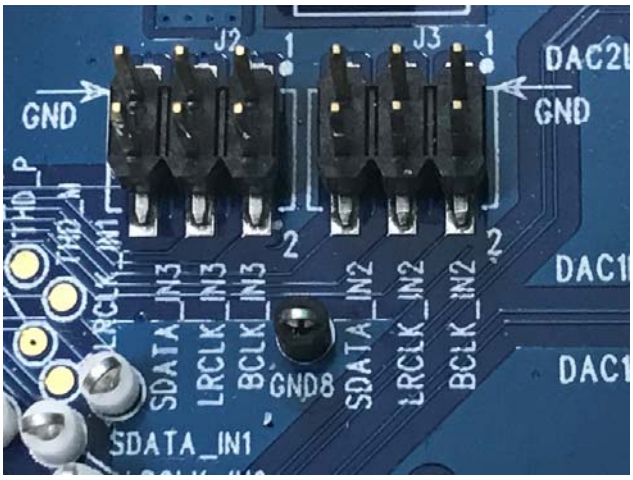


Figure 62. Serial Input Port 2 and Serial Input Port 3 Signal Access Headers

Table 3. Mapping of SigmaStudio Channels to Output Jacks

Output Jack	Plug Contact	AD1938 DAC Pin	ADAU1452 Serial Output Pin	Output Channel in SigmaStudio
J10	Left (tip)	OL1	SDATA_OUT0	0
J10	Right (ring)	OR1	SDATA_OUT0	1
J8	Left (tip)	OL2	SDATA_OUT1	16
J8	Right (ring)	OR2	SDATA_OUT1	17
J6	Left (tip)	OL3	SDATA_OUT2	32
J6	Right (ring)	OR3	SDATA_OUT2	33
J5	Left (tip)	OL4	SDATA_OUT3	40
J5	Right (ring)	OR4	SDATA_OUT3	41

Standard headers with 0.1 inch (2.54 mm) spacing provide connections from user selected external sources. The J2 and J3 headers are each comprised of two columns and three rows of pins. There is one signal column and one ground column. Always connect at least one ground wire between the header and the external signal source to maintain proper signal integrity. A standard ribbon cable provides signal integrity over longer distances because signal wires are separated by ground wires (see Figure 63).

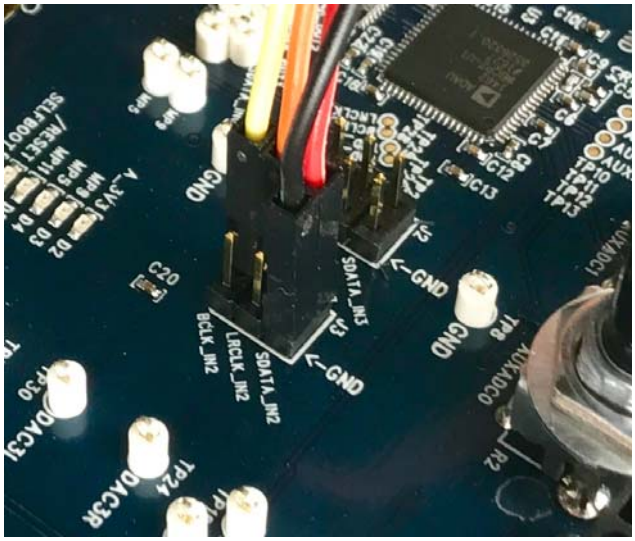


Figure 63. Connecting External I²S Signals to Serial Input Port 2

The signals passing between the ADAU1452 serial output ports and the AD1938 DAC are also accessible via the test points (see Figure 64) situated between the two ICs. Signals can be tapped from these test points and connected to external digital audio sinks if desired (see Figure 64 for connection details). When connecting these signals to external devices, connect at least one ground signal to maintain signal integrity.

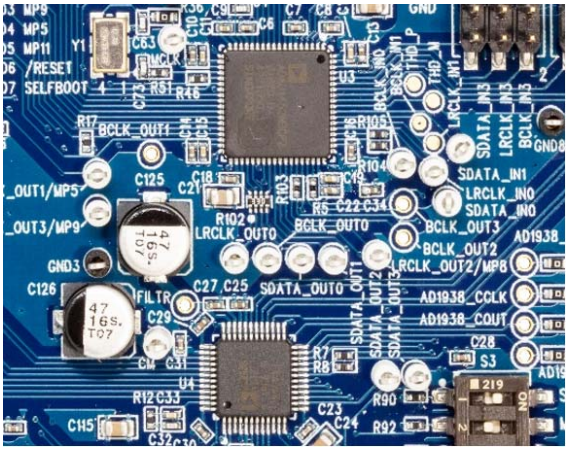


Figure 64. Test Points for Monitoring Digital Audio Signals

MULTIPURPOSE (MPx) PINS

The MPx pins on the ADAU1452 can use GPIOs when configured to do so by using the ADAU1452 control registers.

Of the 14 MPx pins, three are connected to switches that pull the signals low or tie them high, three are on test points and connected to high impedance inputs to LED drivers, and two GPIO pins are available on headers. The remaining six pins are used for other functionalities and cannot be used as multipurpose pins.

The signal from the LRCLK_OUT1/MP5 pin is fed to an inverter that drives LED D4. The signal from the LRCLK_OUT3/MP9 pin is fed to an inverter that drives LED D3. The signal from the LRCLK_IN1/MP11 pin is fed to an inverter that drives LED D5.

See the Status LEDS section for more information about the LEDs.

Table 4 describes the five MPx pins available for use as GPIOs, along with the corresponding access points on the evaluation board.

Table 4. Multipurpose Pins and Hardware Access Points

MPx Pin	Connection	Access Point
LRCLK_OUT1/MP5	Input to inverter (LED D4)	TP56
LRCLK_OUT3/MP9	Input to inverter (LED D3)	TP48
LRCLK_IN1/MP11	Input to inverter (LED D5)	TP29
LRCLK_IN2/MP12	Pin multiplexed with LRCLK_IN2	Header J3, Pin 4
LRCLK_IN3/MP13	Pin multiplexed with LRCLK_IN3	Header J2, Pin 4

To configure the operation of the MPx pins as desired, navigate to the **MULTIPURPOSE/AUXADC** tab in the **Hardware Configuration** tab in SigmaStudio (see Figure 65).

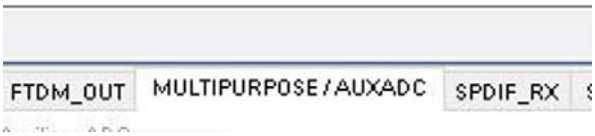


*Figure 65. **MULTIPURPOSE/AUXADC** Tab in SigmaStudio*

AUXADCx PINS

The ADAU1452 AUXADC is a 10-bit, successive approximation register (SAR) multiplexed across six input channels. These channels are used for analog control signals to the DSP. Channel AUXADC0 and Channel AUXADC1 (see Figure 66) are connected to Linear Potentiometer R1 and Linear Potentiometer R2. Channel AUXADC2 to Channel AUXADC5 are accessible on test points next to the ADAU1452 (see Figure 66). Inputs to the ADCs between 0 V and 3.3 V can be connected to these test point pads and used in the SigmaStudio signal flow (see Figure 66 for the inputs).

Figure 66 shows the potentiometers with installed knobs that are not included with the EVAL-ADAU1452REVB board. Order these knobs from Digi-Key using part number 1722-1241-ND. The part number of the manufacturer part is 1221-J.

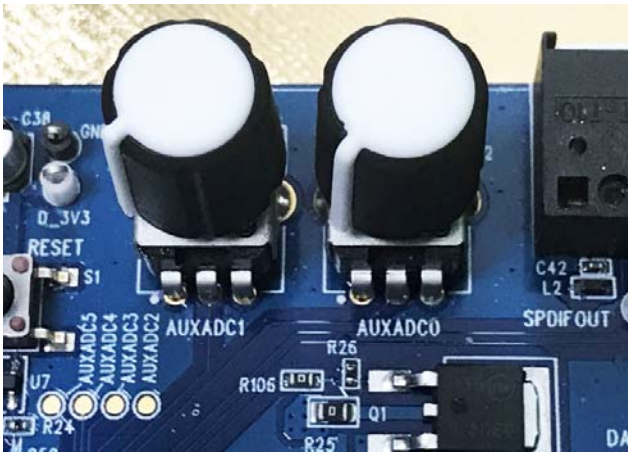


Figure 66. Potentiometers and Copper Pads for Inputting Signals to the AUXADC

COMMUNICATIONS HEADER

The communications header is a 10-pin header designed to work with the EVAL-ADUSB2EBZ (USBi). The SPI signals are wired from the communications header to the corresponding SPI slave port pins on the ADAU1452. The I²C pins are not used in this design. A reset line is also included, which allows the user to reset the devices on the EVAL-ADAU1452REVBZ board via a command in SigmaStudio, search the EngineerZone™ forums or contact SigmaDSP@analog.com for more information. When the EVAL-ADUSB2EBZ board is connected to the EVAL-ADAU1452REVBZ board and PC, powered, and recognized by the PC, LED D1 illuminates (see Figure 10).

SigmaStudio also controls the 5 V output to LED D1.

SELF BOOT

A 1 Mb, 20 MHz, SPI, serial EEPROM memory is included on the EVAL-ADAU1452REVBZ evaluation board. The ADAU1452 can boot and execute a program without help from an external microcontroller. This self boot feature allows any project developed within SigmaStudio to execute on a rising edge of the $\overline{\text{RESET}}$ pin signal or when the ADAU1452 powers up. Section 1 of the S3 DIP switch (see Figure 67) sets the state of the ADAU1452 SELFBOOT pin. Setting Section 1 of the S3 switch to off disables the self boot feature. LED D7 illuminates when the EVAL-ADAU1452REVBZ board is set to self boot (see Figure 76).

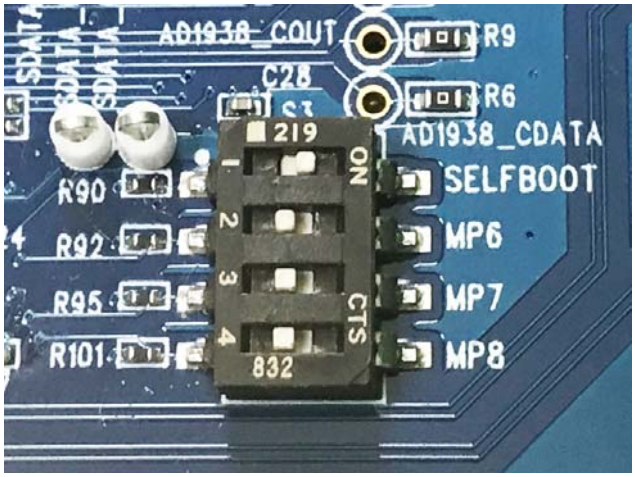


Figure 67. Self Boot EEPROM and Slide Switch

To use the self boot functionality, take the following steps:

1. Add an **IC2** (E2Prom) block to the project space of the **Hardware Configuration** tab from the **Tree ToolBox**. From the **Processors (ICs / DSPs)** folder, click **E2Prom** (see Figure 68) and drag it to the project space.

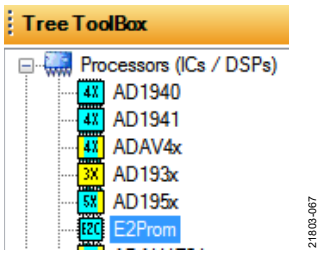


*Figure 68. Adding an **E2Prom** Component*

2. Connect the green input pin of the **IC2** block to one of the available blue output pins of the **USB Interface** block in SigmaStudio.
3. Set the communication mode to **SPI 0x1 ADR0** by clicking the text fields of the **USB Interface** block (see Figure 69). There is no physical connection between the USBi connector (a connector to the evaluation board) and the evaluation EEPROM on the EVAL-ADAU1452REVBZ board. Therefore, SigmaStudio cannot directly communicate with the EEPROM. To circumvent this lack of communication, SigmaStudio writes a program to the ADAU1452, which then uses the master SPI port to write the self boot data to the EEPROM. Adding the **IC2** block allows users to configure the EEPROM and informs SigmaStudio that a hex file must be produced.
4. The pull-down text field in the **USB Interface** block sets the type of communication the EEPROM uses. Both SPI and I^2C are supported communication types and can differ from the communication standard used by ADAU1452 the slave port. As shown in Figure 69, users are recommended to connect the **IC2** block to an unused pin on the **USB Interface** block.

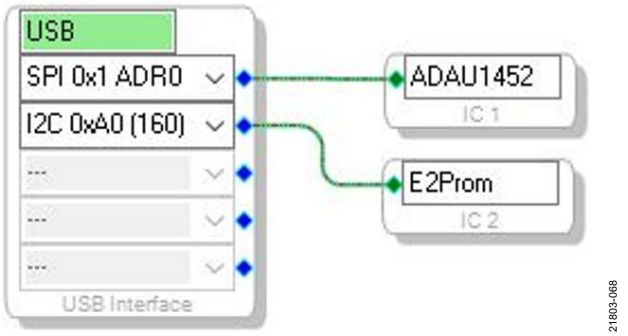


*Figure 69. **E2Prom** Setup in **Hardware Configuration** Tab*

5. Before downloading the self boot data to the EEPROM, click the **Link/Compile/Download** button (see Figure 28) or press the **F7** key to compile the SigmaStudio project file.
6. When writing to the EEPROM, set the self boot switch (Section 1 of Switch S3) to the disabled position.
7. To write to the EEPROM through the ADAU1452 master SPI port, right-click the white space in the **IC1** block in the **Hardware Configuration** tab. From the pull-down menu that appears, select the **Self-boot Memory >Write Latest Compilation through DSP** option (see Figure 70).

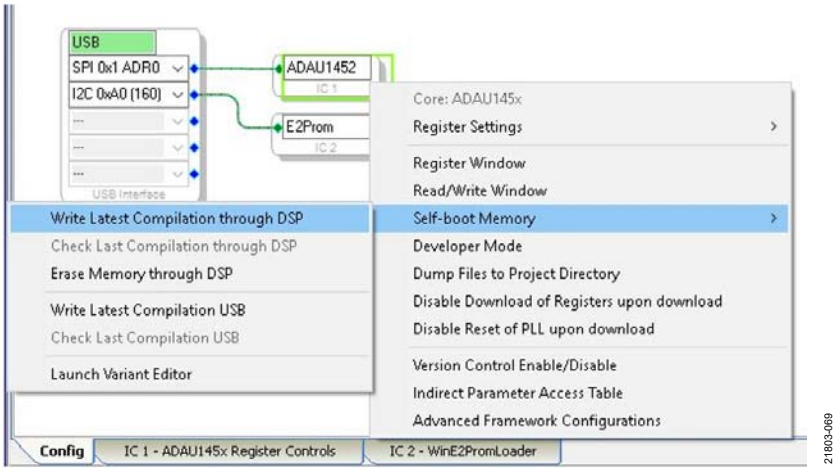


*Figure 70. **ADAU1452** Block Pull-Down Menu*

8. An **EEPROM Properties** dialog box appears. Enter the values shown in Figure 71 to the text fields and then click **OK**.

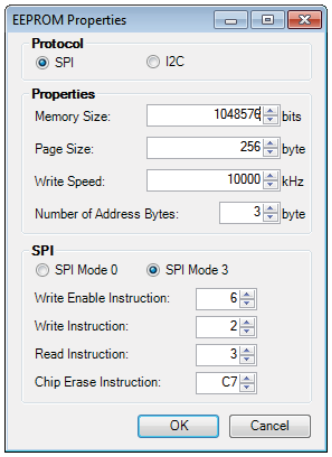


*Figure 71. **EEPROM Properties** Window and Required Settings*

9. A warning dialog window appears to remind the user that executing an external memory write erases and overwrites any data currently stored on the EEPROM (see Figure 72). Click **OK** to proceed.

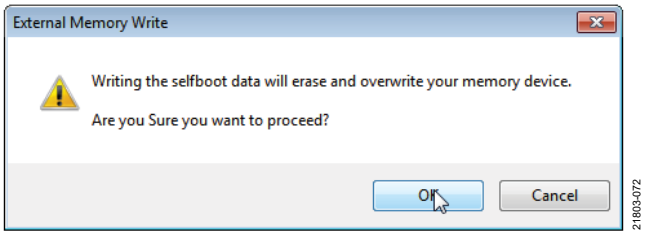


Figure 72. External Memory Erase and Overwrite Warning Window

10. SigmaStudio begins the EEPROM write operation. This operation can take several minutes to complete. Users can view the progress o the write operation with the status window shown in Figure 73. When the window disappears, the operation is complete.

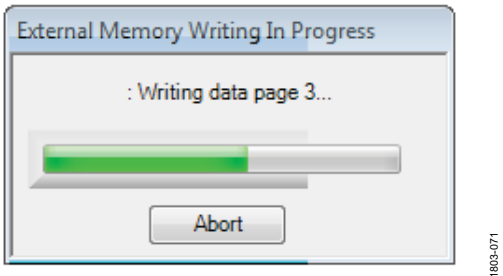


Figure 73. External Memory Write Operation Status Window

To execute a self boot operation, take the following steps:

1. Set the **SELFBOOT** switch (Section 1 of S3) to the enabled position on the EVAL-ADAU1452REVBZ board (see Figure 67).
2. Press and release the **RESET** push-button (S1) (see Figure 74).
3. A self boot operation is performed and the ADAU1452 runs the user created program.

RESET

To manually reset the ADAU1452 and AD1938, press and release the **RESET** push-button, S1 (see Figure 74). A reset generator circuit toggles the reset pins on the ADAU1452 and AD1938 to perform a full hardware reset of both devices.

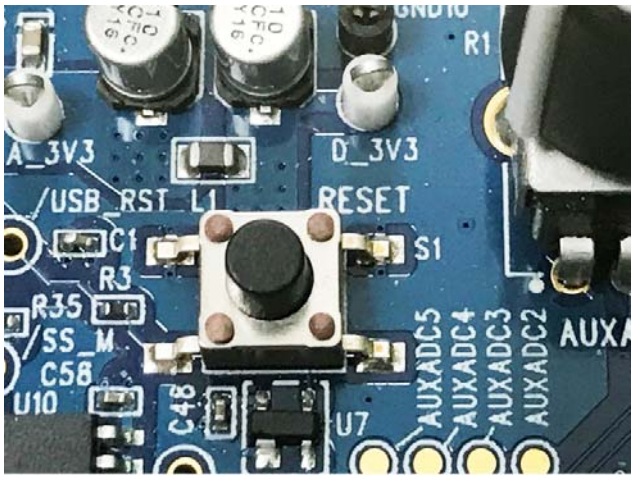


*Figure 74. Manual **RESET** Push-Button*

To generate a reset in the software, right-click the white border of the **USB Interface** block in the **Hardware Configuration** tab, and then choose the **Device Enable/Disable** option from the pull-down menu that appears (see Figure 75). Choosing this option sets the system reset signal to logic low.

Figure 75. Toggling the Reset Signal in SigmaStudio

STATUS LEDs

Six status LEDs provide information about the state of the EVAL-ADAU1452REVBZ evaluation board (see Figure 76 for LED locations). For more information about the status LEDs, see Table 6.

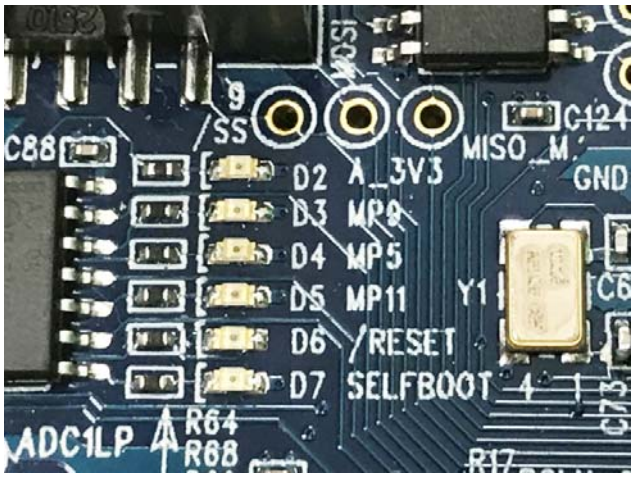


Figure 76. Status LEDs

CODEC CONTROL FROM SigmaStudio MODIFICATION

The AD1938 codec is set up to operate in standalone hardware mode. Therefore, the codec and the evaluation board only operate at a 48 kHz sampling rate and the serial communication between the codec and DSP must be in I²S format. The codec and DSP are capable of operating at different sample rates and data formats but cannot do this if the codec is in standalone mode. Users must modify the USBi and EVAL-ADAU1452REVBZ board to control the codec from SigmaStudio.

The master port of the SigmaDSP can also control the codec but this method requires a more complicated setup. Controlling the codec from SigmaStudio allows the user to both change the codec setup in real time, and to read data back from the codec. After the settings are set as the user desires, the SigmaDSP or a controller can easily capture or use the register settings after the product application is developed.

The ADAU1452 CLKOUT pin clocks the master clock of the codec, allowing flexibility of clock rates to the codec.

The only limitation in sample rate is the crystal on the evaluation board, Y1. Y1 is a 12.288 MHz crystal. Therefore, the codec can only use sample rates in multiples of 48 kHz.

The DSP has other clock generators, but the codec must be divided down from the master clock. Otherwise, it can be operated by using the DLRCLK pin or the ARLCLK pin of the codec as a phase-locked loop (PLL) input. Operating the codec PLL from the DLRCK pin or the ARLCLK pin complicates evaluation board modifications because the codec loop filter must be changed. See the AD1938 data sheet for more information. If the sample rate must operate at a rate of 44.1 kHz, Y1 must be changed to 256 × sample rate (f_S).

MODIFYING THE EVAL-ADUSB2EBZ (USBi)

In addition to modifying the evaluation board, the EVAL-ADUSB2EBZ must also be modified. J1 on the EVAL-ADUSB2EBZ PCB is a footprint for a 14-pin ribbon cable but only a 10-way ribbon is used. The unused pins are the extra SPI latch signals and one of the extra SPI latch signals control the codec. See the AN-1006 Application Note for more details about using the extra SPI latch signals.

SPI Latch 0x02 is found on Pin 1 on the 14-pin ribbon footprint. The 10-way ribbon uses Pin 3 to Pin 12 of the 14-pin footprint so that Pin 1 is unused. See Figure 77 for the location of Pin 1, the square pin on the PCB footprint. Only one pin connection (Pin 1 in this example) is required for the modification shown in Figure 77. It is recommended to use prefabricated header jumpers that can be cut in half. Solder one half to the PCB and connect the other half to the EVAL-ADAU1452REVBZ board. This way, users can remove the USBi when needed without desoldering a wire.

Figure 79 shows the single pin connector that allows the CLATCH connection to the USBi to be removed. See the Modifying the EVAL-ADAU1452REVBZ section for more information.

Figure 77. Jumper Wires Soldered to EVAL-ADUSB2EBZ J1 Pin 1 and Pin 2

MODIFYING THE EVAL-ADAU1452REVBZ

Perform the following steps to modify the EVAL-ADAU1452REVBZ board and see Figure 78 for a graphical representation of all modifications:

1. Remove the R6, R9, R10, and R11 resistors.
2. Add a single square header pin onto the AD1938_/CLATCH test point located near R11.
3. Solder a jumper wire from the AD1938_CCLK test point near R10 to the SCLK test point located near Pin 10 of J1.
4. Solder a jumper wire from the AD1938_COUT test point near R9 to the MISO test point near U5.
5. Solder a jumper wire from the AD1938_CDATA test point near R6 over to the MOSI test point near J1.
6. Add a 10 kΩ pull-up resistor on the AD1938_/CLATCH signal line test point. The $\overline{\text{CLATCH}}$ signal must be pulled up to the D3V3 power supply. This power supply is located to the left of the C20 capacitor.

It is best practice to run and glue the jumper wires to the bottom of the PCB so that the wires run close to the ground plane of the PCB for optimal signal integrity.

Figure 79 shows the four resistors (R6, R9, R10, and R11) removed and placed on one of the pads for future use. Figure 79 also shows the 10 kΩ resistor connected between the pin soldered at the AD1938_/CLATCH test point, and the D3V3 voltage located to the left of the C20 capacitor. See the ADAU1452 data sheet for more information about the pins.

Figure 80 shows the three jumper wires attached to the bottom of the PCB. The blue wire is the AD1938_CDATA connection, the yellow wire is the AD1938_COUT connection, and the red wire is the AD1938_CCLK connection.

Figure 81 shows the EVAL-ADAU1452REVBZ board with all completed modifications and the EVAL-ADUSB2EBZ board attached and ready for use.

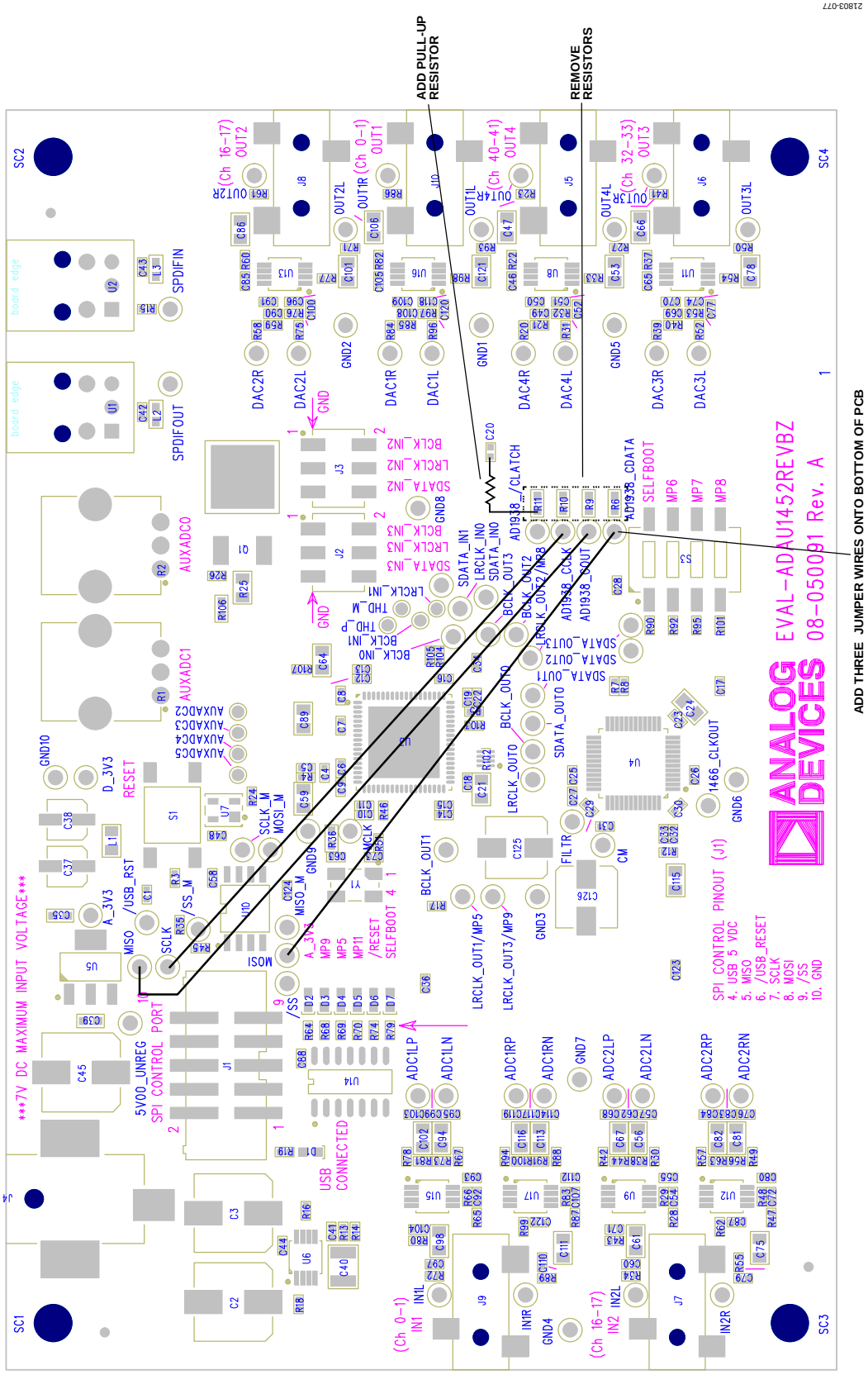


Figure 78. Codec Control Modification Overview

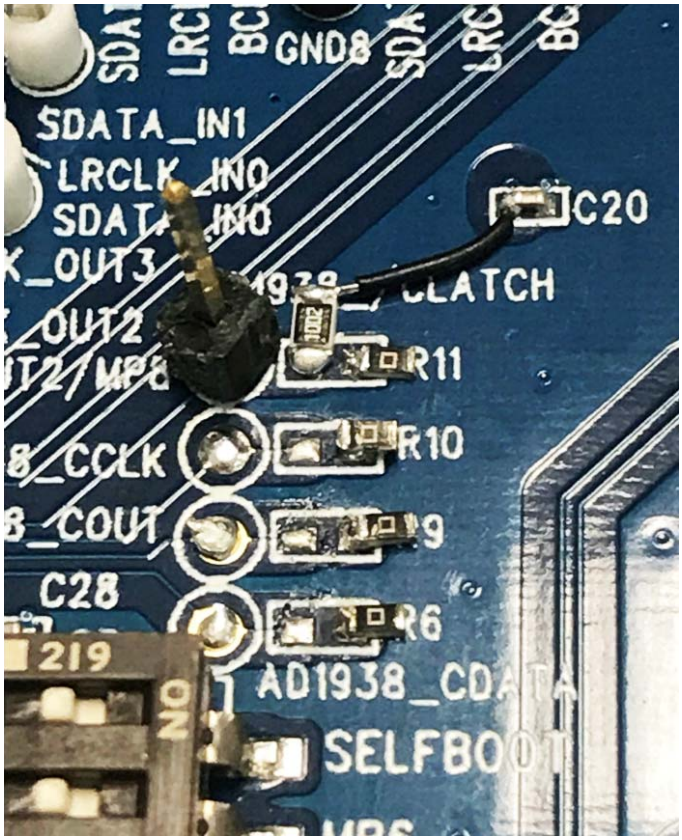


Figure 79. Resistor Modifications and AD1938_/CLATCH Connection

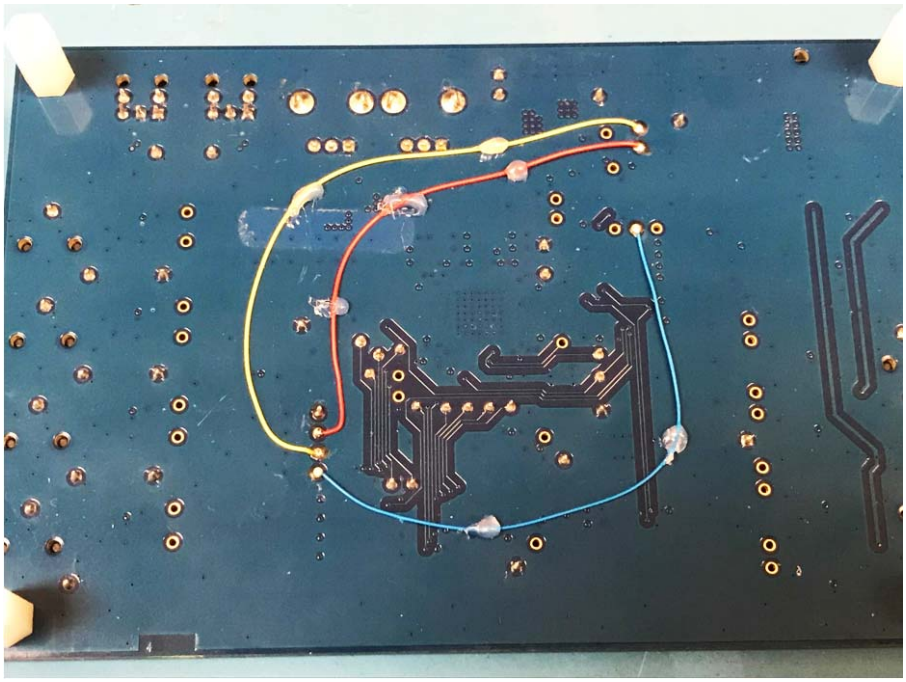
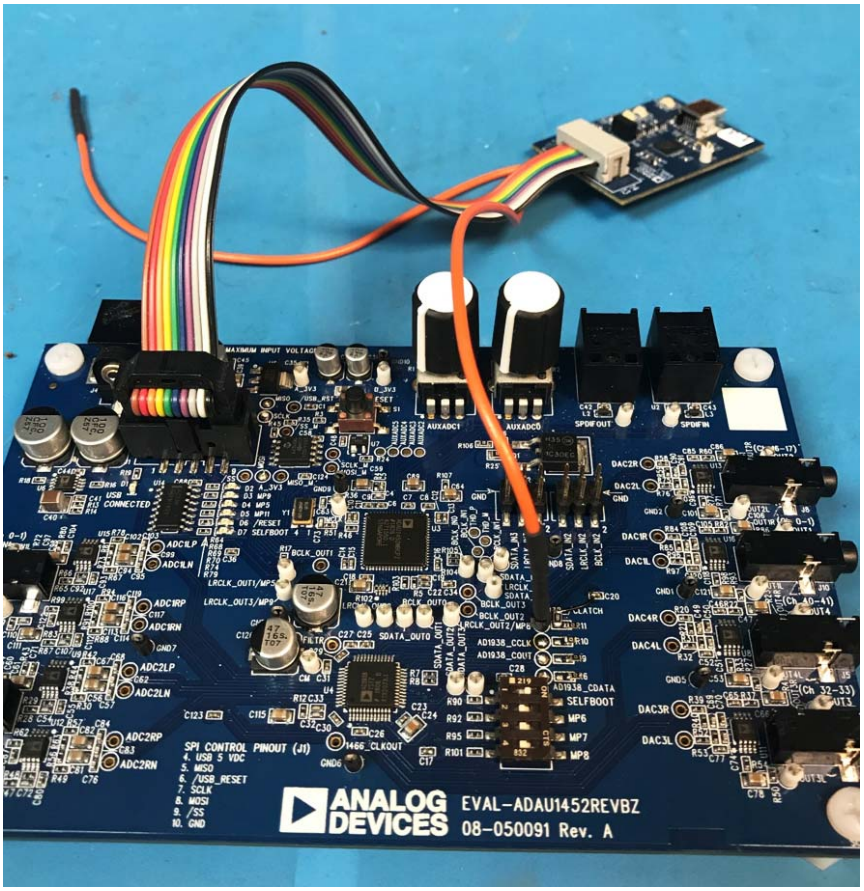


Figure 80. Jumper Wires Soldered on Bottom of the PCB.



21803-080

Figure 81. Completed Modification with EVAL-ADUSB2EBZ (USBi) Connected.

USING THE MODIFIED EVAL-ADAU1452REVBZ BOARD AND USBi

Figure 82 shows the required setup to control the DSP and codec using SigmaStudio. Drag the **AD193x** block to the **Hardware Configuration** tab from the **Tree ToolBox**. The SPI latch (**SPI 0x2 ADR0**) on the **USB Interface** block must be changed from the default **SPI 0x1 ADR0** to **SPI 0x2 ADR0** so that the AD1938 codec uses the second SPI latch output of the USBi. Clicking the register control tabs of either device allows real-time changes of register settings.

After the user sets the registers as desired for the codec, the **Get Current Setting from Chip** button (see Figure 83) can be used to read the registers to the **Capture** window (see Figure 84) to be copied and exported. Use the following procedure to read the registers to the **Capture** window:

1. Clear the **Capture** window with the red X on the upper left of the window.
2. In the **IC 1 - AD193x Register Controls** tab, click the **Get Current Setting from Chip** button (see Figure 83). Clicking this button performs a register dump of all current codec settings and the register settings are then displayed in the **Capture** window and register control window.
3. Click the first element in the list shown in Figure 84, press the **Shift** key, and then click the last element in the list to highlight all elements.
4. Hover over the list and right-click it to open the pull-down menu with the options **Save as Text…** or **Save as Raw Data** (see Figure 85). The second option gives the user several more options to either save the data to import into a microcontroller or to save the list as an **.XML** file for the DSP to use to boot the codec. To allow the DSP to boot the codec, move the codec SPI connections to the master communications port. This information is not described in this user guide. Contact SigmaDSP@analog.com for more information.

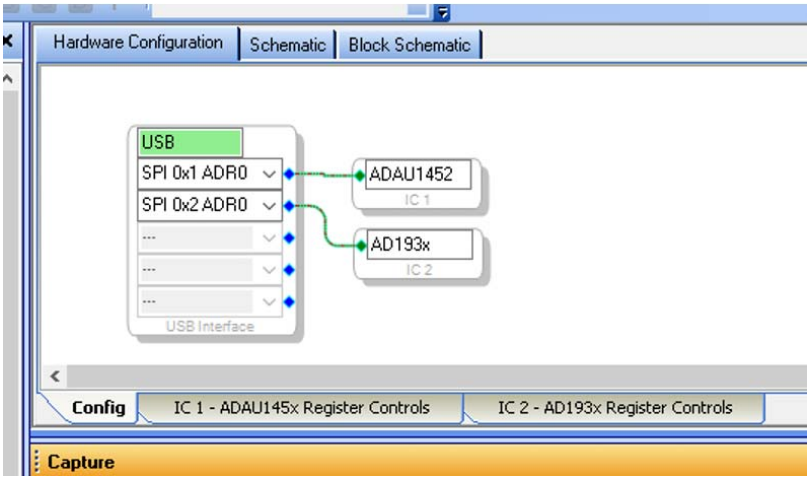


Figure 82. SigmaStudio Configuration to Control the DSP and the Codec

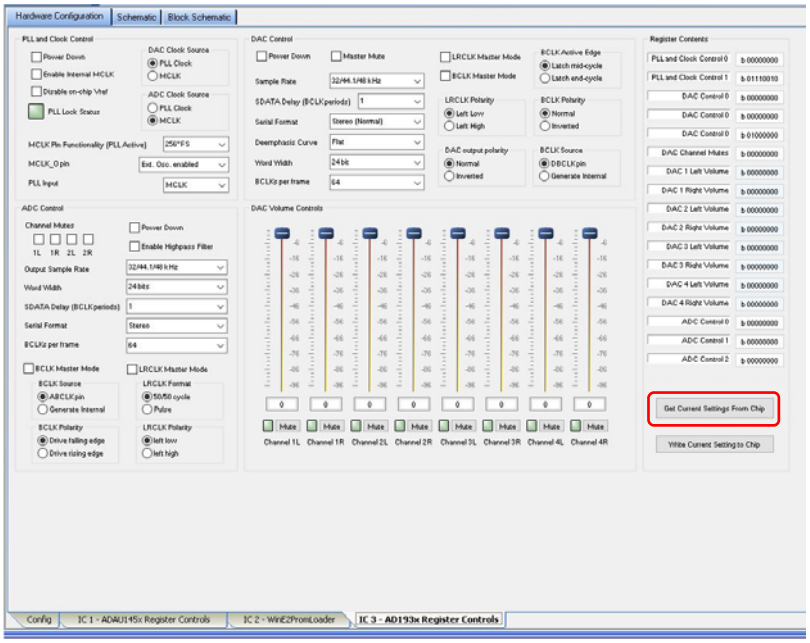


Figure 83. SigmaStudio Downloading the Current Codec Settings, Register Dump

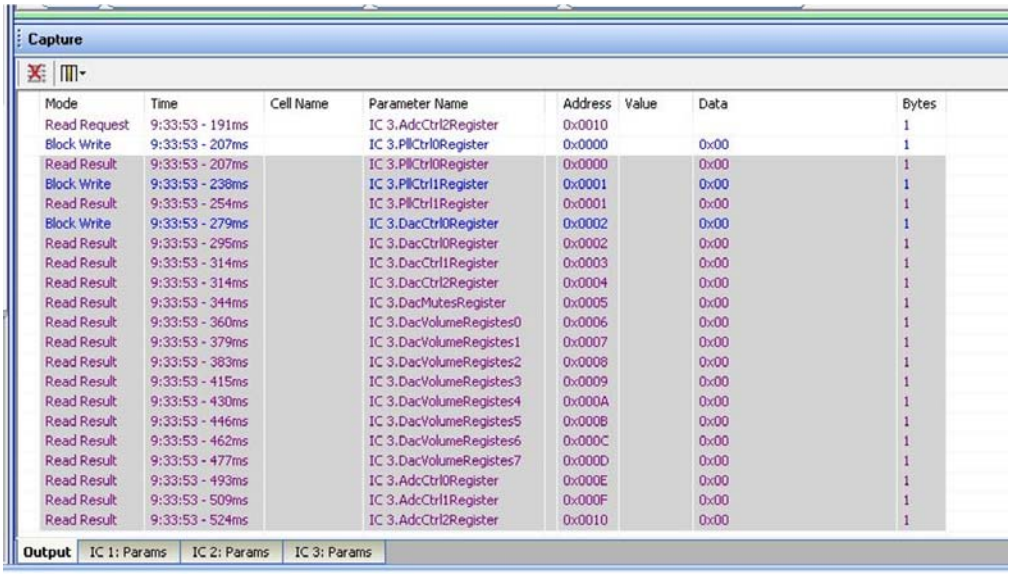


*Figure 84. SigmaStudio **Capture** Window Codec Register Dump*

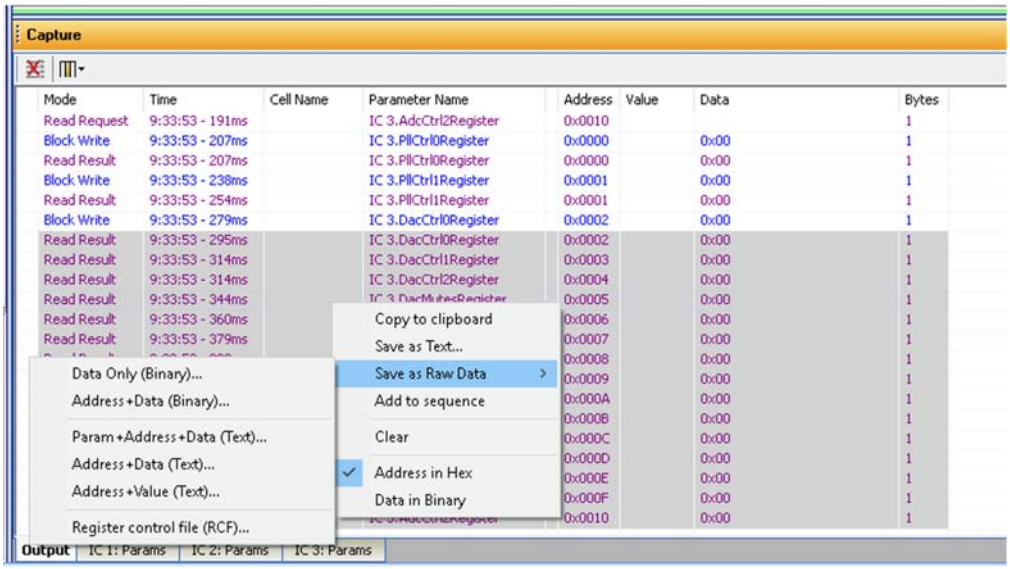


*Figure 85. SigmaStudio **Capture** Window Save Options*

HARDWARE DESCRIPTIONS

ICs

Table 5. IC Descriptions

Reference	Functional Name	Description
U1	Everlight PLT133/T8 optical transmitter	S/PDIF optical (TOSLINK) output.
U2	Everlight PLT133/T10W optical receiver	S/PDIF optical (TOSLINK) input.
U3	ADAU1452 SigmaDSP audio processor	Acts as an audio hub for all audio inputs and outputs in the system and performs digital signal processing on those input and output signals.
U4	AD1938 audio codec	Converts analog audio inputs to digital data for the ADAU1452 processor and takes the digital data back from the ADAU1452 to convert to analog audio outputs signals.
U5	ADP3338AKCZ-3.3-RL or ADP3338AKCZ-3.3RL7 LDO voltage regulator	Accepts the unregulated dc supply voltage between 5 V and 7 V that is provided on Connector J4 and regulates the supply voltage down to 3.3 V.
U7	ADM811TARTZ reset supervisor	Generates a master reset signal for the ADAU1452 and the AD1938 if the **RESET** push-button (S1) is pressed, or if SigmaStudio sends a reset command via the USBi.
U10	Microchip 25AA1024 serial EEPROM	Stores data, allowing the ADAU1452 to perform a self boot operation.
U6, U8, U9, U11, U12, U13, U15, U16, U17	ADA4841-2 dual, low power, low noise, and low distortion rail-to-rail output amplifier	Implements the analog audio filtering required for the stereo line inputs and outputs.
U14	74ACT04SC hexadecimal inverter	Buffers logic signals and drives status LEDs.

STATUS LEDS

Table 6. LED Descriptions

Reference	Functional Name	Description
D1	USB connected	Illuminates when the USBi is recognized by Windows after the USBi is connected to Control Port J1 and the USB 2.0 port of the computer.
D2	3.3 V supply status LED	Illuminates when the output of the ADP3338AKCZ-3.3-RL or ADP3338AKCZ-3.3RL7 LDO voltage regulator reaches a level sufficient to exceed the V_{IH} logic high input level of the 74ACT04SC inverter. When this LED is illuminated, it does not guarantee that the LDO output is 3.3 V. It only shows that the LDO output is ~2 V or greater. To perform more detailed measurements of the LDO output level, check the voltage on the A_3V3 test point, TP1.
D3	MP9 general-purpose LED	Illuminates when the status of the ADAU1452 LRCLK_OUT3/MP9 pin is set to logic high by the ADAU1452.
D4	MP5 general-purpose LED	Illuminates when the status of the ADAU1452 LRCLK_OUT1/MP5 pin is set to logic high by the ADAU1452.
D5	MP11 general-purpose LED	Illuminates when the status of the ADAU1452 LRCLK_IN1/MP11 pin is set to logic high by the ADAU1452.
D6	Master reset status LED	Illuminates when the master reset signal generated by the ADM811TARTZ reset supervisor IC is logic low, which puts the ADAU1452 and AD1938 in hardware reset. LED D3 does not illuminate when the master reset signal is logic high and the ADAU1452 and AD1938 are out of reset.
D7	Self boot status LED	Illuminates when the self boot switch (Position 1 of Switch S3) is set to the on position, signifying that a self boot operation is executed on the rising edge of the ADAU1452 $\overline{\text{RESET}}$ signal, or when ADAU1452 is powered up. LED D2 does not illuminate when the self boot slide switch (S2) is set to the disabled position, which signifies that no self boot operation is to occur.

SWITCH AND PUSH-BUTTON DESCIPTIONS

Table 7. Switch and Push-Button Descriptions

Reference	Functional Name	Description
S1	**RESET** push-button	When this switch is pressed and released, a reset signal is generated and causes the ADM811TARTZ reset supervisor to generate a master reset signal for the ADAU1452 and AD1938.
S3	Self boot, MP6, MP7, and MP8 switches	When in the on position, Position 1 of Switch S3 asserts the SELFBOOT pin of the ADAU1452. When in the on position, Position 2 of Switch S3, Position 3 of Switch S3, and Position 4 of Switch S3 tie the MP6, MP7, and MP8 pins high, respectively. When in the off position, these switches pull the MP6, MP7, and MP8 pins low.

EVALUATION BOARD SCHEMATICS AND ARTWORK

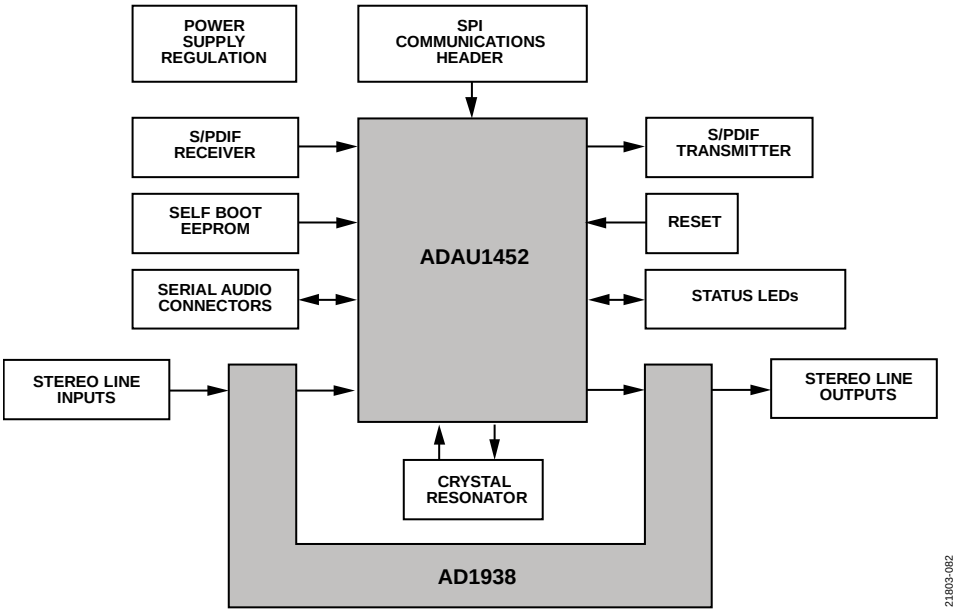


Figure 86. Functional Block Diagram

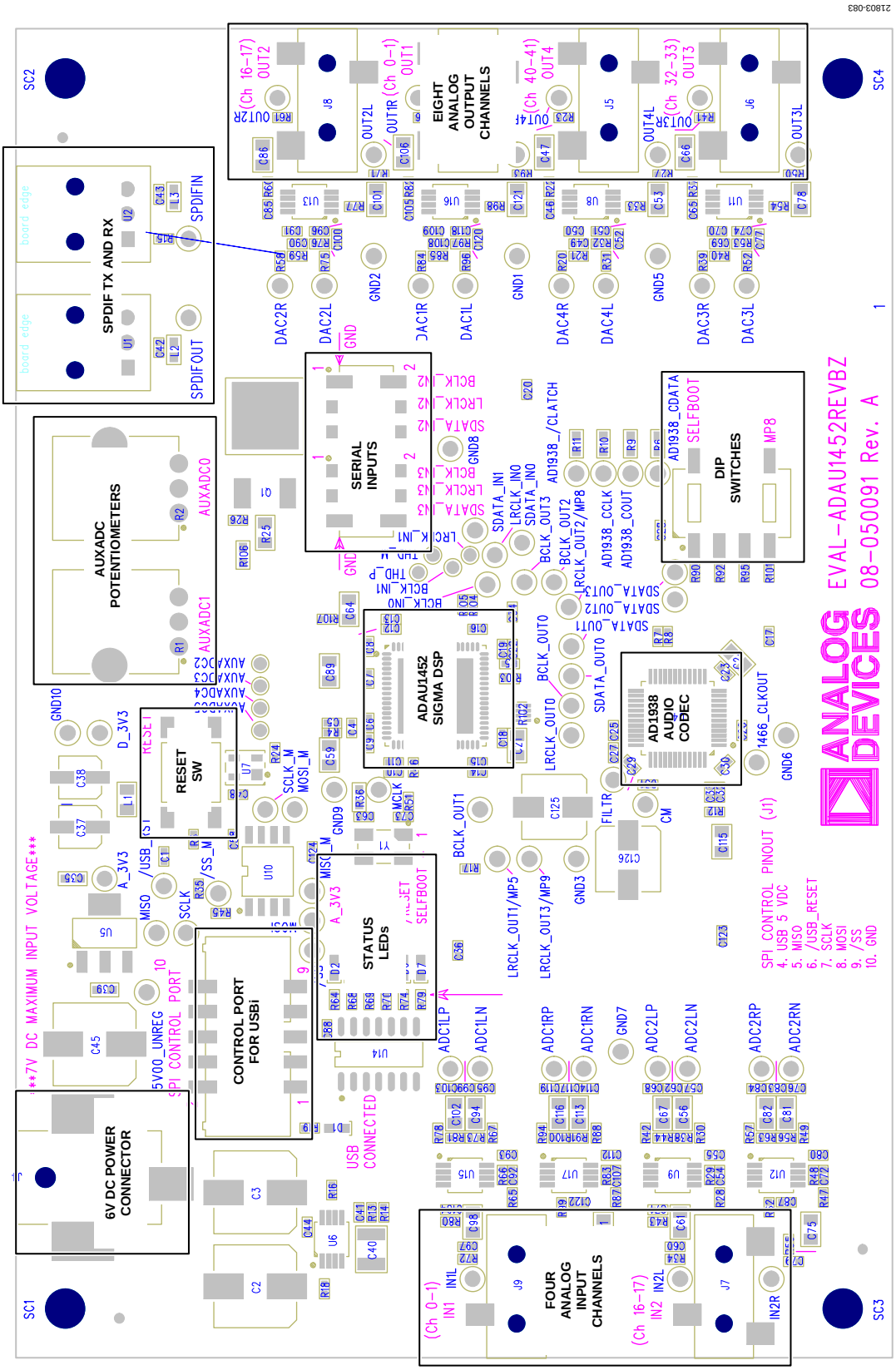


Figure 87. EVAL-ADAU1452REVBZ Evaluation Board Layout Block Diagram

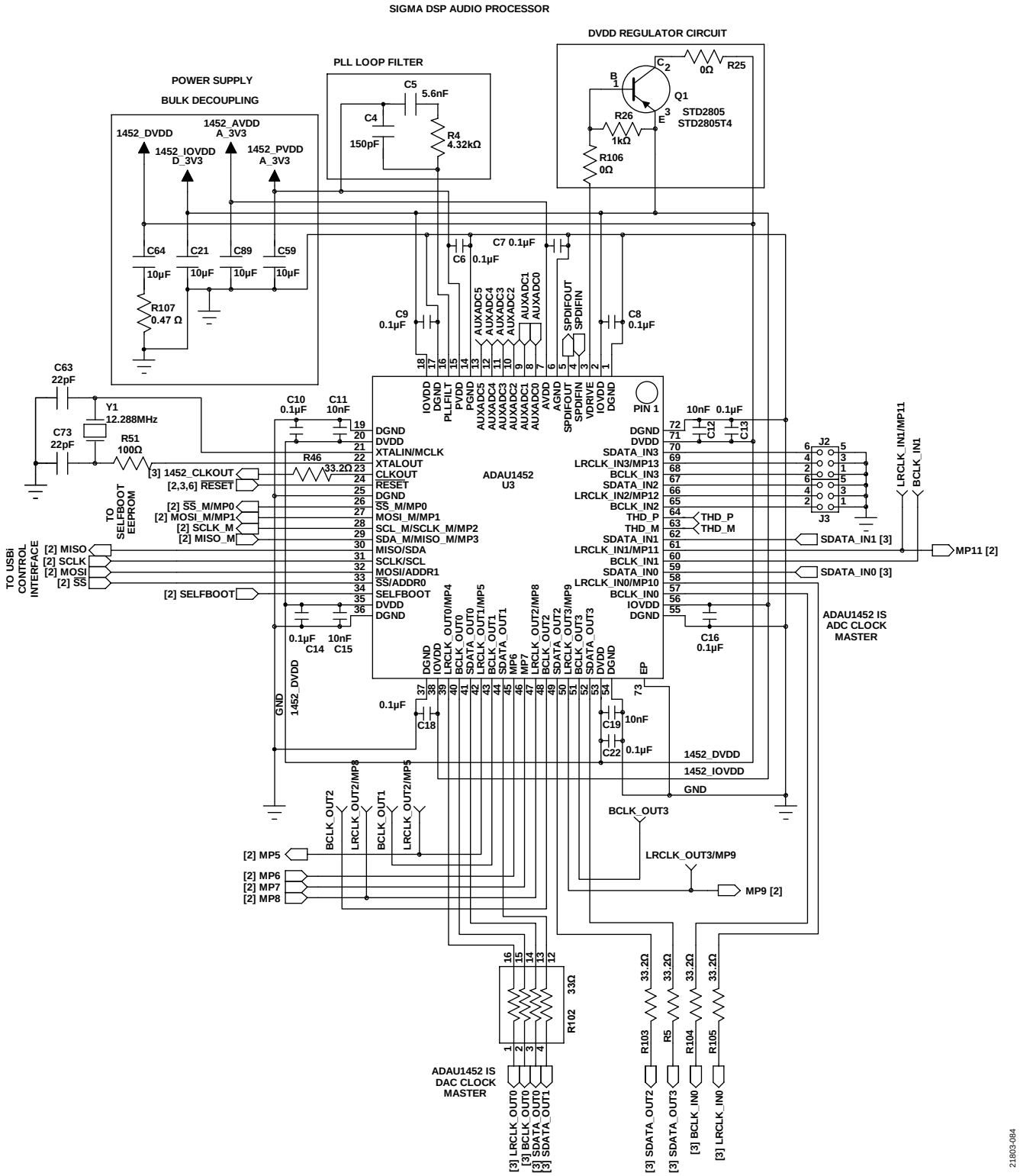


Figure 88. SigmaDSP Audio Processor Schematic

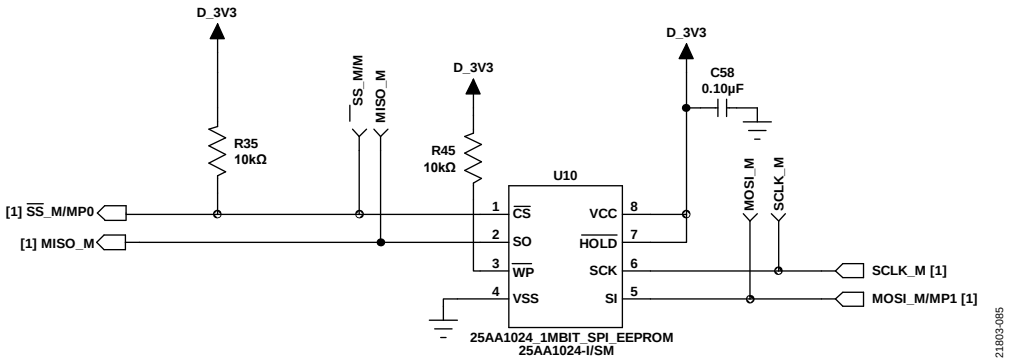


Figure 89. Self Boot Circuit Schematic

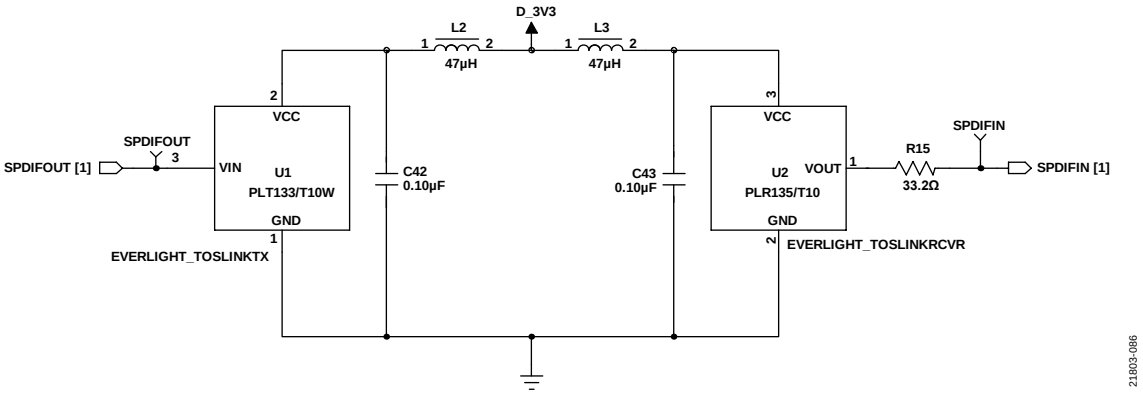


Figure 90. S/PDIF Optical Interfaces Schematic

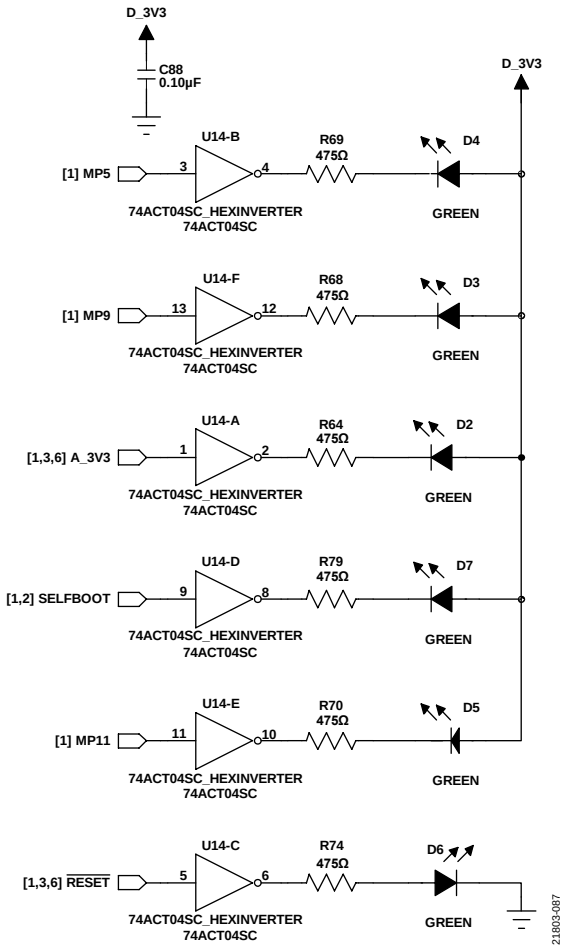


Figure 91. Status LEDs Schematic

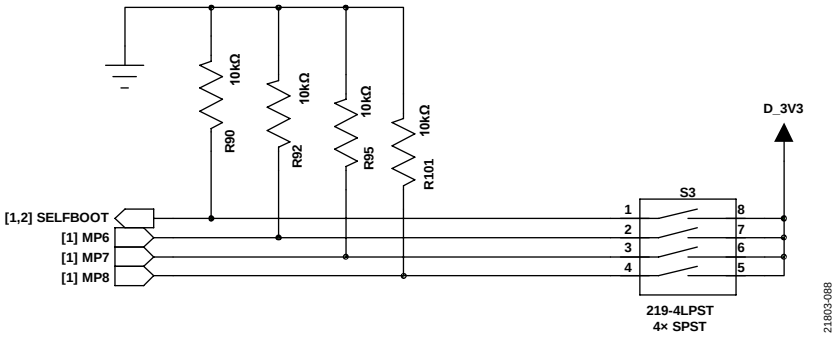


Figure 92. DIP Switch Schematic

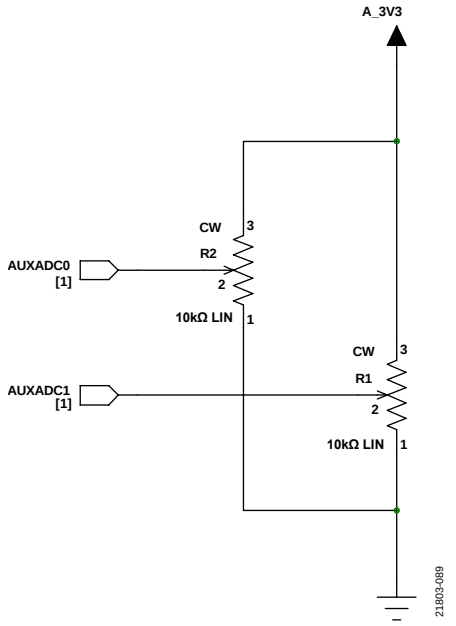


Figure 93. AUXADC Potentiometer Schematic

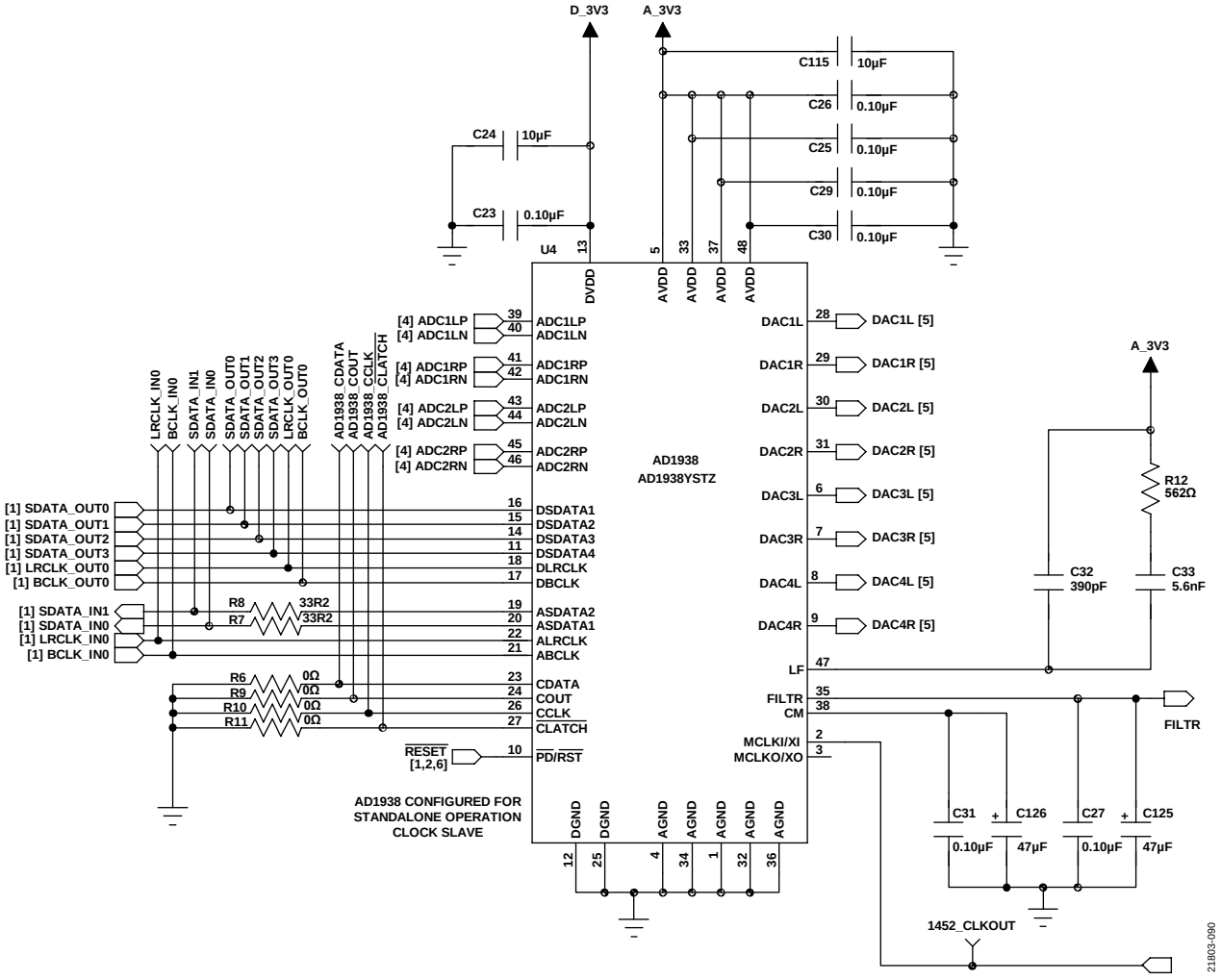


Figure 94. AD1938 Audio Codec Schematic

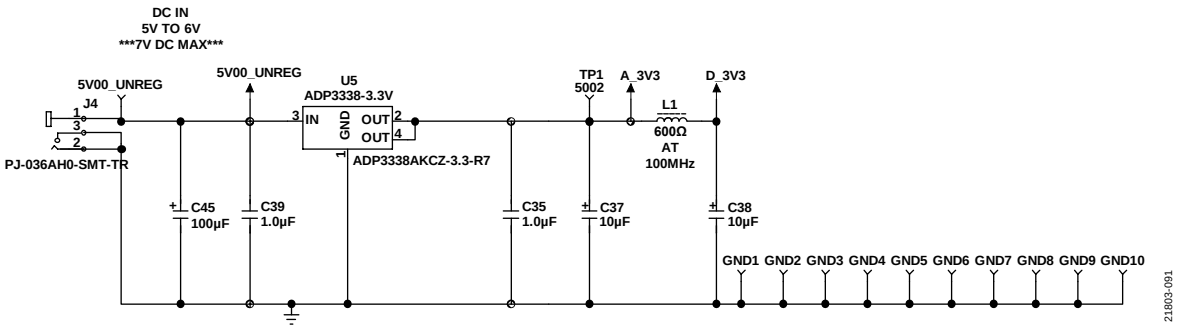


Figure 95. Power Supply Schematic

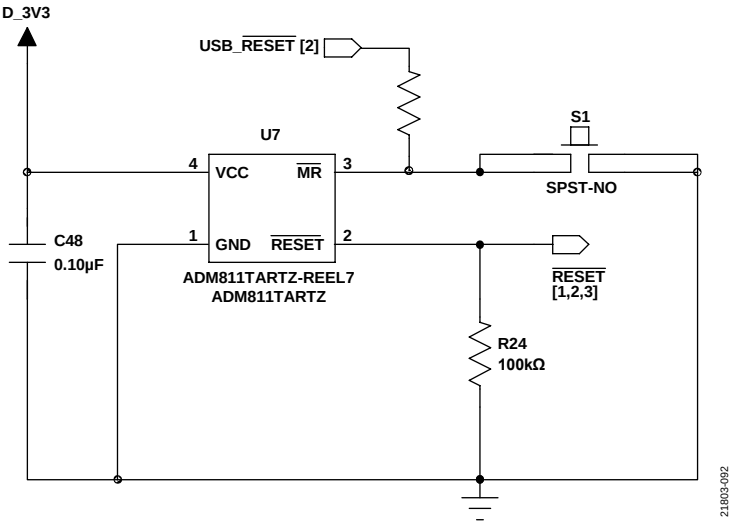


Figure 96. Reset Generator Circuit Schematic

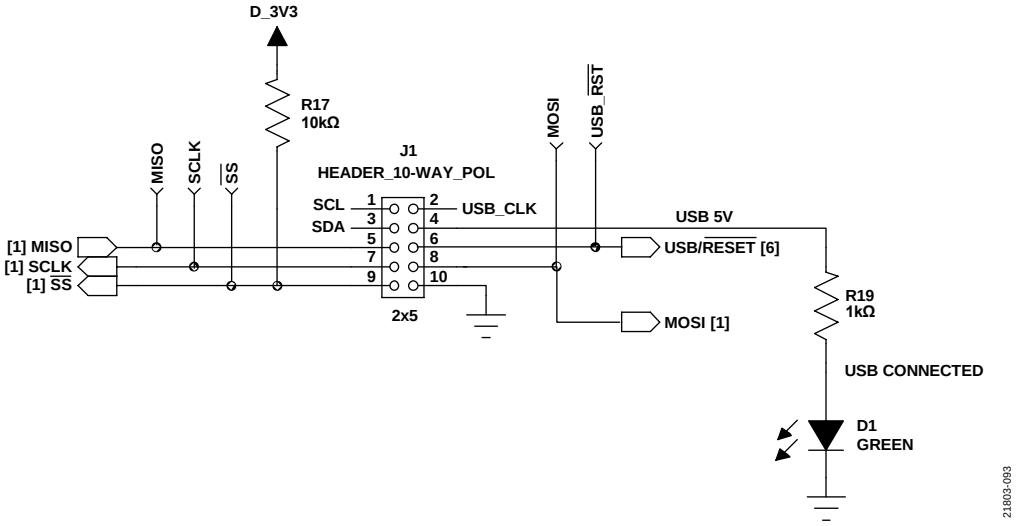


Figure 97. SPI Communication Interface Header Schematic

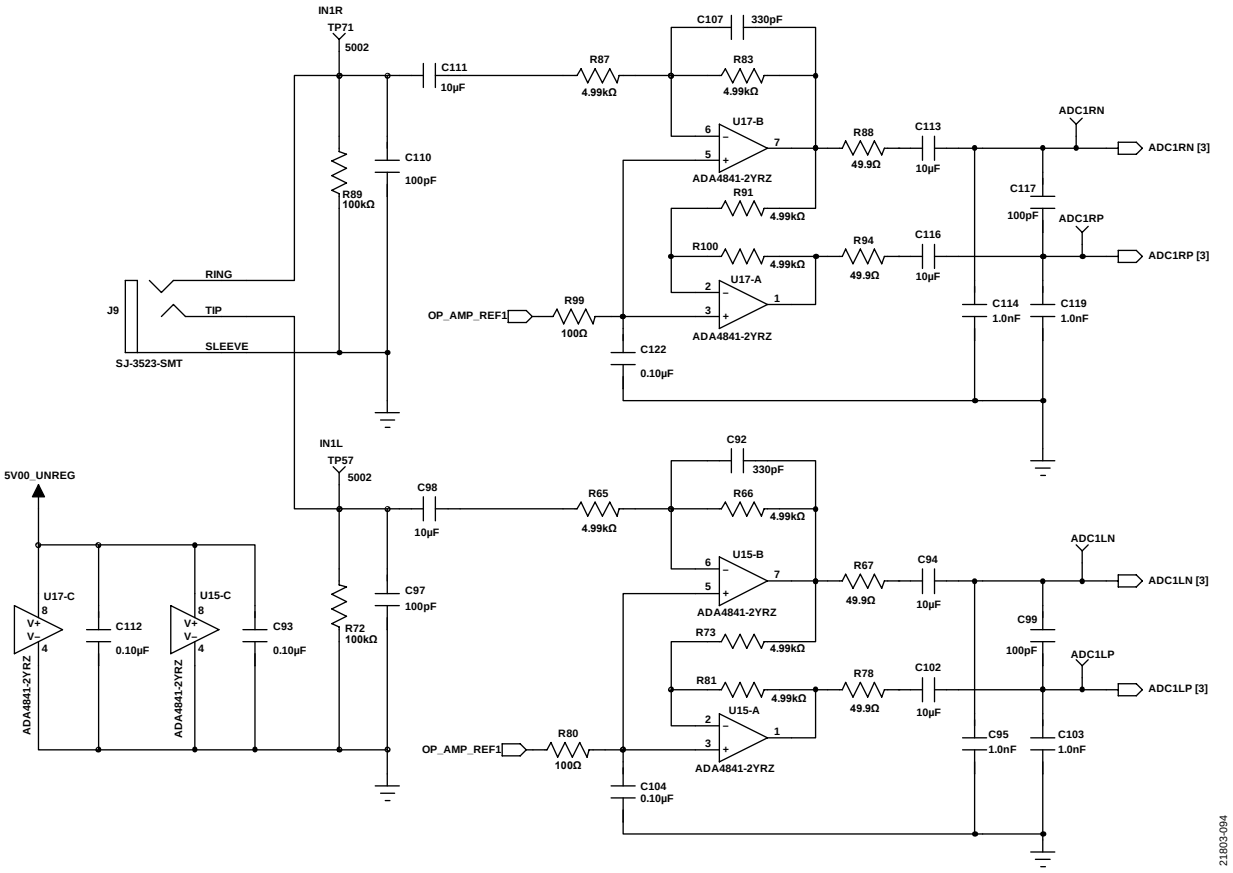


Figure 98. Analog Input Channel 0 and Channel 1 Schematic

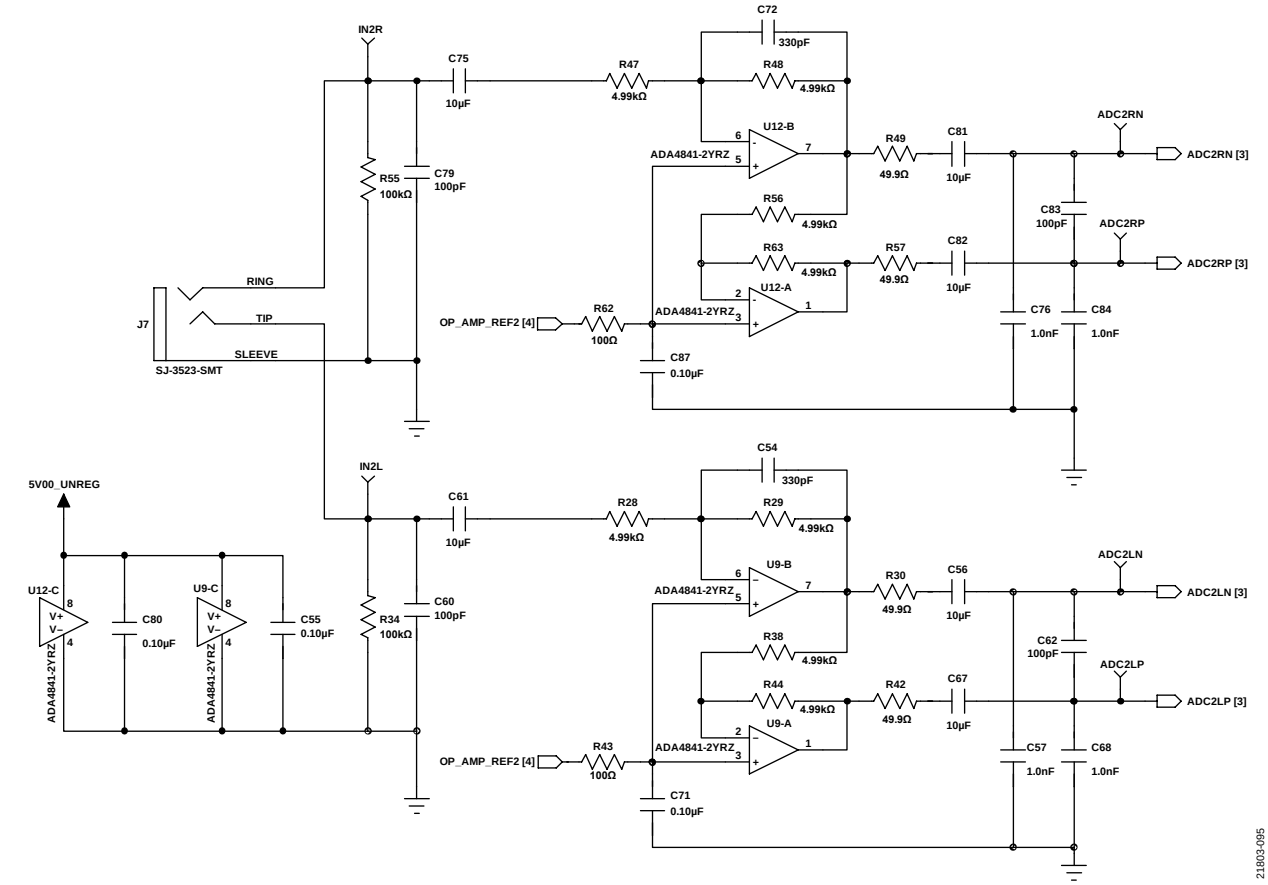


Figure 99. Analog Input Channel 16 and Channel 17 Schematic

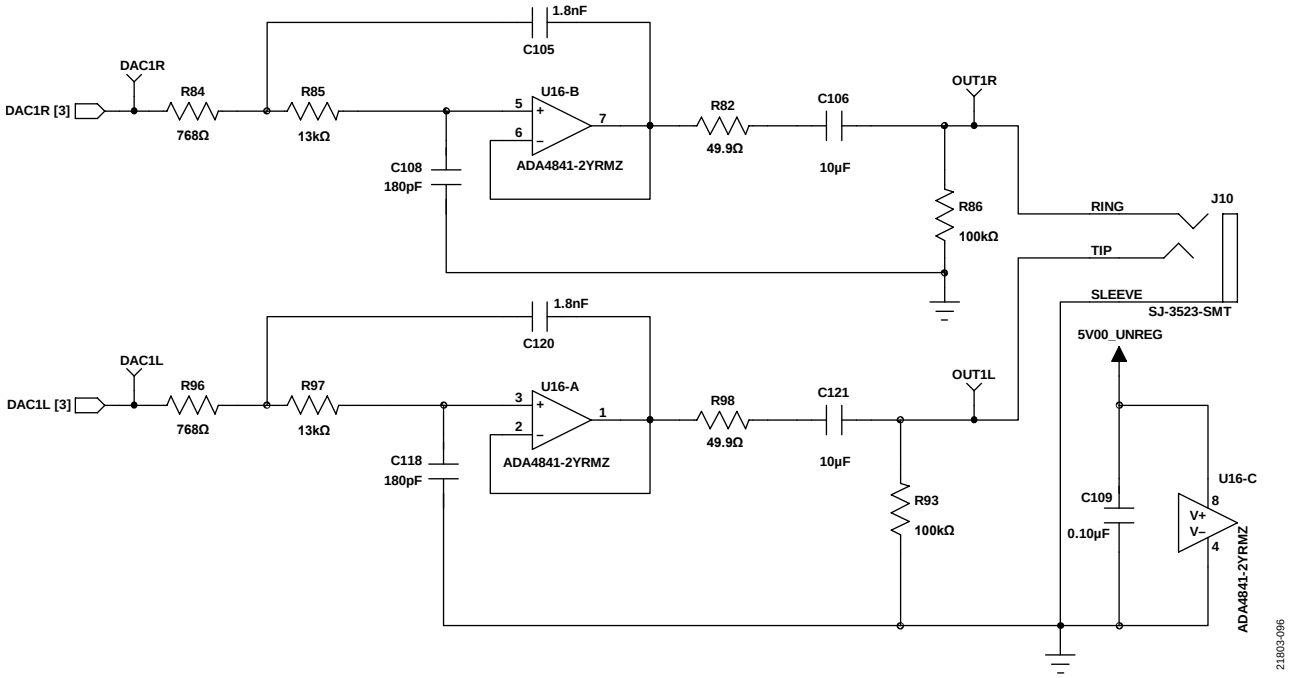


Figure 100. Analog Output Channel 0 and Channel 1 Schematic

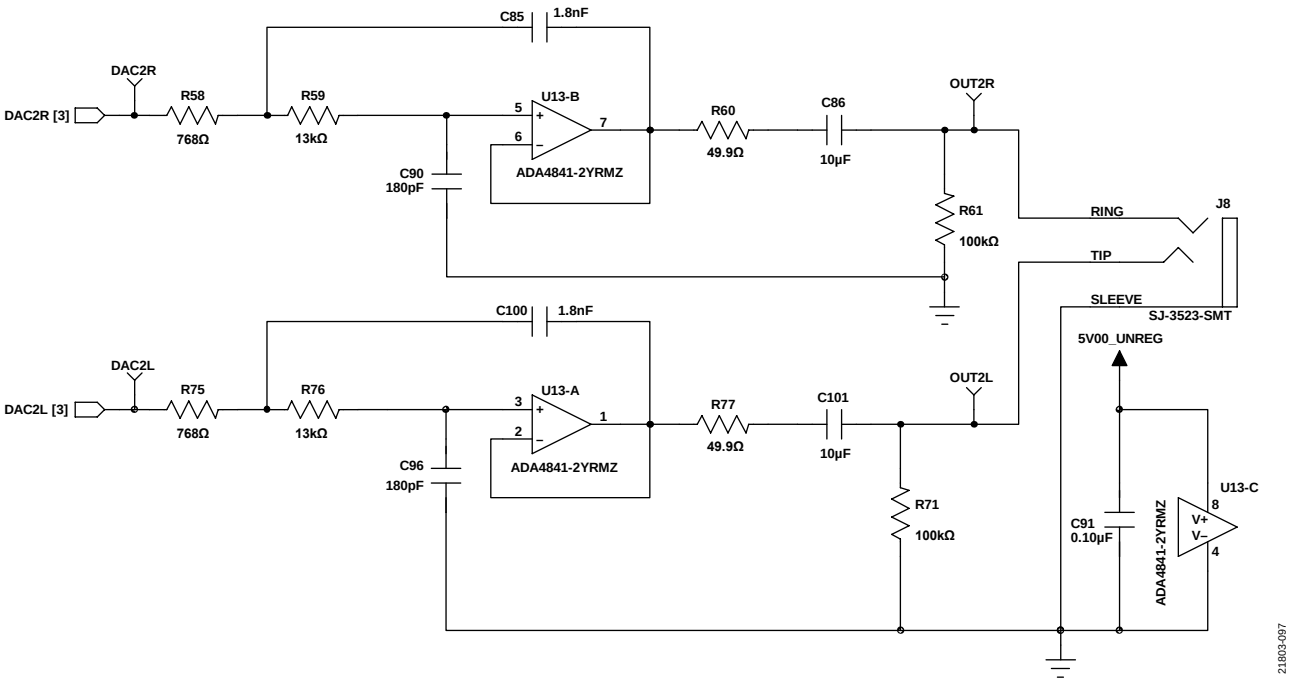


Figure 101. Analog Output Channel 16 and Channel 17 Schematic

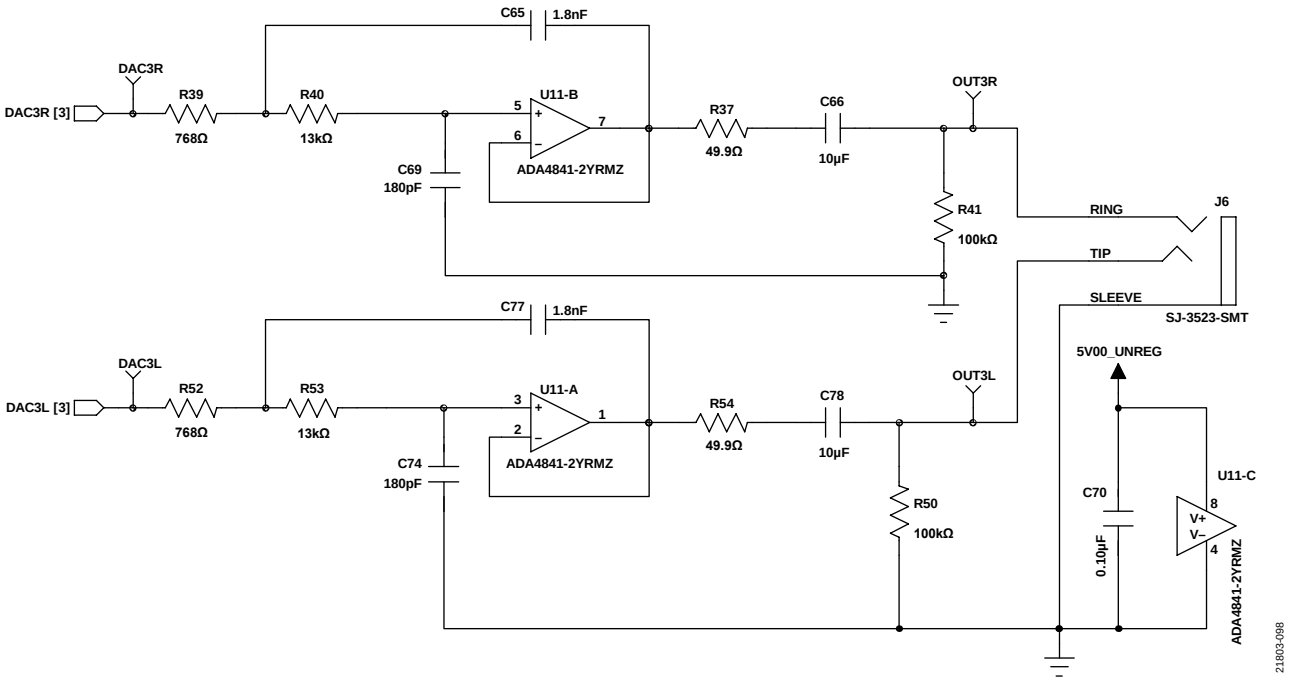


Figure 102. Analog Output Channel 32 and Channel 33 Schematic

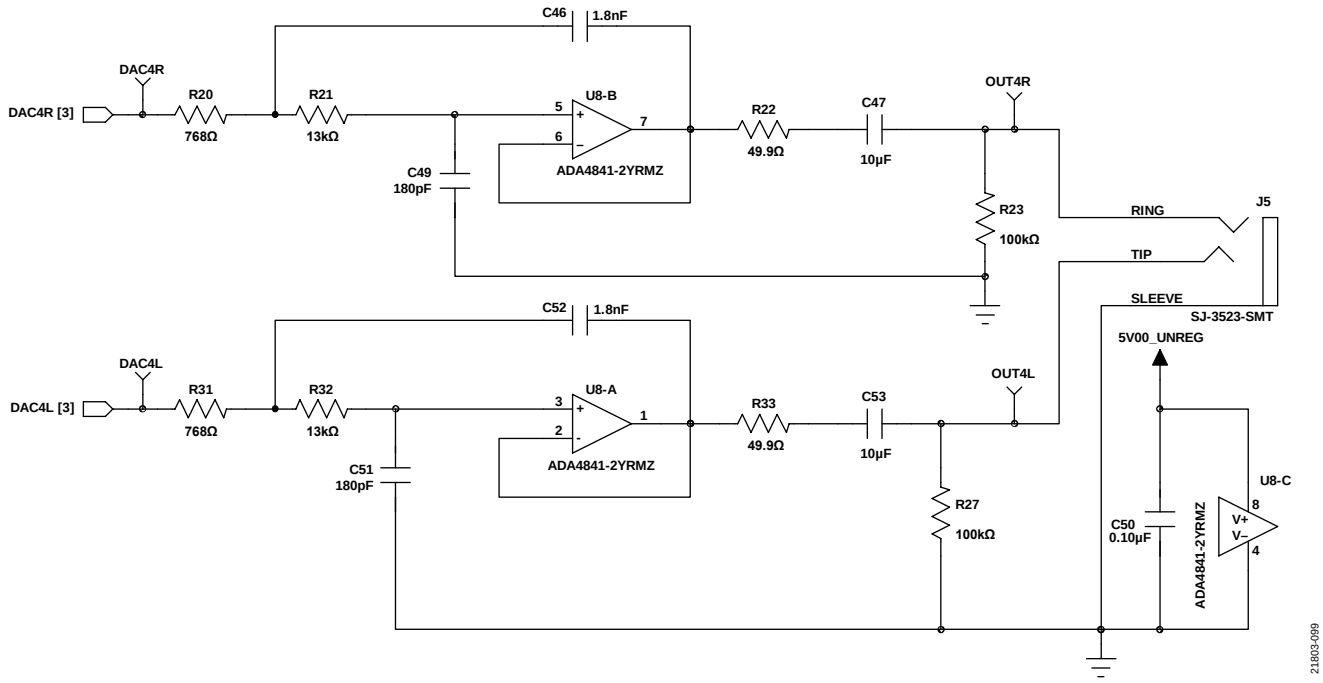


Figure 103. Analog Output Channel 40 and Channel 41 Schematic

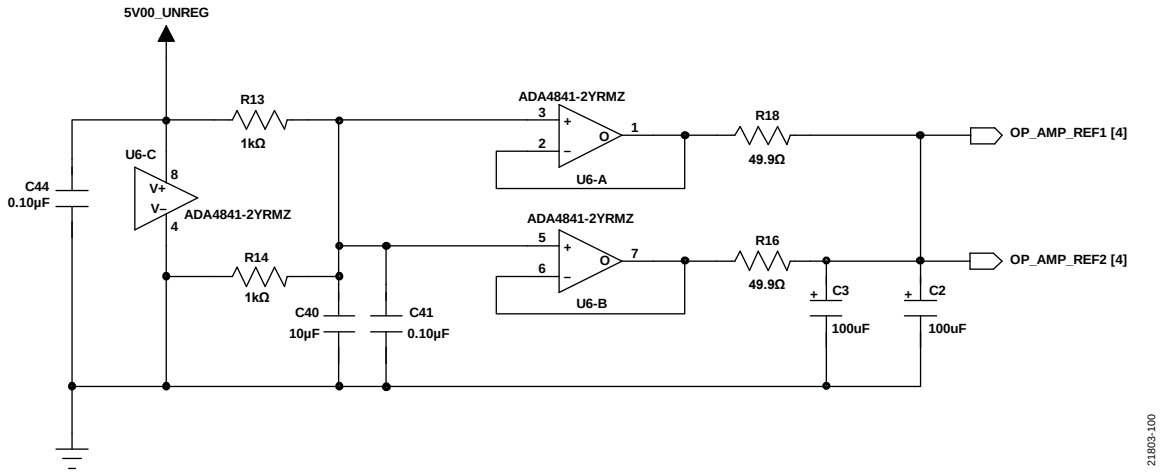


Figure 104. ADC Op Amp Reference Voltage Schematic

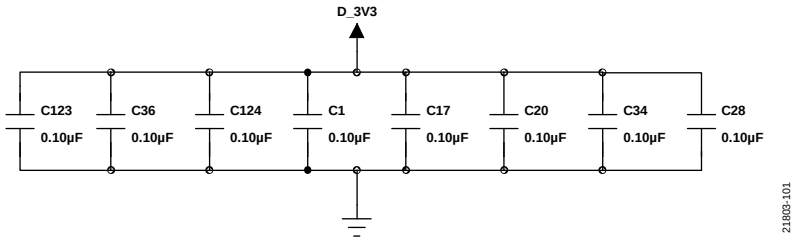


Figure 105. Plane Decoupling Capacitors Schematic

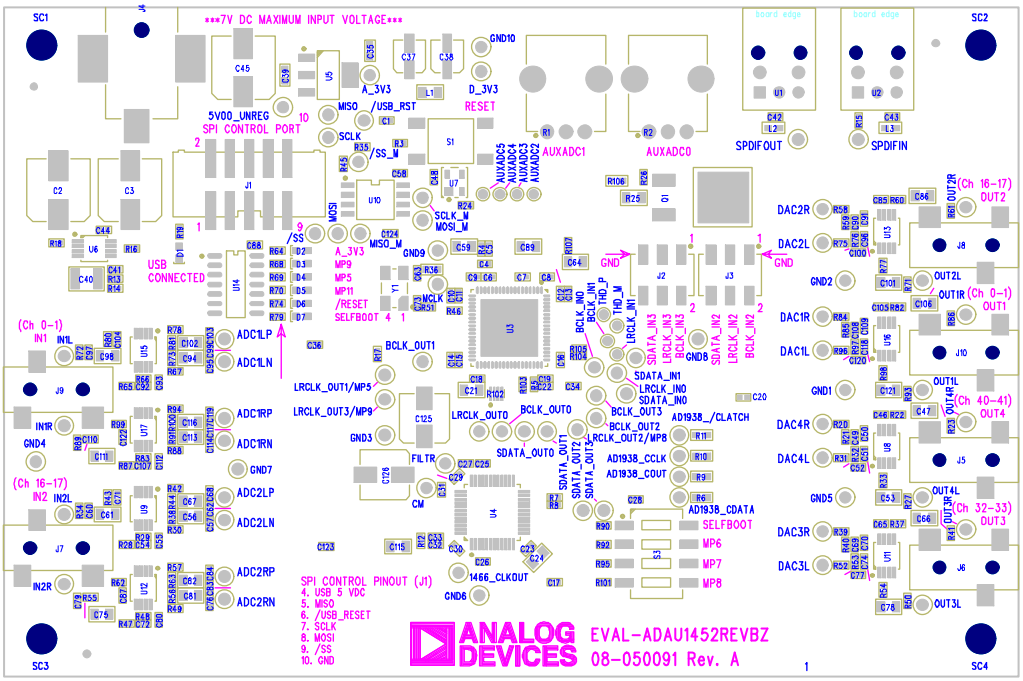


Figure 106. EVAL-ADAU1452REVBZ Layout, Top Assembly

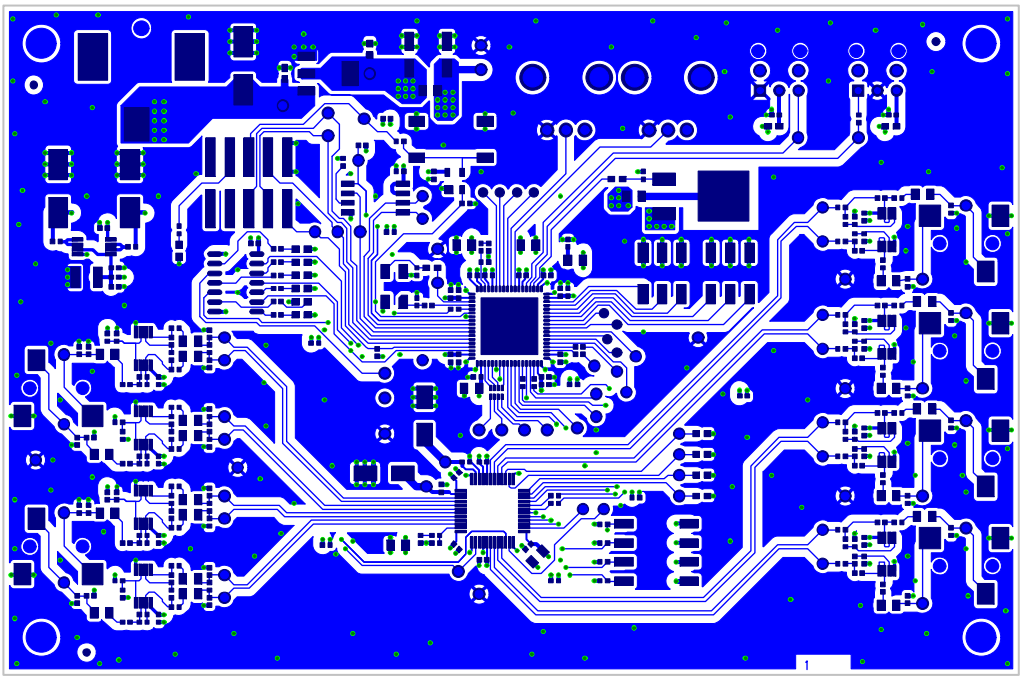


Figure 107. EVAL-ADAU1452REVBZ Layout, Top Copper

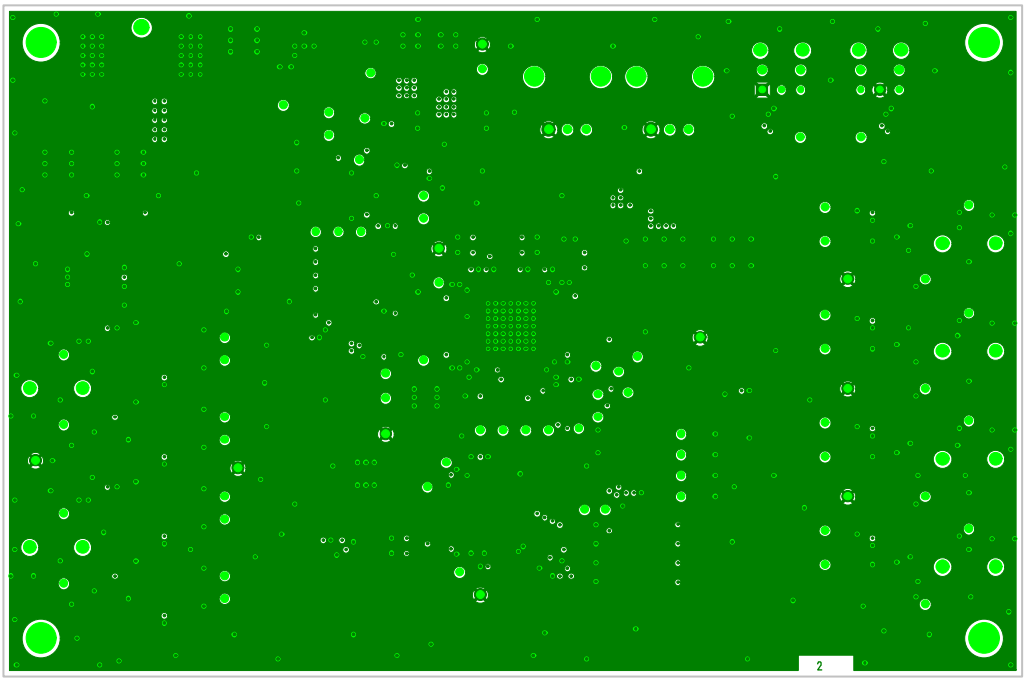


Figure 108. EVAL-ADAU1452REVBZ Layout, Ground Plane

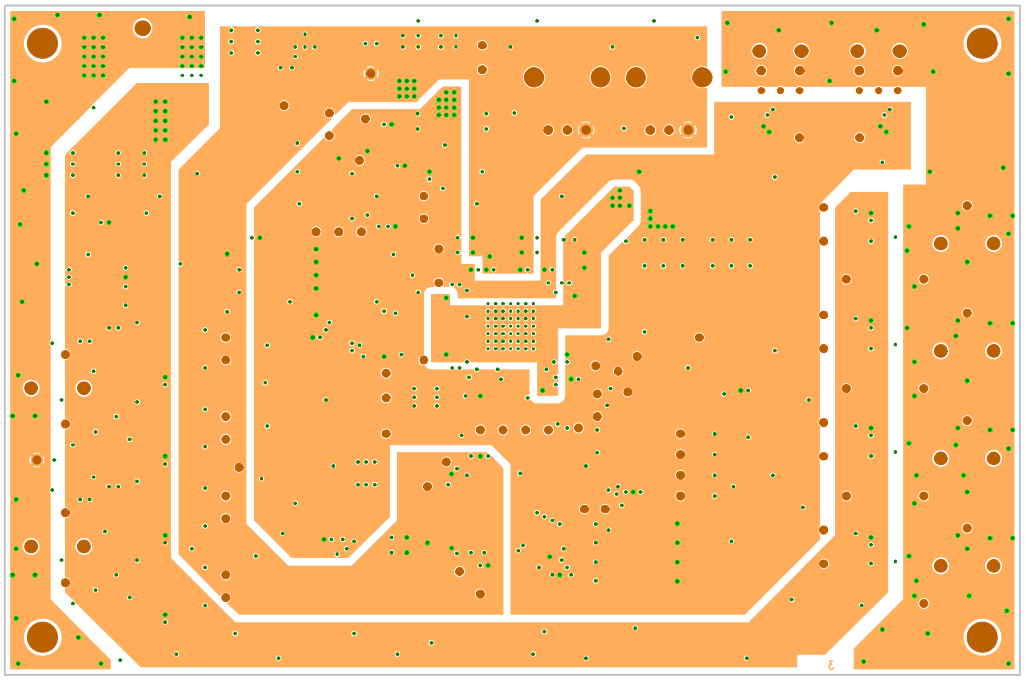


Figure 109. EVAL-ADAU1452REVBZ Layout, Power Plane

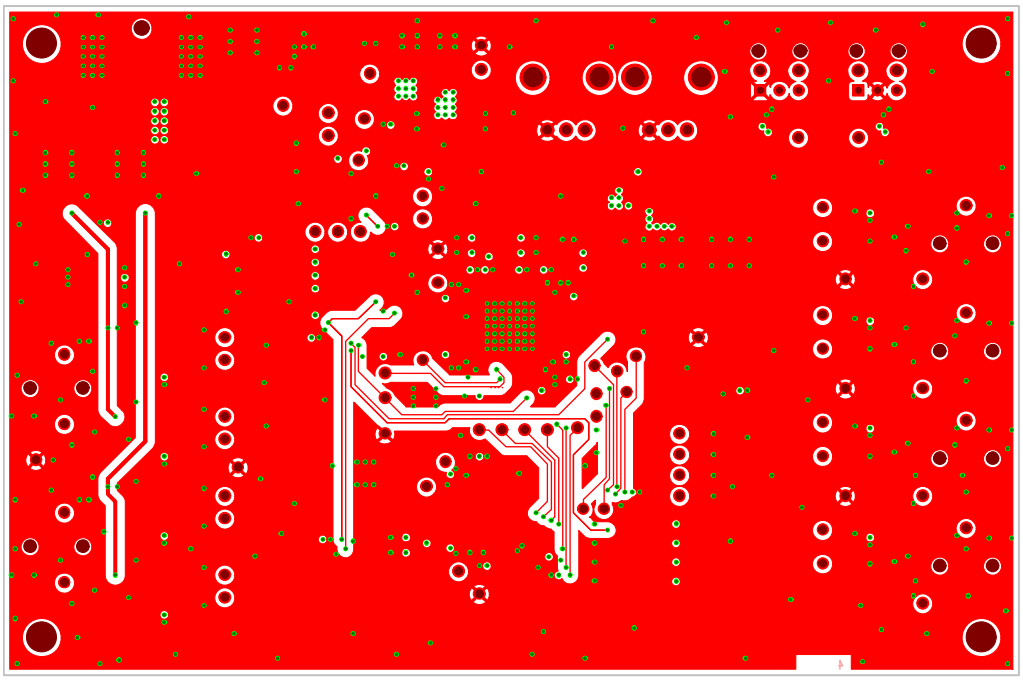


Figure 110. EVAL-ADAU1452REVBZ Layout, Bottom Copper

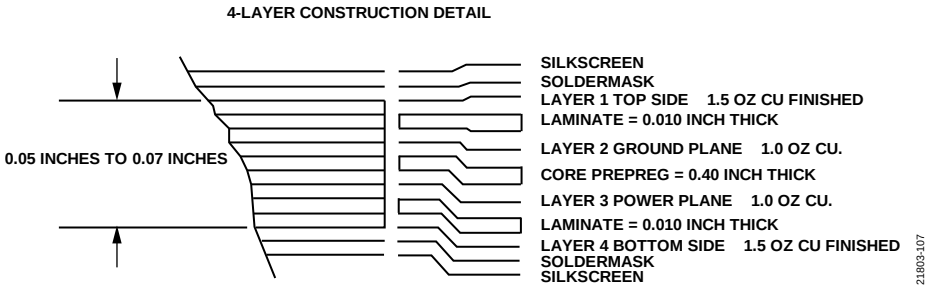


Figure 111. Cross Section of PCB Stack Up

ORDERING INFORMATION

BILL OF MATERIALS

Table 8.

Qty.	Value[1]	Reference Designator	Description	Manufacturer	Part Number
44	0.10 µF	C1, C6 to C10, C13, C14, C16 to C18, C20, C22, C23, C25 to C31, C34, C36, C41 to C44, C48, C50, C55, C58, C70, C71, C80, C87, C88, C91, C93, C104, C109, C112, C122 to C124	Multilayer ceramic capacitors, 16 V, X7R, 0402	Murata	GRM155R71C104KA88D
4	10 nF	C11, C12, C15, C19	Multilayer ceramic capacitors, 25 V, X7R, 0402	Murata	GRM155R71E103JA01J
2	47 µF	C125, C126	Aluminum electrolytic capacitors, 105°C, SMD_D	Panasonic	EEE-FC1C470P
26	10 µF	C21, C24, C47, C53, C56, C59, C61, C64, C66, C67, C75, C78, C81, C82, C86, C89, C94, C98, C101, C102, C106, C111, C113, C115, C116, C121	Multilayer ceramic capacitors, 10 V, X7R, 0805	Murata	GRM21BR71A106KE51L
3	100 µF	C2, C3, C45	Aluminum, electrolytic capacitors, 105°C, SMD_E	Panasonic	EEE-FC1C101P
1	390 pF	C32	Multilayer ceramic capacitor, 50 V, NP0, 0402	Murata	GRM1555C1H391JA01D
2	1.0 µF	C35, C39	Multilayer ceramic capacitors, 16 V, X7R, 0603	Murata	GRM188R71C105KA12D
2	10 µF	C37, C38	Aluminum electrolytic capacitors, 105°C, SMD_B	Panasonic	EEE-FC1C100R
1	150 pF	C4	Multilayer ceramic capacitor, 50 V, NP0, 0402	Murata	GRM1555C1H151JA01D
1	10 µF	C40	Multilayer ceramic capacitor, 25 V, X7R, 1210	Murata	GCM32ER71E106KA57L
8	1.8 nF	C46, C52, C65, C77, C85, C100, C105, C120	Multilayer ceramic capacitors, 25 V, NP0, 0402	Kemet	C0402C182J3GACTU
8	180 pF	C49, C51, C69, C74, C90, C96, C108, C118	Multilayer ceramic capacitors, 50 V, NP0, 0402	Murata	GRM1555C1H181GA01D
2	5.6 nF	C5, C33	Multilayer ceramic capacitors, 25 V, NP0, 0402	Murata	GRM155R71E562KA01D
4	330 pF	C54, C72, C92, C107	Multilayer ceramic capacitors, 50 V, NP0, 0402	Murata	GRM1555C1H331JA01D
8	1.0 nF	C57, C68, C76, C84, C95, C103, C114, C119	Multilayer ceramic capacitors, 50 V, NP0, 0402	Murata	GRM1555C1H102JA01D
8	100 pF	C60, C62, C79, C83, C97, C99, C110, C117	Multilayer ceramic capacitors, 50 V, NP0, 0402	Murata	GRM1555C1H101JZ01D
2	22 pF	C63, C73	Multilayer ceramic capacitors, 50 V, NP0, 0402	Murata	GRM1555C1H220JZ01D
7	571 nm	D1 to D7	LEDs, green, 2 V, 3 mcd, 0603	Lite-On	LTST-C191KGKT
1	N/A	J1	Header, 2 × 5, 0.1 inch, shrouded, polarized	3M	N2510-6002RB
2	N/A	J2, J3	Headers, 2 × 3, 0.1 inch, unshrouded	3M	PBC06DAAN, or cut PBC36DAAN
1	N/A	J4	Jack, power connector, 2.0 mm ID, 5.5 mm, outside diameter, through hole, right angle	Switchcraft	RAPC722X
6	N/A	J5 to J10	Jacks, 3.5 mm headphone, stereo, right angle, SMD	CUI Inc.	SJ-3523-SMT
1	600 Ω	L1	Chip ferrite bead, at 100 MHz, 500 mA, 0805	Steward	HZ0805E601R-10
2	47 µH	L2, L3	Chip inductors, 140 mA, 3.25 Ω, 0603	Taiyo Yuden	CBMF1608T470K

Qty.	Value[1]	Reference Designator	Description	Manufacturer	Part Number
1	N/A	Q1	Transistor, BJT, PNP, 60 V, 5 A, TO-252AA	STMicroelectronics	STD2805T4
1	562 Ω	R12	Chip resistor, 1%, 63 mW, thick film, 0402	Stackpole	RMCF0402FT562R
2	10 kΩ	R1, R2	Potentiometers, linear taper, 9 mm, vertical	Panasonic	EVU-F2MFL3B14
5	1 kΩ	R3, R13, R14, R19, R26	Chip resistors, 1%, 63 mW, thick film, 0402	Yageo	RC0402FR-071KL
18	49.9 Ω	R16, R18, R22, R30, R33, R37, R42, R49, R54, R57, R60, R67, R77, R78, R82, R88, R94, R98	Chip resistors, 1%, 63 mW, thick film, 0402	Yageo	RC0402FR-0749R9L
7	10 kΩ	R17, R35, R45, R90, R92, R95, R101	Chip resistors, 1%, 100 mW, thick film, 0402	Panasonic	ERJ-2RKF1002X
8	768 Ω	R20, R31, R39, R52, R58, R75, R84, R96	Chip resistors, 1%, 63mW, thick film, 0402	Yageo	RC0402FR-07768RL
8	13 kΩ	R21, R32, R40, R53, R59, R76, R85, R97	Chip resistors, 1%, 63 mW, thick film, 0402	Yageo	RC0402FR-0713KL
13	100 kΩ	R23, R24, R27, R34, R41, R50, R55, R61, R71, R72, R86, R89, R93	Chip resistors, 1%, 100 mW, thick film, 0402	Panasonic	ERJ-2RKF1003X
1	0 Ω	R25	Jumper, 125 mW, 0805	Panasonic	ERJ-6GEY0R00V
16	4.99 kΩ	R28, R29, R38, R44, R47, R48, R56, R63, R65, R66, R73, R81, R83, R87, R91, R100	Chip resistors, 1%, 63 mW, thick film, 0402	Stackpole	RMCF0402FT4K99
1	4.32 kΩ	R4	Chip resistor, 1%, 100 mW, thick film, 0402	Panasonic	ERJ-2RKF4321X
5	100 Ω	R43, R51, R62, R80, R99	Chip resistors, 1%, 100 mW, thick film, 0402	Panasonic	ERJ-2RKF1000X
1	33 Ω	R102	Resistor network, 4-resistor, isolated, 5%, 63 mW	CTS	741X083330JP
6	0 Ω	R6, R9 to R11, R36, R106	Resistors, 125 mW, 0603	Panasonic	ERJ-3GEY0R00V
6	475 Ω	R64, R68 to R70, R74, R79	Chip resistors, 1%, 63 mW, thick film, 0402	Stackpole	RMCF0402FT475R
8	33.2 Ω	R5, R7, R8, R15, R46, R103 to R105	Chip resistors, 1%, 63 mW, thick film, 0402	Stackpole	RMCF0402FT33R2
1	0.50 Ω	R107	Chip resistor, 1%, 167 mW, thick film, 0402	Panasonic	ERJ-2BQFR47X
1	N/A	S1	Switch, top actuated, tactile, SPST normally open, 6 mm gull wing	Tyco/Alcoswitch	FSM6JSMA
1	N/A	S3	Switch, 4-section, SPST, surface-mount device (SMD)	CTS Corp	219-4LPST
68	N/A	TP1 to TP9, TP14 to TP25, TP30 to TP76	Test points, white	Keystone Electronics	5002
1	N/A	U1	Optical transmitter, 16 Mbps	Everlight	PLT133/T10W
1	N/A	U10	EEPROM, 128 kB × 8, 1.8 V to 5.5 V, SOIJ-8	Microchip	25AA1024-I/SM
1	N/A	U14	Inverter, 6-channel, SOIC-14	Fairchild Semi	74ACT04SC
1	N/A	U2	Optical receiver, 16 Mbps	Everlight	PLR135/T10
1	N/A	U3	SigmaDSP processor, 300 MHz	Analog Devices	ADAU1452WBCPZ
1	N/A	U4	Codec, 4-ADC, 8-DAC, 192 kHz, 24-bit	Analog Devices	AD1938YSTZ
1	N/A	U5	Voltage regulator, high accuracy, low dropout, 3.3 V dc	Analog Devices	ADP3338AKCZ-3.3-R7
9	N/A	U6, U8, U9, U11 to U13, U15 to U17	Op amp, dual, low power, low noise, low distortion, rail-to-rail, 8-lead SOIC	Analog Devices	ADA4841-2YRZ

Qty.	Value[1]	Reference Designator	Description	Manufacturer	Part Number
1	N/A	U7	Supervisor reset generator, 3.08 V, logic low output, 4-lead SOT-143	Analog Devices	ADM811TARTZ-REEL7
1	18 pF	Y1	Crystal, 12.288 MHz, SMD-4	Abracon Corp	ABM3B-12.288MHZ-10-1-U-T

[1] N/A means not applicable.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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