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Evaluating the ADAU1962/ADAU1966 High Performance, Low Power, Multibit Sigma-Delta DACs

PACKAGE CONTENTS

ADAU1962/ADAU1966 evaluation board
USBi control interface board
USB cable
D-sub 25-pin to (8) XLR male
12 V desktop supply

OTHER SUPPORTING DOCUMENTATION

ADAU1962 data sheet
ADAU1966 data sheet

EVALUATION BOARD OVERVIEW

This user guide details the design and setup of the evaluation board for the ADAU1962/ADAU1966. Because the ADAU1962 is a 12-channel device and the ADAU1966 is a 16-channel device, the DAC 13 through DAC 16 outputs do not function on the ADAU1962 evaluation board. The evaluation board must be connected to an external 12 V dc power supply and ground; the board draws approximately 150 mA.

On-board regulators derive 9 V, 5 V, and 3.3 V supplies for the ADAU1962/ADAU1966 and peripherals. The ADAU1962/ADAU1966 can be controlled through either an I²C or SPI interface. A small external interface board, EVAL-ADUSB2EBZ, also called an USBi, connects to a PC USB port and provides either I²C or SPI access to the evaluation board through a ribbon cable. A graphical user interface (GUI) program, the Automated Register Window Builder, is provided for easy programming of the chip in a Microsoft® Windows® PC environment. The evaluation board allows demonstration and performance testing of most ADAU1962/ADAU1966 features, including high performance digital-to-analog converter (DAC) operation.

The board has an S/PDIF receiver with RCA and optical connectors, as well as a discrete serial audio interface that is available on the Analog Devices, Inc. system development platform (SDP) interface. Analog outputs are accessible with two D-sub, 25-pin connectors using the professional audio standard. A single D-sub, 25-pin to XLR male cable is included with the board for connecting individual DAC channels to an audio system.

EVALUATION BOARD DIAGRAM

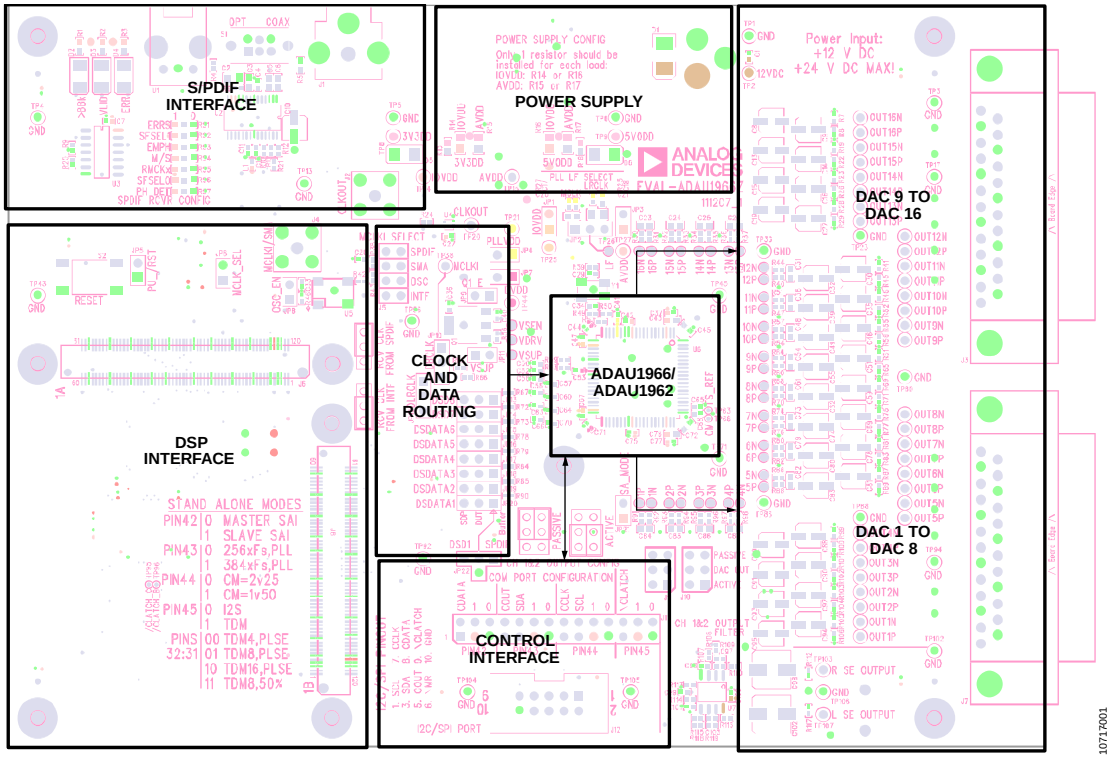

Figure 1.

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REVISION HISTORY

1/14—Rev. 0 to Rev. A

Added ADAU1962 ..... Universal
Changes to Evaluation Board Overview Section and Figure 1 .. 1

5/12—Revision 0: Initial Version

SETTING UP THE EVALUATION BOARD

STANDALONE MODE

The ADAU1962/ADAU1966 have a standalone mode that allows the user to choose between a limited number of operation modes without the need for a control interface. Applying a jumper across JP21, as shown in Figure 2, pulls SA_MODE (Pin 46) high, enabling the standalone mode in the ADAU1962/ADAU1966. The SA_MODE selections are listed in Table 1.

Table 1. Standalone Modes

Pin(s)	Jumper Setting	Description
42	0	Serial audio interface, master mode
	1	Serial audio interface, slave mode
43	0	MCLK select: 256 × f_S, PLL
	1	MCLK select: 384 × f_S, PLL
44	0	CM = 2.25 V (for AVDD = 5 V)
	1	CM = 1.50 V (for AVDD = 3.3 V)
45	0	Serial audio interface, I²S mode
	1	Serial audio interface, TDM mode
32:31	00	TDM4, pulse
	01	TDM8, pulse
	10	TDM16, pulse
	11	TDM8, 50% duty

On the ADAU1962/ADAU1966 evaluation board, each of the four ADAU1962/ADAU1966 control port pins is brought to a block of jumpers, allowing each pin to be assigned to either the I²C port or the SPI port. In standalone mode, these jumpers can connect the individual pins to high or low to put the ADAU1962/ADAU1966 in the desired mode.

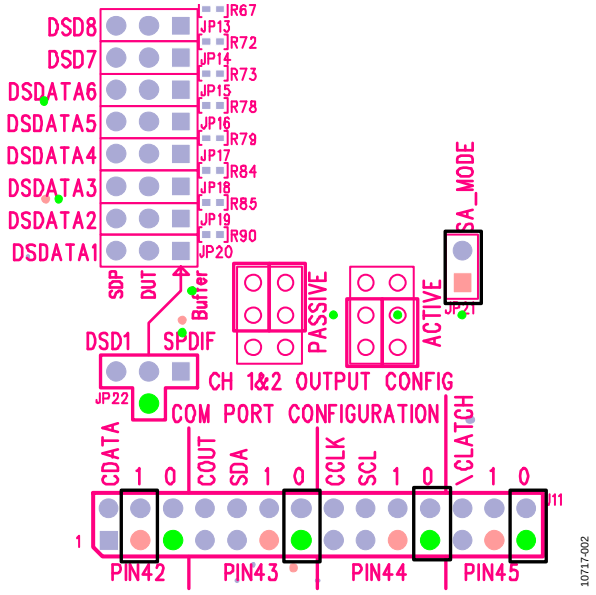

Figure 2. SA_MODE—Slave, 256 × f_S, CM = 2.25 V, I²S

The ADAU1962/ADAU1966 evaluation board arrives configured for S/PDIF input. The S/PDIF receiver operates as a clock master, putting out an I²S stream at 256 × f_S. For a quick startup, the ADAU1962/ADAU1966 are in standalone mode with the settings shown in Figure 2. Pin 42 is pulled high (1) and Pin 43 to Pin 45 are pulled low (0). According to Table 1, this puts the ADAU1962/ADAU1966 in slave mode, running at 256 × f_S, while common mode (CM) is set to 2.25 V and the audio serial port is in I²S mode. Notice in Figure 2 that the jumper for Pin 42 is assigned to 1 and that the other pins are assigned to 0.

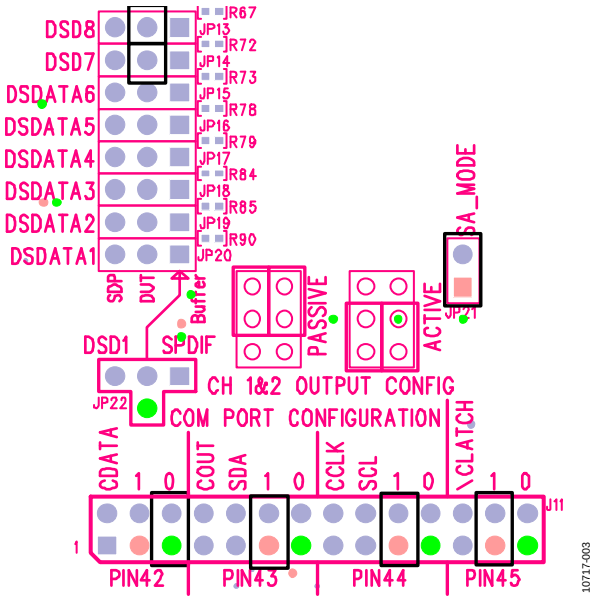

Figure 3. SA_MODE—Master, 384 × f_S, CM = 1.50 V, TDM

Figure 3 shows the other options for each SA_MODE configuration pin; master mode, running at 384 × f_S, CM set to 1.50 V, and the audio serial port in TDM mode. In the case where the ADAU1962/ADAU1966 are put in TDM mode, Pin 31 and Pin 32 can be pulled high or low to achieve the modes listed in Table 1. The correct pins are outlined in the top left corner of Figure 3, as DSD8 and DSD7.

I²C AND SPI CONTROL

The evaluation board can be configured for live control over the registers in the ADAU1962/ADAU1966. When the **Automated Register Window Builder** software is installed and the USBi control interface is plugged into the board, the software can control the ADAU1962/ADAU1966. For this configuration, the ADAU1962/ADAU1966 must be assigned to I²C mode using Address 00. See Figure 4 for the correct jumper positions.

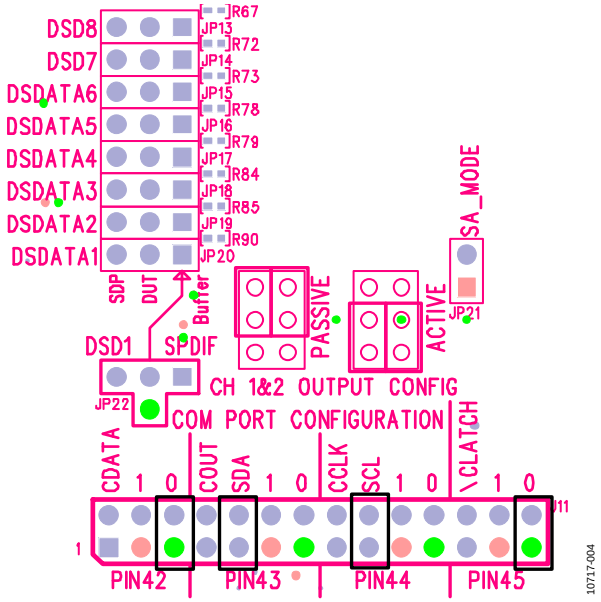

Figure 4. ADAU1962/ADAU1966 I²C Control, Address 00

The **Automated Register Window Builder** controls the ADAU1962/ADAU1966 and is available for download under the **Tools, Software, & Simulation Models** section of the ADAU1962 and ADAU1966 product pages.

In addition, the ADAU1962/ADAU1966 can be put into SPI mode for control by other means. See Figure 5 for the correct jumper positions.

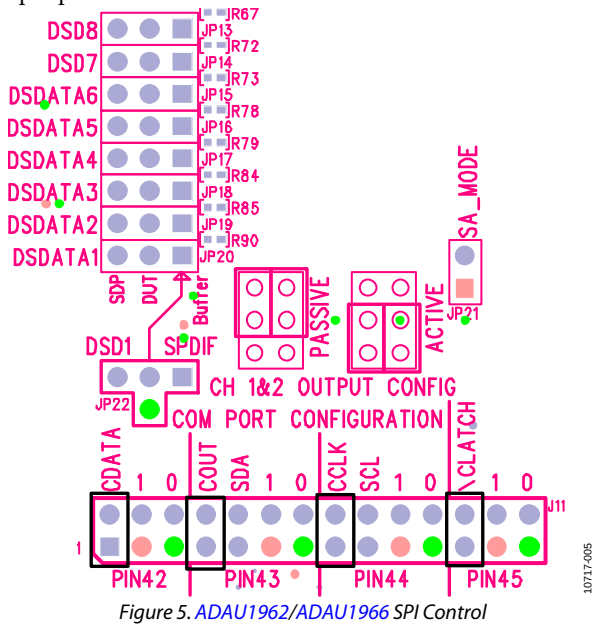

Figure 5. ADAU1962/ADAU1966 SPI Control

AUTOMATED REGISTER WINDOW BUILDER SOFTWARE INSTALLATION

The **Automated Register Window Builder** is a program that launches a graphical interface for direct, live control of the ADAU1962/ADAU1966 registers. The GUI content for a specific part is defined in a part-specific .xml file; these files are included in the software installation. To install the **Automated Register Window Builder** software, follow these steps:

1. Go to the ADAU1962 and ADAU1966 product pages and download the 64-Bit OS (ARWB_64BIT.zip) or 32-Bit OS (ARWB_32Bit.zip) file, which can be found under the **Tools, Software, & Simulation Models** section of the ADAU1962 and ADAU1966 product pages.
2. Open the downloaded.zip file and extract the files to an empty folder on your PC.
3. Install the **Automated Register Window Builder** by double-clicking **setup.exe** and following the prompts. A computer restart is not required.
4. Copy the .xml file for the ADAU1962/ADAU1966 from the extraction folder into the **C:\ProgramFiles\Analog Devices Inc\AutomatedRegWin** folder, if it is not already installed.

HARDWARE SETUP—USBi

To set up the USBi hardware, follow these steps:

1. Plug the USBi ribbon cable into J12, the I²C/SPI port.
2. Connect the USB cable to the PC and to the USBi.
3. When prompted for drivers, follow these steps:
   a. Choose **Install from a list or a specific location**.
   b. Choose **Search for the best driver in these locations**.
   c. Check the box for **Include this location in the search**.
   d. Find the USBi driver **C:\Program Files\Analog Devices Inc\AutomatedRegWin\USB drivers**.
   e. Click **Next**.
   f. If prompted to choose a driver, select **CyUSB.sys**.
   g. If the PC is running Windows XP and a message appears saying that the software has not passed Windows logo testing, click **Continue Anyway**.
4. Open the **Automated Register Window Builder** application and load the .xml file for the part on the evaluation board. Plug the 10-way ribbon cable on the USBi into the I²C/SPI port (J12) on the evaluation board.

POWERING THE BOARD

The ADAU1962/ADAU1966 evaluation board requires a power supply input of 12 V dc and ground to the power jack; 12 V draws ~150 mA at higher sample rates with all channels running. The on-board regulators provide 9.0 V, 5.0 V, and 3.3 V rails. The 9.0 V rail is derived from 12 V by a linear regulator; it provides voltage to the audio op amp in the active output filter for Channel 1 and Channel 2. The 5.0 V rail is derived from 12 V by a switching regulator; it can supply AVDD as well as IOVDD for the ADAU1962/ADAU1966 and other peripherals. The 3.3 V rail is derived from the 5.0 V supply by an LDO linear regulator; it provides voltage to AVDD and IOVDD as well as other active peripherals.

AVDD and IOVDD are selected on the board using 0 Ω, 0805 package resistors. Install only one resistor for each load, AVDD and IOVDD, as described in Figure 6. Figure 6 shows AVDD fed from 5.0 V and IOVDD fed from 3.3 V.

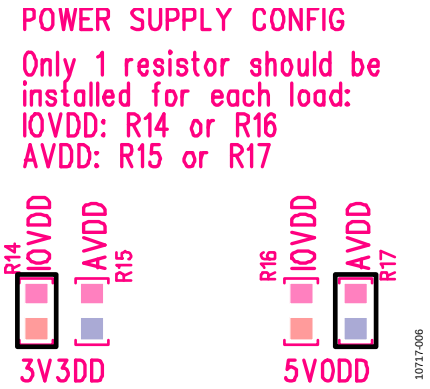

Figure 6. AVDD and IOVDD Selection Resistors

The ADAU1962/ADAU1966 have an internal voltage regulator that allows the user to derive DVDD and PLLVDD from the AVDD voltage source. The external PNP transistor, Q1, and passives, C36, C40 and R56, make the regulator circuit shown in Figure 7. Short both JP9 and JP11 to activate the circuit; JP9 supplies the emitter of the PNP, and JP11 powers the VSUPPLY pin (Pin 25) on the ADAU1962/ADAU1966.

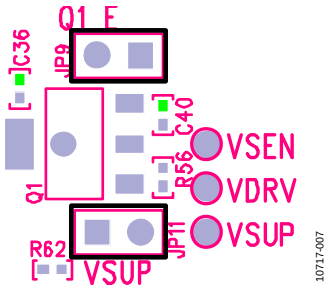

Figure 7. ADAU1962/ADAU1966 Internal Regulator Jumpers

Links are provided along each ADAU1962/ADAU1966 power rail to give access for current measurement (see Figure 8). These links also allow directly supplying voltage from an outside source.

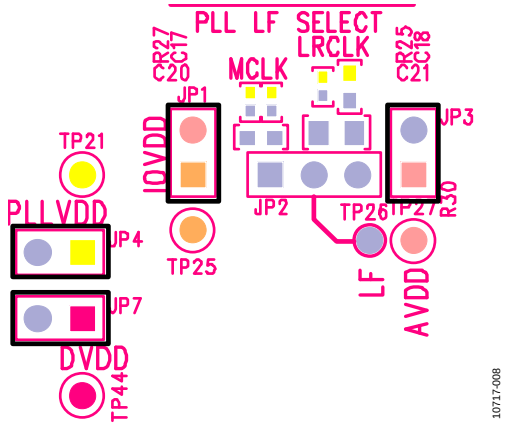

Figure 8. ADAU1962/ADAU1966 Power Links

RESET FOR THE EVALUATION BOARD

The ADAU1962/ADAU1966 evaluation board has provision for resetting and powering down the ADAU1962/ADAU1966. S2 on the evaluation board, shown in Figure 9, is a momentary reset switch that pulls the master reset ($\overline{MR}$) line low; this line controls the reset generator U10. $\overline{MR}$ is also connected to the USBi and SDP INTF connectors through steering diodes and protection resistors so that outside devices can control the reset state of the evaluation board, as shown in Figure 26. The power down jumper, JP5, allows the $\overline{MR}$ line to be tied low. The output of the reset generator drives the PU_/RST line.

The PU_/RST line is directly connected to two devices: the S/PDIF receiver and the ADAU1962/ADAU1966. A pull-down resistor holds the line low until the reset generator, U10, asserts the line high, as shown in Figure 26. The PU_/RST line is also connected to a pin on the SDP INTF through a steering diode and protection resistor, allowing external reset control.

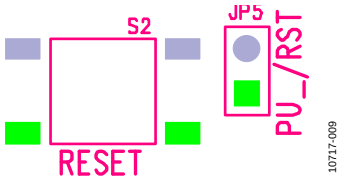

Figure 9. RESET Switch and Power-Down Jumper

SETTING UP THE MASTER CLOCK (MCLK)

The MCLK routing on the evaluation board is handled by a block of jumpers, J5, allowing any one of four sources to be selected: SPDIF, SMA connector, active OSC, and INTF connector. The board comes with SPDIF selected, as shown in Figure 10.

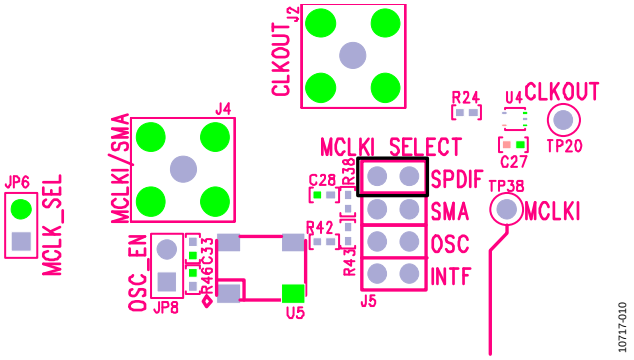

Figure 10. SPDIF Selected as MCLK Source

The evaluation board has a 12.288 MHz active oscillator that can be selected by shorting the OSC_EN jumper, JP8, and selecting OSC on J5, as shown in Figure 11.

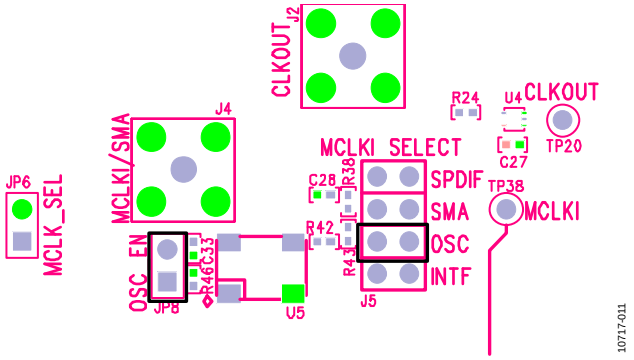

Figure 11. Active OSC-Enabled and Selected as MCLK

When using the SDP interface to add serial audio onto the evaluation board, MCLK can either be supplied by the SDP board, or it can be supplied by the MCLKO pin of the ADAU1962/ADAU1966.

To route MCLK from the SDP interface to the ADAU1962/ ADAU1966, apply a shorting jumper across JP6 (MCLK_SEL), as shown in Figure 12; this sets the direction of the level translators on the board to receive an MCLK signal from the SDP interface, EI3 1A, Pin 119 (EI3_MCLK), as shown in Figure 28. Next, select INTF on JP5 to route the output of the MCLK level translator to the MCLKI pin of the ADAU1962/ADAU1966.

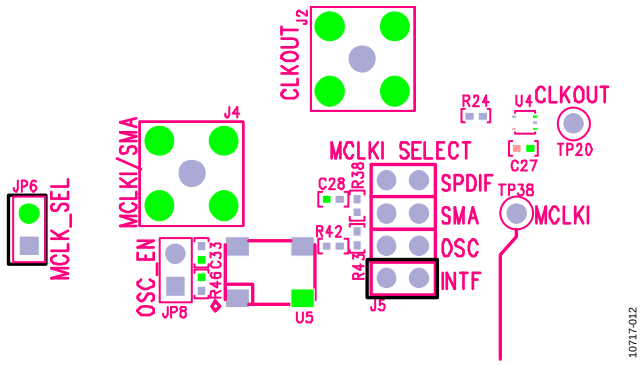

Figure 12. INTF Input Enabled and Selected

To route MCLK from the ADAU1962/ADAU1966 to the SDP interface, remove the shorting jumper from JP6 (MCLK_SEL); this changes the direction of the level translators and feeds a buffered version of the MCLKO signal from the ADAU1962/ADAU1966 to the EI3_MCLK pin on the SDP interface.

CRYSTAL OPERATION

The ADAU1962/ADAU1966 evaluation board is shipped without R49 on the board, effectively disabling the crystal circuit. For operation with a crystal, install a 150 Ω, 0402 resistor and remove any jumpers from J5. For permanent use of the crystal, remove the 0 Ω resistor, R39.

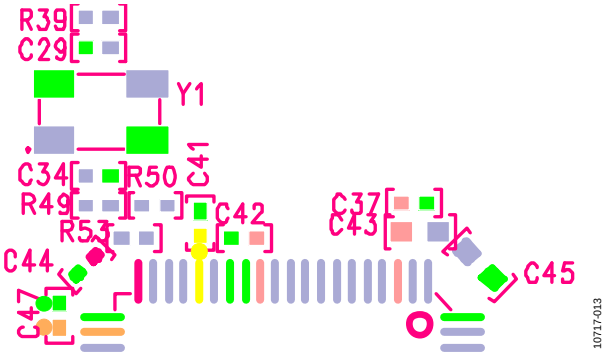

Figure 13. Crystal Circuit Near ADAU1962/ADAU1966

PLL SELECTION

The PLL in the ADAU1962/ADAU1966 is very flexible, allowing the part to run from a wide range of either MCLK or LRCLK frequencies. It is also possible to shut the PLL off altogether and use the part in direct MCLK mode; functionality with no PLL is limited to 256 × f_S.

By default, the ADAU1962/ADAU1966 run from the PLL using MCLK as the clock source. The MCLK loop filter must be selected using JP2, as shown in Figure 14.

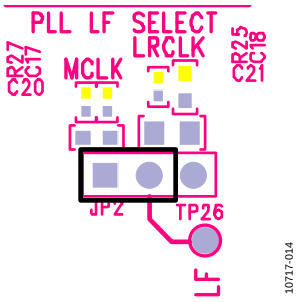

Figure 14. MCLK Selection for PLL Loop Filter

DLRCLK can be selected as the PLL clock source using the PLL and Clock Control Register 0, Register 0x00, Bits[7:6]. In this case, the LRCLK loop filter must be selected, as shown in Figure 15. If DLRCLK is selected as the PLL clock, there is no need for an MCLK signal.

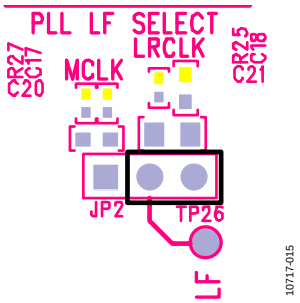

Figure 15. LRCLK Selection for PLL Loop Filter

DIGITAL AUDIO CONNECTIONS AND ROUTING

The ADAU1962/ADAU1966 evaluation board has two separate inputs for digital audio signals: S/PDIF and SDP interface.

The S/PDIF receiver can handle either of two options: COAX uses the RCA jack, J1, and OPT uses the Toslink jack, U1. The S/PDIF input is selected using S1, as shown in Figure 16.

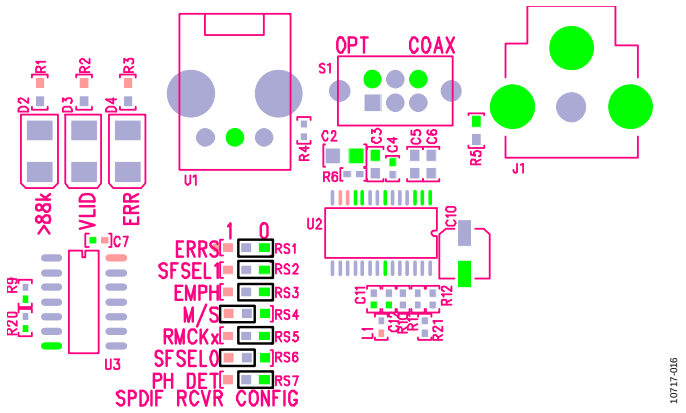

Figure 16. S/PDIF Input Selector Switch, SW1

A series of resistors is provided to set the functional mode of the S/PDIF receiver. By default, the S/PDIF receiver runs in master mode, 256 × f_S, I^2S format; consult the data sheet for the S/PDIF receiver to make changes to the hardware mode.

The jumpers shown in Figure 17 are set for the S/PDIF receiver to drive the DBCLK and DLRCLK clock ports and the eight DSDATAx lines of the ADAU1962/ADAU1966. JP22 selects the input to the buffer; the output of this buffer shows up on the right-hand column of JP13 to JP20. The pins in the middle column of these jumpers are connected to the DSDATAx pins of the ADAU1962/ADAU1966 through the appropriate line termination. DBCLK and DLRCLK selections are made with JP10 and JP12, respectively, where the middle pins are connected to the DBCLK and DLRCLK pins of the ADAU1962/ADAU1966.

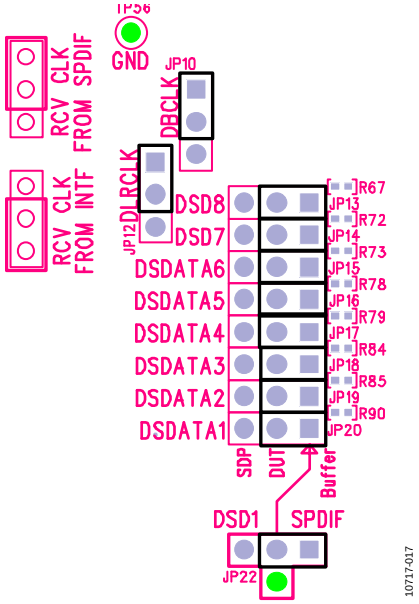

Figure 17. S/PDIF Data and Clock Routing

The SDP interface, J6 and J8, make up a standard interconnect within Analog Devices. They provide for transfer of digital audio, clocks, and control between boards. For additional information, see the pinout included in the schematic in Figure 28.

Figure 18 shows the jumpers configuration for using the SDP interface connector as the digital audio source. JP22 is set so that the DSDATA1 source from the SDP interface is driving the buffer, and this buffer is connected to all eight/six DSDATAx inputs of the ADAU1962/ADAU1966. JP10 and JP12 are set for the ADAU1962/ADAU1966 to run in slave mode from clocks supplied by the SDP interface.

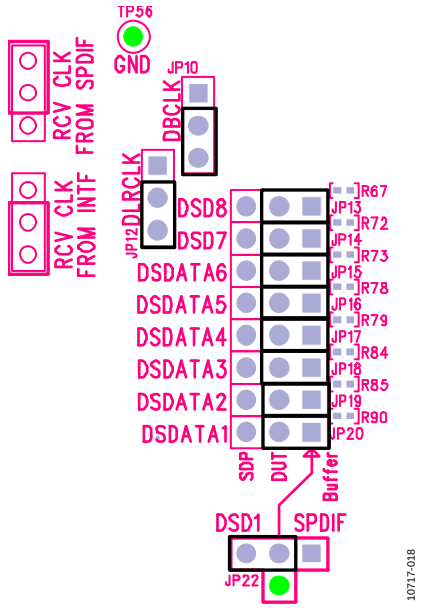

Figure 18. SDP Interface DSDATA1 Distribution

CONNECTING ANALOG AUDIO CABLES

There are two forms of the analog outputs of the ADAU1962/ADAU1966 evaluation board: differential outputs and single-ended outputs.

The differential outputs appear on through hole test points as well as on 25-way, female D-sub connectors. The pinout of these D-sub connectors follows the professional audio standard for eight differential signals on a single jack. A single 25-pin male D-sub to XLR male harness has been provided for testing and evaluation purposes. These cables are widely available on the open market.

The differential outputs of the ADAU1962/ADAU1966 drive the connectors directly through a simple 1-pole RC filter and appropriate ac coupling.

Channel 1 and Channel 2 are also available as single-ended outputs on a stereo, 3.5 mm stereo jack, J14. The J9 and J10 jumpers assign the differential outputs of the DAC to either the passive differential output or the active single-ended filter.

Figure 19 shows J9 and J10 set for the passive differential output available on the D-sub connector.

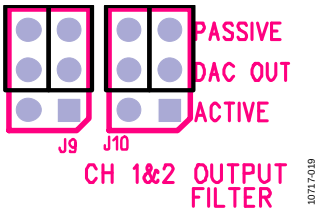

Figure 19. Channel 1 and Channel 2 in Passive Differential Output Mode

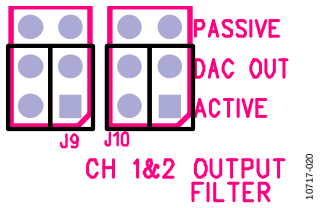

Figure 20. Channel 1 and Channel 2 in Active Single-Ended Output Mode

Figure 20 shows J9 and J10 set for the active single-ended output available on the 3.5 mm TRS connector, J14.

USING THE ADAU1962/ADAU1966

When the ADAU1962/ADAU1966 start in standalone mode, it is operational upon power up.

If the ADAU1962/ADAU1966 are not powered up in standalone mode, the USBi must be connected to set the appropriate registers to make the part operational. First, the ADAU1962/ADAU1966 must be activated using the PLL and Clock Control 0 register (Address 0x00) by setting the PUP bit (Bit 0) to 1 for master power-up. Next, using the DAC Control 0 register (Address 0x06) set the MMUTE bit (Bit 0) to 0 for normal operation. The ADAU1962/ADAU1966 now pass audio in its default mode: I^2S, 256 × f_S, slave mode, and CM = 2.25 V.

If different settings are desired, it is recommended to program the custom settings before unmuting the part.

SCHEMATICS AND ARTWORK

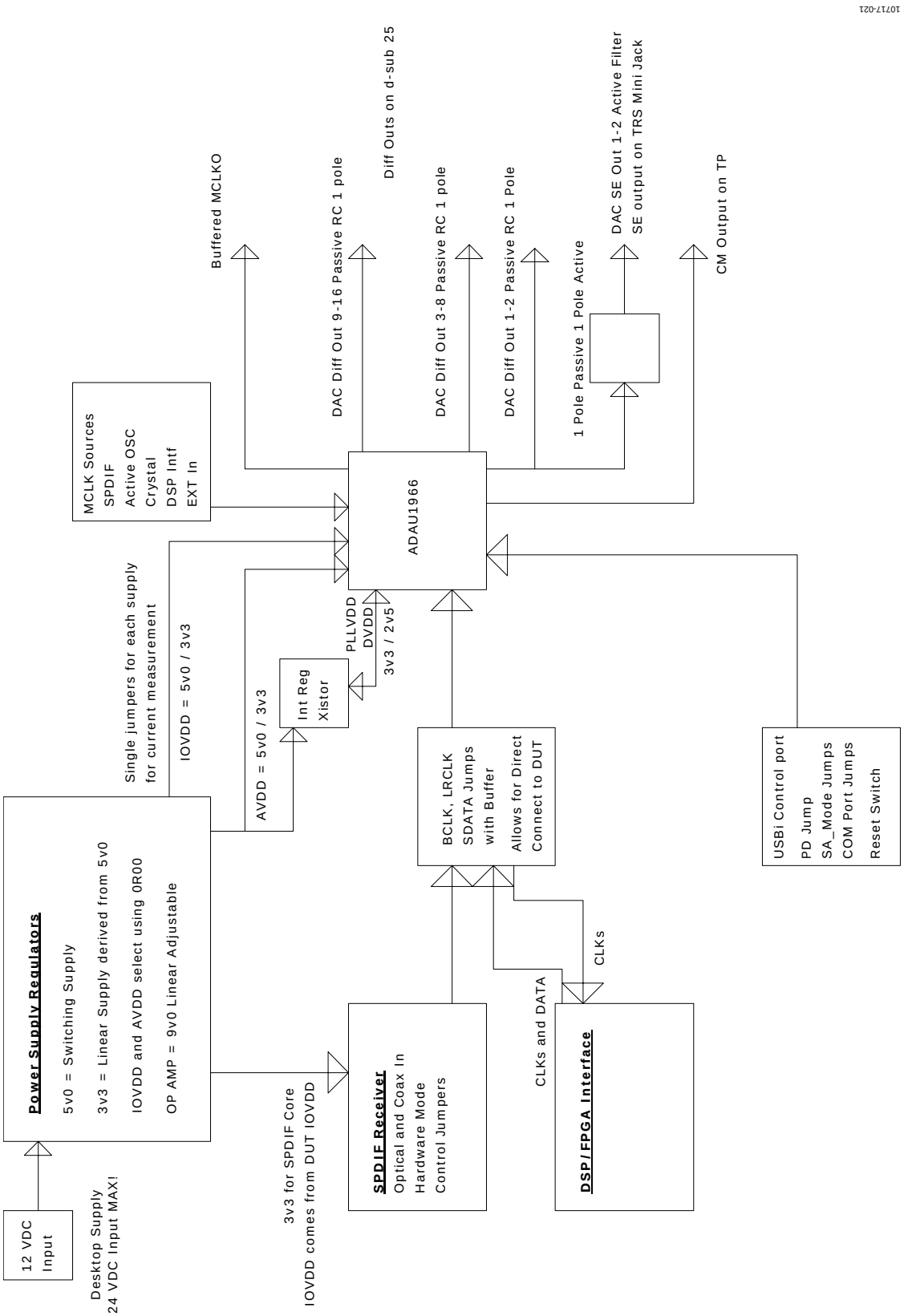

Figure 21. ADAU1962/ADAU1966 Evaluation Board Block Diagram Schematic, Page 1

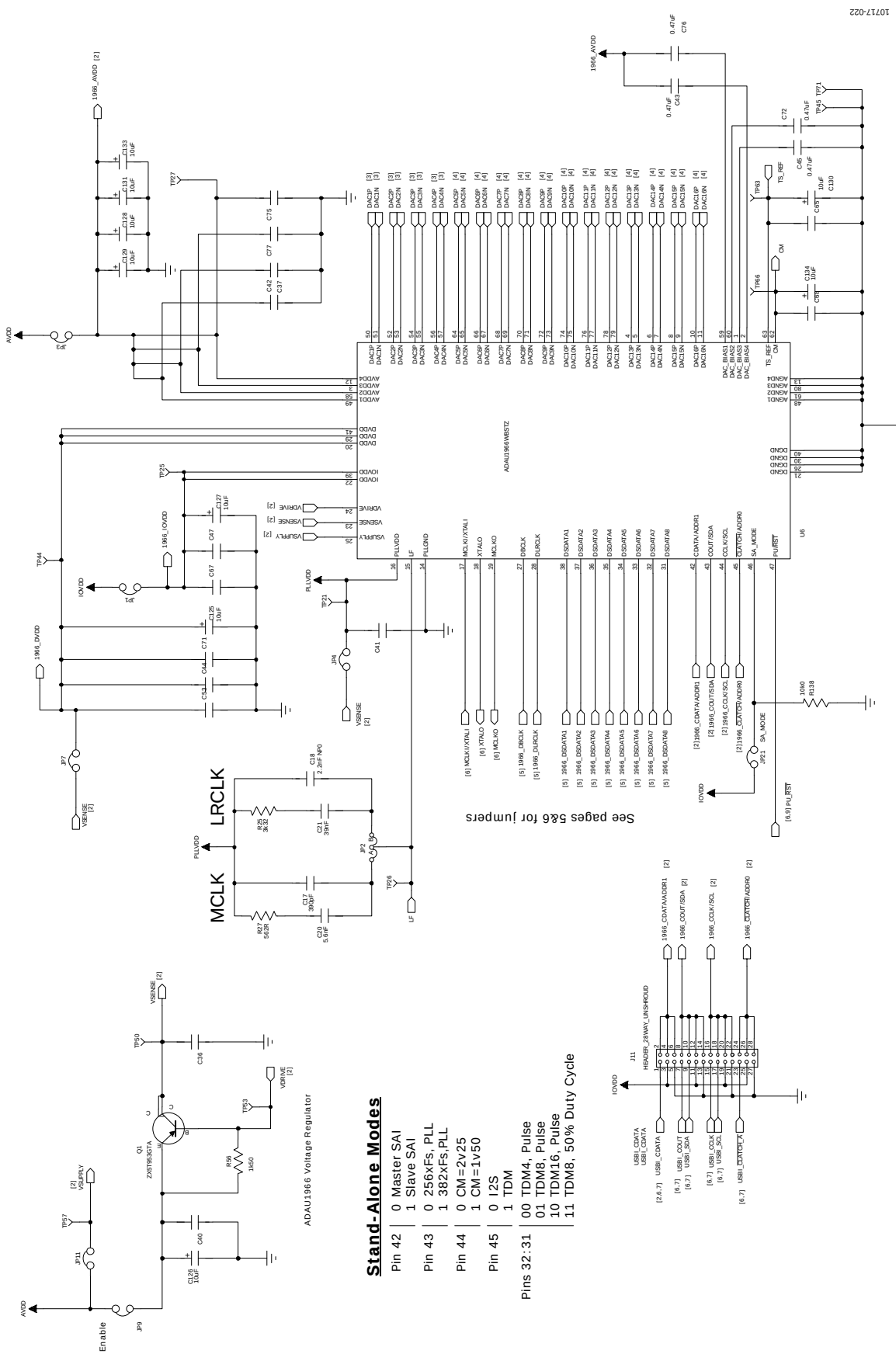

Figure 22. ADAU1962/ADAU1966 Evaluation Board, PLL LF Selection and Internal Regulator Schematic, Page 2

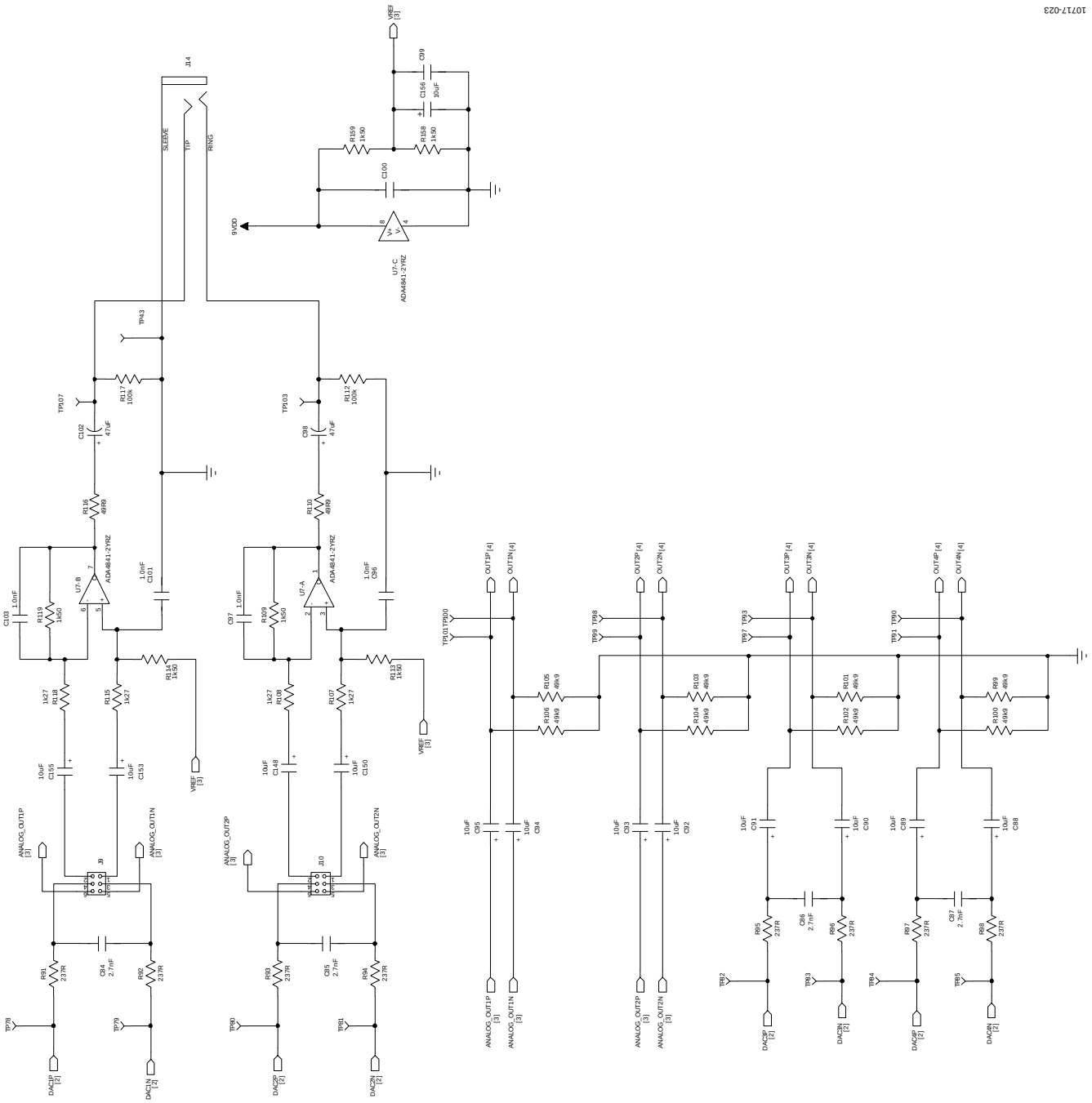

Figure 23. ADAU1962/ADAU1966 Evaluation Board, DAC Outputs, CH1 and CH2 Active Buffer and CH1 to CH4 Passive Filters Schematic, Page 3

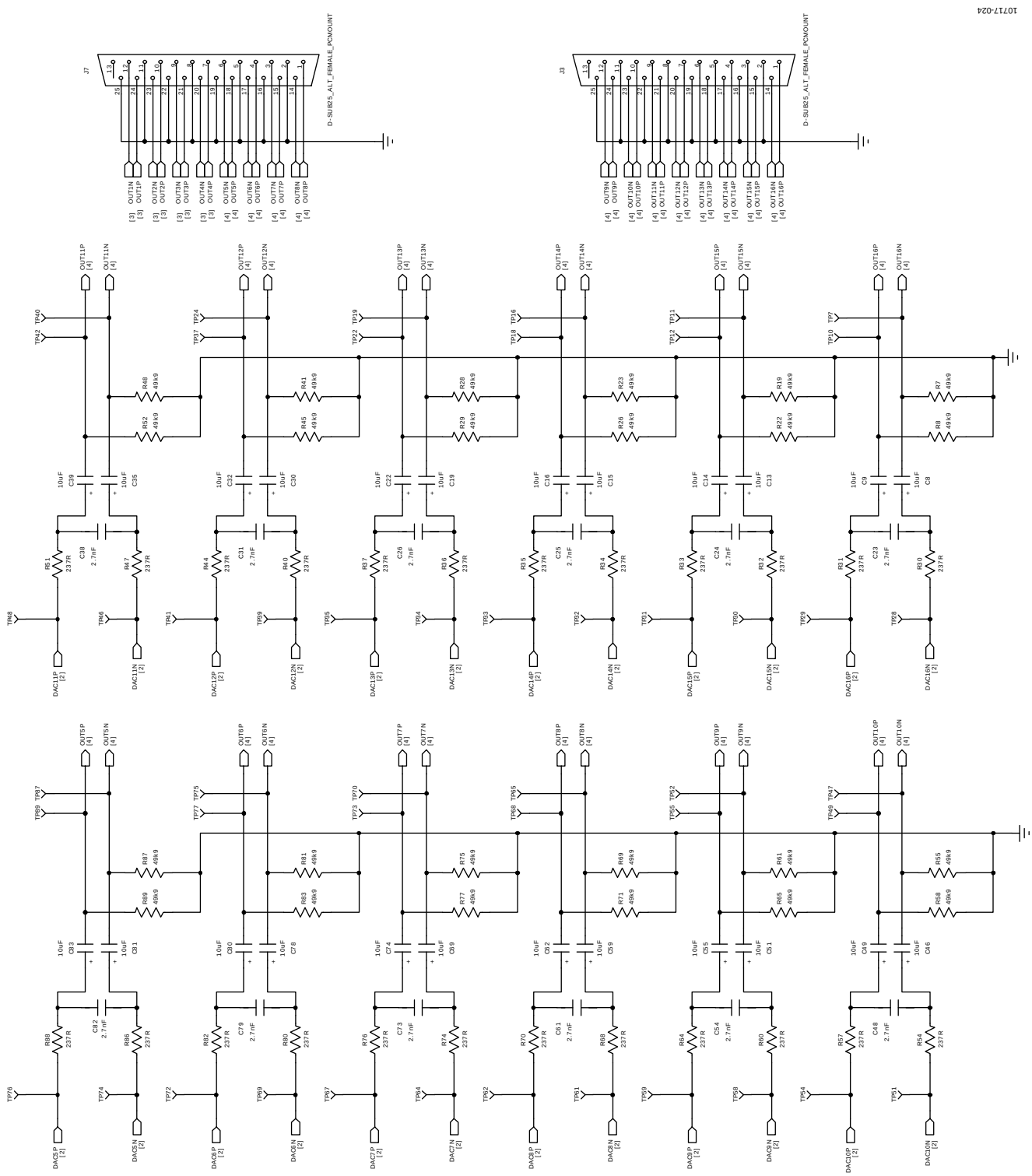

Figure 24. ADAU1962/ADAU1966 Evaluation Board, RC Output Filters and D-Sub 25-Pin Connectors Schematic, Page 4

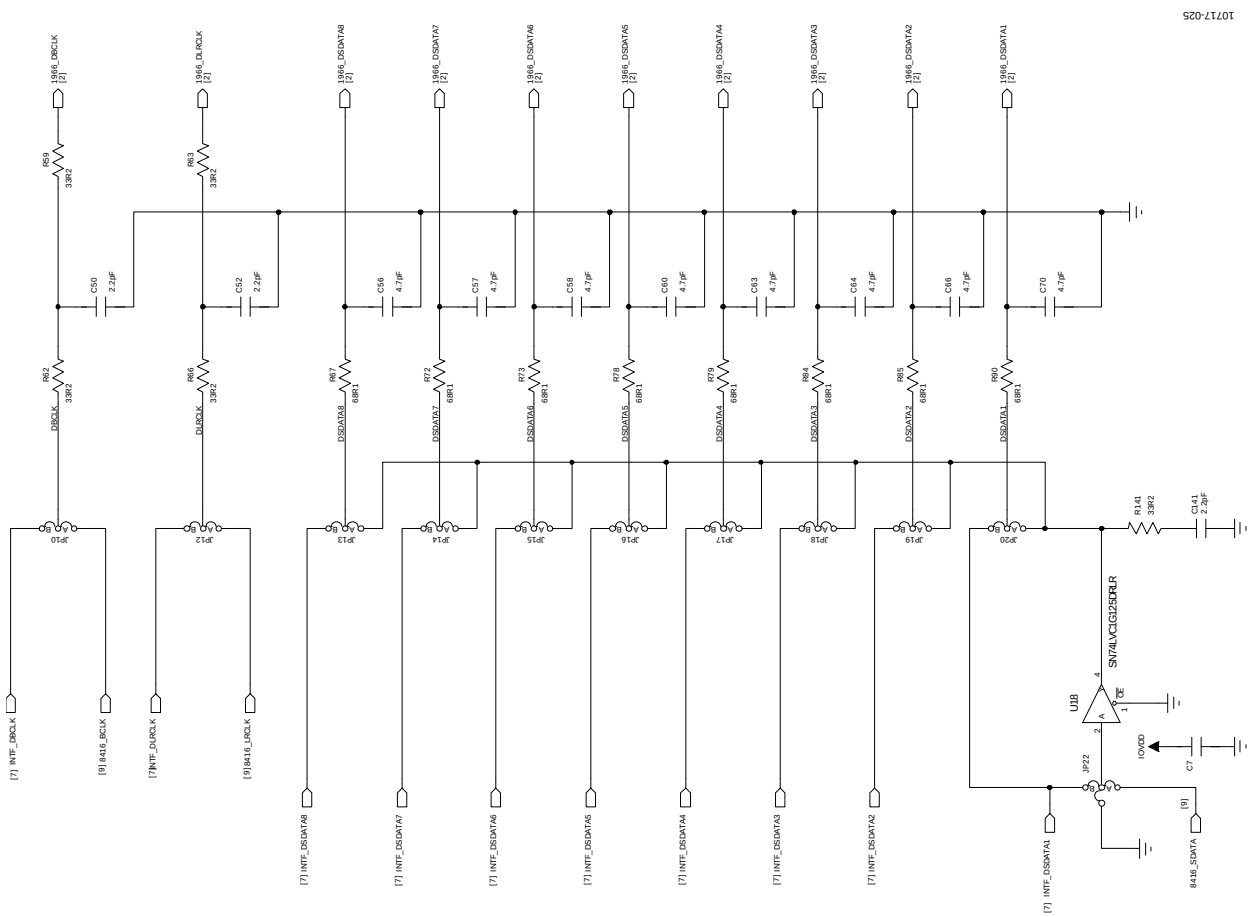

Figure 25. ADAU1962/ADAU1966 Evaluation Board, BCLK, LRCLK, and SDATA Jumpers and Routing Schematic, Page 5

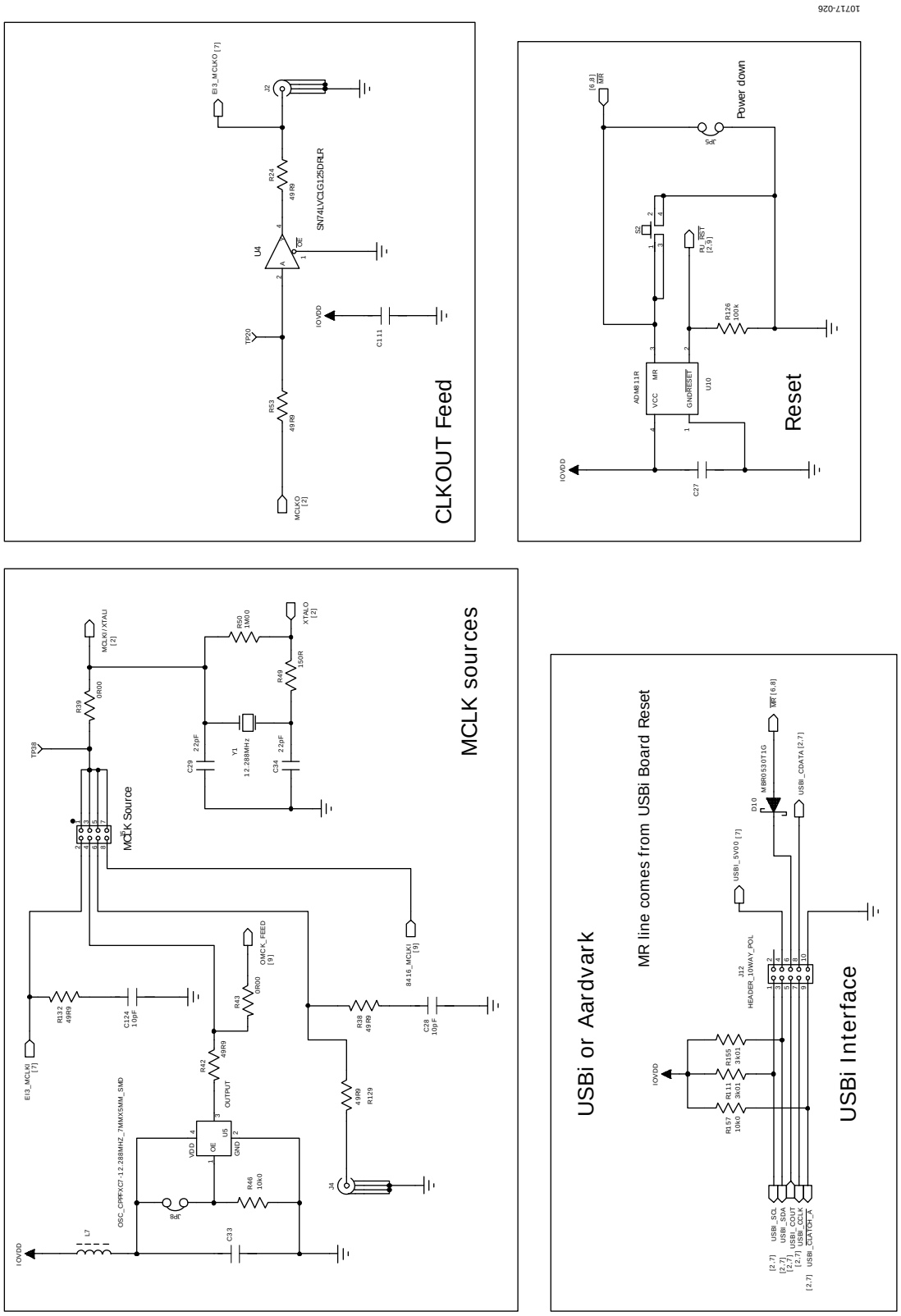

Figure 26. ADAU1962/ADAU1966 Evaluation Board, MCLK Source, USBi Interface, CLKOUT Feed, and Reset Generator Schematic, Page 6

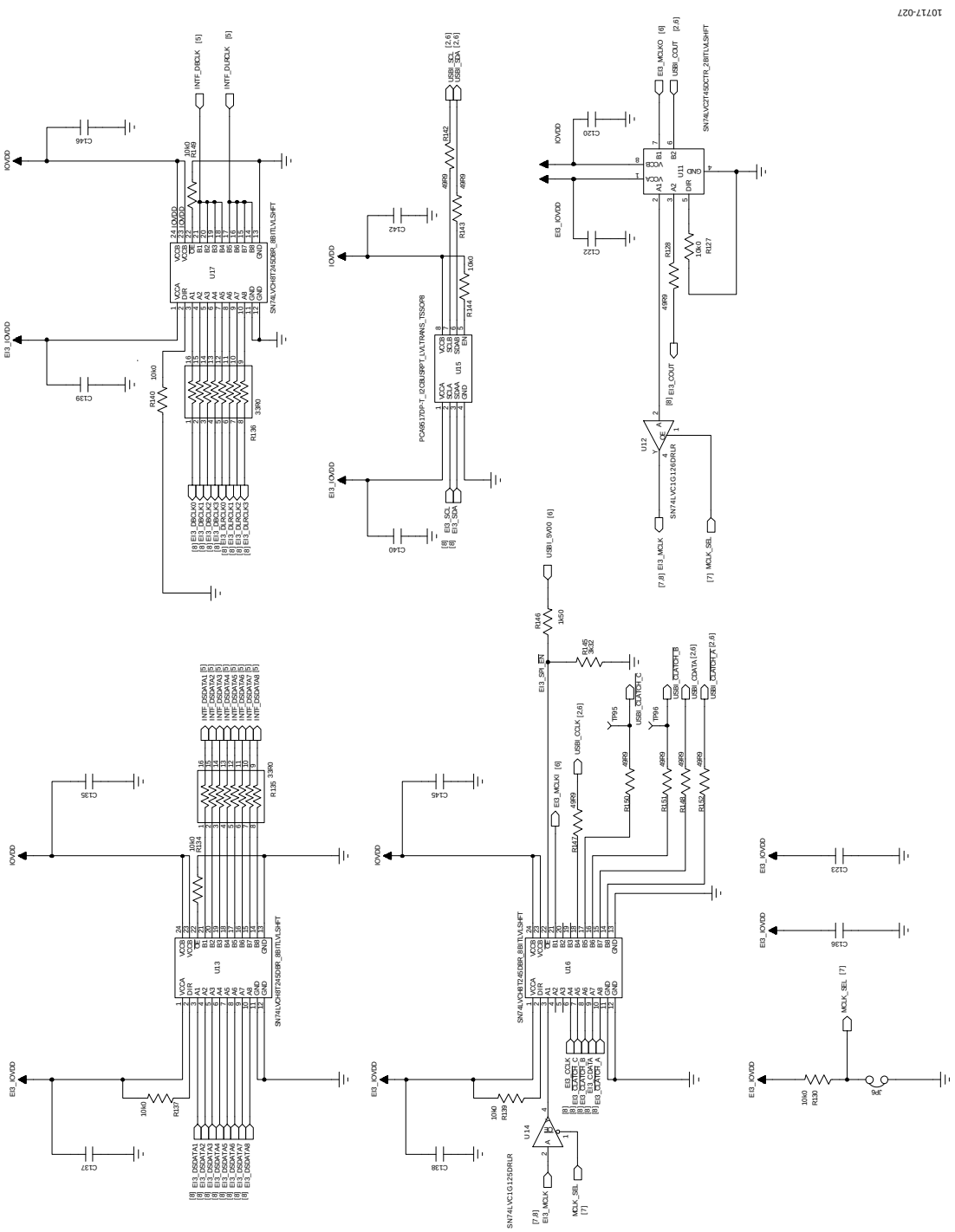

Figure 27. ADAU1962/ADAU1966 Evaluation Board, Level Shift and Clock Direction Control Schematic, Page 7

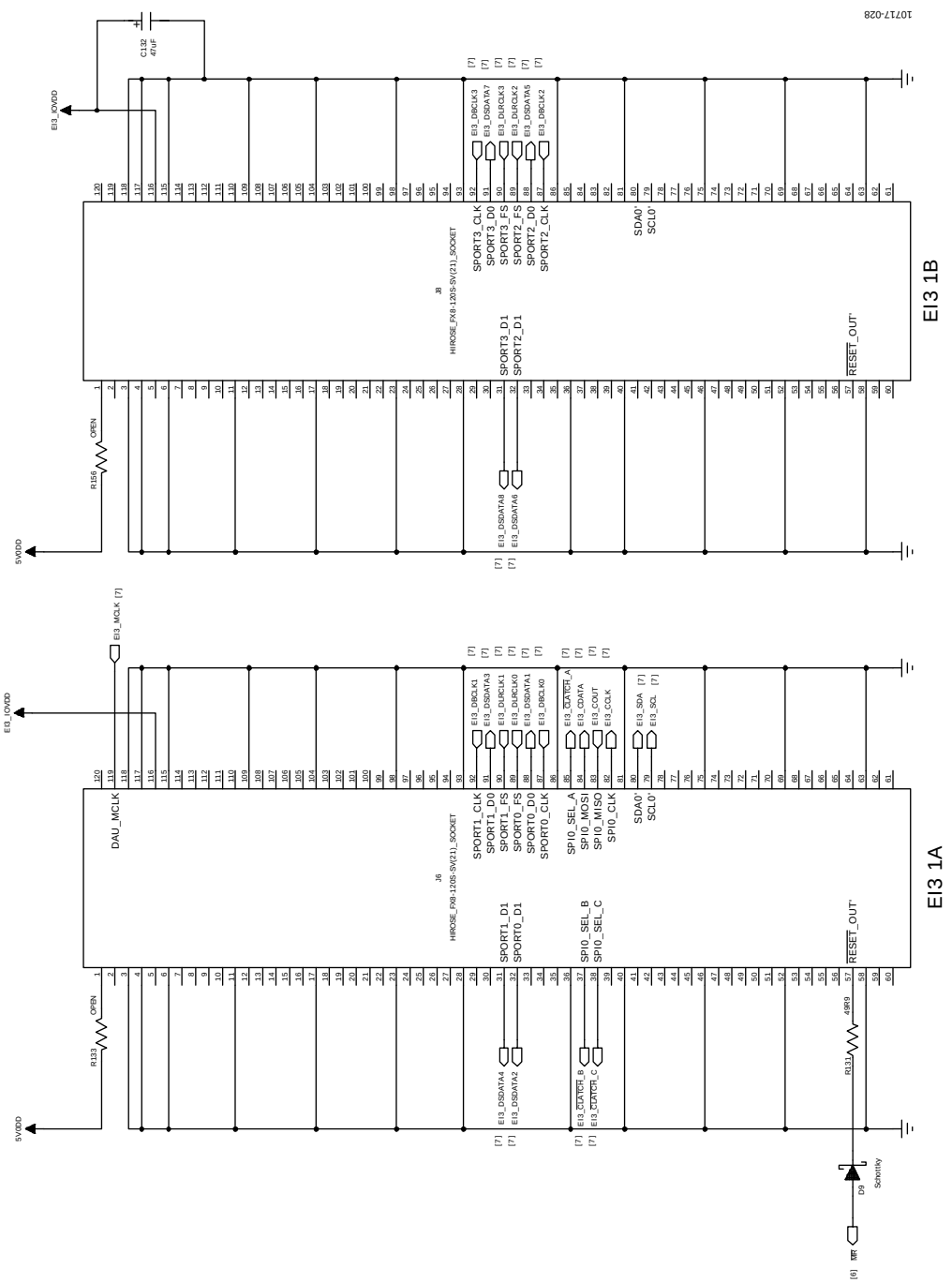

Figure 28. ADAU1962/ADAU1966 Evaluation Board, SDP Interface Connectors Schematic, Page 8

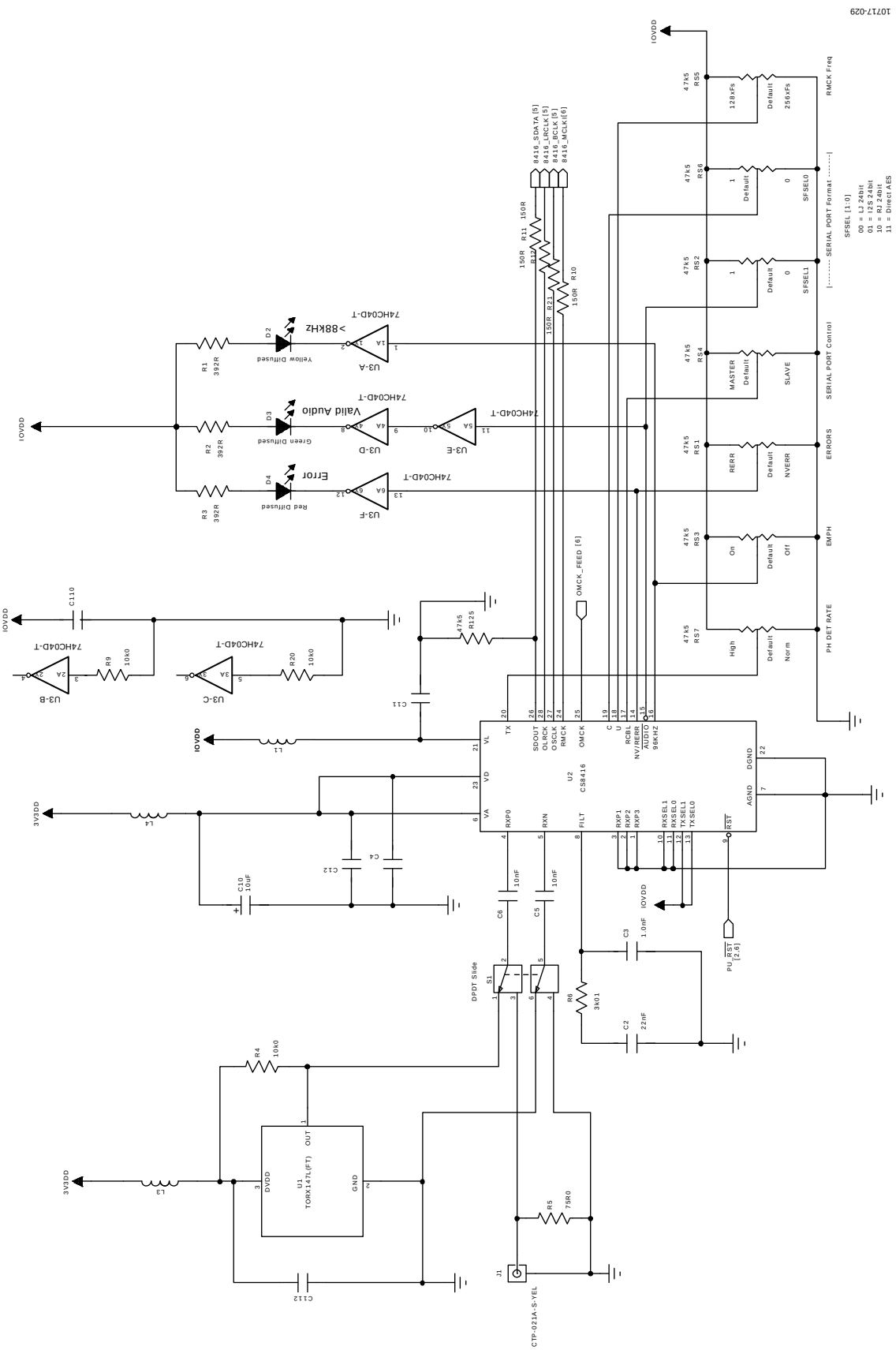

Figure 29. ADAU1962/ADAU1966 Evaluation Board, S/PDIF Receiver Schematic, Page 9

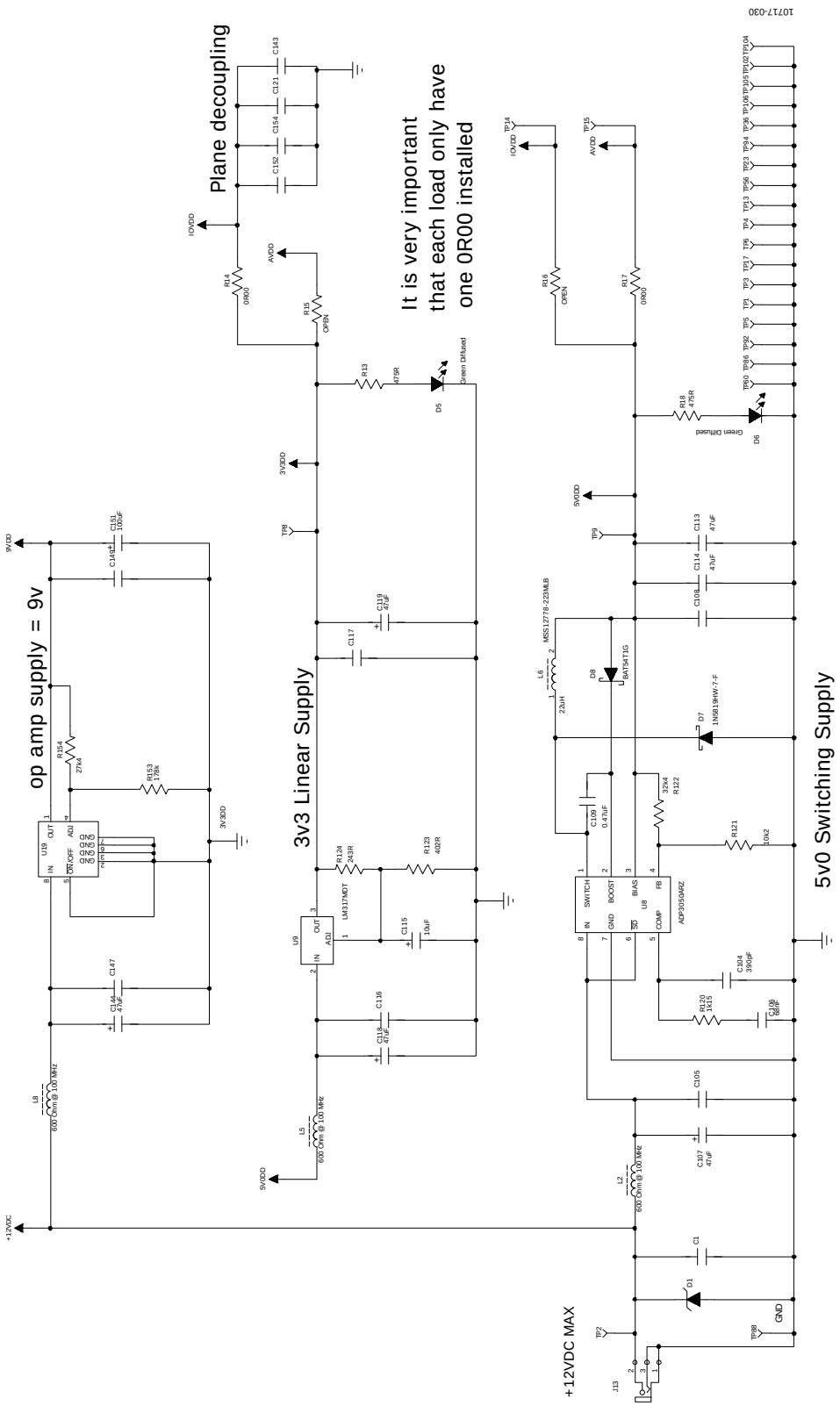

Figure 30. ADAU1962/ADAU1966 Evaluation Board, Power Supply Schematic, Page 10

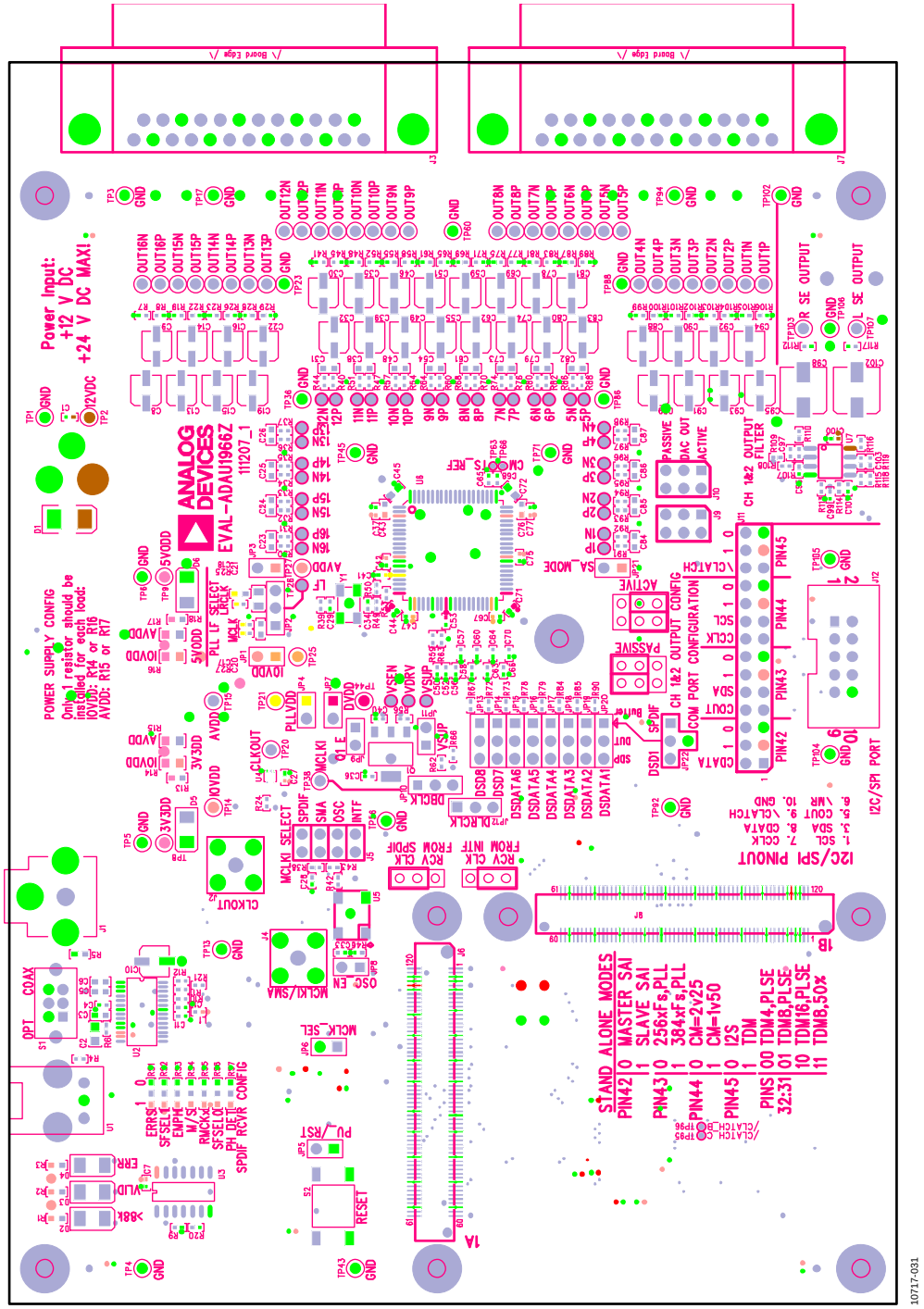

Figure 31. ADAU1962/ADAU1966 Evaluation Board, Top Assembly

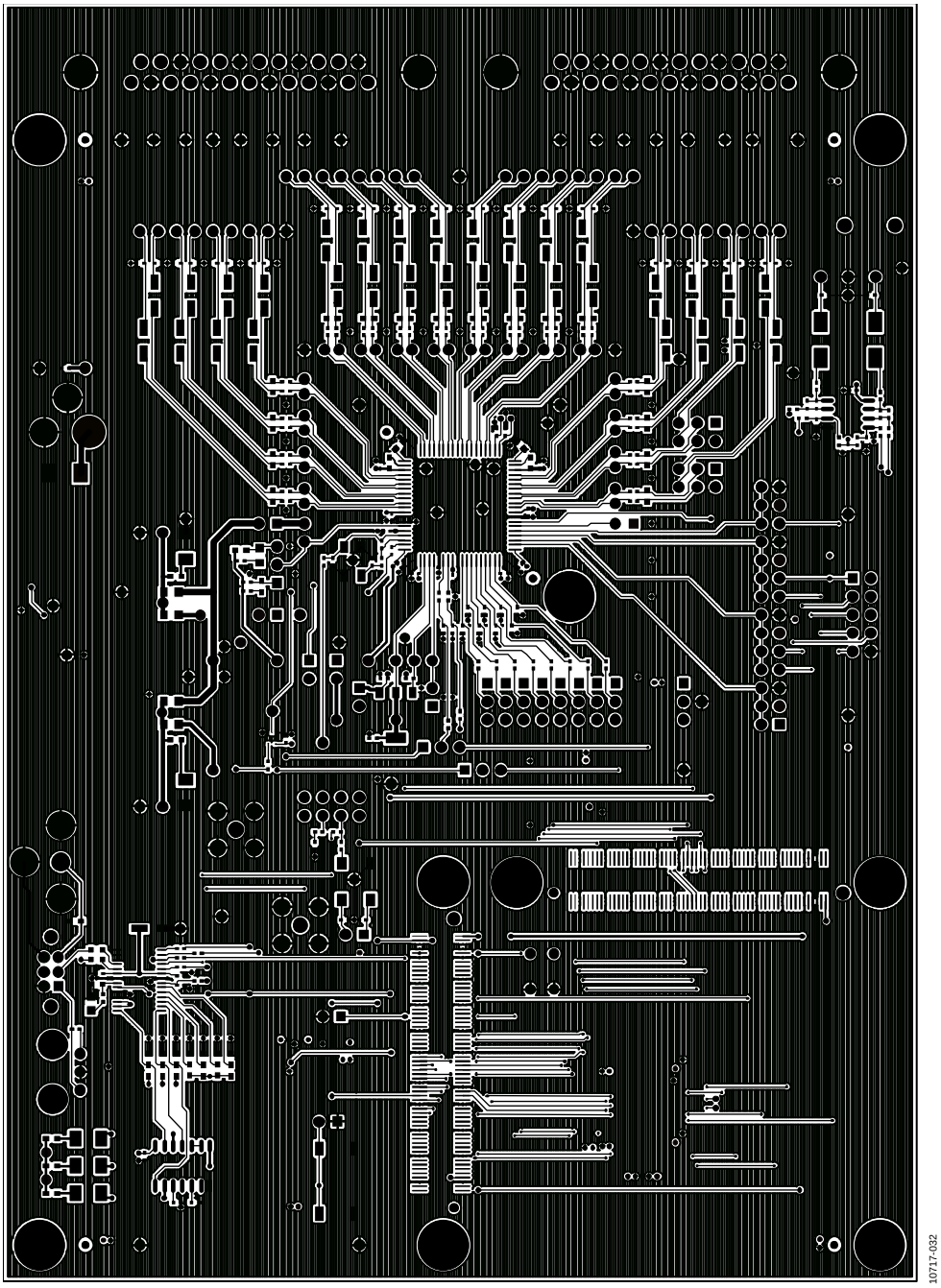

Figure 32. ADAU1962/ADAU1966 Evaluation Board, Top Layer Copper

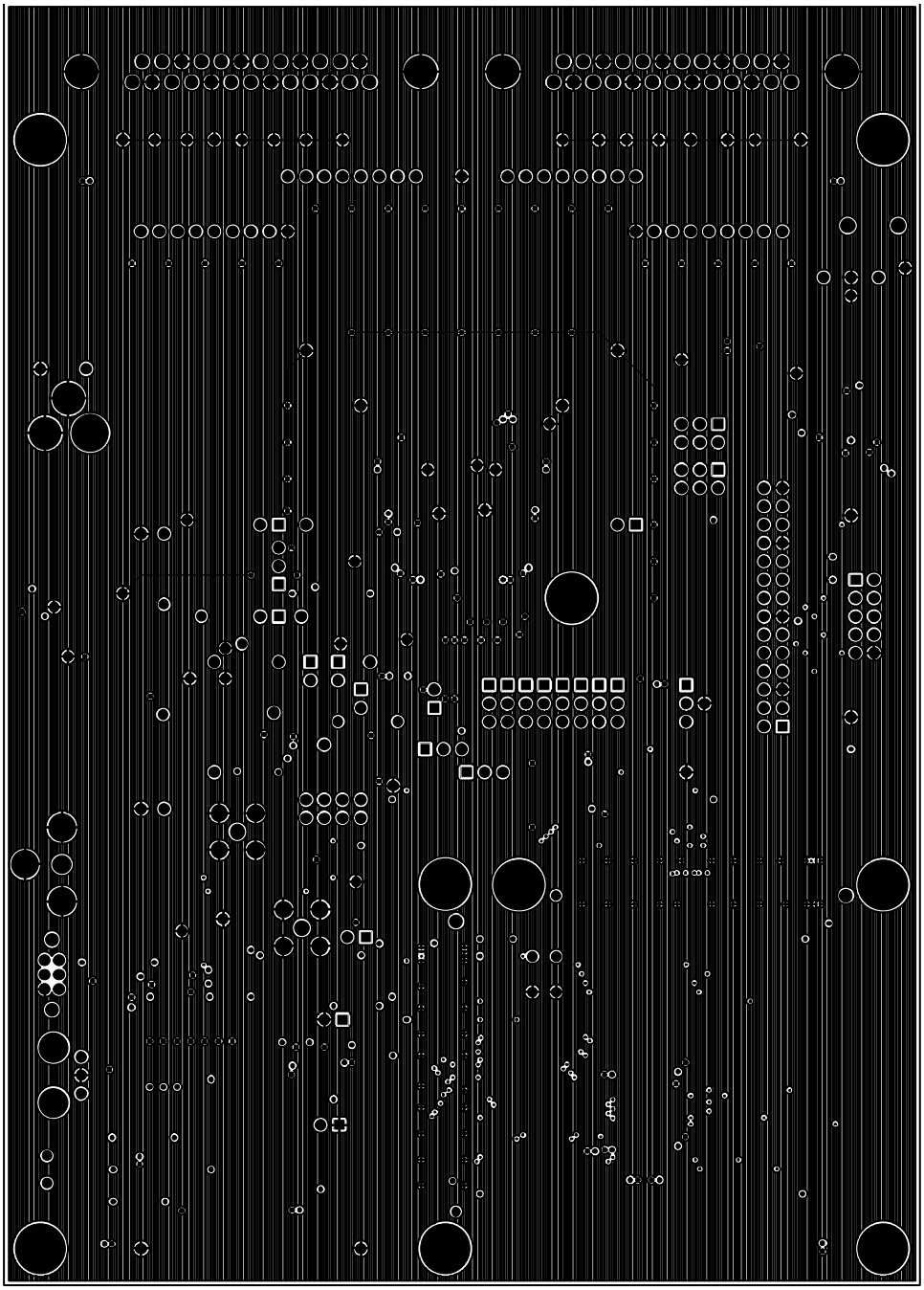

Figure 33. ADAU1962/ADAU1966 Evaluation Board, L2 Ground

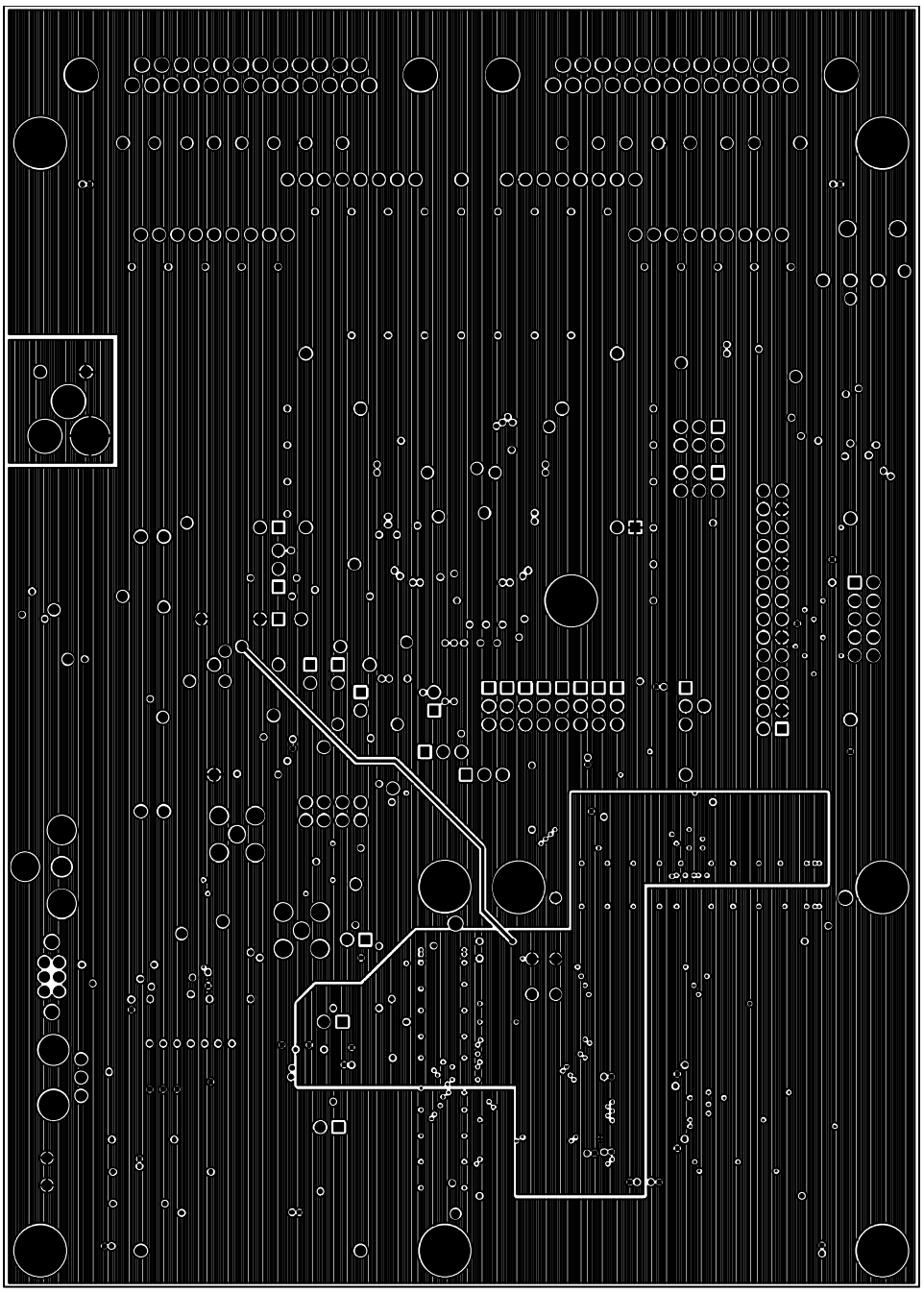

Figure 34. ADAU1962/ADAU1966 Evaluation Board, L3 Power

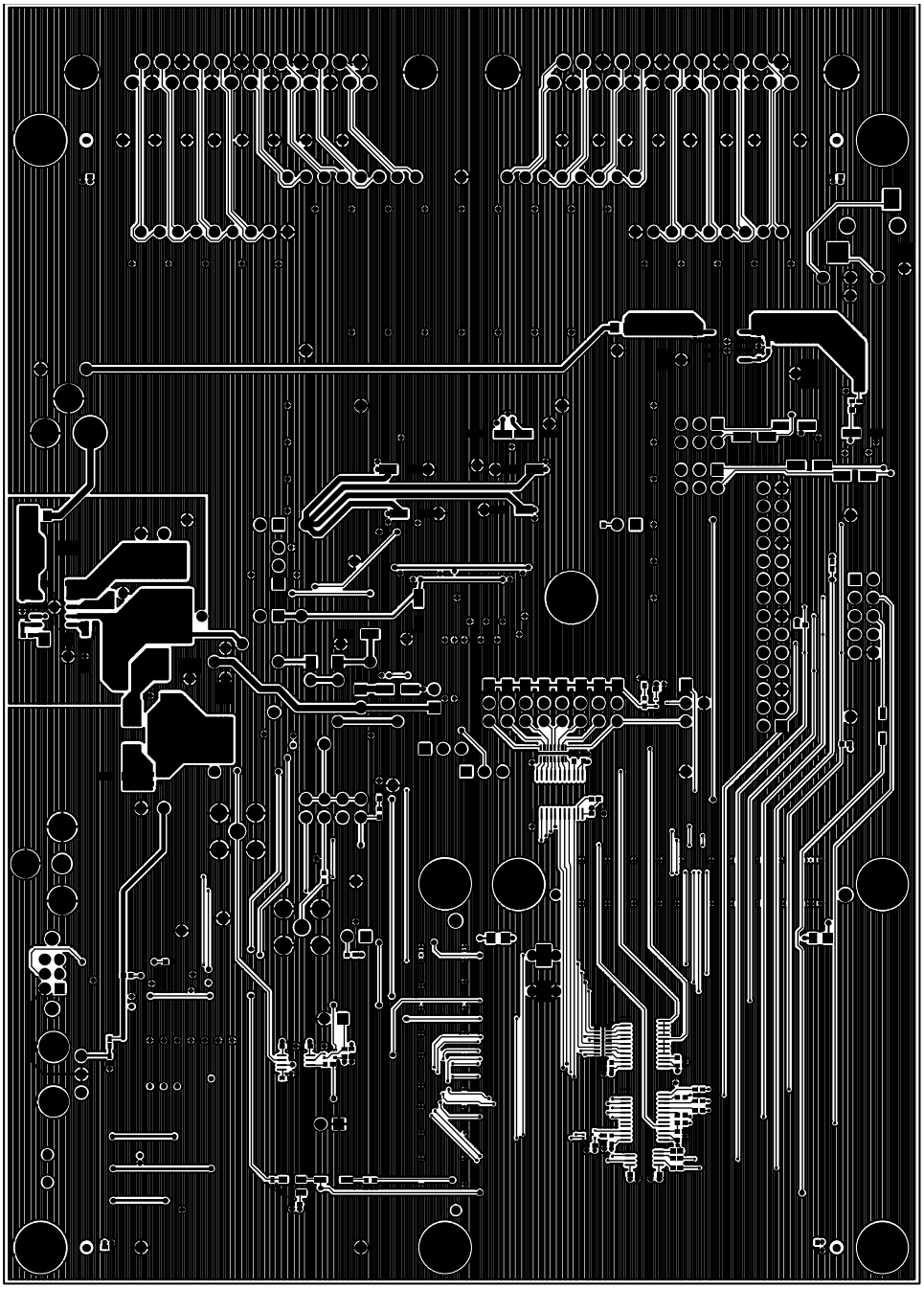

Figure 35. ADAU1962/ADAU1966 Evaluation Board, Bottom Copper

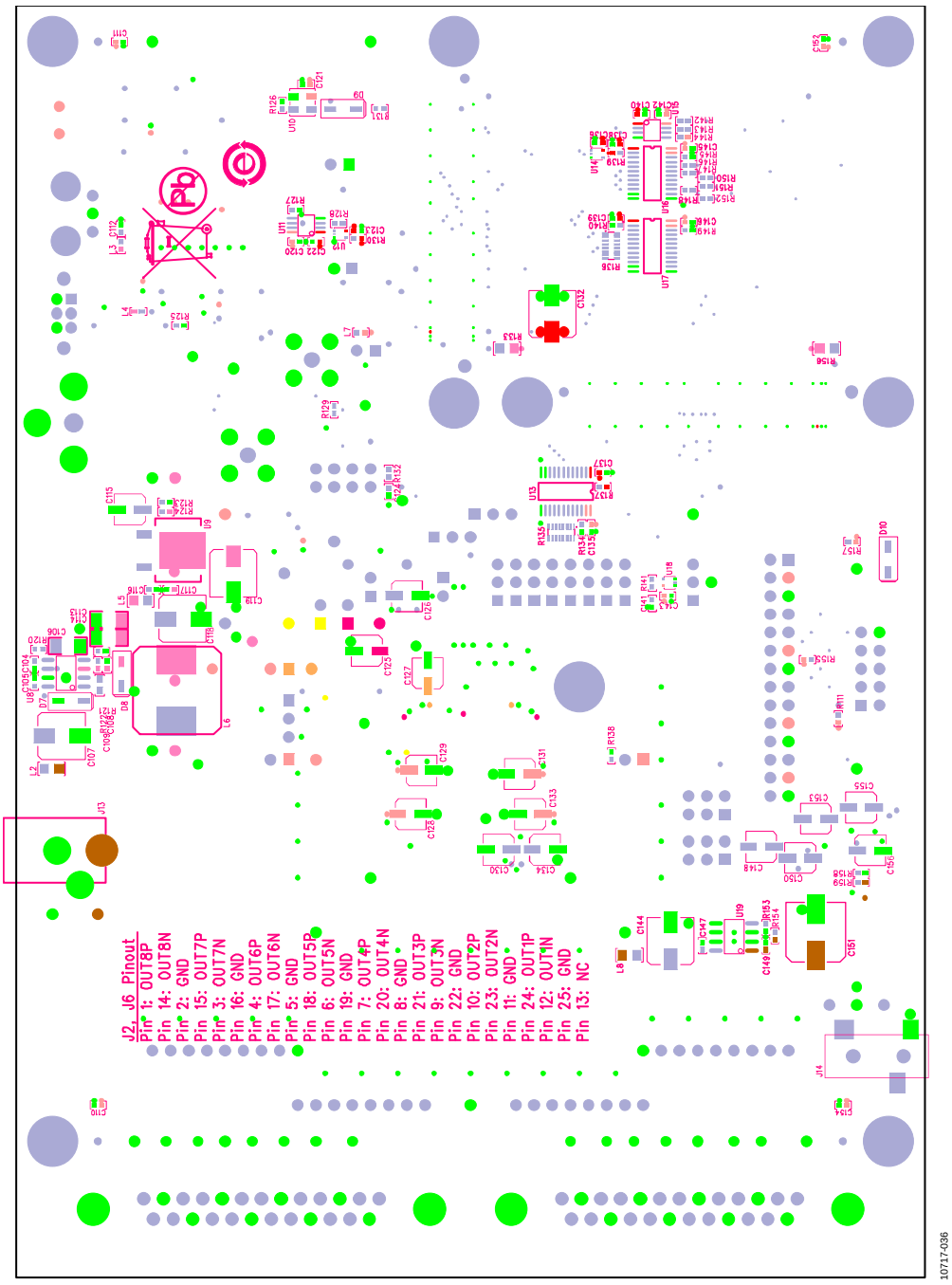

Figure 36. ADAU1962/ADAU1966 Evaluation Board, Bottom Assembly

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I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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