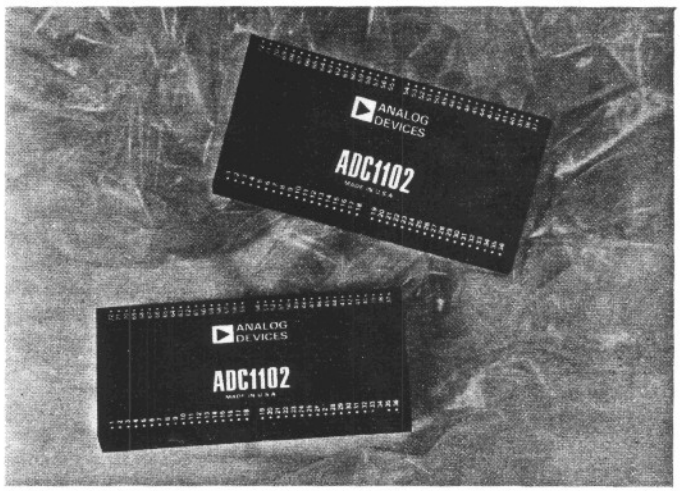
ANALOG DEVICES

High Speed Analog to Digital Converter

ADC1102

FEATURES

- 12-Bit Resolution and Accuracy
- Fast 8μs Conversion Time
- Low 10ppm/°C Maximum Gain TC
- User Choice of Input Range
- No Missing Codes 0° to +70°C
- Small Module Size



GENERAL DESCRIPTION

The ADC1102 is a high speed analog-to-digital converter, packaged in a small 2″ x 4″ x 0.4″ (51 x 102 x 10mm) module, which performs complete 12-bit conversions in less than 8μs. Using the successive approximations technique, it converts analog input voltages into natural binary, offset binary, or two's complement coded outputs. Data outputs are provided in both parallel and non-return-to-zero serial form.

Four analog input ranges are available: 0 to +20V, 0 to +10V, ±10V, ±5V. The user selects the desired range by making various connections to the module terminals. The ADC1102 can also be connected so as to perform conversions of less than 12-bit resolution with a proportionate decrease in conversion time.

Performance specifications include ±½LSB maximum error relative to full scale, ±10ppm/°C maximum gain temperature coefficient, and ±3ppm/°C differential nonlinearity temperature coefficient. The ADC1102 has no missing codes from 0° to +70°C.

TIMING

As shown in Figure 1, the leading edge of the convert command sets the MSB output to logic "0" and the CLOCK OUT, STATUS, MSB, and BIT 2 through BIT 12 outputs to logic "1". Nothing further happens until the convert command returns to logic "0", at which time the clock starts to run and the conversion proceeds.

With the MSB in the logic "0" state, the internal digital-to-analog converter's output is compared with the analog input. If the D/A output is less than the analog input, the first "0" to "1" clock transition resets the MSB to logic "1". If the D/A output is greater than the analog input, the MSB remains at logic "0".

The first "0" to "1" clock transition also sets the BIT 2 output to logic "0" and another comparison is made. This process continues through each successive bit until the BIT 12 (LSB) comparison is completed. At this point the STATUS and CLOCK OUT return to logic "0" and the conversion cycle ends.

The serial data output is of the non-return-to-zero (NRZ) format. The data is available, MSB first, 20ns after each of the twelve "0" to "1" clock transitions.

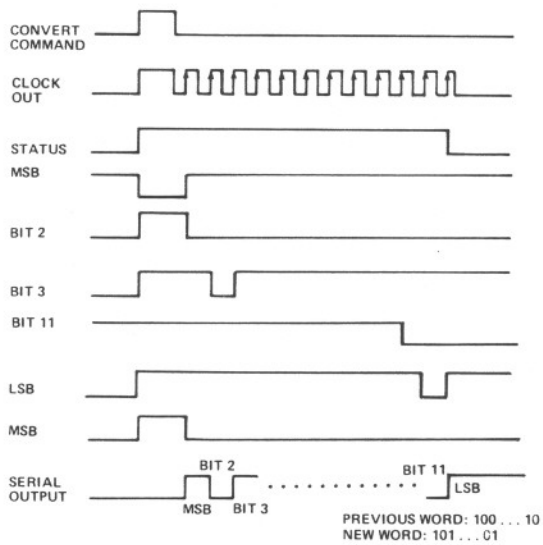


Figure 1. Timing Diagram

Route 1 Industrial Park; P.O. Box 280; Norwood, Mass. 02062
Tel: 617/329-4700 TWX: 710/394-6577

West Coast	Mid-West	Texas
213/595-1783	312/894-3300	214/231-5094

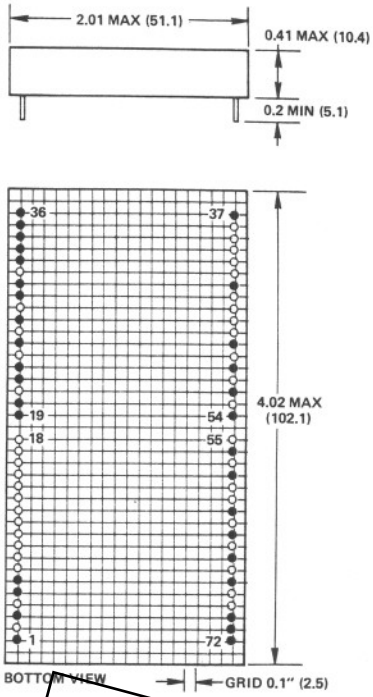
SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise noted)

MODEL	ADC1102
RESOLUTION	12 Bits
CONVERSION TIME	8μs (max)
ACCURACY	
Error Relative to Full Scale	±½LSB (max)
Quantization Error	±½LSB (max)
Differential Nonlinearity Error	±½LSB (max)
Missing Codes	No Missing Codes from 0 to +70°C
TEMPERATURE COEFFICIENTS	
Gain	±7ppm/°C (±10ppm/°C max)
Unipolar Offset	±0.7ppm/°C (±3ppm/°C max)
Bipolar Offset	±3ppm/°C (±7ppm/°C max)
Differential Nonlinearity	±3ppm/°C (±8ppm/°C max)
INPUT VOLTAGE RANGES	±5V, ±10V, +10V, +20V
INPUT IMPEDANCE (10V RANGE)	2500Ω
CONVERT COMMAND	Positive Pulse, 100ns min Width, Leading Edge Resets, Trailing Edge Starts, TTL/DTL Compatible
PARALLEL DATA OUTPUT	
Unipolar	Positive True Binary
Bipolar	Positive True Offset Binary, Two's Complement
SERIAL DATA OUTPUT	
Unipolar	Positive True Binary
Bipolar	Positive True Offset Binary
STATUS OUTPUT	"1" During Conversion. Complement also available. TTL/DTL Compatible.
LOGIC FANOUTS AND LOADINGS	
Convert Command Input	1TTL Unit Load
Clock Input	3TTL Unit Loads
Short Cycle Input	1TTL Unit Load
Parallel Data Outputs	3TTL Unit Loads/Bit
Serial Data Output	8TTL Unit Loads
STATUS Output	2TTL Unit Loads
STATUS Output	12TTL Unit Loads
Clock Output	4TTL Unit Loads
ADJUSTMENT RANGES	
Gain	±12LSB
Offset	±10LSB
POWER REQUIREMENTS	+15V ±10% @ 40mA -15V ±10% @ 60mA +5V ±5% @ 250mA
POWER SUPPLY SENSITIVITY	
To ±15V Tracking Supplies	
Gain	±4.5ppm/%ΔV_S
Offset	±4.5ppm/%ΔV_S
To ±15V Non-Tracking Supplies	
Gain	±10ppm/%ΔV_S
Offset	±7ppm/%ΔV_S
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	-55°C to +85°C
PRICE (1-9)	$219

Specifications subject to change without notice.

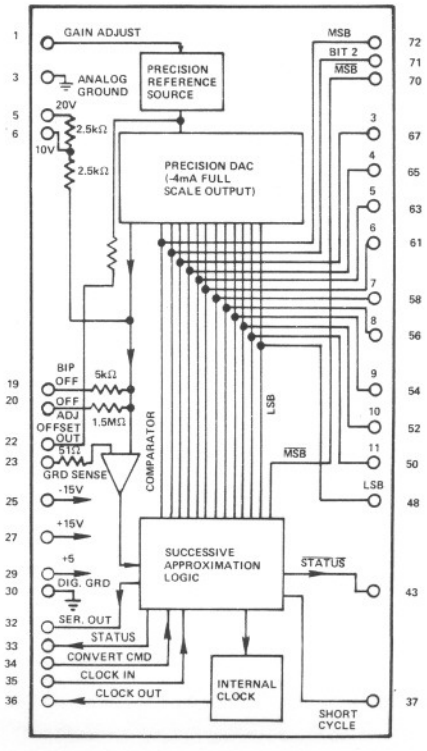
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTE:
Terminal pins installed only in shaded hole locations.
Module weight: 3.5 ounces (99.3 grams).
All pins are gold plated half-hard brass (MIL-G-45204), 0.019" ±0.001" (0.48 ±0.03mm) dia.
For plug-in mounting card order Board No. AC1546 @ $25.

BLOCK DIAGRAM AND PIN DESIGNATIONS



ANALOG INPUT CHARACTERISTICS

The input circuit of the ADC1102 is shown below in block diagram form.

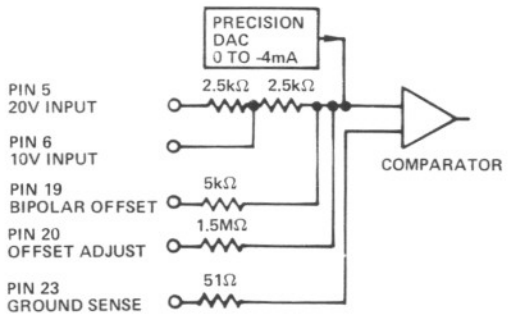


Figure 2. Input Circuit Block Diagram

When the ADC1102 is connected as a unipolar device, Pin 19 is left open circuit and, thus, no offset current is applied to the comparator input. The 0 to +10V input signal applied to Pin 6 (or the 0 to +20V input signal applied to Pin 5) develops a 0 to +4mA current which is compared to the 0 to -4mA output of the D/A converter. A voltage between +15V and -15V can be applied to Pin 20 from the wiper of a 100kΩ potentiometer to adjust the zero point by ±10LSB.

With the offset output, Pin 22, connected to Pin 19, a +2mA offset current is applied to the comparator input. The ADC1102 will then accept bipolar inputs of ±5V at Pin 6, or ±10V at Pin 5 and compare the 0 to +4mA sum of the offset and input signal currents to the 0 to -4mA D/A converter output. The offset adjustment potentiometer is once again used as described in the preceding paragraph.

Signal ground sense, Pin 23, should normally be jumpered to analog ground, Pin 3. However, in the event that there is an offset in the ground wiring, it may be possible to eliminate it by connecting Pin 23 directly to the signal or analog ground of the device feeding the analog input signal to the ADC1102. In any case, Pin 23 must not be left open.

If a high input impedance is required, it can be achieved by using a high speed operational amplifier as an input buffer. Analog Devices' model 48 fast settling amplifier, packaged in a small 1.125″ x 1.125″ x 0.4″ (28.58 x 28.58 x 10.16mm) module, is an ideal choice.

PARALLEL DATA OUTPUT

The ADC1102 produces natural Binary Coded outputs when configured as a unipolar device. As a bipolar device, it can produce either Offset Binary or Two's Complement output codes. The most significant bit is represented by Pin 72 (MSB output) for Binary and Offset Binary codes, or by Pin 70 ($\overline{\text{MSB}}$ output) for the Two's Complement code. Tables I and II illustrate the relationship between analog input and digital output for all three codes.

ANALOG INPUT		DIGITAL OUTPUT
0 to +10V Range	0 to +20V Range	Binary Code
+9.9976V	+19.9951V	111111111111
+5.0000V	+10.0000V	100000000000
+1.2500V	+2.5000V	001000000000
+0.0024V	+0.0048V	000000000001
+0.0000V	+0.0000V	000000000000

TABLE I: NOMINAL UNIPOLAR INPUT-OUTPUT RELATIONSHIPS

±5V RANGE	±10V RANGE	OFFSET BINARY CODE	TWO'S COMPLEMENT CODE
+4.9976V	+9.9951V	111111111111	011111111111
+2.5000V	+5.0000V	110000000000	010000000000
+0.0024V	+0.0048V	100000000001	000000000001
0.0000V	0.0000V	100000000000	000000000000
-5.0000V	-10.0000V	000000000000	100000000000

TABLE II: NOMINAL BIPOLAR INPUT-OUTPUT RELATIONSHIPS

SERIAL DATA OUTPUT

The serial data output, available on Pin 32, is of the non-return-to-zero format. The data is transmitted MSB first and is Binary coded for unipolar units and Offset Binary coded for bipolar units.

Figure 3, shown below, indicates one method for transmitting data serially using only three wires (plus a digital ground). The data is clocked into a receiving shift register using the delayed clock output of the ADC1102.

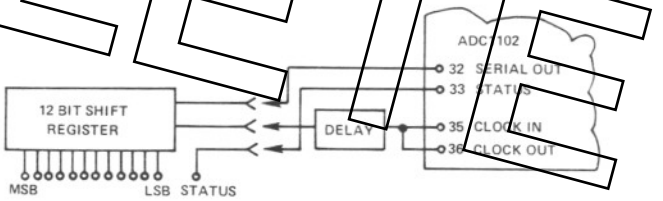


Figure 3. Serial Data Transmission

The timing diagram presented in Figure 4 shows that the converter's clock output must be delayed by an amount of time greater than or equal to the sum of the receiving shift register setup time plus the 20ns clock output to serial output delay.

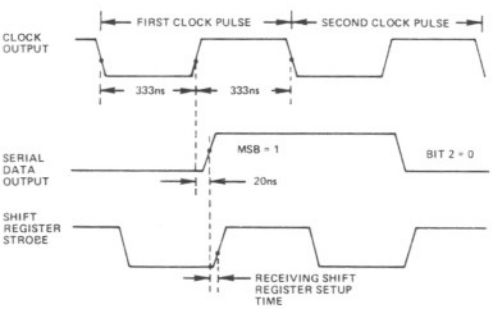


Figure 4. Serial Data Timing Diagram

The 50ns span between the time that the last serial output bit is available and the time that the STATUS output returns to zero insures that the data in the shift register will be valid on the "1" to "0" transition of the STATUS signal.

GAIN AND OFFSET ADJUSTMENTS

The potentiometers used for making gain and offset adjustments are connected as shown in Figure 5. Note that a jumper is connected between Pin 19 and Pin 22 for bipolar operation; these pins *must* be left open for unipolar operation.

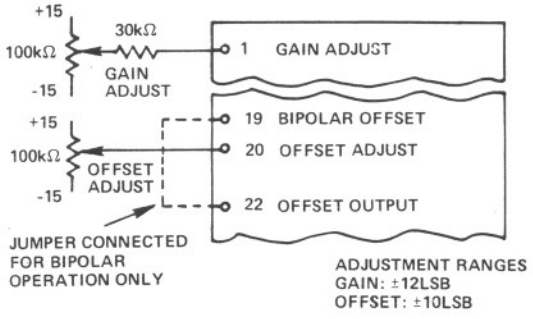


Figure 5. Adjustment Connections

Proper gain and offset calibration requires great care and the use of extremely sensitive and accurate reference instruments. The voltage standard used as a signal source must be very stable. It should be capable of being set to within 1mV of the desired value at both ends of its range.

The gain and offset calibrations will be independent of each other if the offset adjustment is made first. These adjustments are not made with zero and full scale input signals and it may be helpful to understand why. An A/D converter will produce a given digital output for a small range of input signals, the nominal width of the range being one LSB. If the input test signal is set to a value which should cause the output of the converter to be on the verge of switching from one digital value to the adjacent digital value, the unit can be calibrated so that it does change values at just that point. With a high speed convert command rate and a visual display, these adjustments can be performed in a very accurate and sensitive way. Analog Devices' Conversion Handbook gives more detailed information on testing and calibrating A/D and D/A converters.

OFFSET CALIBRATION

For 0 to +10V unipolar units set the input voltage precisely to +0.0012V; for 0 to +20V units set it to +0.0024V. Adjust the zero potentiometer until the converter is just on the verge of switching from 000000000000 to 000000000001.

For ±5V bipolar units set the input voltage precisely to -4.9988V; for ±10V units set it to -9.9976V. Adjust the zero potentiometer until Offset Binary coded units are just on the verge of switching from 000000000000 to 000000000001 and Two's Complement coded units are just on the verge of switching from 100000000000 to 100000000001.

GAIN CALIBRATION

Set the input voltage precisely to +19.9927V for 0 to +20V units, +9.9963V for 0 to +10V units, +4.9963V for ±5V units, or +9.9927V for ±10V units. Note that these values are 1½LSB's less than nominal full scale. Adjust the gain potentiometer until Binary and Offset Binary coded units are just on the verge of switching from 111111111110 to 111111111111 and Two's Complement coded units are just on the verge of switching from 011111111110 to 011111111111.

POWER SUPPLY AND GROUNDING CONNECTIONS

The ADC1102 does not have an internal connection between analog power ground and digital ground and, thus, a connection must be provided in the external circuitry. The choice of an optimum "star" point for these grounds is an important consideration in the performance of the system. No strict rules can be given, only the general guidelines that the grounding should be arranged in such a manner as to avoid ground loops and to minimize the coupling of voltage drops (on the high current carrying logic supply ground) to the sensitive analog circuit sections. One suggested approach is shown in Figure 6.

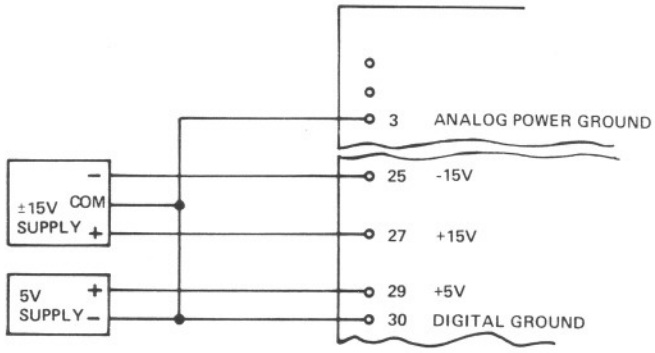


Figure 6. Power Supply and Grounding Connections

The ±15V and +5V power supplies must be externally bypassed with 10μF (or greater) capacitors. These capacitors should be connected between Pin 27 and Pin 3, between Pin 25 and Pin 3, and between Pin 29 and Pin 30. Capacitor connections should be made as close to the module pins as possible.

CLOCK CONNECTIONS

When the ADC1102 is used with its own internal clock, Pin 36 is simply jumpered to Pin 35. When the internal clock is not used, Pin 36 is grounded and an external clock capable of driving three TTL loads is connected to Pin 35. The external clock must have a frequency of 1.5MHz (±10%) and a 50 ±10% duty cycle. The convert command should be synchronized with the external clock.

REPETITIVE CONVERSIONS

When making repetitive conversions, a new convert command may be initiated any time after the "1" to "0" transition of the STATUS output. The STATUS output may not, however, be connected directly to the CONVERT COMMAND input for the purpose of automatically generating convert command pulses.

SHORT CYCLE CONNECTIONS

When the ADC1102 is operated as a 12-bit device, Pin 37 is left open. If, however, it is to perform conversions of less than 12 bits, Pin 37 is connected to the N+1 bit output (where N is the number of bits in the conversion). The conversion time in this mode of operation is 8μs x N/12.

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