ANALOG DEVICES

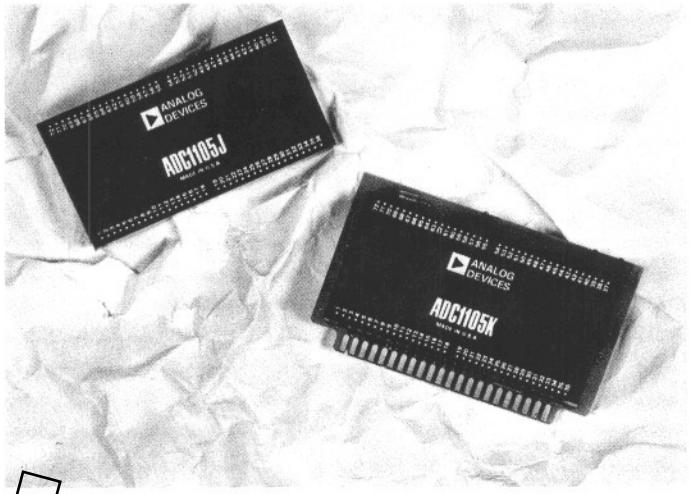
High Resolution, Dual Slope A/D Converter

ADC1105

PRELIMINARY TECHNICAL DATA

FEATURES

- Output Versatility With External Counters and Registers
- High Resolution
  - Up to 1:20,000 (ADC1105K)
  - Up to 1:2,000 (ADC1105J)
- Excellent Zero Stability
- User Choice of Input Ranges
- Accepts Unipolar or Bipolar Inputs
- Low Profile 2" x 4" x 0.6" Module
- Special Mounting Card Available
- Ratiometric Capability
- Automatic Sample Capability



GENERAL DESCRIPTION

The ADC1105 is a precision dual slope analog-to-digital converter which is designed for use with external counters and registers. With this product, the designer can build conversion systems which utilize any desired counting scheme and which have resolutions up to and including 4 BCD digits (or 14 binary bits) plus 100% overrange plus sign. This versatility is particularly useful in instrumentation applications where it is desired to have outputs scaled directly in terms of engineering or physical units (e.g. pounds and ounces).

Performance specifications for the ADC1105 include 2μV/°C zero stability, 5ppm/°C gain temperature coefficient, and ±0.0015%/%V_S power supply sensitivity. Two versions are available with accuracies of 0.01% and 0.1% of reading ±1 count respectively.

The ADC1105 is compatible with TTL/DTL as well as certain older RTL systems. It can be configured to perform conversions on command or automatically at a rate controlled by simple external circuitry. The ADC1105 also offers both a ±10V and a ±1V input range, each with 100% overrange capability.

BASIC OPERATION

As a dual slope converter, the ADC1105 produces a pulse train output, the number of pulses in which is proportional to the analog input voltage. It also provides all of the signals needed to properly control the external counters and registers. A simple parallel output analog-to-digital converter built around the ADC1105 is shown in Figure 1.

Although this represents a typical arrangement it is by no means the only one possible. Detailed timing diagrams and descriptions of terminal input/output characteristics will be presented in a later section to aid the designer in adapting the ADC1105 to his system's particular requirements.

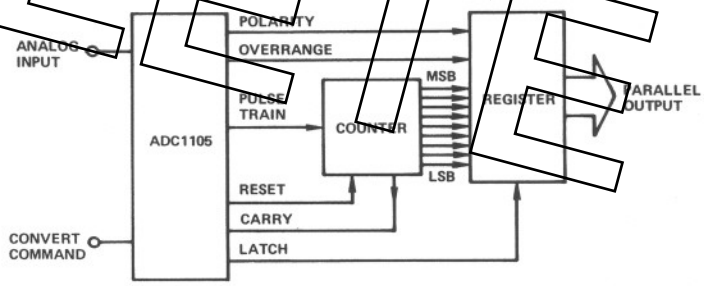


Figure 1. Basic Converter Block Diagram

The conversion cycle begins when the convert command is applied. The counter is reset to zero, input integration begins, and output pulses are generated. When the counter reaches full scale, a carry signal is sent back to the ADC1105 to initiate reference integration. When the integrator voltage returns to zero, the pulse train stops and the output register is strobed. The polarity signal is generated at the end of the input integration period; the overrange signal is generated during the reference integration period and is valid at the end of conversion.

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West Coast Tel: 213/595-1783
Mid-West Tel: 312/297-8710

SPECIFICATIONS (typical @ +25°C and nominal supply voltages, unless otherwise noted)

MODEL		ADC1105J	ADC1105K
RESOLUTION		Up to 3½BCD Digits or 10 Binary Bits Plus Sign	Up to 4½BCD Digits or 14 Binary Bits Plus Sign
RELATIVE ACCURACY		±0.1% of Reading (±1 Count)	±0.01% of Reading (±1 Count)
ANALOG INPUT RANGES[1]		±1V Full Scale ±10V Full Scale	* *
INPUT IMPEDANCE		100kΩ/Volt ±1%	*
TEMPERATURE COEFFICIENTS			
Gain[2]		±10ppm/°C max	±5ppm/°C max
Offset		±2μV/°C max; 1V Range ±20μV/°C max; 10V Range	* *
Reference		±20ppm/°C max	±5ppm/°C max
CONVERSION TIME		See Table 2	*
CONVERSION RATE		See Table 2	*
REFERENCE VOLTAGE			
Fixed Reference		±6.2V ±5%	*
Ratiometric		±20V max	*
CLOCK FREQUENCY		200kHz ±10%	*
Adjustment Range		±10kHz	*
DIGITAL INPUTS		See Page 4	*
DIGITAL OUTPUTS		See Page 4	*
POWER SUPPLY REQUIREMENTS		+5V ±5% @ 120mA +15V ±5% @ 45mA -15V ±5% @ 35mA	* * *
POWER SUPPLY SENSITIVITY		±0.0015%/%V_S	*
TEMPERATURE RANGE			
Operating		0 to +50°C	*
Storage		-25°C to +85°C	*
MTBF (CALCULATED)		70,000 Hours	*
PRICE			
ADC1105 Module	(1–9)	$159	$209
	(10–24)	$140	$186
	(25–99)	$125	$167
	(100–249)	$115	$150
ADC1105 Module			
With Mounting Card	(1–9)	$199	$249
	(10–24)	$179	$225
	(25–99)	$163	$205
	(100–249)	$151	$186

*Same as ADC1105J.

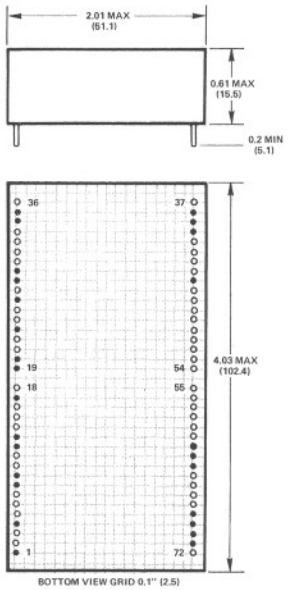
[1] Each input range has 100% overrange capability, thereby permitting inputs of ±2V and ±20V respectively.

[2] Exclusive of reference.

Specifications subject to change without notice.

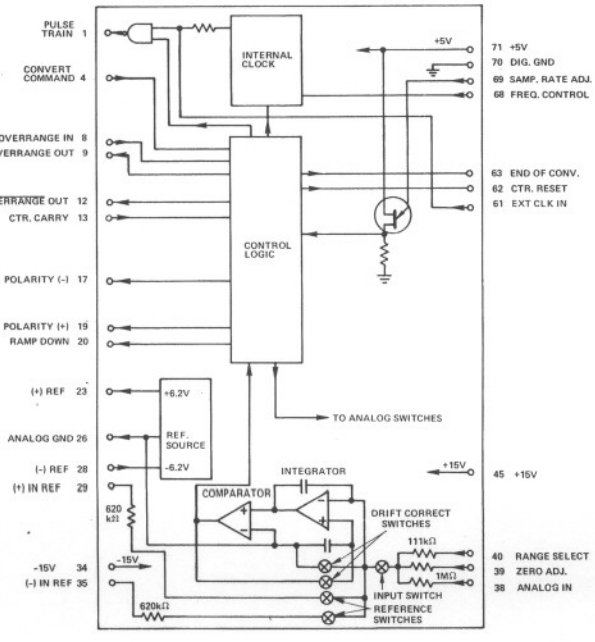
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTE:
Terminal pins installed only in shaded hole locations.
Module weight: 4 ounces (114 grams).
All pins are gold-plated half-hard brass plated per MIL-G-45204; 0.019" ±0.001" dia. (0.48mm ±0.03mm).

BLOCK DIAGRAM AND PIN DESIGNATIONS



ORDERING GUIDE:

ADC1105J	**(Module Only)**
ADC1105K	**(Module Only)**
ADC1105J/AC1547J	**(Module Mounted on Card)**
ADC1105K/AC1547K	**(Module Mounted on Card)**

CONVERSION SEQUENCE

Figures 2a and 2b below illustrate the interaction of the ADC1105's various inputs and outputs during two conversion cycles. Figure 2a shows the sequence of events for a negative polarity, overrange input of –12V while Figure 2b shows the sequence for a positive, in-range input of +8V. Both examples assume that the 10V range of the ADC1105 is selected and that a 4 digit BCD counter with a full scale count of 9999 is being used.

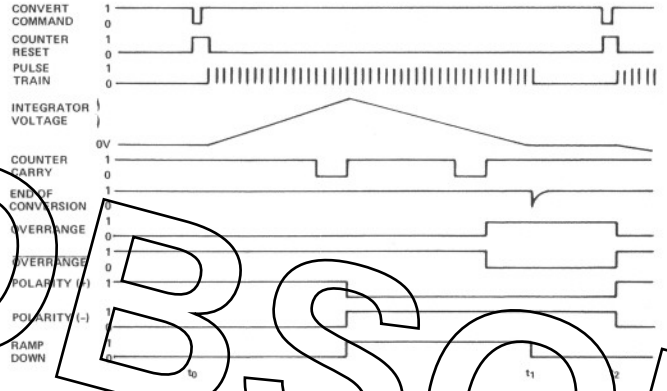


Figure 2a. Timing Diagram

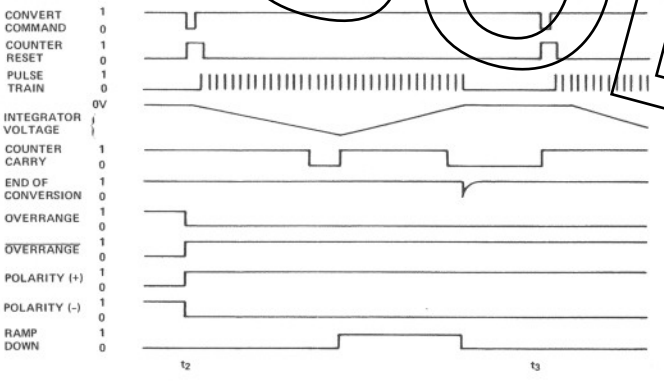


Figure 2b. Timing Diagram

At time t_0 a conversion is commanded by the "1" to "0" transition of the CONVERT COMMAND input (Pin 4). This causes a 1μs positive pulse to be generated at the COUNTER RESET terminal (Pin 62) which sets the counter to 0000. After the counter is reset, a 200kHz pulse signal is generated at the PULSE TRAIN OUTPUT terminal (Pin 1), the integrator comes out of drift correct, and input integration begins. The pulse train causes the counter to increment upwards and when the transition from 9999 to 0000 finally occurs, a "0" to "1" transition is sensed at the COUNTER CARRY INPUT terminal (Pin 13). This causes reference integration to begin. Since the input signal was negative, the POLARITY (+) output (Pin 19) goes to a "0" and the POLARITY (–) output (Pin 17) goes to a "1" at this time. The RAMP DOWN output (Pin 20) also goes to a "1" indicating that reference integration is in progress.

Because the input signal exceeds –10V, the integrator does not fully discharge before the counter reaches 9999. Therefore, when the counter goes from 9999 to 0000, a "0" to "1" transition is sensed at the OVERRANGE IN terminal (Pin 8) causing the OVERRANGE output (Pin 9) to go to a "1" and the $\overline{\text{OVERRANGE}}$ output (Pin 12) to go to a "0". At time t_1 the integrator finally discharges and a 1μs negative pulse i generated at the END OF CONVERSION output (Pin 63). T pulse train stops and the RAMP DOWN output returns to "(

At time t_2 another conversion is commanded with the analo input at +8V. The events which occur are identical to those the previous conversion except that on the "1" to "0" trans tion of the CONVERT COMMAND input, the $\overline{\text{OVERRANG}}$ and the POLARITY (+) are reset to "1" and the OVERRAN and the POLARITY (–) are reset to "0". Because the input s nal is positive, the POLARITY (+) and POLARITY (–) outp do not change state at the start of reference integration and since the integrator fully discharges before the external cour carries, the OVERRANGE and $\overline{\text{OVERRANGE}}$ do not chang state.

CONVERSION TIME

The conversion time of the ADC1105 consists principally of the input and reference integration periods. The length of th input integration period (T_{in}) depends on the clock frequenc (f_c) and the counter's full scale setting (C_{FS}) as expressed b the following equation:

$$T_{in}\ (\text{ms}) = \frac{C_{FS}}{f_c\ (\text{kHz})}$$

The following table, Table 1, lists input integration periods f various counter configurations at the nominal 200kHz clock frequency.

Counter Size	Input Integration Period
8 Bit Binary	1.28ms
10 Bit Binary	5.12ms
12 Bit Binary	20.48ms
14 Bit Binary	81.92ms
3 Digit BCD	5.00ms
4 Digit BCD	50.00ms

Table 1. Input Integration Period

Note that because of the OVERRANGE and POLARITY ou puts, the total converter resolution will be greater than the counter size. For example, a converter using an 8 bit binary counter can have a 10 bit sign-magnitude binary coded outpu

The reference integration period (T_{ref}) is related to the input integration period (T_{in}) by the following expression:

$$T_{ref}\ (\text{ms}) = T_{in} \times \frac{V_{in}}{V_{fs}}$$

V_{in} = analog input in volts

V_{fs} = 10V or 1V (depending on the range selected)

Because the 100% overrange condition represents the maxim permissible input level, the maximum reference integration period is twice the input integration period. Table 2 below lists the maximum total conversion times and resulting mini- mum conversion rates for various counter configurations at t nominal 200kHz clock frequency

Counter Size	Total Conversion Time	Conversion Ra
8 Bit Binary	3.84ms	260/sec
10 Bit Binary	15.36ms	65/sec
12 Bit Binary	61.44ms	16/sec
14 Bit Binary	245.76ms	4/sec
3 Digit BCD	15.00ms	66/sec
4 Digit BCD	150.00ms	6/sec

Table 2. Maximum Total Conversion Time and Minimum Conversion Rates

DIGITAL INPUT CHARACTERISTICS

Convert Command (Pin 4)

A "1" to "0" transition with a 2μs max fall time initiates conversion. The "0" state must be held for at least 100ns. If conversions are to be commanded by the automatic sample rate circuitry, this input must be tied to ground. 1TTL load (max).

Counter Carry (Pin 13)

A "0" to "1" transition at this terminal indicates that the external counter has reached full scale and returned to zero. The "1" state must be held for at least 30ns. 2TTL loads (max).

Overrange In (Pin 8)

A "0" to "1" transition at this terminal indicates that the external counter has reached full scale and returned to zero. It is used to determine if an overrange condition has occurred and in normal operation is jumpered to Pin 13. 2TTL loads (max).

External Clock In (Pin 61)

An external clock with a maximum frequency of 250kHz will override the internal clock when connected to this terminal. In this mode of operation the convert command must be synchronized to the 1 to 0 transition of the clock pulse. 1TTL load (max).

DIGITAL OUTPUT CHARACTERISTICS

Gated Pulse Train (Pin 1)

This is a 200kHz (nominal) positive pulse output with a 1μs pulse duration. It is capable of driving 10TTL loads (min).

Counter Reset Output (Pin 62)

This is a 1μs positive pulse which is used to reset the counter at the start of conversion. The output circuit consists of an NPN emitter-follower with a 39Ω series resistor which is capable of supplying 40mA (max). When a 270Ω resistor is connected between this pin and ground, one standard TTL load can be driven.

End of Conversion (Pin 63)

This is a 1μs negative pulse which is used to signal the end of conversion and/or strobe an external register. The output circuit consists of an NPN emitter follower with a 22Ω series resistor which is capable of supplying 40mA (max). When a 270Ω resistor is connected between this pin and ground, one standard TTL load can be driven.

Polarity (–) (Pin 17)

This output is set to a "0" each time a conversion is commanded. If the analog input signal is negative it will go to "1" at the start of reference integration and remain there until the next conversion. This output is capable of driving 8TTL loads (min).

Polarity (+) (Pin 19)

This is the complement of the signal at Pin 19. It is also capable of driving 8TTL loads (min).

Overrange (Pin 9)

This output is set to "0" each time a conversion is commanded. If an overrange condition is detected during reference integration it will go to a "1" and remain there until the next conversion. This output is capable of driving 10TTL loads (min).

Overrange (Pin 12)

This is the complement of the signal at Pin 9. It is also capable of driving 10TTL loads (min).

Ramp Down (Pin 20)

This output goes from a "0" to a "1" at the end of input integration and returns to "0" at the end of conversion. It is capable of driving 4TTL loads (min). The "1" state indicates that reference integration is in progress.

OTHER EXTERNAL CONNECTIONS

Sample Rate Control

The ADC1105 will automatically perform conversions at a rate which can be varied from 0.2 to 260 conversions per second if the external circuitry of Figure 3 is connected.

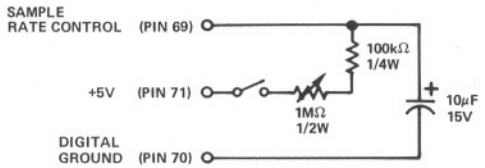


Figure 3. External Sample Rate Control Circuit

Range Selection

The nominal ±1V and ±10V input ranges will accept inputs of ±2V max and ±20V max because of their 100% overrange capability. Figure 4 shows a switching arrangement which allows selection of either input range.

Figure 4. Range Selection Circuit

Clock Frequency Adjustment

The internal clock runs at 200kHz ±10%. If the external circuitry of Figure 5 is connected, this clock frequency can be varied by as much as ±10kHz.

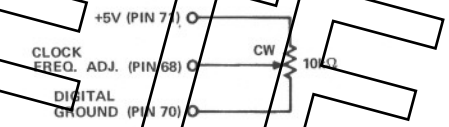


Figure 5. Clock Frequency Adjust Circuit

Zero Adjustment

The circuit of Figure 6 is used to precisely adjust the zero point. A detailed description of the adjustment procedure follows in a later section.

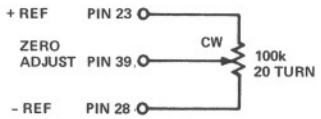


Figure 6. Zero Adjust Circuit

Gain Adjustment

The circuit of Figure 7 is used to set the +FS and –FS points once the zero point has been adjusted. A detailed description of the adjustment procedure follows in a later section.

Figure 7. Gain Adjust Circuits

External Reference Connections

As shown in Figure 8, external reference sources may be used in place of the ADC1105's internal references. These external sources must supply +6.2V ±5% @ +10μA and –6.2V ±5% @ –10μA respectively.

Figure 8. External Reference Connections

Two quadrant ratiometric operation is achieved by applying any voltage between 0 and +20V to the EXTERNAL REFERENCE SOURCE (+) input of Figure 8 while the same voltage is applied with opposite polarity to the EXTERNAL REFERENCE SOURCE (–) input. The converter's output (C_{out}) in this case is related to the analog input (V_{in}) and the magnitude of the reference signal (V_{ref}) by the following equations:

$$C_{out} = 6.2C_{FS} \times \frac{V_{in}}{V_{ref}} \text{; for the 1V range}$$

$$= 0.62C_{FS} \times \frac{V_{in}}{V_{ref}} \text{; for the 10V range}$$

Where C_{FS} is the counter's full scale count.

In no case should values of V_{in} and V_{ref} be applied which would result in a C_{out} which exceeds 2 $C_{full\ scale}$. A typical external circuit used to implement ratiometric operation is shown below in Figure 9.

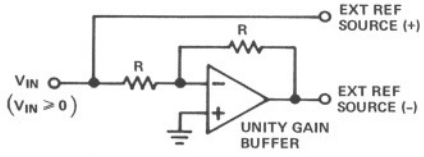


Figure 9. Additional Circuit for 2-Quadrant Ratiometric Operation

Power Supply Connections

The power supplies should be connected as shown below in Figure 10.

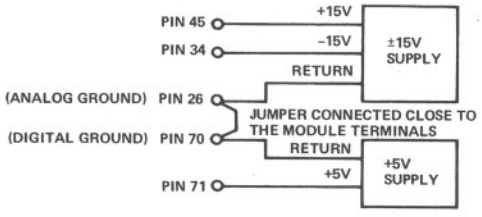


Figure 10. Power Supply Connections

Appropriate bypass capacitors have been included to reduce the effects of stray high frequency noise on the power supply busses.

THE AC1547 MOUNTING CARD

The AC1547 is an optional 4.50″ x 2.77″ printed circuit mounting card which has been specifically designed for use with the ADC1105 module. This card contains the three required adjustment potentiometers (+Gain, –Gain, and Zero), plated-through holes which are drilled out if external references are used, and a capacitor which simplifies connection of the external sample rate control circuit. When both an ADC1105 and an AC1547 are ordered, the module and card are soldered together and shipped as a single unit. Connections to the card are made with a Cinch 251-22-30-160 (or equivalent) dual 22 pin edge connector. The pin designations are listed below in Table 3.

Card Pin	Function	Module Pin	Card Pin	Function	Module Pin
1	END OF CONVERSION	63	A	POLARITY (-)	17
2	COUNTER CARRY	13	B	NC	–
3	NC	–	C	POLARITY (-)	17
4	NC	–	D	CLOCK FREQ. ADJ.	68
5	OVERRANGE IN	8	E	EXT. CLOCK IN	61
6	OVERRANGE OUT	9	F	CONVERT COMMAND	4
7	$\overline{\text{OVERRANGE}}$ OUT	12	H	RAMP DOWN	20
8	GATED PULSE TRAIN	1	J	NC	–
9	DIGITAL GROUND	70	K	DIGITAL GROUND	70
10	+5V	71	L	+5V	71
11	SAMPLE RATE CONTROL	69	M	POLARITY (+)	19
12	–15V	34	N	–15V	34
13	+15V	45	P	+15V	45
14–20	NC	–	R	COUNTER RESET	62
21	+ REF	23	S-W	NC	–
22	- REF	28	X	ANALOG INPUT	38
			Y	RANGE SELECT	40
			Z	ANALOG GROUND	26

Table 3. Pin Designations

The two plated-through holes located between the +Gain and –Gain potentiometers must be drilled out to disconnect the module's internal references if external reference sources are to be used. When this is done, the circuit of Figure 8 results, with mounting card pins 21 and 22 representing the External Reference Source (+) and External Reference Source (–) inputs respectively.

The external sample rate control circuit may be configured in several ways. If the circuit of Figure 3 is connected external to the mounting card, the sample rate can be varied from 4 conversions per minute to 86 conversions per second. If this same circuit is used but the +15V rather than the +5V supply is used, the sample rate can be varied from 0.2 to 260 conversions per second. If a fixed sample rate is desired, mounting card pin 11 is connected to the +5V supply and a 1/4W resistor is substituted for the jumper which is physically located between the zero adjust pot and the 10μF capacitor. A resistance decade box can be used to empirically determine the value of resistance needed to achieve the desired sample rate.

Figure 11 below shows the outline dimensions and layout of the AC1547 mounting card.

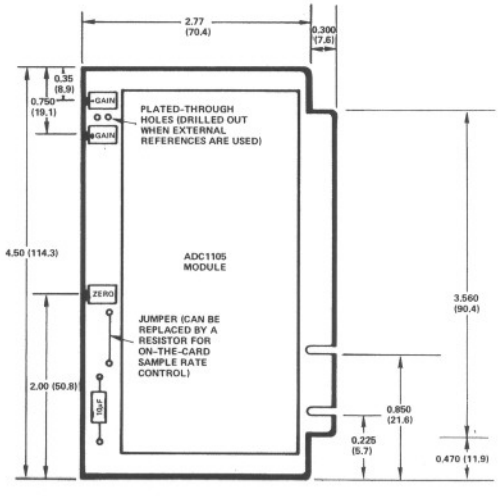


Figure 11. AC1547 Mounting Board Outline Dimensions; Dimensions Shown in Inches and (mm).

ADJUSTMENT PROCEDURE

The adjustment procedure described in this section should be carefully followed to take full advantage of the ADC1105's high degree of resolution and accuracy. The voltage standard used in this procedure must be capable of providing stable outputs with ±1/10LSD resolution and accuracy in the region of ZERO, +FULL SCALE, and –FULL SCALE.

To adjust the zero point, apply a small positive signal to the analog input (e.g., +1mV for the 1V scale of a 4½ digit BCD converter). Use the zero adjust potentiometer to increase the counter output until it just changes to the correct value. Reverse the analog input polarity and observe that the polarity output has changed and that the counter output is within one count of the previous reading. Apply small adjustments to the zero adjust potentiometer as necessary until the counter output is the same for the positive and negative inputs.

Once the zero point has been adjusted, apply a +FULL SCALE analog input. Use the +GAIN adjustment potentiometer to increase the counter output until it just changes to one count above +FULL SCALE. Reverse the analog input polarity and repeat the procedure this time using the –GAIN potentiometer.

APPLICATIONS

Several converter configurations are shown below to demonstrate the versatility of the ADC1105. Because so many different TTL counters and registers are available, each one having its own interface requirements, block diagrams rather than schematics are used.

Figure 12 below shows the ADC1105 connected as a 14-bit sign-magnitude binary coded converter. Because of the nature of sign-magnitude code, the POLARITY (+) output is equivalent to the MSB. The OVERRANGE output is used as the next least significant bit and three 4-bit binary counters are used for the remaining 12 bits. A simple flip-flop is used to indicate the status of the digital output. The CONVERT COMMAND sets the STATUS output to a "1" and the END OF CONVERSION pulse resets it to a "0". The digital output is only valid while the STATUS output is low.

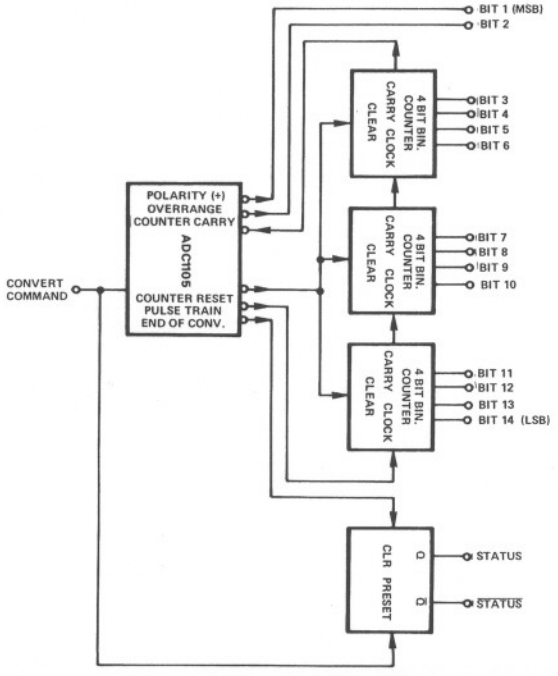


Figure 12. 14-Bit Sign-Magnitude Binary Converter

The converter of Figure 13 demonstrates how the external counter can be configured to give outputs expressed directly in engineering units. In this case the ADC1105 is used in a simple weighing system to receive analog inputs from a load cell and send latched BCD outputs (199 lbs. 15 oz. max) to a display. The 0 to 15 count which corresponds to the number of ounces is implemented with a 4-bit binary counter and a Binary-to-BCD converter. The 2½ digits corresponding to the number of pounds are generated by two decade counters and the OVERRANGE output. In this type of application the external sample rate control circuit would be used to provide automatic repetitive conversions.

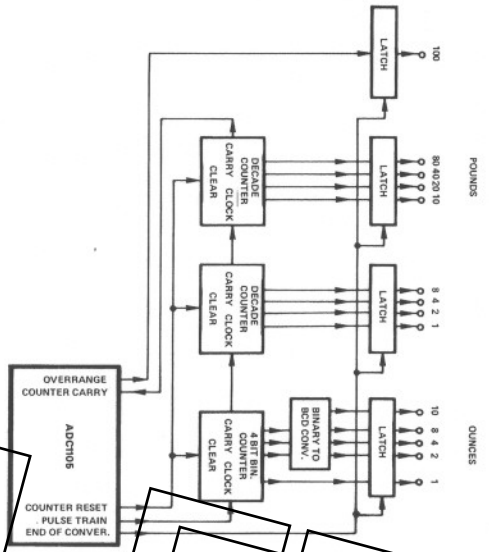


Figure 13. Simple Weighing System

Note that exclusive of polarity, the ADC1105K can resolve up to one part in 20,000 while the ADC1105J can resolve up to one part in 2000. When designing a converter which uses a specialized counting scheme, the number of possible counter states must be computed to determine which version to use. In the above example, the full scale count was 199.15 and, therefore, the number of possible states is 200 x 16 = 3200. It is clear that the ADC1105K would be the proper model to choose.