DUAL SLOPE A/D CONVERTERS
ADC-14I, ADC-17I, ADC1100

GENERAL DESCRIPTION

Dual slope integrating A/D converters perform a conversion by first integrating the input signal for a fixed period of time, and then measuring the time required to return the integrator to zero when it is integrated in the opposite direction with a fixed reference signal. A major benefit of this technique is that it results in very high rejection of normal mode noise when the signal integration time period is set equal to one cycle of the power line.

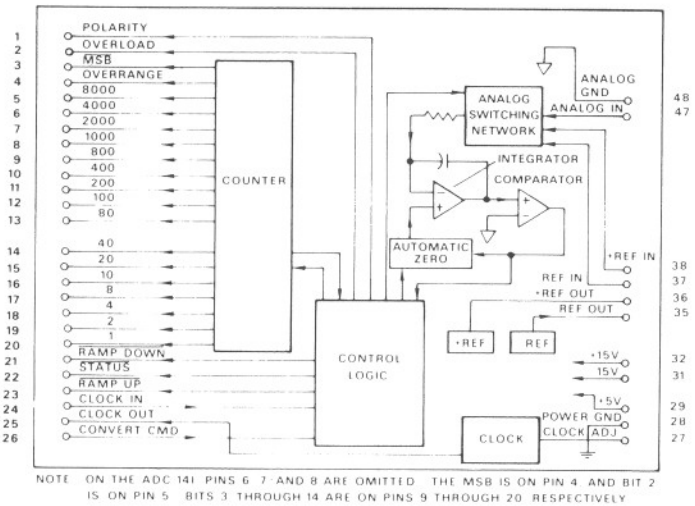
ADC-14I and ADC-17I

These two high resolution converters are identical except for output coding. The ADC-14I has 14-bit binary plus sign coding, while the ADC-17I has 4½ digits plus sign output coding. Both feature a normal mode rejection ratio of 70dB, an automatic zero correction cycle, and a gain TC of only ±10ppm/°C.

ADC1100

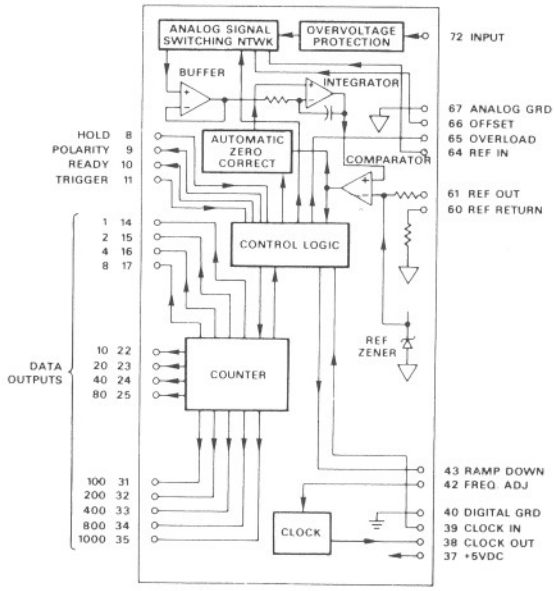
The ADC1100 is a new dual slope A/D converter in a compact 2″ x 4″ x 0.4″ module. It can be triggered externally, or internally at a rate of about 4 conversions/sec, or it can be wired to start a new conversion when the conversion in progress is completed. It is ideal for driving a display, or feeding data to a computer, or for doing both jobs simultaneously. Since it requires only +5V power, and has a normal mode noise rejection ratio of 40dB minimum, it is a natural choice for installation at transducer locations.

BLOCK DIAGRAM
ADC-14I & ADC-17I



NOTE: ON THE ADC 14I, PINS 6, 7, AND 8 ARE OMITTED. THE MSB IS ON PIN 4, AND BIT 2 IS ON PIN 5. BITS 3 THROUGH 14 ARE ON PINS 9 THROUGH 20, RESPECTIVELY.

BLOCK DIAGRAM
ADC1100

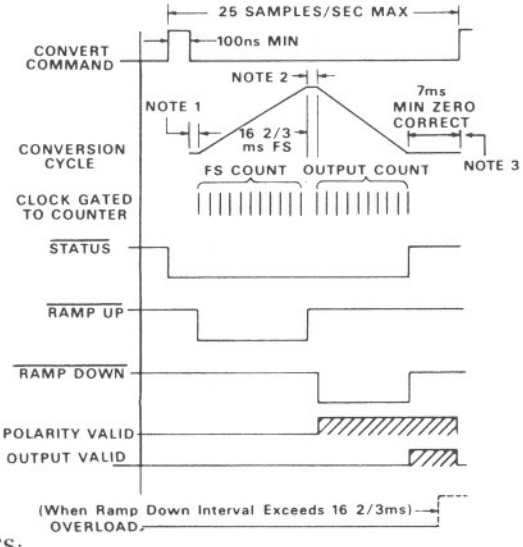


SPECIFICATION SUMMARY (Typical @ +25°C unless otherwise noted)

Model	ADC-14I	ADC-17I	ADC1100
Resolution	14 binary bits plus sign	4½ BCD digits[1] plus sign	3½ BCD digits plus sign
Linearity Error	±0.01%	*	±0.05%
Analog Input			
Range	±10V	±12V	±199.9mV
Impedance	180kΩ	*	10^8 Ω
Bias Current	N/A	*	1.5nA
Resolution	0.61mV/bit	1.0mV/bit	0.1mV/bit
Continuous Overload[2]	±100V max	*	±20V max
Normal Mode Rejection @ 60Hz[3]	70dB	*	40dB min[4]
Conversion Time	40ms max	*	42ms max[5]
Digital Control			
Inputs and Outputs	TTL/DTL Compatible	*	*
Data Outputs	TTL Positive True	*	*
Output Code	Sign plus magnitude binary	Sign plus magnitude BCD	Sign plus magnitude BCD
Temperature Coefficients			
Gain	±10ppm/°C	*	±50ppm/°C max
Offset	±10μV/°C	*	±2ppm/°C max
Power Required	+15V @ 30mA	*	+5V @ 200mA
	-15V @ 30mA	*	—
	+5V @ 200mA	*	—
Package Style	C-5	*	C-3
Package Dimensions	3" x 4" x 0.4"	*	2" x 4" x 0.4"
Price (1-9)	$259.	*	$99.
(100+)			$67.

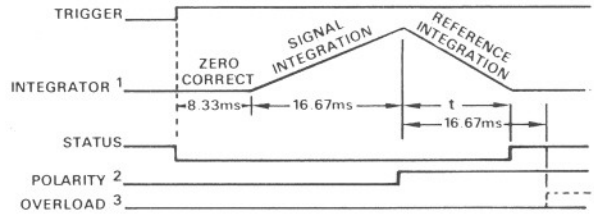
[1] Maximum digital output code is 11999, which corresponds to an input of 11.999V.
[2] Maximum overload that can be sustained indefinitely, with power on or off, without endangering the unit.
[3] Both the ADC-I and ADC1100 can be adjusted by the user to optimize the normal mode rejection of 50Hz noise, rather than 60Hz noise, if desired.
[4] The ADC1100 has provisions for connecting an external phase locked loop that can increase the normal mode noise rejection ratio to over 100dB.
[5] In the event of an overload, it can take as long as 70ms to complete a conversion.
*Specifications same as for model ADC-14I.

TIMING DIAGRAM
ADC-14I & ADC-17I



NOTES:
1. Maximum delay of one clock pulse to synchronize with clock.
2. Delay of ∿1½ clock periods to reset counter and strobe comparator for polarity data.
3. 7ms min delay for drift correction phase.

TIMING DIAGRAM
ADC1100



[1] Reference integration time $t = \frac{E_{IN}}{200mV} \times 16.67ms$. In the event of an overloaded input, $t_{max} = 50ms$.
[2] Polarity data is valid anytime after the completion of the signal integration time period.
[3] In the event of an overloaded input, the overload output will go to a logic "1" approx. 42ms after the conversion commences. However, the status output will not return to zero until the integrator has been integrated back to zero, which can be as long as 70ms after the conversion began.