DOCSIS 3.1 Power Doubler Amplifier, 45 MHz to 1218 MHz

Data Sheet **ADCA3270**

FEATURES

Drop-in replacement for RFCM3327 and RFCM3328
Total composite power: 73 dBmV
High power gain: 25 dB at 1218 MHz
Excellent linearity
Very low distortion
- **Composite triple beat: −80 dBc typical**
- **Composite second-order: −80 dBc typical**
- **Carrier to intermodulation noise: 59 dB typical**

Low noise figure: 3 dB typical at 45 MHz and 4 dB typical at 1218 MHz
Unconditionally stable
Configurable current: 350 mA to 480 mA at 24 V
Temperature monitor
9-terminal thermally enhanced chip array small outline no lead cavity [LGA_CAV]

APPLICATIONS

45 MHz to 1218 MHz community access television (CATV) infrastructure amplifier systems
Remote physical layer (PHY)
DOCSIS 3.1 compliant

GENERAL DESCRIPTION

The Analog Devices, Inc., ADCA3270 is a 24 V power doubler, monolithic microwave IC (MMIC) with 25 dB of power gain. The device achieves high RF output up to 73 dBmV composite power under 18 dB tilt conditions by using advanced circuit design techniques with gallium arsenide (GaAs), pseudomorphic high electron transistor (pHEMT), and gallium nitride (GaN) HEMT technologies. The dc current and supply voltage can be adjusted externally for optimum distortion performance vs. power consumption over a range of output levels. The ADCA3270 provides high gain, simplifying the design and manufacturing of DOCSIS 3.1 infrastructure equipment.

The ADCA3270 is packaged in a 9-terminal thermally enhanced chip array small outline no lead cavity [LGA_CAV] with an industry-standard footprint.

FUNCTIONAL BLOCK DIAGRAM

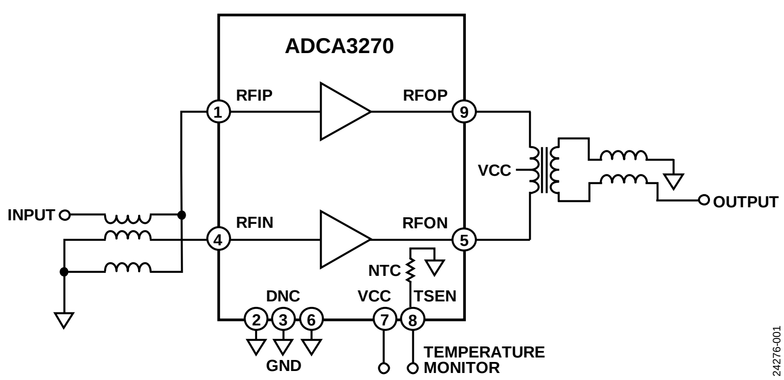

Figure 1.

Rev. 0 Document Feedback

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REVISION HISTORY

7/2021—Revision 0: Initial Version

SPECIFICATIONS

GENERAL PERFORMANCE

Supply voltage (V_{CC}) = 24 V, exposed paddle temperature (T_{PADDLE}) = 35°C, source impedance (Z_S) = load impedance (Z_L) = 75 Ω, and dc current (I_{CC}) = 480 mA, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
POWER GAIN	S21	22.0	23.6	25.0	dB	Frequency = 45 MHz, see Figure 4
		23.0	25	26.5	dB	Frequency = 1218 MHz, see Figure 4
SLOPE STRAIGHT LINE[1]			2.0		dB	Frequency = 45 MHz to 1218 MHz
FLATNESS OF FREQUENCY RESPONSE[2]			0.75		dB	Frequency = 45 MHz to 1218 MHz
REVERSE ISOLATION	S12		28		dB	Frequency = 45 MHz to 1218 MHz, see Figure 5
RETURN LOSS						See Figure 3 and Figure 6
Input	S11		−20		dB	Frequency = 45 MHz to 320 MHz
			−15		dB	Frequency = 320 MHz to 640 MHz
			−12		dB	Frequency = 640 MHz to 870 MHz
			−12		dB	Frequency = 870 MHz to 1000 MHz
			−12		dB	Frequency = 1000 MHz to 1218 MHz
Output	S22		−20		dB	Frequency = 45 MHz to 320 MHz
			−20		dB	Frequency = 320 MHz to 640 MHz
			−20		dB	Frequency = 640 MHz to 870 MHz
			−20		dB	Frequency = 870 MHz to 1000 MHz
			−18		dB	Frequency = 1000 MHz to 1218 MHz
NOISE FIGURE			3		dB	Frequency = 45 MHz
			4		dB	Frequency = 1218 MHz
SUPPLY						
Voltage	V_{CC}	18	24	26	V	Supply voltage can be adjusted for different applications, see the Applications Information section
DC Current (Total)	$I_{CC (TOTAL)}$	350	480	500	mA	Can be biased between 350 mA and 480 mA (see the Applications Information section)
RF Input Bias Voltage	V_{BIAS}		1.08		V	

[1] Slope straight line is defined as the delta between the gain at the start frequency and the gain at the stop frequency.
[2] Flatness of frequency response is defined as the delta between the gain at any frequency between the start and stop frequencies and a straight line reference drawn between the gain at the start frequency and the gain at the stop frequency.

DISTORTION DATA (ALL DIGITAL CHANNEL PLAN)

V_{CC} = 24 V, T_{PADDLE} = 35°C, and Z_S = Z_L = 75 Ω, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
TOTAL COMPOSITE POWER	TCP		73		dBmV	18 dB tilt, 190 digital (256 QAMs) channels from 57 MHz to 1215 MHz
			73		dBmV	9 dB tilt, 190 digital (256 QAMs) channels from 57 MHz to 1215 MHz
ERROR RATES						
Modulation Error Rate	MER		47		dB	
Bit Error Rate	BER		$<1 \times 10^{-10}$			PostViterbi, 18 dB tilt, 190 digital (256 QAMs) channels from 57 MHz to 1215 MHz
			$<1 \times 10^{-9}$			PreViterbi, 9 dB tilt, 190 digital (256 QAMs) channels from 57 MHz to 1215 MHz

DISTORTION DATA (MIXED SIGNAL CHANNEL PLAN)

V_{CC} = 24 V, T_{FLANGE} = 35°C, and Z_S = Z_L = 75 Ω, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DISTORTION						TCP = 72.4 dBmV, the analog and digital channel plan consists of 18 dB extrapolated tilt, 79 continuous wave channels plus 111 digital channels, a National Television System Committee (NTSC) frequency raster range of 55.25 MHz to 547.25 MHz, and −6 dB offset
Composite Triple Beat	CTB		−80		dBc	Defined by the National Cable and Telecommunications Association (NCTA)
Composite Second-Order	CSO		−80		dBc	Defined by NCTA
Carrier to Intermodulation Noise			59		dB	Defined by American National Standard/Society of Cable Telecommunications Engineers (ANSI/SCTE) 17 (test procedure for carrier to noise)

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
V_{CC}	
DC Supply over Voltage (5 minute)	30 V
RF Input Voltage (RF_{INPUT}), Single Tone	75 dBmV
Temperature	
Operating Range, T_{PADDLE}	−30°C to +110°C
Peak Reflow (Moisture Sensitivity Level (MSL) 3	260°C
Junction (T_J) to Maintain 1 Million Hour Mean Time to Failure (MTTF)	170°C
Nominal Junction (T_J)	
T_{PADDLE} = 110°C, I_{CC} = 480 mA, V_{CC} = 24 V	144°C
Storage (T_S) Range	−40°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the thermal resistance from the operating portion of the PHEMT device to the outside surface of the package closest to the device mounting area (the exposed paddle on the bottom of the case). See the Thermal Considerations section for additional information.

Table 5. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
CE-9-2	2.9	°C/W

[1] Thermal resistance (θ_{JC}) is defined as between the T_{PADDLE} and the internal device junction (T_J).

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADCA3270

Table 6. ADCA3270, 6-Terminal LGA_CAV

ESD Model	Withstand Threshold (V)	Class
HBM	500	Class 1B, passed

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

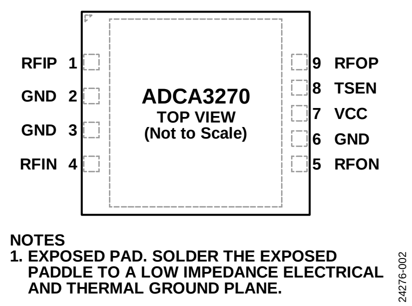

Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4	RFIP, RFIN	RF Differential Inputs.
2, 3, 6	GND	Ground.
5, 9	RFON, RFOP	RF Differential Outputs.
7	VCC	Positive Supply Voltage, 24 V Typical.
8	TSEN	Temperature Sensing Pin.
		Exposed Pad. Solder the exposed paddle to a low impedance electrical and thermal ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 24 V, T_{PADDLE} = 35°C, and Z_S = Z_L = 75 Ω, unless otherwise noted.

S-PARAMETERS

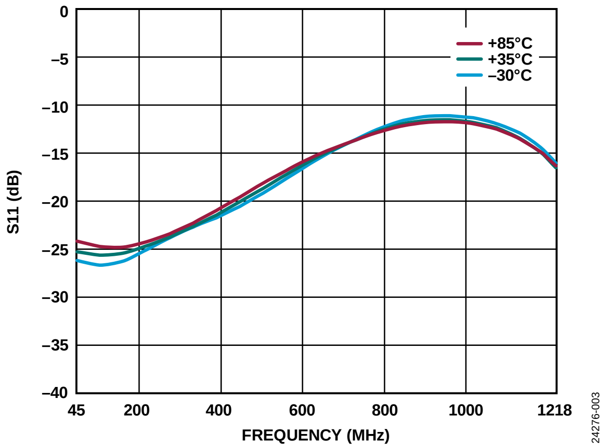

Figure 3. S11 vs. Frequency at Various Temperatures

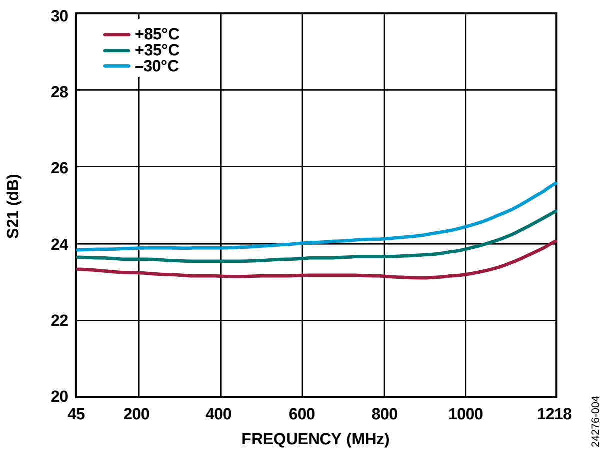

Figure 4. S21 vs. Frequency at Various Temperatures

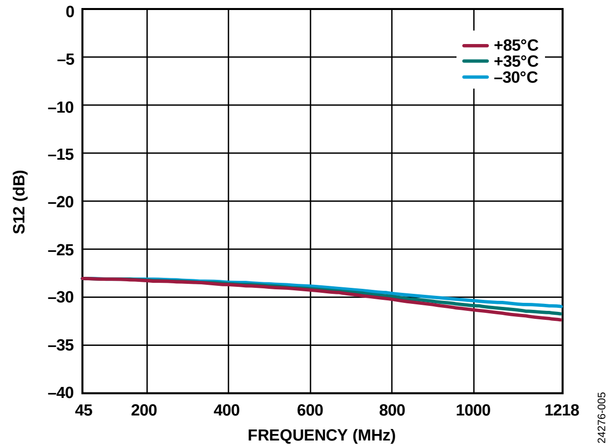

Figure 5. S12 vs. Frequency at Various Temperatures

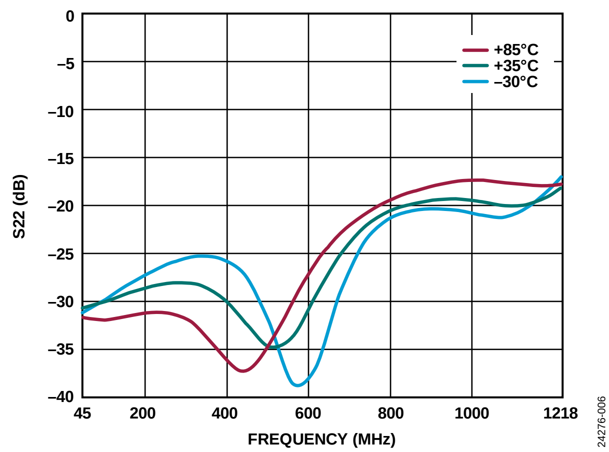

Figure 6. S22 vs. Frequency at Various Temperatures

9 dB TILT PERFORMANCE

9 dB extrapolated tilt and 190 digital channels (QAM256, ITU-T J.83, Annex B).

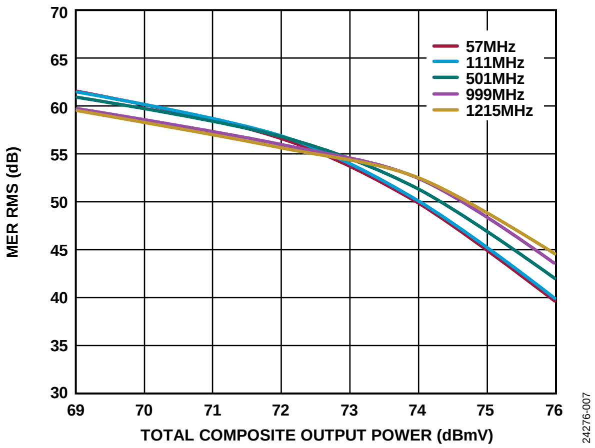

Figure 7. MER RMS vs. Total Composite Output Power at Various Frequencies, 35°C, 9 dB Tilt

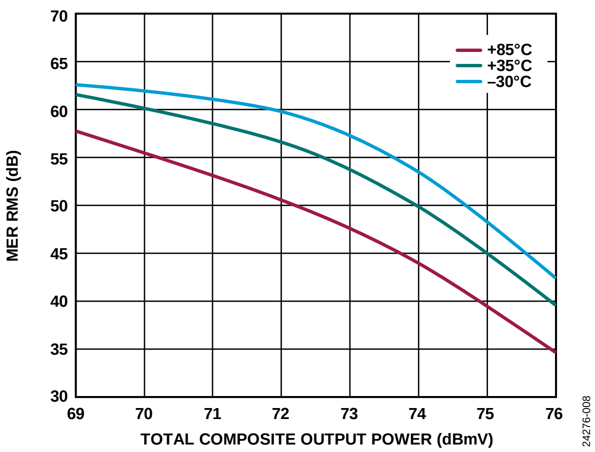

Figure 8. MER RMS vs. Total Composite Output Power at Various Temperatures, 57 MHz, 9 dB Tilt

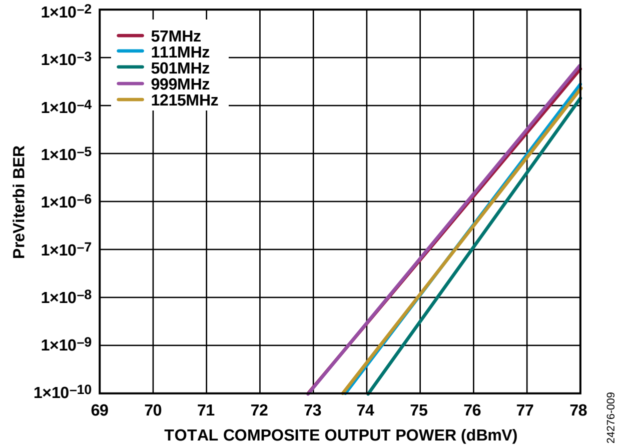

Figure 9. PreViterbi BER vs. Total Composite Output Power at Various Frequencies, 35°C, 9 dB Tilt

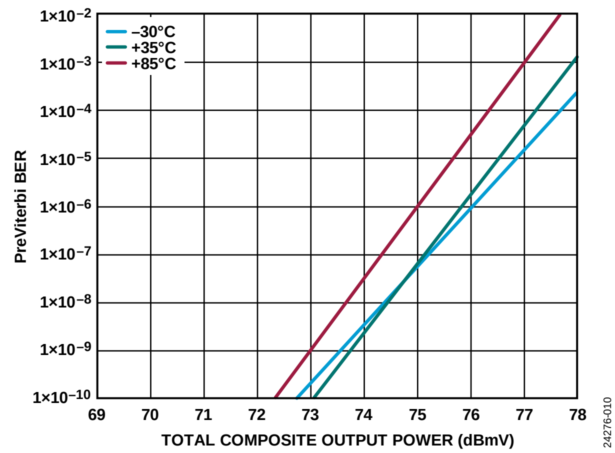

Figure 10. PreViterbi BER vs. Total Composite Output Power at Various Temperatures, 57 MHz, 9 dB Tilt

18 dB TILT PERFORMANCE

18 dB extrapolated tilt and 190 digital channels (QAM256, ITU-T J.83, Annex B).

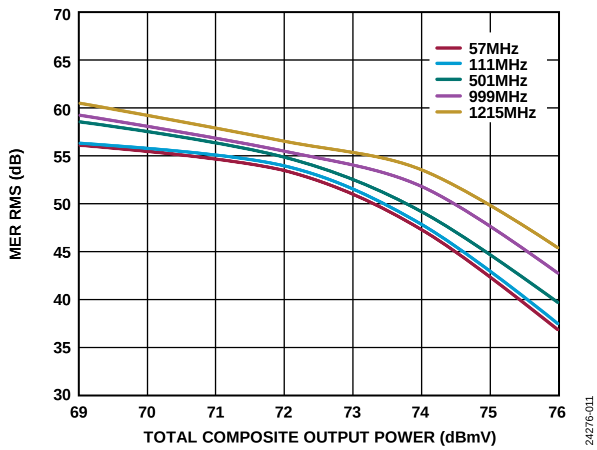

Figure 11. MER RMS vs. Total Composite Output Power at Various Frequencies, 35°C, 18 dB Tilt

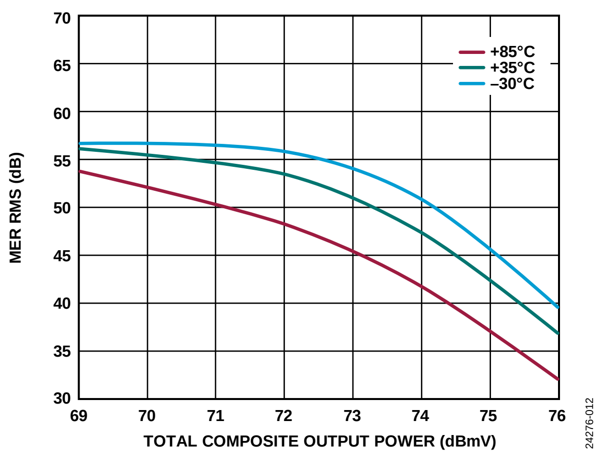

Figure 12. MER RMS vs. Total Composite Output Power at Various Temperatures, 57 MHz, 18 dB Tilt

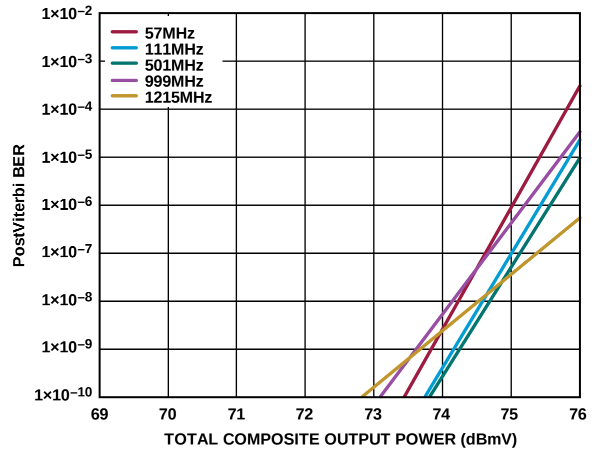

Figure 13. PostViterbi BER vs. Total Composite Output Power at Various Frequencies, 35°C, 18 dB Tilt

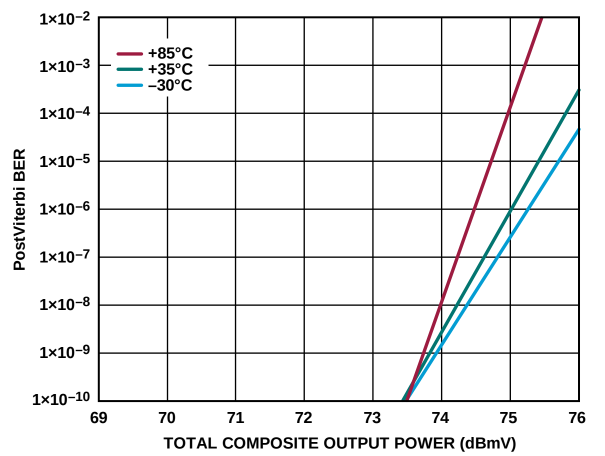

Figure 14. PostViterbi BER vs. Total Composite Output Power at Various Temperatures, 57 MHz, 18 dB Tilt

THEORY OF OPERATION

The ADCA3270 is a balanced amplifier packaged in a LGA_CAV. The application circuit interfaces the ADCA3270 to a 75 Ω input and output matched impedance consistent with a matched module designed for CATV applications. The ADCA3270 uses cascode field effect transistor (FET) feedback amplifiers in a Class A push pull configuration. The bottom half of the cascode stages are implemented in a single die, linear FET process that minimizes parasitics, thereby enabling higher gain. The top devices in the cascodes are implemented using a linear GaN process that is able to swing high RF voltages. The frequency of operation is from 45 MHz to 1218 MHz.

The ADCA3270 is unconditionally stable for robust operation in systems targeting DOCSIS 3.1 and legacy DOCSIS standards.

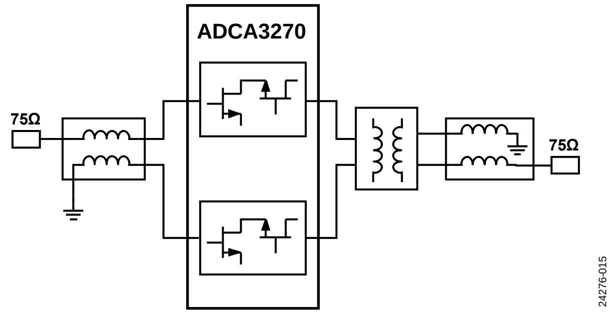

Figure 15. Simplified Schematic

APPLICATIONS INFORMATION

ADCA3270 TEMPERATURE SENSE MONITOR

The ADCA3270 has an internally mounted, negative temperature coefficient (NTC) thermistor that, when used as the bottom of a resistive voltage divider, provides an output voltage that is correlated to the ground temperature at the T_{PADDLE} of the LGA_CAV package. When configured as shown in Figure 16, the typical relationship between V_{TSEN} and T_{PADDLE} results in what is shown in Figure 17.

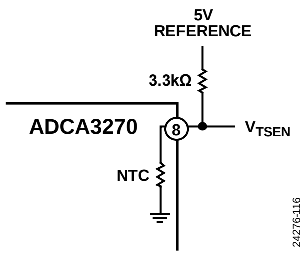

Figure 16. Recommended NTC Configuration

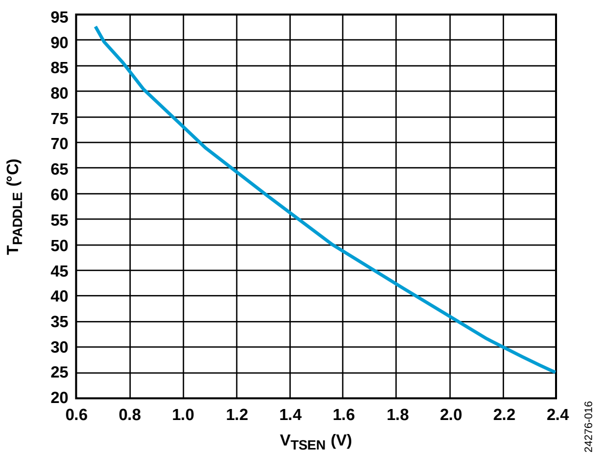

Figure 17. T_{PADDLE} vs. V_{TSEN}

THERMAL CONSIDERATIONS

The ADCA3270 is packaged in a thermally efficient, 9-terminal chip array small outline no lead cavity [LGA_CAV]. The thermal resistance from θ_{JC} is 2.9°C/W, where the case is defined by the exposed paddle on the bottom of the package. For the best thermal performance, it is recommended that as many thermal vias as possible be added under the exposed paddle of the LGA_CAV package. For optimal performance, it is recommended that these vias be filled with a paste that has high thermal conductivity. It is also recommended that the array of vias under the ADCA3270 interface to an external heat sink such as a pedestal on the system chassis.

SOLDERING INFORMATION AND RECOMMENDED PCB LAND PATTERN

Figure 18 shows the recommended land pattern for the ADCA3270. To minimize thermal impedance, the exposed paddle on the 9.00 mm × 8.00 mm LGA_CAV is soldered to a ground plane along with Pin 2, Pin 3, and Pin 6. To improve thermal dissipation, 188 thermal vias are arranged in an array under the exposed paddle. The array consists of alternating rows of 13 vias and 12 vias, maximizing the number of vias within the area. The area under the paddle is also tied to ground on the bottom layer of the PCB. If multiple ground layers exist, tie these layers together by the vias. The external layer of the PCB must be a minimum of 2 oz. copper. The minimum average plated hole wall thickness of the vias must not be less than 0.001 inch, and it is recommended that the vias be filled with a conductive paste, such as Tatsuta AE3030, and plated over. The full recommended PCB footprint design is shown in Figure 19.

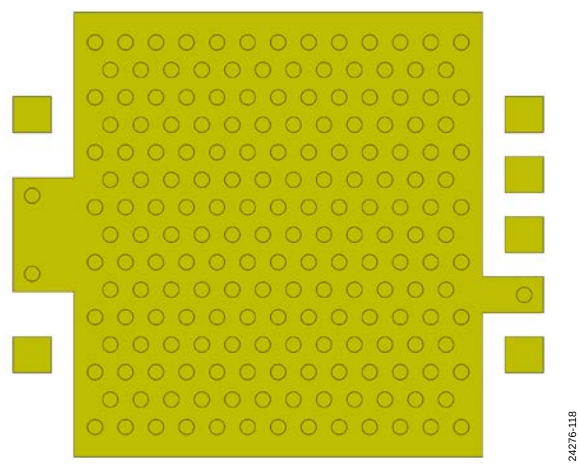

Figure 18. Recommended Land Pattern

For further information on optimizing the thermal performance while using the ADCA3270, refer to the AN-1604 Application Note, *Thermal Management Calculations for RF Amplifiers in LFCSP and Flange Packages*.

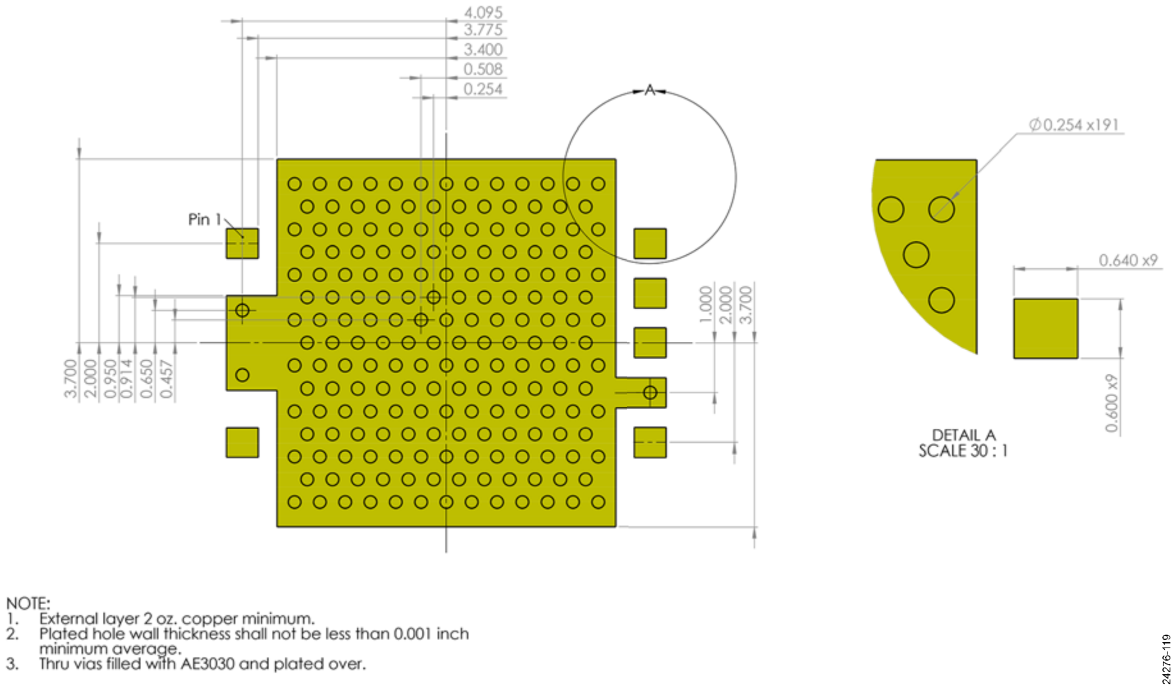

Figure 19. Recommended PCB Layout (Dimensions Shown in Millimeters)

ADCA3270 BIAS CURRENT

The ADCA3270 employs a versatile circuit design, allowing system designers to configure the supply voltage at the VCC connection (Pin 7) and the bias control voltage (V_{BIAS}) at the RFIP (Pin 1) and RFIN (Pin 4) connections to optimize the power dissipation in any given application. It is recommended that the I_{CC} be controlled by employing a precision 5 V reference and a resistor divider (R1 and R2) to set I_{CC} as illustrated in Figure 20. The voltage is connected to each input through a ferrite bead (FB1 and FB2). The dc output of the balun used to feed the RF into the power amplifier must be blocked using a capacitor.

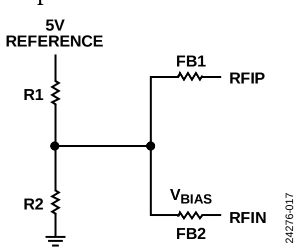

Figure 20. Setting the Bias Control Voltage

Figure 21 provides the typical transfer function of I_{CC} to V_{BIAS}, which allows the user to adjust I_{CC} from 380 mA to 480 mA.

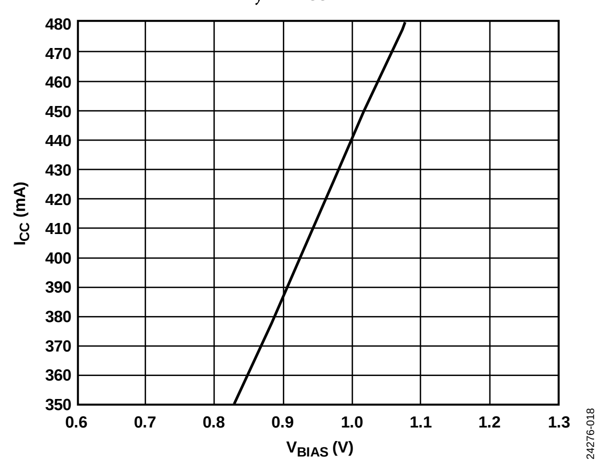

Figure 21. I_{CC} vs. V_{BIAS}

Figure 22 and Figure 23 illustrates the MER performance trade-off for different supply voltage configurations. Figure 24 and Figure 25 illustrates the modulation error ratio performance trade-off for different bias current configurations.

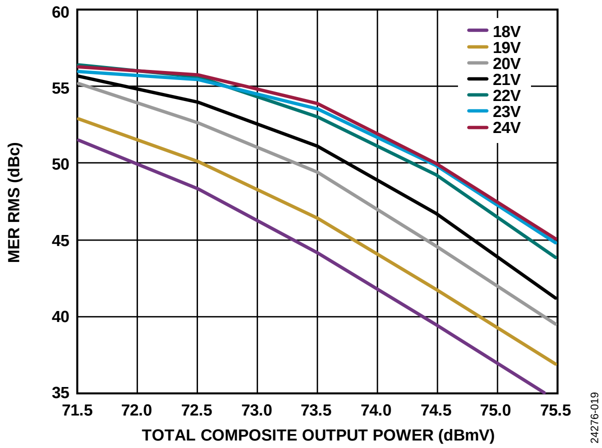

Figure 22. MER RMS vs. Total Composite Output Power, I_{CC} = 475 mA, V_{CC} = 18 V to 24 V, 1 V Steps, 9 dB Tilt

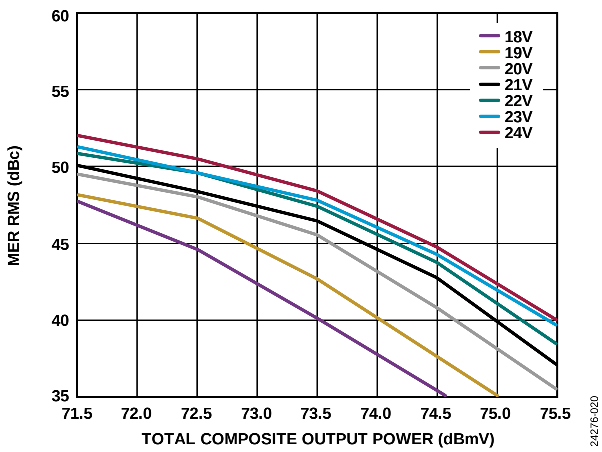

Figure 23. MER RMS vs. Total Composite Output Power, I_{CC} = 475 mA, V_{CC} = 18 V to 24 V, 1 V Steps, 22 dB Tilt

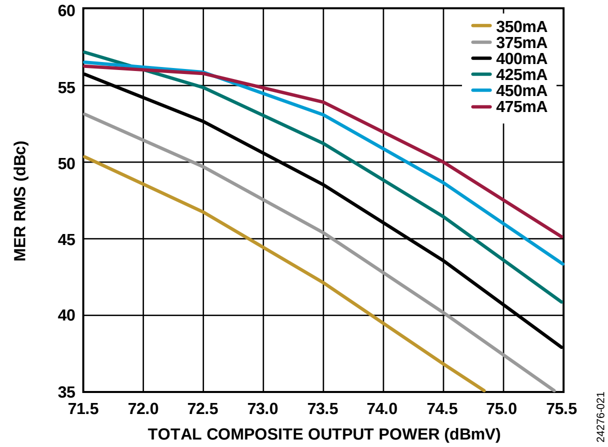

Figure 24. MER RMS vs. Total Composite Output Power, V_{CC} = 24 V, 25 mA Steps from 350 mA to 475 mA, 9 dB Tilt

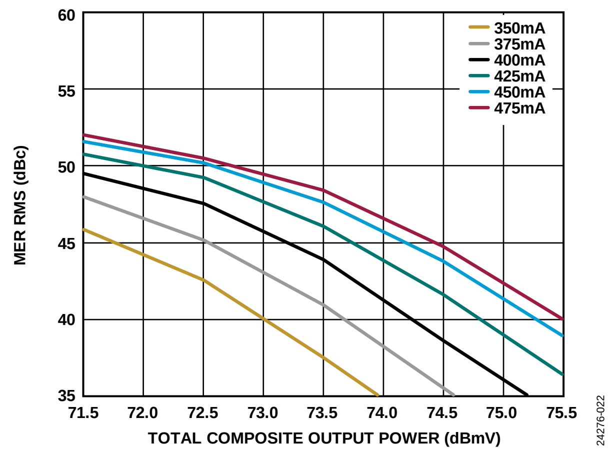

Figure 25. MER RMS vs. Total Composite Output Power, V_{CC} = 24 V, 25 mA Steps from 350 mA to 475 mA, 22 dB Tilt

OUTLINE DIMENSIONS

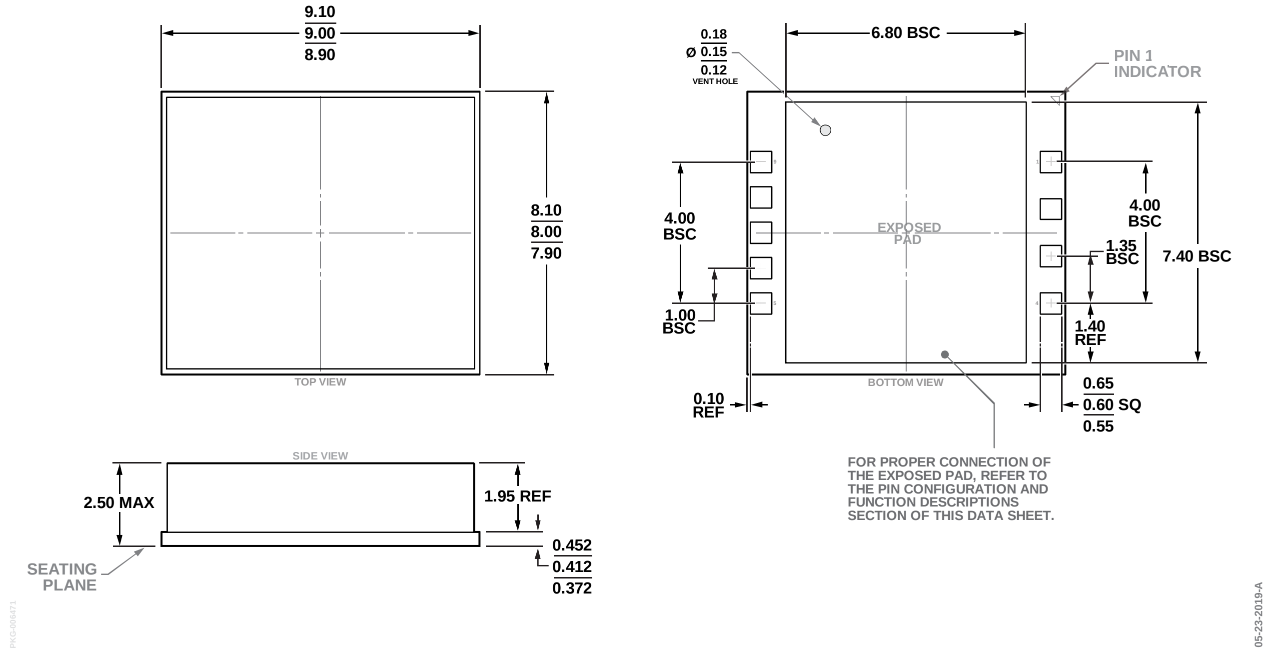

Figure 26. 9-Terminal Chip Array Small Outline No Lead Cavity [LGA_CAV]
9.00 mm × 8.00 mm Body and 2.50 mm Package Height
(CE-9-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADCA3270ACEZ	−30°C to +110°C	9-Terminal Chip Array Small Outline No Lead Cavity [LGA_CAV]	CE-9-2
ADCA3270ACEZ-R7	−30°C to +110°C	9-Terminal Chip Array Small Outline No Lead Cavity [LGA_CAV]	CE-9-2
ADCA3270-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

D24276-7/21(0)