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Clock Distribution Circuit with Pin-Programmable Output Frequency, Output Logic Levels, and Fanout

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards
   AD9552 Evaluation Board (AD9552-PCBZ)
   ADCLK854 Evaluation Board (ADCLK854-PCBZ)
Design and Integration Files
   Schematics, Layout Files, Bill of Materials
   Software

CIRCUIT FUNCTION AND BENEFITS

The AD9552 oscillator frequency upconverter and ADCLK854 LVDS/CMOS clock fanout buffer together create a flexible clock distribution solution that is pin-programmable. The AD9552 is equipped with an SPI port to program the device. This interface enables a wide output frequency range up to 900 MHz. However, it is also pin-programmable which simplifies use in many designs that do not require software programmability.

In the pin-programmable mode, there are up to 64 standard output frequencies available, based on the input frequency selection. The AD9552, therefore, functions like a frequency pin-programmable VCXO. The AD9552 is also equipped to operate from a crystal resonator at the input for additional flexibility. A simplified block diagram of the AD9552 is shown in Figure 1, and a simplified block diagram of the ADCLK854 is shown in Figure 2.
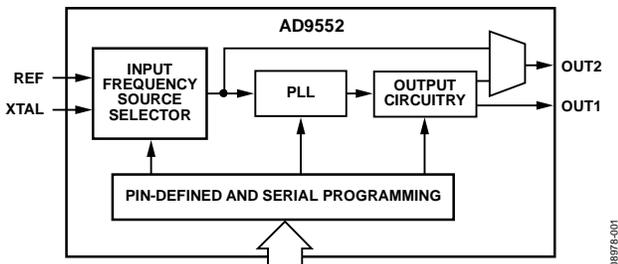

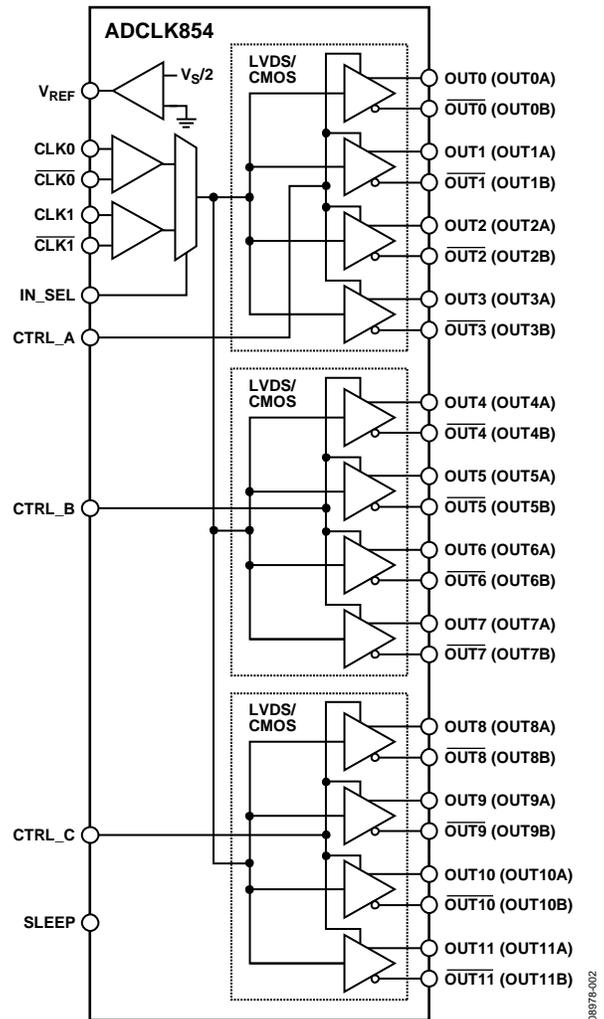Figure 1. Simplified Block Diagram of AD9552 Oscillator Frequency Upconverter

Figure 2. Simplified Block Diagram of ADCLK854 Clock Fanout Buffer

The ADCLK854 is a clock fanout buffer and is pin-programmable for both LVDS and 1.8 V CMOS outputs. The ADCLK854 has up to 12 LVDS outputs, 24 CMOS outputs, or combinations of both. The ADCLK854 could be replaced with several other clock fanout clock buffers available from Analog Devices with fewer outputs and/or different output logic choices.

CIRCUIT DESCRIPTION

Table 1. Devices Connected/Referenced

Product	Description
AD9552	Oscillator frequency upconverter
ADCLK854	LVDS/CMOS clock fanout buffer

The simplified circuit in Figure 3 displays the setup between the AD9552 and the ADCLK854 customer evaluation boards. The AD9552 is setup to run off a 26 MHz crystal resonator. The AD9552 LVPECL output then drives the ADCLK854 evaluation board for LVDS and/or CMOS fanout capability. The LVPECL output is selected for its low jitter and phase noise.

Using the AD9552 and ADCLK854 together is a natural fit for low jitter clock distribution. The pin-programmability feature of both parts enables a stand-alone clock generator solution that avoids interface control lines back to an FPGA or microcontroller. In addition, both of these parts make for a small footprint. The simplified circuit bock diagram is shown in Figure 3. Details of the internal connections and bill of materials can be found in the individual AD9552 Evaluation Board and the ADCLK854 Evaluation Board documentation.
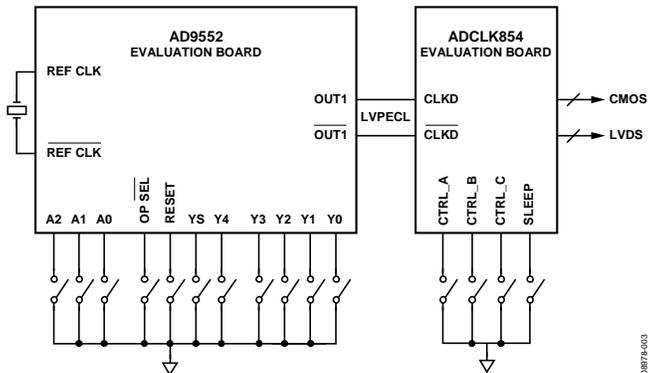

Figure 3. Simplified Diagram of AD9552 and ADCLK854 Circuit Combination

The following procedure explains how the AD9552 evaluation board can be manually programmed by using on-board jumpers and dip switches to set the logic levels for the input and output frequency selection. In this example, the crystal frequency is 26 MHz, and the output frequency is 625 MHz.

1. Ensure that Jumper JMP3 is positioned for manual control.
2. Verify that all five jumpers are removed on Connector P2.
3. Set the positions of the S3 dip switches to 0111 to indicate a 26 MHz crystal is being used.
4. Set the positions of the S2 dip switches to 0010 and the positions of the S1 dip switches to 0011.
5. Connect an oscilloscope, spectrum analyzer, or other lab equipment to any of the J3 to J6 SMA connectors on the upper right side of the board.
6. Power the evaluation board by plugging it into the USB port.
7. A frequency of 625 MHz must be observed on the OUT1 SMA connector.
8. If another output frequency is desired, remove the USB port. Then change the dip switch settings and reapply the USB port connection.

After each dip switch setting, the AD9552 must be powered down by removing the USB cable to reprogram the AD9552. See the AD9552 data sheet for a detailed explanation of pin programming.

The ADCLK854 outputs are pin-programmable up to 12 differential LVDS outputs or 24 single-ended 1.8 V CMOS outputs. The CTRL_A, CTRL_B, CTRL_C, and SLEEP jumpers are used to configure the outputs. See Table 2 to configure the outputs to the desired setting.

Table 2. ADCLK854 Configuration

Jumper	Setting	Outputs
CTRL_A	Logic 0 = LVDS; Logic 1 = CMOS	Output 0 to Output 3
CTRL_B	Logic 0 = LVDS; Logic 1 = CMOS	Output 4 to Output 7
CTRL_C	Logic 0 = LVDS; Logic 1 = CMOS	Output 8 to Output 11
SLEEP	Logic 0 = LVDS; Logic 1 = CMOS	Output 0 to Output 11

The absolute phase noise and spectrum plot shown in Figure 4 and Figure 5 are from the LVDS output of the ADCLK854 clock fanout buffer.

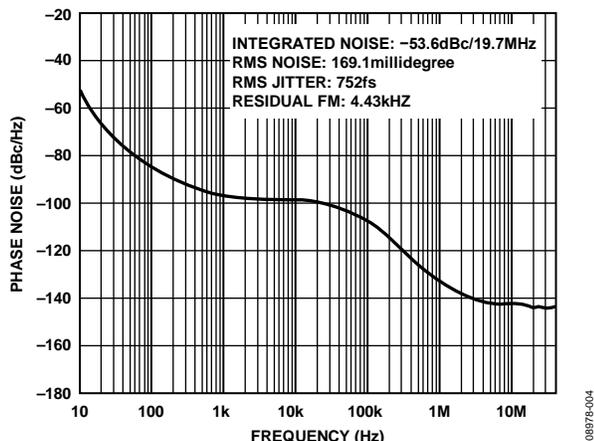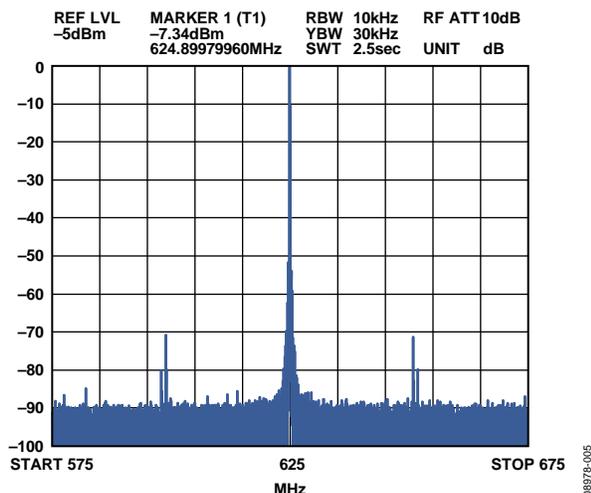*Figure 4. ADCLK854 LVDS Output Phase Noise at 625 MHz (Spurious = Off)*

Figure 5. ADCLK854 Output Spectrum Using the ADCLK854 Evaluation Board (LVDS Outputs)

A complete design support package for this circuit note can be found at www.analog.com/CN0152-DesignSupport.

COMMON VARIATIONS

Analog Devices offers a variety of clock distribution chips and clock buffers. Refer to www.analog.com/clock for more information.

CIRCUIT EVALUATION AND TEST

This circuit note describes how to operate the AD9552 as a pin-programmable device requiring no software support.

Equipment Needed

A 1.8 V at 400 mA supply for the ADCLK854 evaluation board and a 3.3V at 300 mA supply for AD9552 evaluation board are required. If the software programmable features of the AD9552 are used, connect a PC to the AD9552 evaluation board using a USB cable, and the USB 5 V can be used to supply power to the AD9552 board. For this circuit note, USB power is used, although the software programmable features of the AD9552 are not exercised.

In addition, a high quality spectrum analyzer is required to measure the phase noise and spectral output results described in this circuit note.

Getting Started

Connect the power supplies to the evaluation boards. Then connect the differential LVPECL outputs of the AD9552 board, J3 and J4, to the CLK0 and CLK0B inputs of the ADCLK854 board. The recommended setup for the ADCLK854 evaluation board is shown in Figure 2 of UG-070. The supply voltage is set to 1.8 V. The IN_SEL jumper provides the desired input configuration. Logic 0 on the IN_SEL pin selects the CLK0 and CLK0B inputs, and Logic 1 on the IN_SEL pin selects the CLK1 and CLK1B inputs. On the ADCLK854 evaluation board, the CLK0 and CLK0B inputs are set up for ac-coupled, differential inputs. This input configuration requires the user to provide the appropriate ac swing to both inputs. For this circuit note, the CLK0 and CLK0B inputs are used for the lowest jitter.

CLK1 is set up to evaluate the ADCLK854 with a single-ended source via the balun on the evaluation board. This input is not used in this circuit note.

Functional Block Diagram

A functional diagram of the basic setup is shown in Figure 3 of this circuit note, with the exception of the external power supplies and the spectrum analyzer. UG-070 shows the configuration for the ADCLK854 evaluation board.

Setup and Test

After connecting the boards and applying power as described above, this circuit note describes how to manually program the AD9552 using the jumpers and dip switches. The output signal from the ADCLK854 can then be examined using an oscilloscope or a spectrum analyzer.

LEARN MORE

CN0152 Design Support Package:
http://www.analog.com/CN0152-DesignSupport

AN-1051 Application Note, *Reference Design for the AD9553 Oscillator Frequency Up Converter*, Analog Devices.

AN-0988 Application Note, *The AD9552: A Programmable Crystal Oscillator for Network Clocking Applications*, Analog Devices.

Kester, Walt. 2005. *The Data Conversion Handbook.* Chapters 6 and 7. Analog Devices.

Kester, Walt. 2006. *High Speed System Applications.* Chapter 2, "Optimizing Data Converter Interfaces." Analog Devices.

Kester, Walt. 2006. *High Speed System Applications.* Chapter 3, "DACs, DDSs, PLLs, and Clock Distribution." Analog Devices.

MT-007 Tutorial, *Aperture Time, Aperture Jitter, Aperture Delay Time—Removing the Confusion*, Analog Devices.

MT-008 Tutorial, *Converting Oscillator Phase Noise to Time Jitter.* Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of AGND and DGND.* Analog Devices.

MT-085 Tutorial, *Fundamentals of Direct Digital Synthesis (DDS).* Analog Devices.

MT-086 Tutorial, *Fundamentals of Phase Locked Loops (PLL).* Analog Devices.

MT-101 Tutorial, *Decoupling Techniques.* Analog Devices.

Data Sheets and Evaluation Boards

AD9552 Data Sheet

AD9552 Evaluation Board

ADCLK854 Data Sheet

ADCLK854 Evaluation Board

REVISION HISTORY

4/13—Rev. A to Rev. B
Document Title Changed from CN-0152 to AN-1217 .... Universal

11/10—Rev. 0 to Rev. A
Added Evaluation and Design Support Section 1
Changes to Circuit Description Section 2
Added Circuit Evaluation and Test Section 3

4/10—Revision 0: Initial Version

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