ANALOG DEVICES

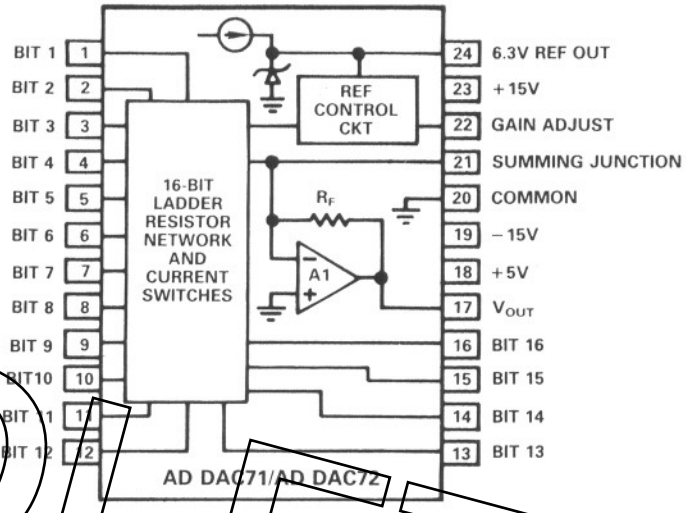
High Resolution 16-Bit D/A Converters

AD DAC71/AD DAC72*

FEATURES

16-Bit Resolution
±0.003% Maximum Nonlinearity
Low Gain Drift ±7ppm/°C
0 to +70°C Operation (AD DAC71, AD DAC71H, AD DAC72C)
−25°C to +85°C Operation (AD DAC72)
Current and Voltage Models Available
Improved Second-Source
Low Cost

AD DAC71/AD DAC72 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD DAC71 and AD DAC72 are high resolution 16-bit hybrid IC digital-to-analog converters including reference, scaling resistors and output amplifier (V models).

The devices offer outstanding accuracy, including maximum linearity error of 0.003% at room temperature and maximum gain drifts of 15ppm/°C (AD DAC71, AD DAC71H, AD DAC72C) and 7ppm/°C (AD DAC72). This performance is possible due to the innovative design, using proprietary monolithic D/A converter chips. Laser-trimmed thin film resistors provide the linearity and wide temperature range for guaranteed monotonicity.

The AD DAC71 and AD DAC72 digital inputs are TTL-compatible. Coding is complementary straight binary (CSB) for unipolar output versions and complementary offset binary (COB) for bipolar output versions.

All versions are packaged in a 24-pin metal DIP. The AD DAC71, AD DAC71H and AD DAC72C are specified for operation from 0 to +70°C, and the AD DAC72 is specified from −25°C to +85°C. The AD DAC71H, AD DAC72 and AD DAC72C are supplied in hermetically-sealed packages.

The AD DAC71 and AD DAC72 are intended to serve as improved second sources to DAC71 and DAC72 devices from other manufacturers.

PRODUCT HIGHLIGHTS

1. The AD DAC71 and AD DAC72 provide 16-bit resolution with 0.003% linearity error.
2. The proprietary chips used in the hybrid design provide excellent stability over temperature and improved reliability.
3. Unipolar and bipolar current and voltage output versions are available to fill a wide range of system requirements.
4. The AD DAC71 and AD DAC72 are improved second source replacements for DAC71 and DAC72 devices from other manufacturers.

***Covered by Patent Numbers: 3,978,473; RE28,633; 4,020,486; 3,747,088; 3,803,590; 3,961,326; 4,213,806; 4,136,349.**

SPECIFICATIONS (@ T_A = +25°C, rated power supplies unless otherwise noted)

MODEL	AD DAC71/AD DAC71H MIN	TYP	MAX	AD DAC72C MIN	TYP	MAX	AD DAC72 MIN	TYP	MAX	UNITS
DIGITAL INPUTS										
Resolution		16			16			16		Bits
Logic Levels (TTL-Compatible)[1]										
Logical "1"	+2.4		+5.5	+2.4		+5.5	+2.4		+5.5	V dc
Logical "0"	+0		+0.4	+0		+0.4	+0		+0.4	V dc
ACCURACY[2]										
Linearity Error at 25°C			±0.003			±0.003			±0.003	% of FSR[3]
Gain Error[4], Voltage		±0.01	±0.1		±0.05	±0.15		±0.05	±0.15	%
Current		±0.05	±0.25		±0.05	±0.25		±0.05	±0.25	%
Offset Error[4], Voltage, Unipolar		±0.1	±2.0		±0.1	±2.0		±0.1	±2.0	mV
Voltage, Bipolar			±5.0			±10.0			±10.0	mV
Current, Unipolar			±1.0			±1.0			±1.0	μA
Current, Bipolar			±5.0			±5.0			±5.0	μA
Monotonicity Temp. Range (14-Bits)	0		+50	0		+50	0		+70	°C
DRIFT (Over Specified Temp. Range)										
Total Bipolar Drift (includes gain, offset, and linearity drift)										
Voltage										
T_{min} to 25°C		±7	±15		±7	±15		±5	±19	ppm of FSR/°C
25°C to T_{max}		±7	±15		±7	±15		±5	±11	ppm of FSR/°C
Current										
T_{min} to T_{max}		±15			±15			±10		ppm of FSR/°C
TOTAL ERROR OVER TEMP. RANGE[5]										
Voltage, Unipolar										
T_{min} to +25°C			±0.083			±0.083			±0.100	% of FSR
+25°C to T_{max}			±0.083			±0.083			±0.072	% of FSR
Voltage, Bipolar										
T_{min} to +25°C			±0.071			±0.071			±0.100	% of FSR
+25°C to T_{max}			±0.071			±0.071			±0.072	% of FSR
Current, Unipolar (T_{min} to T_{max})			±0.23			±0.23			±0.24	% of FSR
Bipolar (T_{min} to T_{max})			±0.23			±0.23			±0.24	% of FSR
TEMPERATURE COEFFICIENTS										
Gain										
Voltage										
T_{min} to +25°C			±15			±15			±15	ppm of FSR/°C
+25°C to T_{max}			±15			±15			±7	ppm of FSR/°C
Current		±15			±15			±10		ppm of FSR/°C
Offset										
Voltage, Unipolar		±1	±2		±1	±2		±1	±2	ppm of FSR/°C
Bipolar			±10			±10			±8	ppm of FSR/°C
Current, Unipolar			±1			±1			±1	ppm of FSR/°C
Bipolar		±15			±15			±10		ppm of FSR/°C
Differential Linearity over Temperature			±2			±2			±1	ppm of FSR/°C
Linearity Error over Temperature			±2			±2			±1	ppm of FSR/°C
SETTLING TIME										
Voltage Models (to ±0.003% of FSR)										
Output: 20V Step		5	10		5	10		5	10	μs
1LSB Step[6]		3	5		3	5		3	5	μs
Slew Rate		20			20			20		V/μs
Current Models (to ±0.003% of FSR)[7]										
Output: 2mA step 10Ω to 100Ω Load			1			1			1	μs
1kΩ Load			3			3			3	μs
Switching Transient		500			500			500		mV
ANALOG OUTPUT										
Voltage Models										
Ranges–CSB		0 to +10			0 to +10			0 to +10		V
COB		±10			±10			±10		V
Output Current	±5			±5			±5			mA
Output Impedance (dc)		0.05			0.05			0.05		Ω
Short Circuit Duration		Indefinite to Common			Indefinite to Common			Indefinite to Common		
Current Models										
Ranges–CSB		0 to −2			0 to −2			0 to −2		mA
COB		±1			±1			±1		mA
Output Impedance–Unipolar		6.0			6.0			6.0		kΩ
Bipolar		3.0			3.0			3.0		kΩ
Compliance	1.5		+10	1.5		+10	1.5		+10	V
INTERNAL REFERENCE VOLTAGE	6.0	6.3	6.6	6.0	6.3	6.6	6.0	6.3	6.6	V
Maximum External Current[8]			±3			±3			±3	mA
Temp. Coeff. of Drift			±10			±10			±5	ppm/°C
POWER SUPPLY SENSITIVITY										
Unipolar Offset										
±15V dc		±0.0001			±0.0001			±0.0001		% of FSR/% V_S
+5V dc		±0.0001			±0.0001			±0.0001		% of FSR/% V_S
Bipolar Offset										
±15V dc		±0.0004			±0.0004			±0.0004		% of FSR/% V_S
+5V dc		±0.0001			±0.0001			±0.0001		% of FSR/% V_S

MODEL	AD DAC71/AD DAC71H MIN	TYP	MAX	AD DAC72C MIN	TYP	MAX	AD DAC72 MIN	TYP	MAX	UNITS
POWER SUPPLY SENSITIVITY (Continued)										
Gain										
± 15V dc		± 0.001			± 0.001			± 0.001		% of FSR/% V_S
+ 5V dc		± 0.0005			± 0.0005			± 0.0005		% of FSR/% V_S
POWER SUPPLY REQUIREMENTS										
DAC71/72	± 14.5, + 4.75	± 15.0, + 5.0	± 15.5, + 5.25	± 14.5, + 4.75	± 15.0, + 5.0	± 15.5, + 5.25	± 14.5, + 4.75	± 15.0, + 5.0	± 15.5, + 5.25	V dc
Supply Drain, + 15V dc (no load)		10	20		10	20		10	20	mA
− 15V dc (no load)		30	55		30	55		30	55	mA
+ 5V dc (logic supply)		10	20		10	20		10	20	mA
TEMPERATURE RANGE										
Specification	0		+ 70	0		+ 70	− 25		+ 85	°C
Operating (double above Drift Specs)	− 25		+ 85	− 25		+ 85	− 55		+ 100	°C
Storage	− 55		+ 100	− 55		+ 100	− 55		+ 110	°C

NOTES
[1]Adding external CMOS hex buffers CD4009A will provide 15V dc CMOS input compatibility.
[2]Accuracy is specified when using internal feedback resistors. Current output specifications are guaranteed at the voltage output of an external op amp using the internal feedback resistor.
[3]FSR means Full Scale Range and is 20V for ± 10V range.
[4]Adjustable to zero with external trim potentiometer.
[5]With gain and offset errors adjusted to zero at 25°C.
[6]1 LSB is for 14-bit resolution.
[7]Parameter guaranteed, not tested.
[8]Maximum with no degradation of specification.

Specifications subject to change without notice.

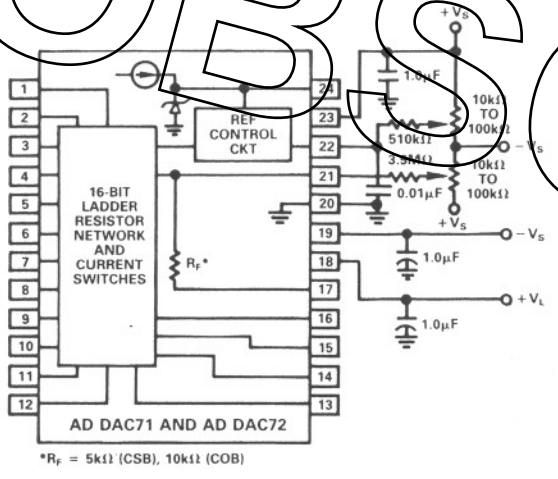


Figure 1. External Adjustment and Voltage Supply Connection Diagram, Current Model

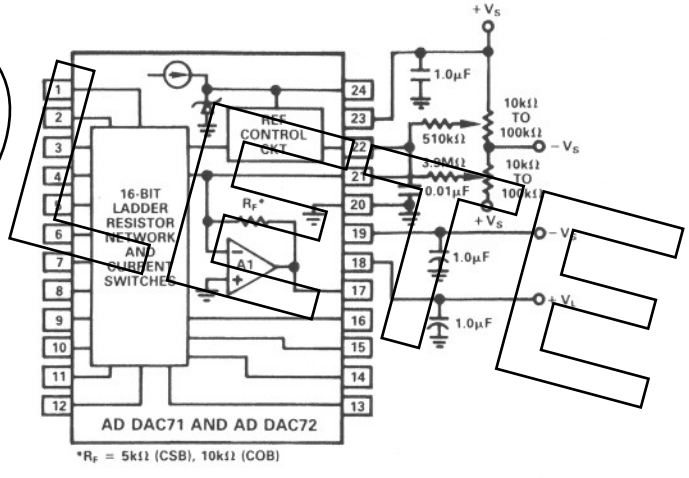


Figure 2. External Adjustment and Voltage Supply Connection Diagram, Voltage Model

ORDERING GUIDE

Model	Output	Input Code	Temperature Range	Seal	Package Option*
AD DAC71–COB–I	Current	Comp. Offset Binary	0 to + 70°C	Polymer	DH-24D
AD DAC71–CSB–I	Current	Comp. Straight Binary	0 to + 70°C	Polymer	DH-24D
AD DAC71H–COB–I	Current	Comp. Offset Binary	0 to + 70°C	Hermetic	DH-24D
AD DAC71H–CSB–I	Current	Comp. Straight Binary	0 to + 70°C	Hermetic	DH-24D
AD DAC72C–COB–I	Current	Comp. Offset Binary	0 to + 70°C	Hermetic	DH-24D
AD DAC72C–CSB–I	Current	Comp. Straight Binary	0 to + 70°C	Hermetic	DH-24D
AD DAC72–COB–I	Current	Comp. Offset Binary	− 25°C to + 85°C	Hermetic	DH-24D
AD DAC72–CSB–I	Current	Comp. Straight Binary	− 25°C to + 85°C	Hermetic	DH-24D
AD DAC71–COB–V	Voltage	Comp. Offset Binary	0 to + 70°C	Polymer	DH-24D
AD DAC71–CSB–V	Voltage	Comp. Straight Binary	0 to + 70°C	Polymer	DH-24D
AD DAC71H–COB–V	Voltage	Comp. Offset Binary	0 to + 70°C	Hermetic	DH-24D
AD DAC71H–CSB–V	Voltage	Comp. Straight Binary	0 to + 70°C	Hermetic	DH-24D
AD DAC72C–COB–V	Voltage	Comp. Offset Binary	0 to + 70°C	Hermetic	DH-24D
AD DAC72C–CSB–V	Voltage	Comp. Straight Binary	0 to + 70°C	Hermetic	DH-24D
AD DAC72–COB–V	Voltage	Comp. Offset Binary	− 25°C to + 85°C	Hermetic	DH-24D
AD DAC72–CSB–V	Voltage	Comp. Straight Binary	− 25°C to + 85°C	Hermetic	DH-24D

*See Section 13 for package outline information.

PRESERVING THE ACCURACY OF THE AD DAC71 AND AD DAC72

A great deal of care must be exercised when using high resolution converters such as the AD DAC71 and AD DAC72. Since one least significant bit of a 16-bit converter (LSB) represents an analog voltage of only 153 microvolts out of a 10V scale, normally negligible error sources become significant. Series resistances of connectors and wiring can be major contributors, as can thermocouple effects. Figure 3 illustrates the connections for voltage output versions of the AD DAC71 and AD DAC72.

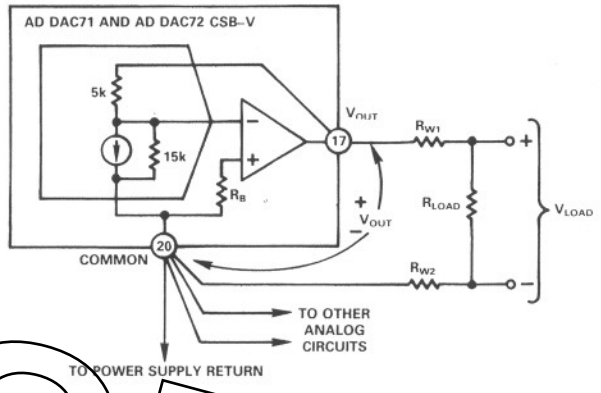


Figure 3. AD DAC71 and AD DAC72 Connection Diagram (Voltage Models)

In this circuit, the analog output voltage is accurately developed between pin 17 and pin 20 of the DAC. The voltage measured at the load will be inaccurate if there is significant resistance in the wiring (and any connectors) between the DAC and the load. If the load resistance is constant, the effects of R_{W1} and R_{W2} can be treated as a simple gain error, and can be trimmed out. However, if R_L is variable, then R_{W1} and R_{W2} should be reduced to a value less than $\frac{R_{L\ MIN}}{2^{16}}$. This will reduce the effect of the wiring resistances to a gain error of less than 1LSB. The AD DAC71 and AD DAC72 are rated at an output current of 5mA which translates to a minimum load resistance of 2kΩ. Thus wiring resistances should be held to a maximum of 30 milliohms. This corresponds to approximately six inches of #28 wire or a six inch long printed circuit track 0.050 inches wide.

The current output versions of the AD DAC71 and AD DAC72 use an external operational amplifier to convert the output current to an output voltage. The recommended configuration is shown in Figure 4. Notice that this configuration permits the voltage at the load to the sensed remotely. The resistance (R_{W1}) of the lead connecting the load to the internal feedback resistor introduces a gain error equal to $\frac{R_{W1}}{R_{LOAD}}$, independent of R_{LOAD} and R_{W2}. The error contributed by R_{W3} depends upon where the output is measured. If the output is measured between the top of R_{LOAD} and pin 20 of the DAC, no error results since R_{W3} effectively becomes part of the load resistance.

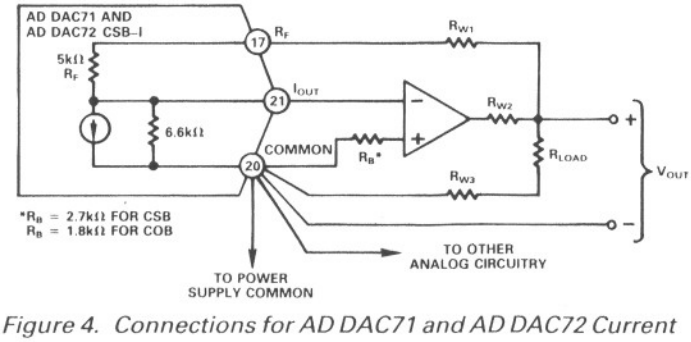


Figure 4. Connections for AD DAC71 and AD DAC72 Current Output Versions

In applications where R_{W3} is large or large currents flow in R_{W3}, it is necessary to use remote sensing as shown in Figure 5.

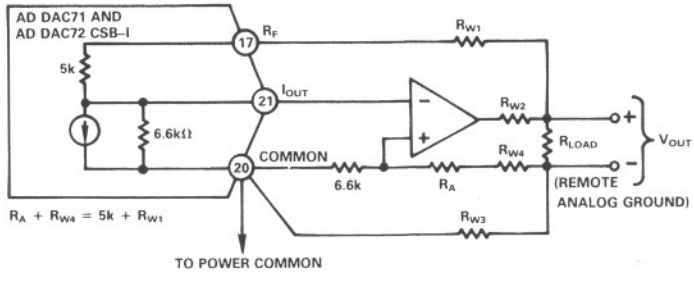


Figure 5. Use of Output Amplifier as Subtractor for Remote Ground Sensing

This circuit uses the output amplifier as a subtractor stage. Any spurious voltage developed across R_{W3} becomes a common mode voltage and its error contribution is reduced by the common mode rejection of the op amp.

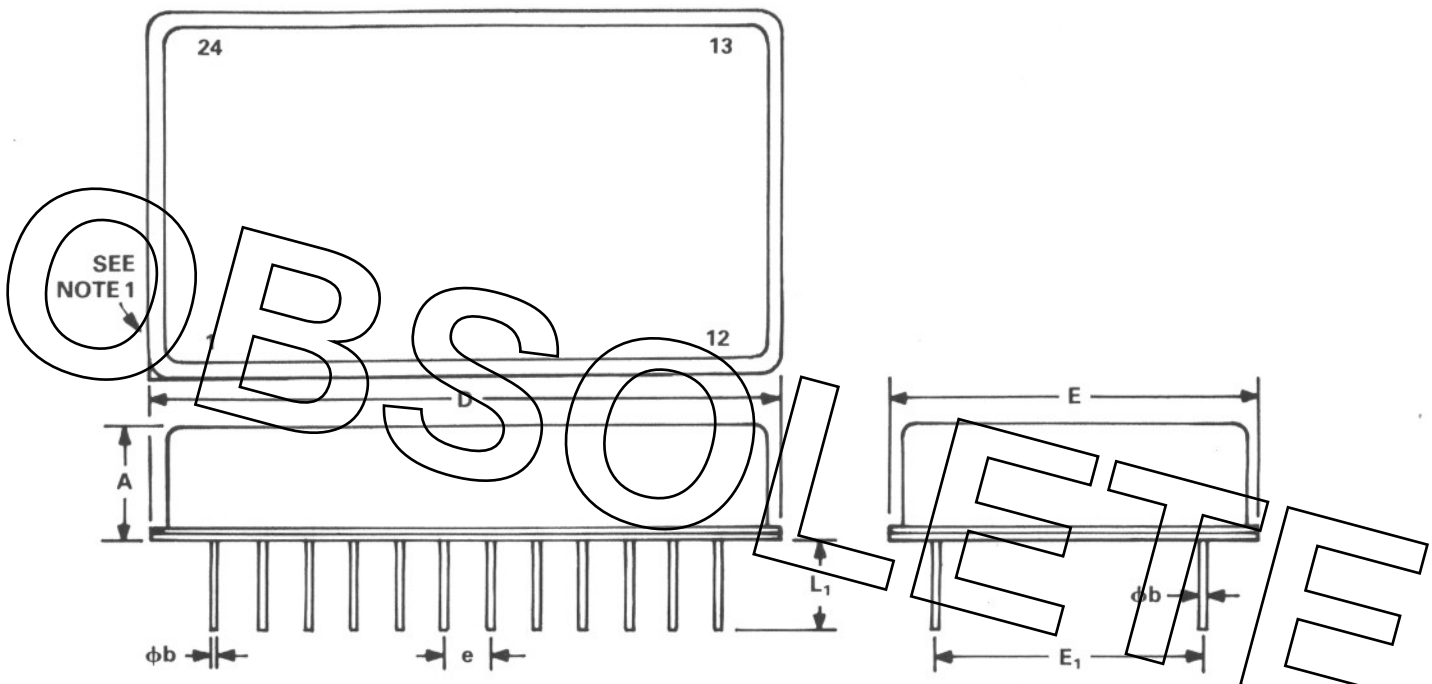
In the circuits of both Figure 4 and Figure 5, R_{W2}'s effect is negligible since it is inside the loop of the amplifier. If current boosting is required in order to drive heavy loads, a suitable booster stage can be inserted between the amplifier's output and the load. Since the loop is closed from the load end, offsets and other errors induced by the booster are eliminated.

It is also important to minimize thermocouple effects in circuitry using the AD DAC71 and AD DAC72. Recalling that 1LSB of a 16 bit, 10 volt scale converter is only 153 microvolts, a stray uncompensated thermocouple can introduce several LSBs of offset in response to minor changes in ambient temperature. Any part of a circuit which includes a junction between two dissimilar metals forms a thermocouple. Such junctions include connectors, sockets, and any soldered connections. The solution to thermocouple errors is to insure that every junction is cancelled by an identical, but opposite, junction at the same temperature. While this is often automatically accomplished (for example, in a connector carrying both signal and return leads), careful attention should be given to the physical layout of circuits using the AD DAC71 and AD DAC72.

Another source of signal degradation in high-resolution converter circuits is magnetically-coupled interference from stray fields. Signal and return leads should be arranged in a way which minimizes both length and the total cross-section area of the loop. Of course, high resolution circuits should be located as far as possible from any sources of electromagnetic interference, including power transformers, digital logic and electromechanical devices.

DH-24D

24-Lead Metal Platform DIP



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.250		6.35	
ϕb	0.016	0.020	0.41	0.51	
D		1.385		35.18	
E		0.810		20.57	
E_1	0.590	0.610	15.00	15.50	3
e	0.100 BSC		2.54 BSC		2
L_1	0.140	0.210	3.56	5.33	

NOTES

1. Index area; a colored bead or identification mark is located at lead one.
2. The basic pin spacing is 0.100″ (2.54mm) between centerlines.
3. E_1 shall be measured at the centerline of the leads.