SOLID STATE SOLUTIONS FOR ELECTRICITY METROLOGY

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1.0 Introduction

Significant changes are taking place in the electric energy industry worldwide. Deregulation of the utilities will produce a tougher competitive environment for the suppliers of electricity. Increased demand for electrical energy will require better management of distribution. Suppliers will need to identify ways of supplying a better level of service at a reduced cost. One way to do this is to install a solid state electricity meter.

Apart from tangible benefits like higher accuracy – especially in the presence of nonsinusoidal waveforms [1,2], the solid state meter offers more than just the measurement of kWhrs. Given the accuracy, flexibility and powerful network management possibilities offered by solid state metrology the days of the electromechanical meter are numbered.

This paper gives an overview of electricity meter design using solid state electronics. It discusses various architectures and some of the key technologies that allow reliable and cost effective solid state meters to be implemented. It also discusses semiconductor reliability issues.

2.0 Anatomy of a Solid State Meter

Solid state electricity meters are generally based on one of two types of electronic technologies, analog or digital signal processing. Signal processing refers to multiplication and filtering in order to extract the required information (kWhrs, VARS etc.). An analog electronic meter processes analog signals, i.e. signals which exist at every instance of time - like voltage and current signals, see figure 1. By the same definition an electromechanical meter can be said to be an analog meter.

Analog signal processing is an older solid state technology that struggles to achieve the same price/performance ratio as its digital counterpart.

Disadvantages of analog signal processing

- Analog signal processing is not a flexible technology. Analog meters can not be easily reconfigured to meet specific local requirements or upgraded at a later date.
- Analog meters do not offer the same stability as their digital counter parts over large variations in operating environment and with time.
- Analog meters do not offer the same simple, cost effective and stable calibration features, which may be implemented using digital technology.
- Analog meters do not offer the same high integration (cost reduction) path that digital electronics does.

For these reasons the remainder of this discussion will focus on digital solid state electricity meters.

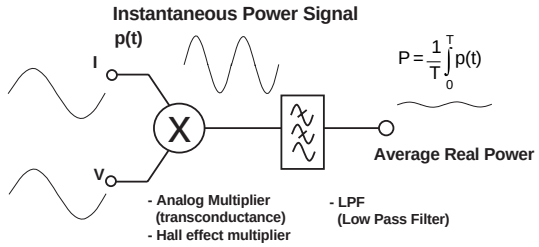

Figure 1. Analog (continuous time) Signal Processing

2.1 Digital Solid State Electricity Meters

The digital meter relies on a process called analog-to-digital conversion. It does this by using a device called an ADC (Analog to Digital Converter). The ADC takes samples or “snap shots” of the analog signals at discrete instances of time. These “snap shots” or discrete time signals are in turn converted to numeric values by the ADC - see figure 2.

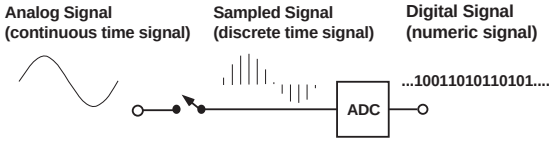

Figure 2. Analog to Digital Conversion

Once in this numeric or digital format, digital circuits, e.g., microprocessors, can easily and reliably process these signals. Figure 3 shows a graphical representation of this digital processing.

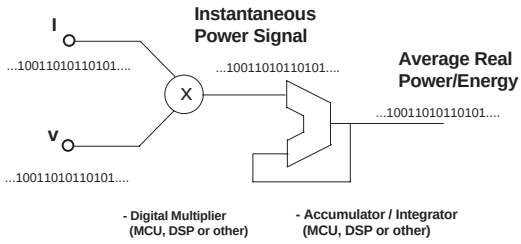

Figure 3. Digital (discrete time) Signal Processing

2.2 Selecting an Analog to Digital Converter for Energy Metering

The Analog to Digital conversion can be carried out using one of several schemes or architectures [3]. Each of the architectures has its own associated advantages and disadvantages. It is important to be aware of these differences when matching an ADC to a specific application.

2.2.1 ADC Requirements for Energy Metering

- High Resolution, i.e., 16 Bits.
  Because of the relatively wide dynamic range (4%Ib to 400%Ib) and the accuracy requirements (0.5%) of the application, the resolution of the ADC needs to be high. Another approach which, is discussed later, is to use over sampling and DSP to improve resolution.
- A Sampling rate of at least 2 to 4 kSPS (kilo Samples Per Second) is required for the application. A basic rule of sampling theory states that the rate (frequency) of sampling must be at least twice the highest frequency content of the signal. This is called the Nyquist rate. In energy metering current ANSI and IEC specifications [6] call for accurate measurement of frequency content up to the 20th harmonic (1kHz or 1.2kHz depending on the line frequency).
- Low Cost. The solution must be a low cost one because the end application is particularly cost sensitive, especially in residential metering applications. The choice of ADC may not only impact cost because of the price of the ADC itself, but also because of external components required by the ADC.
- The ADC must not consume excessive power. One of the challenging aspects of solid state meter design is the design of the PSU (Power Supply Unit). This must be low cost and reliable for the life of the meter (15-20 yr.). Typically these supplies are capacitor based, as the cost of a transformer is often prohibitive. Capacitor based designs have a low VA rating and are typically only capable of providing 10 to 15 mA at 5V.

2.2.2 Oversampling

Another approach which reduces the resolution requirements for the ADC, is to use quantization theory to increase the effective resolution over the desired bandwidth. This is done by oversampling the analog signal, i.e., sampling at a rate which is much greater than the Nyquist rate and then digitally processing the resulting data [4]. For example by using a 12 bit ADC and sampling a pass band signal of 2kHz at 100kSPS the SNR over the 2kHz bandwidth is calculated as:

$$\mathrm{SNR} = 6.02 \times 12 \text{ Bits} + 1.76\mathrm{dB} + 10\log_{10}\left[\frac{100\mathrm{kHz}}{4\mathrm{kHz}}\right]$$

$$\mathrm{SNR} = 87.98\mathrm{dB} \text{ or } 14.3 \text{ Bits}$$

The effective resolution of the ADC over the 2kHz bandwidth of interest has been increased to 14.3 bits. In general the effective resolution of the ADC is improved by ½ LSB for every doubling of the sampling frequency.

2.2.3 ADC Architectures

The main architectures for Analog to Digital Conversion are listed below.

- SAR types (Successive Approximation)
- Flash (Parallel) and Half Flash ADC
- Integrating (Dual Slope) ADC
- Voltage to Frequency (V/F)
- Σ-Δ (Sigma Delta) ADC

SAR Converters

The successive approximation ADC is a very widely used and understood technology. The conversion technique is based upon continuously comparing the sampled input signal to know voltages in order to convert it to a binary word.

Advantages

1. High Speed, up to 1 million conversions per second is possible.
2. Relatively low power consumption when compared to other architectures.
3. Relatively low cost when the required resolution (conversion accuracy) is low, i.e., less than 12 Bits (4096 counts)

Disadvantages

1. Becomes costly when high resolution is required (>14 Bits).
2. Output signals from transducers generally require substantial signal conditioning. Depending on the application this can add significant cost.

Flash converters

A Flash converter converts a sampled signal to a binary word in one step (or two steps in the case of a half-flash). Hence the time to do a conversion is very short. The flash and half-flash architecture is usually used in applications requiring low resolution (256 – 1024 counts) but high-speed conversion (20 – 50 Million samples per second). Applications typically include video and communications.

Advantages

1. Very high speed conversions

Disadvantages

1. Low resolution
2. High power consumption
3. Relatively high Cost
4. Output signals from transducers generally require substantial signal conditioning. Depending on the application this can add significant cost.

Integrating Converters
Integrating ADCs are used for slow, precise measurements such as in digital voltmeters and many applications involving slow transducers. They can offer up to 22 bits of resolution and an implicit rejection of high frequency background noise, e.g., AC mains pickup.

Advantages

1. High accuracy
2. Relatively low power consumption
3. Relatively low cost solution

Disadvantages

1. Limited conversion rate. Accuracy decreases as conversion rate increases. Typical accuracy at 100 – 300 conversions per second is 12 Bits.

Voltage-to-Frequency Converters
The VFC performs an indirect conversion by first converting the input signal to a frequency and then using a counter to convert the frequency to a digital word. Resolution can, in theory be increased almost indefinitely by simply waiting long enough to resolve the output frequency to the degree desired [5].

Advantages

1. High accuracy
2. Relatively low power consumption
3. Relatively low cost solution – however needs a counter to perform the frequency to digital conversion.

Disadvantages

1. Like the Integrating ADC, it has a limited conversion rate. Accuracy decreases as conversion rate increases. Typical accuracy at 100 – 300 conversions per second is 12 Bits.
2. Needs external counter (MCU or other) to complete the Analog to Digital Conversion

Sigma-Delta ADCs
Within the last several years, the sigma-delta architecture has become more popular for realizing high-resolution Analog to Digital Conversion. One of the more important advantages is that the ADC can be combined with DSP functions on one mixed signal VLSI chip.
Basically, a Sigma-Delta converter digitizes an analog signal with a very low resolution (1 Bit) ADC at a very high sampling rate. By using over-sampling techniques in conjunction with noise shaping and digital filtering (DSP), the effective resolution is increased—see 2.2.2 *Oversampling*.

Advantages

1. High resolution – up to 20 Bits of Peak-to-Peak resolution possible
2. Relatively higher conversion rate when compared to Integrating ADCs and VFCs.
3. Can easily be fabricated on mixed signal CMOS to provide low cost high resolution signal acquisition and digital processing on a single chip.
4. Due to the high over sampling techniques used, minimal filtering of the transducer signal is required and virtually no signal conditioning.

Disadvantages

1. Higher order modulators are required when faster conversion rates are needed.
2. Relatively higher power consumption when compared to similar conversion rates using SAR and Integrating ADCs.

3.0 Processing the Digitized Transducer Outputs

Once converted to a digital signal, the voltage and current waveforms can be multiplied, filtered and integrated by digital circuits to extract just about any information required by the meter. Figure 4 shows the basic building blocks of a generic digital solid state meter. Voltage and current transducers convert these signals to smaller equivalent voltage signals, which can be presented to the ADC for conversion. Once these signals have been digitized they are processed by a digital circuit in order to calculate active, reactive, apparent power etc. The meter requires other functionality like non-volatile memory to store program or calibration coefficients. Some kind of power supply monitoring and watch dog functionality will ensure correct operation especially during power up and power down. The meter will also require a power supply and a display for conveying the measured information. Adding communications capability for AMR (Automatic Meter Reading) can extend the basic meter functionality.

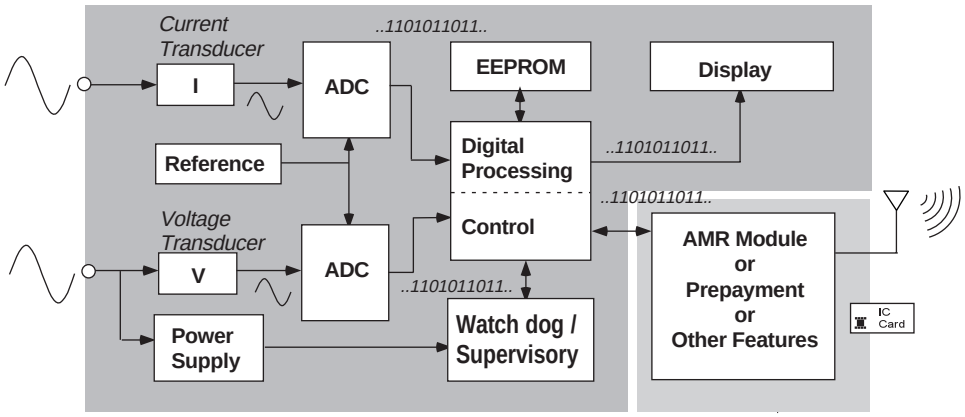

Figure 4 – Solid State Energy Meter (Generic Block Diagram)

3.1 DSP Based Meter

The block diagram in figure 4 shows the basic building blocks of a digital meter. Numerous ways of implementing this functionality in a practical meter design have been proven. One of the most common implementations is shown in figure 5 below. Here a user programmable, general purpose DSP (Digital Signal Processor) or MCU is used as the main computational engine of the meter. The ADCs may be on-chip as shown or external devices may be used. The designer of the meter must write the software needed to calculate the required parameters. A DSP based meter usually requires the use of a MCU (Microcontoller Unit) in a practical implementation. The MCU will likely drive the display and perform the numerous 'house keeping' duties in the meter.

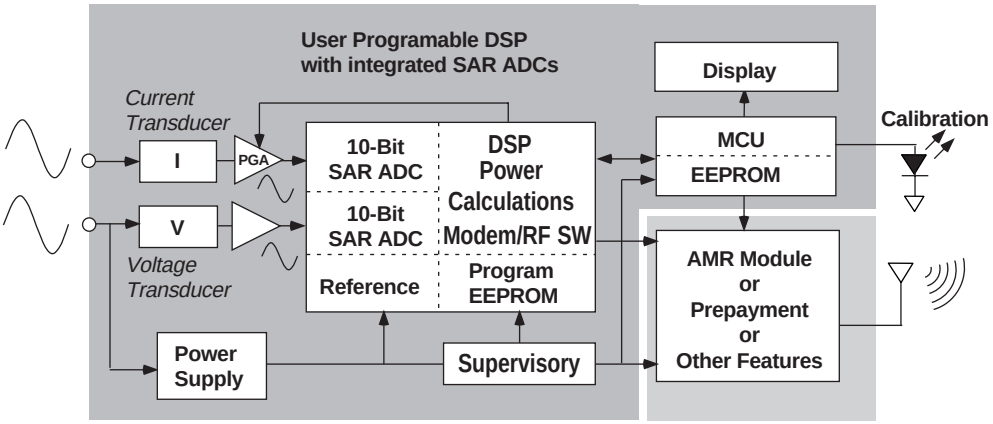

Figure 5 – Solid State Energy Meter (DSP based Solution)

In some cases extra meter functionality can be incorporated into the DSP. For example the base band modulation and encryption in a RF based communications module could also be performed by the DSP. However this requires more computational power and, with it, cost. In addition this approach does not lend itself well to modular design. It is likely that for the foreseeable future AMR, Prepayment and other features of the meter are going to vary considerably from region to region and change at the customer request. Also modular design allows easy on site upgrading of features at a later date. The meter also requires some form of supervisory circuits to monitor the supply voltage and ensure a controlled power up and power down sequence.

3.2 ADC with Fixed Function DSP based Meter

Another approach to digital meter implementation is to use an ADC a with fixed function DSP on chip. The fixed function DSP is a dedicated computational engine, which will calculate the required parameters. The user does not program the device, as the program is hardwired internally. The ADC architecture is such that it can be implemented on small geometry VLSI CMOS (digital) processes. Since the ADC is fabricated on what is essentially a digital process, fixed DSP function can easily be added at little extra cost. The on-chip DSP enhances ADC resolution to that required by energy metering applications and calculates many of the parameters required in energy metering, e.g., Watts, VARS etc.

Figure 6 shows a block diagram of a meter implemented using this architecture.
This added DSP function could also implement many other features that are unique to solid state energy metering. The block diagram in figure 6 shows such features as supervisory and brown out detection. Also many energy meter implementations require a frequency output (LED) for utility or other end customer calibration purposes.
Another important feature of this type of approach is that the development time has been considerably reduced because there is little software and hardware development. This is an important point. Because the ADC has been developed for a specific application and it is not a general-purpose part, the designer can have a high degree of confidence that the manufacturer has resolved all issues regarding the suitability of the ADC for the application. Because the energy computation and frequency generation is carried out on the metering IC, a low power, low cost MCU is usually all that is required.

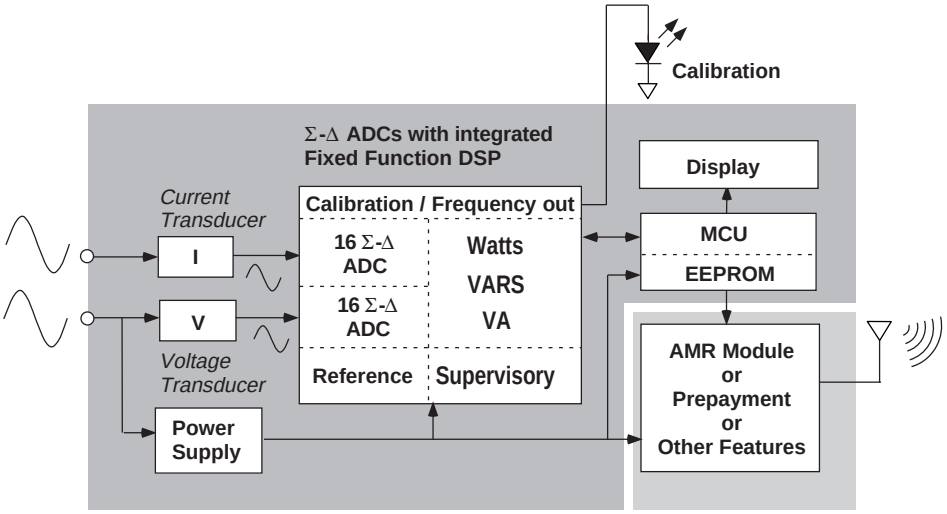

Figure 6 – Solid State Energy Meter (ADC and Fixed Function DSP based Solution)

4.0 Semiconductor Reliability

For many years the electromechanical energy meter has provided a cost effective and most importantly, a reliable energy metering solution. While the accuracy limitations of the technology meant that most meters achieved at best 2% accuracy, this could easily be overlooked in exchange for a 25 to 30 year operating life. With this kind of proven reliability there is a high degree of expectation among the utilities and other end customers that any new meter technology will have a comparable operating life. The mechanisms of semiconductor failure can be roughly divided into two main areas. The first group of failure mechanisms is associated with defects in the manufacturing process itself and the second group can be broadly classified as electrical stress (in-circuit) failures.

4.1 Failures due to the Manufacturing Process

These kinds of failures are often referred to as *intrinsic* and *extrinsic* failure mechanisms. Failure mechanisms inherent to the semiconductor die itself are termed intrinsic. They include, among others, crystal defects and processing defects. Extrinsic failure mechanisms are as a result of device packaging and the interconnection process, e.g., poor environmental integrity of the package leading to corrosion of the die and bond wires lifting due thermal shock.

4.2 Screening Processes

Semiconductor devices are screened by the manufacturer to ensure that there are no failures due to the manufacturing process. There are at least two basic categories of tests that are typically carried out, high temperature tests and mechanical stress tests.

4.2.1 High Temperature Tests

These kinds of tests are often called accelerated life tests because by increasing the operating temperature of the devices, a longer operating period (several years) under normal operation conditions can be simulated. To do this the intrinsic failure mechanisms are assumed to be as a result of a chemical reaction. The rate at which many chemical processes take place is described by the Arrhenius equation[7] .

$$r = A.\exp\left(-\frac{E_a}{kT}\right)$$

where:
r = rate of process, A = proportional multiplier
k = Boltzman constant (1.38×10^{-23}),
T = Temperature (°K),
Ea = a constant known as the activation energy for a given process.

By using the Arrhenius equation, experimental data collected at high temperature allows failure rates over many years (25-30) to be modeled at normal temperatures. Most Semiconductor manufacturers use this technique when calculating failure rates. Published Integrated Circuit reliability data from semiconductor manufacturers usually details specific conditions like activation energy.
Figure 8 below is commonly called the 'bathtube' curve and it illustrates typical failure rates of a system over its lifetime.

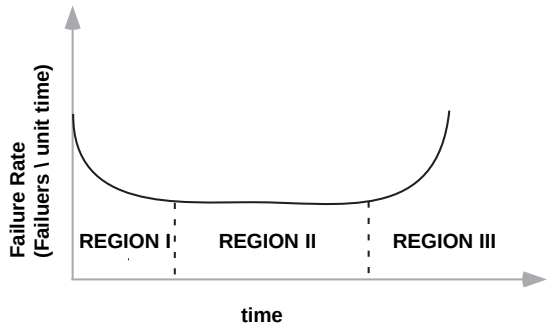

Figure 8 — The "bathtub" curve

The curve consists of three regions as shown in figure 8. Region I of the curve shows decreasing failure rates. The failures in this region are attributed to poor quality due to variations in the production line. Region II shows the working life of the component and failures are small in number and random. These failures are due to long term failure mechanisms which, may be aggravated by the operating environment, e.g., temperature, electrical stress etc. Region III indicates the end of a component life and is called the 'wear out' region. Semiconductors typically do not display this kind of wear out behavior within the typical 25-30 year life span of a device.

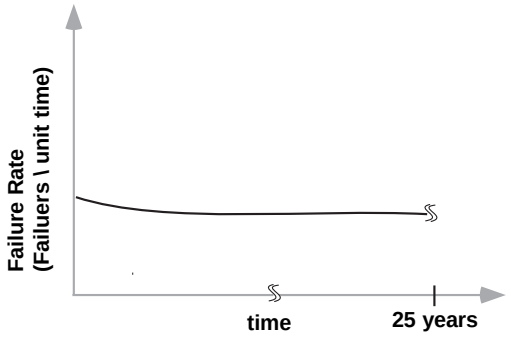

Figure 9 — The "bathtub" curve for a mature process.

A 'bathtub' curve for a mature and well-controlled process might look something like the curve in figure 9.
Semiconductor manufacturers rarely subject all manufactured devices to this kind of high temperature testing called "burn in". Occasionally customers do request this kind of screening for critical applications where very low failure rates are required. "Burn in" is a very costly procedure and would severely affect the manufacturer's ability to produce large volumes with reasonable lead times. However with well-controlled processes and frequent sample testing semiconductor reliability is maintained at a high level.

4.2.2 Mechanical Stress Tests

These kinds of tests are used to detect failures due to extrinsic effects, e.g., weak bonds etc.
A weak bond may operate for many hours at high temperature but could fail immediately under mechanical stress such as vibration.
Mechanical stress tests are usually carried out when a new package type is introduced by the manufacturer. The new package will typically undergo mechanical shock tests, package leakage tests, humidity testing etc. As was the case with high temperature testing it is impractical to test every device, but by using well-controlled assembly procedures and sample testing the package reliability is maintained at a high level.

4.3 Failures due to Electrical Stress

Electrical stress failures are caused by subjecting the component to voltages and currents outside the maximum ratings quoted on the data sheet. The component fails because it is being misused. This may be as a result of poor design or inadequate protection when the device is operating in a harsh electrical environment, e.g., large transients due the lighting and inductive load switching. A device may also fail due to improper handling which can lead to damage as a result of an electrostatic discharge. Although these failures are due to misuse, semiconductor manufacturers take steps to minimize the overstress sensitivity as much as possible. They do this by including on-chip ESD protection and carrying out "latch-up" and power supply sequencing testing. These tests verify that the IC is still functional after a minimal electrical stress condition. Typical requirements for a product release means that devices must pass at least a 100mA latch up test and a 1kV ESD test.

5.0 Conclusion

New solid state technology, improved manufacturing processes and innovative designs are removing the technical barriers and driving down the cost of solid state metrology. New low cost, single chip solutions have significantly reduced design times and improved reliability by providing highly integrated solutions. As semiconductor manufacturers continue to work closely with meter manufacturers and utilities further improvements and cost saving opportunities will be identified as a greater understanding of the application is gained.

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