ANALOG DEVICES

AN-687
APPLICATION NOTE

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A Low Cost Tamper-Resistant Energy Meter Based on the ADE7761 with Missing Neutral Function

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INTRODUCTION

This application note describes a meter design based on the ADE7761. The meter is designed for use in single-phase, 2-wire distribution systems.

The ADE7761 is a low cost, single chip solution for electrical energy measurement. This product is another in the long line of Analog Devices' energy meter solutions. Incorporated within this design is a highly accurate ADC system comprised of four analog-to-digital converters and voltage reference. An integrated oscillator is incorporated within the ADE7761 to provide the system clock. In addition, various functions are realized within the fixed function DSP.

This meter incorporates several antitampering features in the design. The ADE7761 has two FAULT conditions that will continue to measure power. The ADE7761 monitors the phase and neutral currents. A FAULT condition occurs if the two currents differ by more than 6.25%. The power calculation is based on the larger of the two currents. The meter will correctly calculate the power if no current exists in either the phase or neutral wire. A second FAULT mode is unique to the design of this meter. If neutral is disconnected from the meter, the meter will go into a missing neutral fault condition. The meter will continue billing based on current input only with the voltage input missing. See the ADE7761 Data Sheet.

DESIGN GOALS

The International Standard IEC 61036 (2000-9) *Alternating Current Static Watt Hour Meters for Active Energy* was used as the primary specification for this design. The goal for this design is for a Class 1 meter based on the IEC specifications. In addition to the accuracy requirements of the meter in particular, attention was paid to the performance with respect to the electromagnetic compatibility.

This design fully complies with the accuracy requirements of the IEC specification at unity gain power factor and at a low (PF = ±0.5) power factor. Included within this document are accuracy requirements for the meter in accordance with IEC 61036.

Table I. Accuracy Requirements

Current Value[1]	PF[2]	Percentage Error Limits[3]	
		Class 1	Class 2
$0.05\ I_B \le I < 0.1\ I_B$	1	±1.5%	±2.5%
$0.1\ I_B \le I \le I_{MAX}$	1	±1.0%	±2.0%
$0.1\ I_B \le I \le 0.2\ I_B$	0.5 Lag	±1.5%	±2.5%
	0.8 Lead	±1.5%	
$0.2\ I_B \le I \le I_{MAX}$	0.5 Lag	±1.0%	±2.0%
	0.8 Lead	±1.0%	

[1]The current ranges for specified accuracy shown in Table I are expressed in terms of the basic current (I_B). The basic current is defined in IEC 61036 (2000–09) Section 3.5.1.1 as the value of current in accordance with which the relevant performance of a direct connection meter is fixed. I_{MAX} is the maximum current at which accuracy is maintained.

[2]Power factor (PF) in Table I relates to the phase relationship between the fundamental voltage (45 Hz to 65 Hz) and current waveforms. PF, in this case, can be simply defined as PF = cos(ϕ), where ϕ is the phase angle between pure sinusoidal current and voltage.

[3]Class index is defined in IEC 61036 (2000–09) Section 3.5.5, Page 27, as the limits of the permissible percentage error. The percentage error is defined as

$$Percentage\ Error = \frac{Energy\ Registered\ by\ Meter - True\ Energy}{True\ Energy} \times 100\%$$

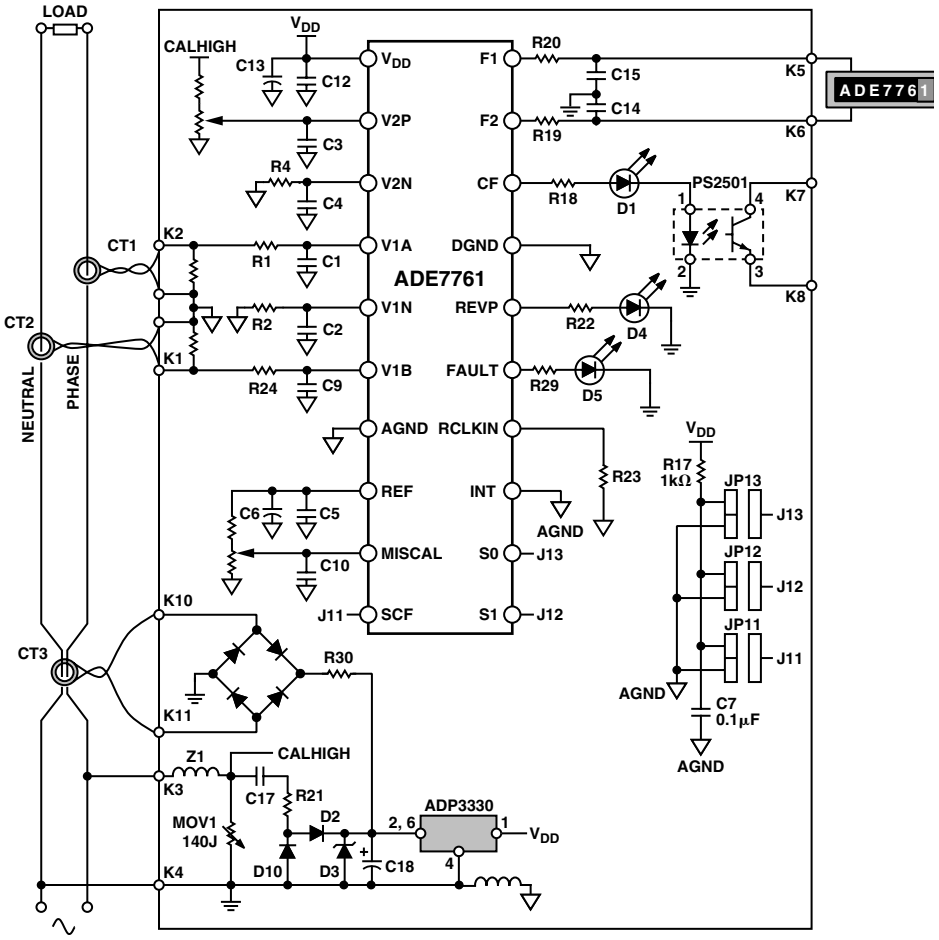

Figure 1. ADE7761 Functional Block Diagram

FUNCTIONAL DESCRIPTION

The diagram in Figure 1 shows the implementation of a simple, low cost watt-hour meter using the ADE7761. The meter consists of three current transformers, a power supply, mechanical counter, and the various support circuitry for the ADE7761.

The energy register (kWh) is a simple electromechanical counter that uses a two-phase stepper motor. The ADE7761 provides direct drive capability for this type of counter. A high frequency pin is provided at the CF pin for a selected calibration frequency of 3200 Imp/kWh. Thus a high frequency output is available at the LED and opto-isolator output. This high frequency output is used to speed up the calibration process and provides a means to quickly verify meter functionality and accuracy in a production environment. The meter is calibrated by varying the line voltage attenuation using the series resistor network. Figure 1 illustrates these resistors as a potentiometer. A second calibration, MISCAL, is accomplished through a second attenuation network from the reference voltage.

The meter has three modes of operation associated with it: normal mode, earth fault, and missing neutral.

In normal mode, the meter senses the load current through a current transformer (See Figure 1, CT1). The current is converted to a voltage through a burden resistor. The line voltage is attenuated through a voltage divider network. The 5 V power supply is provided by the capacitor divider network and a regulator.

A second mode of operation is when the meter's neutral is either disconnected or grounded. In the earth fault mode of operation, the meter senses the currents in CT1 and CT2. If the two currents differ, the meter will measure the larger of the two currents for the power calculation. The meter will continue to use the voltage divider circuit for the voltage channel and the capacitor divider circuit for the power supply.

In the third mode of operation, the meter's neutral is completely disconnected. In the missing neutral mode, current goes through the meter's phase connection only. In a conventional meter, the meter would cease to operate because the supply for the meter would no longer have a return path. In this application, another 5 V power supply is derived from the load current. A current transformer (CT3) provides power to the meter through

a bridge rectifier circuit. The current is sensed through CT1. The meter continues to bill based on the load current (amp-hours). The meter generates an internal signal for the energy measurement since the line voltage is no longer available in this mode. See the ADE7761 Data Sheet for a detailed description. The MISCAL pin adjusts the gain level of the internal signal and is calibrated by the user.

DESIGN EQUATIONS

The ADE7761 produces an output frequency that is proportional to the time average value of the product of two voltage signals. The detailed functionality of the ADE7761 is explained in the ADE7761 Data Sheet. The data sheet also provides an equation that relates the output frequency on F1 and F2 (counter drive) to the product of the rms signal levels at V1 and V2. These signals are the attenuated line voltage and a voltage proportional to the load current.

The four frequency options available on the ADE7761 will allow similar meters (i.e., direct counter drive) with an I_{MAX} of up to 400 A to be designed. The basic current (I_B) for this meter design is selected as 5 A with an I_{MAX} of 40 A. The current range for accuracy will be 2% of I_B to I_{MAX}, or a dynamic range of 400 (100 mA to 40 A). The equation that relates the output frequency to the product of the voltage inputs is

$$Freq = \frac{5.7 \times V1\ rms \times V2\ rms \times F_{1-4}}{V_{REF}^2} \quad (1)$$

The F_{1-4} term of Equation 1 can be chosen from Table II, F_{1-4} Frequency Selection, in the ADE7761 Data Sheet.

In a fault condition, the meter will continue to measure the power using a second method. The missing neutral mode calculates the power based on the load current and an assumed line voltage. A second equation is used to set the output frequency of the meter when in the missing neutral mode. This equation is

$$Freq = \frac{5.7 \times V1\,rms \times \frac{MISCAL}{\sqrt{2}} \times F_{1-4}}{V_{REF}^2} \quad (2)$$

Note that the difference between the two equations is the $MISCAL/\sqrt{2}$ versus the $V2$ rms. In missing neutral, the MISCAL pin voltage is used to set the gain of the missing neutral mode to match the $V2$ input of the normal mode.

The electromechanical register (kWh) will have a constant of 100 imp/kWh, i.e., 100 impulses from the ADE7761 will be required in order to register 1 kWh. IEC 61036 Section 4.2.11 specifies that electromagnetic registers have their lowest values numbered in 10 divisions, each division being subdivided into 10 parts. Therefore, a display with a five plus one digit is used, i.e., 10,000s, 1,000s, 100s, 10s, 1s, 1/10s. The meter constant (for calibration and test) is selected as 3200 imp/kWh.

Design Calculations

The design parameters are as follows:

- Line voltage = 240 V
- I_{MAX} = 40 A
- CF = 3200 imp/kWh
- Meter constant = 100 imp/kWh
- CT turns ratio = 2500:1
- 100 imp/hour = 100/3600 sec = 0.02777 Hz for 1 kW
- Meter calibration at 5 A (I_B)
- Power dissipation at 5 A = 1.2 kW
- Frequency on F1 (and F2) at $I_B = 1.2 \times 0.027777$ Hz or 0.0333324 Hz

Burden Resistor Calculation

In order to ensure the proper dynamic range for the meter, the current channel's burden resistor should be selected based on the maximum current of the meter and the CT's turns ratio. Full scale voltage input to V1 is ±660 mV pk or 467 mV rms when configured with a gain of 1. In order to provide enough headroom, the input voltage to the ADE7761 should be half the maximum input voltage or 233.3 mV rms. A smaller signal may be used as an input to V1, however, to achieve the best dynamic range of the meter; 233.3 mV is the value used for this design. At full load or 40 A and a CT turns ratio of 2500:1, the current output of the CT is

$$\frac{40\ \text{A}\ rms}{2500 Turns} = 16\ mA\ rms \quad (3)$$

The burden resistor is now calculated to be

$$\frac{233.3\ mV\ rms}{16\ mA\ rms} = 14.58\ \Omega \quad (4)$$

A 14.58 Ω resistor is connected across the current transformer output. This provides the correct scaling for the load current to the input of the ADE7761 V1 input. A second resistor is connected to a second current transformer, which monitors the neutral current and is connected to V1B and V1N.

F1-F2 Frequency Calculation

At the full scale input of the meter, the maximum power is 40 A rms × 240 V rms or 9.6 kW. With a meter constant of 100 imp/kWh, the output frequency is

$$\frac{100imp}{kWh} \times 9.6\ kW \times \frac{1\,Hr}{3600\ sec} = 0.2667\ Hz \quad (5)$$

The F_{1-4} frequency is selected from Table VI, F1 and F2 Frequency with Half Scale AC Inputs, in the ADE7761 data sheet. For S0 = 1 and S1 = 0, the output frequency is 0.34 Hz. The output frequency for CF is selected to be 32 ×; therefore SCF is set to zero.

MISCAL Calculation

The input voltage for MISCAL is calculated once the proper frequency is selected for F_{1-4} as follows:

$$0.2667\ Hz = \frac{5.7 \times 233\ mV\ rms \times \frac{MISCAL}{\sqrt{2}} \times 3.44}{2.5^2} \quad (6)$$

Solving for MISCAL, the voltage at the MISCAL pin is 515.9 mV.

Calculating V2

Once the MISCAL voltage has been set, the normal mode can be calibrated. In order to calculate the voltage for V2, the following formula is used:

$$0.2667\ Hz = \frac{5.7 \times 233\ mV\ rms \times V2\ rms \times 3.44}{2.5^2} \quad (7)$$

Solving for V2, the input voltage will be 364.8 mV rms. The input must be attenuated by 657.8 to get the proper output frequency.

CALIBRATING THE METER

The steps used to calibrate the meter are crucial in order to achieve optimal performance. The sequence of calibrating the meter is ground fault, followed by missing neutral, and then normal mode.

Ground Fault

The first calibration point is to match the two current transformers. This is needed for the grounded neutral mode. This ensures that the signal at the second current Channel (V1B) matches that of the phase Channel (V1A). The network for the current channels is shown in Figure 2. Calibration of the grounded neutral channel is accomplished by measuring CF output with no signal on V1B and I_B on the phase Channel (V1A). Next, the signal on V1A must be disconnected and I_B should now be on V1B.

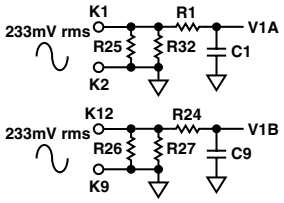

Figure 2. Current Input Network

The resistors R26 and R27 may be changed to ensure CF is the same for Channel V1B as the previous measurement for V1A.

Missing Neutral

From a previous section it can be seen that the meter is calibrated by attenuating the reference voltage to 516 mV for the MISCAL voltage. This attenuation is accomplished through a simple voltage divider network as seen in Figure 3. The range for the attenuation network is from a gain of 0 to 0.28 for a maximum MISCAL voltage of 698 mV. Note: jumper connections are made by shorting out two solder pads. This approach is preferred over the use of trim pots, as the stability of a trim pot over time and environmental conditions are unreliable. In order to calibrate MISCAL the line voltage should be disconnected.

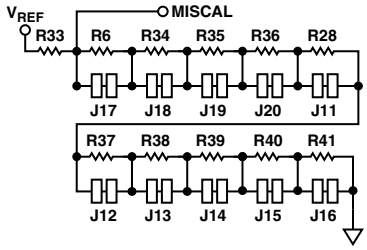

Figure 3. MISCAL Attenuation Network

After disconnecting the line voltage, ensure the load current is at I_B. Short one jumper at a time and measure CF. If the output frequency of CF is less than the calculated CF, keep that short and short the next jumper.

Normal Mode

The next signal to be calibrated is the line voltage. Again, set the load current to I_B. The network shown in Figure 4 allows the line voltage to be attenuated and adjusted in the range 190 mV rms to 363 mV rms with a resolution of 96 μV/LSB. This is achieved by using the binary weighted resistor chain R5, R31, R7 through R14. This will allow the meter to be accurately calibrated using a successive approximation technique. Starting with J2, each jumper is closed in order of ascendance. The output frequency for this sequence should be 5 A rms × 240 V rms × 0.027777 imp/kW × 32 or 1.067 Hz. If the calibration frequency on CF is exceeded when any jumper is closed, it should be opened again. All jumpers are tested with J10 being the last jumper.

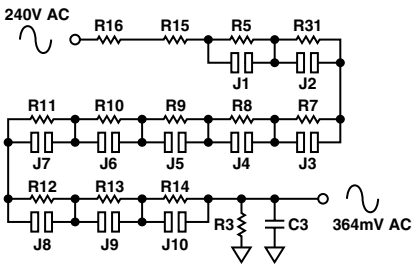

Figure 4. Line Attenuation Network

Since the ADE7761 transfer function is extremely linear, only calibrating the meter (at I_B) at unity power factor is needed. If the correct precautions have been taken at the design stage, no calibration will be necessary at low power factor (PF = 0.5). The following section discusses phase matching for correct calculation of energy at low power factor.

CORRECT PHASE MATCHING BETWEEN CHANNELS

The ADE7761 is internally phase-matched over the frequency range 40 Hz to 1 kHz between the two channels. Correct phase matching is important in an energy metering application because any phase mismatch between channels will translate into significant measurement error at low power factor. Figure 5 shows the voltage and current waveforms for an inductive load. In the example shown, the current lags the voltage by 60° (PF = –0.5). Assuming pure sinusoidal conditions, the power is easily calculated as

$$V\,rms \times I\,rms \times cos(60^\circ) \tag{8}$$

If, however, a phase error (ϕ_e) is introduced externally to the ADE7761, e.g., in the anti-alias filters, the error is calculated as

$$Phase\ Error = \frac{cos(\delta^\circ) - cos(\delta^\circ + \phi_e)}{cos(\delta^\circ)} \times 100\% \tag{9}$$

See note 3 in Table I where δ is the phase angle between voltage and current and ϕ_e is the external phase error. With a phase error of 0.2°, for example, the error at PF = 0.5 (60°) is calculated. As this example demonstrates, even a very small error will produce a large measurement error at low power factor.

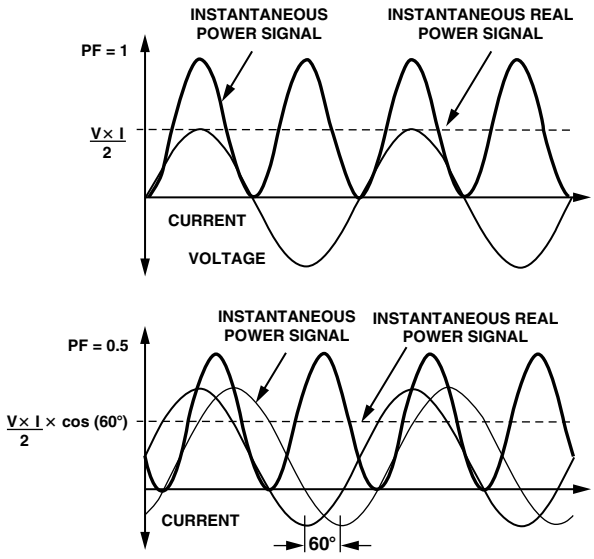

Figure 5. Voltage and Current (Inductive Load)

The topology of the attenuation network(s) is such that the phase-matching between Channel 1 and Channel 2 is preserved when it is calibrated. The –3 dB cutoff frequency of the network in Figure 4 is determined by R3 and C3. Even with all the jumpers closed, the resistance of R16 (330 kΩ), and R15 (330 kΩ) is still much greater than R3 (1 kΩ). Hence varying the resistance of the resistor chain will have little effect on the –3 dB cutoff frequency of the network maintaining the same phase.

ANTI-ALIAS FILTERS

As mentioned in the previous section, the anti-alias filters on Channel 1 and Channel 2 are one possible source of external phase errors. The anti-alias filters are low-pass filters that are placed before the analog inputs of any ADC. They are required to prevent a possible distortion due to sampling, called aliasing. Figure 6 illustrates the effects of aliasing.

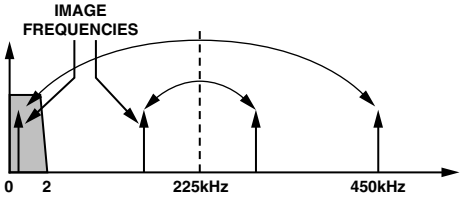

Figure 6. Aliasing Effects

Figure 6 shows how aliasing effects could introduce inaccuracies in an ADE7761-based meter design. The ADE7761 uses two Σ-Δ ADCs to digitize the voltage and current signals. These ADCs have a very high sampling rate, i.e., 450 kHz.

Figure 6 shows frequency components (arrows shown in black) above half the sampling frequency (also know as the Nyquist frequency), i.e., 450 kHz is imaged or folded back down below 225 kHz (arrows shown dashed). This

will happen with all ADCs no matter what the architecture. In the example shown it can be seen that only frequencies near the sampling frequency, i.e., 450 kHz, will move into the band of interest for metering, i.e., 0 kHz to 2 kHz. This will allow the use of a very simple LPF (low-pass filter) to attenuate these high frequencies (near 450 kHz) and so prevent distortion in the band of interest.

The simplest form of LPF is the simple RC filter. This is a single-pole filter with a roll-off or attenuation of –20 dB/dec.

Choosing the Filter –3 dB Cutoff Frequency

As well as having a magnitude response, all filters also have a phase response. The magnitude and phase response of a simple RC filter (R = 1 kΩ, C = 33 nF) are shown in Figure 7 and Figure 8. In Figure 7 the attenuation at 450 kHz for this simple LPF is approximately 40 dB. This is enough attenuation to ensure no ill effects due to aliasing.

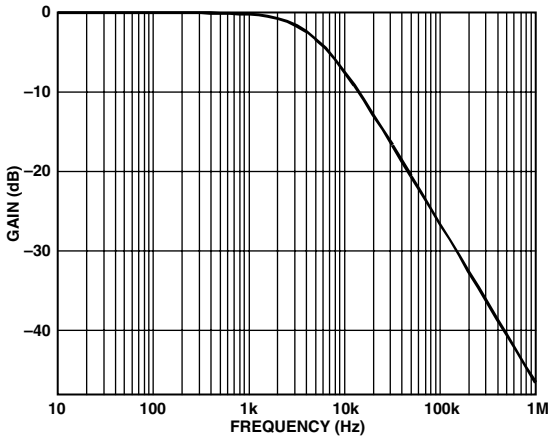

Figure 7. RC Filter Magnitude Response

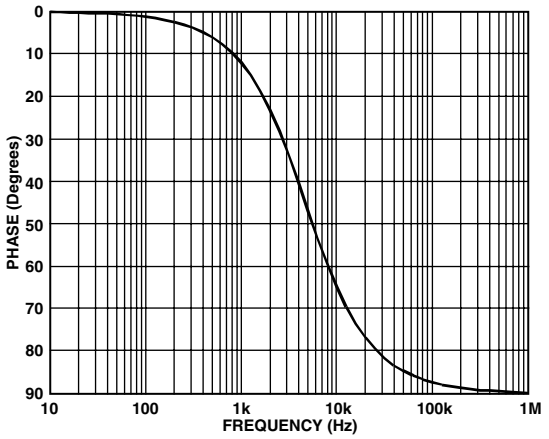

Figure 8. RC Phase Filter Response

As explained in the previous section, the phase response can introduce significant errors if the phase response of the LPFs on both Channel 1 and Channel 2 are not matched. Phase mismatch can easily occur due to poor component tolerances in the LPF. The lower the cutoff frequency in the LPF (anti-alias filter) the more pronounced these errors will be. Even with the corner frequency set at 4.7 kHz (R = 1 kΩ, C = 33 nF) the phase errors due to poor component tolerances can be significant. See Figure 9. The phase response for the simple LPF is shown at 50 Hz for R = 1 kΩ ± 10%, C = 33 nF ± 10%. Remember a phase shift of 0.2° can cause measurement errors of 0.6% at low power factor. This design uses resistors of 1% tolerance and capacitors of 10% tolerance for the anti-alias filters to reduce the possible problems due to phase mismatch.

Alternatively, the corner frequency of the anti-alias filter could be pushed out to 10 kHz to 15 Hz. However, the frequency should not be made too high because this could allow enough high frequency components to be aliased and thus cause accuracy problems in a noisy environment.

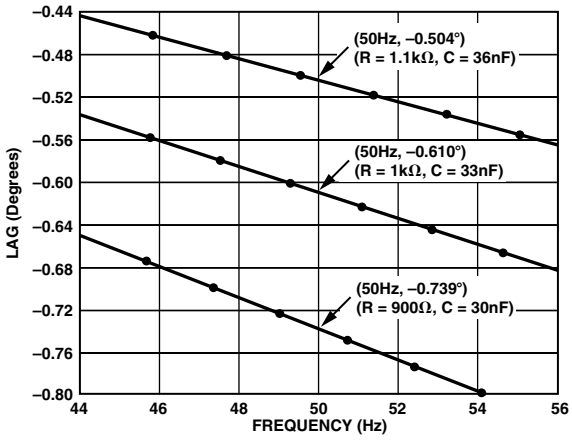

Figure 9. Phase Shift at 50 Hz Due to Component Tolerances

Note that this is also why precautions are taken with the design of the calibration network on Channel 2 (voltage channel). Calibrating the meter by varying the resistance of the attenuation network will not vary the cutoff frequency and therefore the phase response of the network on Channel 2. See Correct Phase Matching Between Channels section. Figure 10 is a plot of phase lag at 50 Hz when the resistance of the calibration network is varied from 660 kΩ (J1–J10 closed) to 1.26 MΩ (J1–J10 open). Note that the variation in phase is less than 0.4 m degrees.

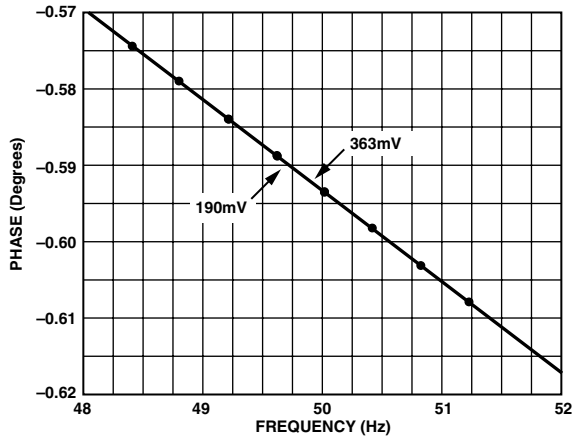

Figure 10. Phase Shift Due to Calibration

Current Transformer

The current transformers for this design should be selected to maximize the use of the dynamic range on Channels V1A and V1B. Selecting the right current transformer is crucial to ensure good linearity of the meter over the selected dynamic range. There are several important considerations when picking a current transformer for the application. First, a CT must be selected that has good linearity over the dynamic range of interest. CT manufacturers often recommend that the burden resistance be as small as possible to preserve linearity over a large current range. A burden resistance of less than 15 Ω is used for this application.

Second, the CT introduces a phase shift between the primary and secondary current. This phase shift should be kept to a minimum. A small phase shift at a power factor of 0.5 can contribute to a significant error. Note that at a power factor of 0.5, a phase shift as low as 0.1° can produce an error as much as 0.3% in the reading. In this design, the phase of the voltage channel is shifted to match the phase shift in the current channel caused by the current transformers. This is accomplished by moving the corner frequency of the anti-aliasing filter in the voltage channel. See the Corrected Phase Matching between Channels and Anti-Alias Filters sections in this application note.

ADE7761 Reference

The on-chip reference circuit for the ADE7761 has a temperature coefficient of typically 40 ppm/°C. On Grade A parts this specification is not guaranteed and may be as high as 80 ppm/°C. An optional external reference may be used. Connecting it to the REF In and REF Out pins will improve the accuracy over temperature.

Oscillator Stability

The integrated oscillator circuitry is designed to be stable over temperature and power supply variation. The initial oscillator frequency is determined by the value of the voltage reference and the RCLKIN resistor. Variation in reference drift is rejected by the unique architecture of the oscillator circuitry. A variation of the RCLKIN resistor value will cause a shift in the oscillator frequency, therefore, a low temperature coefficient resistor is recommended.

NO LOAD THRESHOLD

The ADE7761 has on-chip anticreep functionality. The ADE7761 will not produce a pulse on CF, F1, or F2 if the output frequency falls below a certain level. This feature ensures that the energy meter will not register energy when no load is connected. IEC 61036 (2000-09) Section 4.6.4 specifies the start-up current as being not more that 0.4% I_B at PF = 1.

The starting current for the ADE7761 is based on 0.0045% of max F1 or 0.0045% × 0.68 Hz = 0.000031 Hz. Using 100 imp/kWh, this is equivalent to 1.12 W. For this design at 240 V, the starting current is 4.65 mA. The IEC specification is for a start-up current of 20 mA.

POWER SUPPLY DESIGN

The power supply design for the ADE7761 meter is based on both a capacitor divider network (PS1) and a full wave rectifier (PS2). There are three modes of operation for the meter using the ADE7761; normal mode, earth fault, and missing neutral mode. The meter uses the capacitor divider supply, while in either the normal or earth fault mode. If the meter goes into the missing neutral mode, power is supplied to the ADE7761 through a current transformer and a full wave rectifier circuit. This section describes both power supplies.

In order to design the supply, the load for the meter must be determined. The supply current for the ADE7761 is less than 4 mA. In addition to the ADE7761, current must be provided to drive the stepper motor. A 400 Ω stepper will draw 12 mA while it is on; however, the maximum frequency it switches at is 0.2667 Hz (see Design Equations section). The pulse is 120 ms/F1, F2 or a total of 240 ms of 12 mA current at 0.2667 Hz. This is an average current of less than 1 mA. An additional current is needed for the LED at 4 mA at a maximum CF of 8.53 Hz for 90 ms or 3 mA at full-scale input. An additional milliamp is allowed for the voltage regulator quiescent current. The total power needed for the supply is 9 mA.

CAPACITOR DIVIDER SUPPLY

Supply PS1 provides power through a high voltage capacitor (C17, Figure 11), which is connected to phase. This capacitor provides the charging current through a diode to a large storage capacitor. A low voltage dropout regulator is used to provide the regulated 5 V supply for the meter.

Figure 11 is the schematic for the power supply. This circuit works as long as a return path for the current is provided through ground. If the meter ground (neutral) is disconnected, there is no current return path for the supply and the capacitor divider circuit shuts down. When the AD7761 determines that there is no zero crossing in the phase signal, the ADE7761 goes in to missing neutral mode. The power supply for the capacitor divider supply ceases to operate.

In this supply, capacitor C18 is used to store charge for the voltage regulator. C17 provides the charge through R21. During the positive half-cycle of the line, D3 clamps the voltage on C18 preventing it from exceeding the maximum input voltage to the regulator. On the negative half-cycle, the diodes D2 and D10 are active. D2 blocks the line from C18 preventing it from discharging. D10 is used to charge C17 during the negative half-cycle through ground.

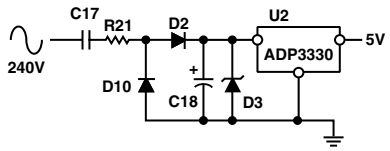

Figure 11. Capacitor Divider Supply (PS1)

CURRENT TRANSFORMER SUPPLY

In missing neutral mode, the capacitor divider supply no longer works because it is missing a return path back to neutral. A current transformer is connected with both phase and neutral through the primary (see Figure 12.) The opposing fields through the primary cancel each other; therefore, the supply is off. If neutral is disconnected to the meter, the output of the current transformer is now proportional to the load current going through phase. See Figure 12.

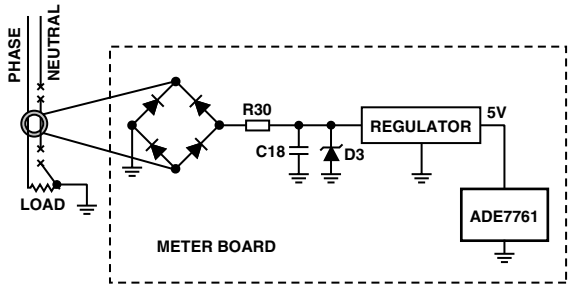

Figure 12. Current Transformer Supply (PS2)

A cheap current transformer for this supply is selected to have a core with high permeability. The core acts as a power transformer providing an ac signal in the secondary. This signal is rectified and filtered by the input capacitor to the voltage regulator.

For this design a CrGo CT core is used. The **C**old-**r**olled **G**rain-**o**riented silicon steel alloy provides low core loss and high permeability needed for transformers. The turns ratio for the current transformer is 2:300. As a result, the secondary current for the transformer at I_B is 33 mA. This is sufficient for the power supply to power the meter. If the load current increases, the secondary current will also increase. This increase is additional current that will have to be dissipated in the power supply. By using a core that is allowed to saturate, the current in the secondary is limited. The resistor R30 (Figure 12) is used to help saturate the core of the current transformer.

DESIGN FOR IMMUNITY TO ELECTROMAGNETIC DISTURBANCE

In Section 4.5 of IEC 61036, it is stated that "the meter shall be designed in such a way that conducted or radiated electromagnetic disturbances as well as electrostatic discharge do not damage nor substantially influence the meter." The considered disturbances are:

- Electrostatic discharge
- Electromagnetic HF fields
- Fast transience burst
- Power line surge

All of the precautions and design techniques (e.g., ferrite beads, capacitor line filters, physically large SMD resistors, PCB layout including grounding) contribute to a certain extent in protecting the meter electronics from each form of electromagnetic disturbance. Some precautions (e.g., ferrite beads), however, play a more important role in the presence of certain kinds of disturbances (e.g., RF and fast transience burst). The following sections discuss the disturbances listed above and what protection has been put in place.

ELECTROSTATIC DISCHARGE (ESD)

Although many sensitive electronic components contain a certain amount of ESD protection on-chip, it is not possible to protect against the kind of severe discharge described below. Another problem is that the effect of an ESD discharge is cumulative, i.e., a device may survive an ESD discharge, but there is no guarantee that it will survive multiple discharges at some stage in the future. The best approach is to eliminate or attenuate the effects of the ESD event before it comes in contact with sensitive electronic devices. This holds true for all conducted electromagnetic disturbances.

Very often no additional components are necessary to protect devices. With a little care, those components already required in the circuit can perform a dual role. For example, the meter must be protected from ESD events at those points where it comes in contact with the outside world, e.g., the connection to the shunt. Here, the ADE7761 is connected to the shunt via two LPFs (anti-alias filters), which are required by the ADC (see Anti-Alias Filters section). This RC filter can also be enough to protect against ESD damage to CMOS devices. However, some care must be taken with the type of components used. For example, the resistors should not be wire-wound as the discharge will simply travel across them. The resistors should also be physically large to stop the discharge from arcing across the resistor. In this design, 1/8W SMD 1206 resistors were used in the anti-alias filters. Ferrite beads can also be effective when placed in series with the connection to the shunt. A ferrite choke is particularly effective at slowing the fast rise time of an ESD current pulse. The high frequency transient energy is absorbed in the ferrite material rather than being diverted or reflected to another part of the system. The PSU circuit is also directly connected to the terminals of the meter. Here, the discharge will be dissipated by the ferrite, the input capacitor (C17), and the rectification diodes D2 and D3. The analog input V2P is protected by the large impedance of the attenuation network that is used for calibration.

Another very common low cost technique employed to arrest ESD events is to use a spark gap on the component side of the PCB (see Figure 13). However, since the meter will likely operate in an open air environment and be subject to many discharges, this is not recommended at sensitive nodes like the shunt connection. Multiple discharges could cause carbon buildup across the spark gap, which could cause a short or introduce an impedance that will in time affect accuracy. A spark gap was introduced in the PSU after the MOV to take care of any very high amplitude/fast rise time discharges.

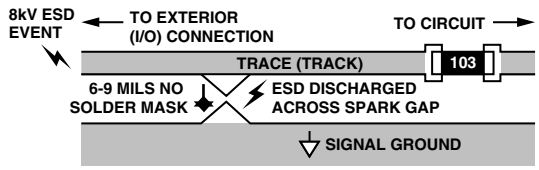

Figure 13. Spark Gap to Arrest ESD Events

ELECTROMAGNETIC HF FIELDS

Testing was carried out according to IEC 61000-4-3. Susceptibility of integrated circuits to RF tends to be more pronounced in the 20 MHz to 200 MHz region. Frequencies higher than this tend to be shunted away from sensitive devices by parasitic capacitances. In general, at the IC level, the effects of RF in the 20 MHz to 200 MHz region will tend to be broadband in nature, i.e., no individual frequency is more troublesome than another. However, there may be higher sensitivity to certain frequencies due to resonances on the PCB. These resonances could cause insertion gain at certain frequencies, which, in turn, could cause problems for sensitive devices. By far the greatest RF signal levels are those coupled into the system via cabling. These connection points should be protected. Some techniques for protecting the system are to:

- Minimize bandwidth
- Isolate sensitive parts of the system

Minimizing Bandwidth

In this application, the required analog bandwidth is only 2 kHz. This is a significant advantage when trying to reduce the effects of RF. The cable entry points can be low-pass filtered to reduce the amount of RF radiation entering the system. The shunt output is already filtered before being connected to the ADE7761. This is to prevent aliasing effects that were described earlier. By choosing the correct components and adding some additional components (e.g., ferrite beads), these anti-alias filters can double as very effective RF filters. Figure 6 shows a somewhat idealized frequency response for the anti-alias filters on the analog inputs. When considering higher frequencies (e.g., >1 MHz), the parasitic reactive elements of each lumped component must be considered. Figure 14 shows the anti-alias filters with the parasitic elements included. These small values of parasitic capacitance and inductance become significant at higher frequencies and, therefore, must be considered.

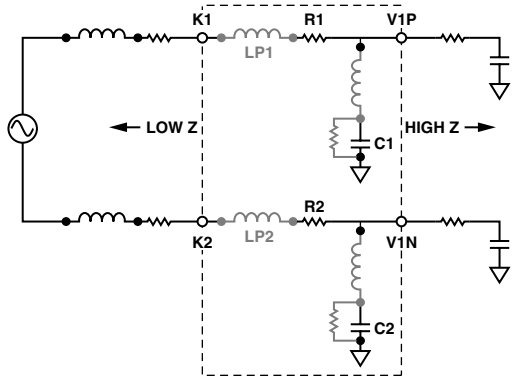

Figure 14. Anti-Alias Filters Showing Parasitics

Parasitics can be kept at a minimum by using physically small components with short lead lengths (i.e., surface mount). Because the exact source impedance conditions are not known (this will depend on the source impedance of the electricity supply), some general precautions should be taken to minimize the effects of potential resonances. These resonances include the resonance of capacitors as well as parasitic components in the layout. Resonances that result from the interaction of the source impedance and filter networks could cause insertion gain effects and so increase the exposure of the system to RF radiation at certain (resonant) frequencies. Figure 14 illustrates the lossy parasitics of a capacitor as seen in C1 and C2. As much as 0.8 nH can cause a zero in the anti-alias filter response at frequencies on the order of 100 MHz. Adding a series inductance to the inputs will further reduce the susceptibility to high frequency signals from either EFT, surge, or ESD events. Ferrite beads added in series with the anti-alias filter will perform quite well in this respect. In this application a series inductor was added to the line input. This helps reject any high frequency signals to the line such as electrical fast transients (EFT).

ELECTRICAL FAST TRANSIENTS (EFT)

The EFT pulse can be particularly difficult to guard against because the disturbance is conducted into the system via external connections, e.g., power lines. Figure 15 shows the physical properties of the EFT pulse used in IEC 61000-4-4. Perhaps the most debilitating attribute of the pulse is not its amplitude (which can be as high as 4 kV), but the high frequency content due to the fast rise times involved. Fast rise times mean high frequency content which allows the pulse to couple to other parts of the system through stray capacitance, among other things. Large differential signals can be generated by the inductance of PCB traces and signal ground. These large differential signals could interrupt the operation of sensitive electronic components. Digital systems are generally most at risk because of data corruption. Minimizing trace lengths and use of ground planes reduces the susceptibility to these high frequency pulses.

Analog electronic systems tend to be affected only for the duration of the disturbance. As the bandwidth of the analog sections tends to be limited, the effect of an EFT event is reduced.

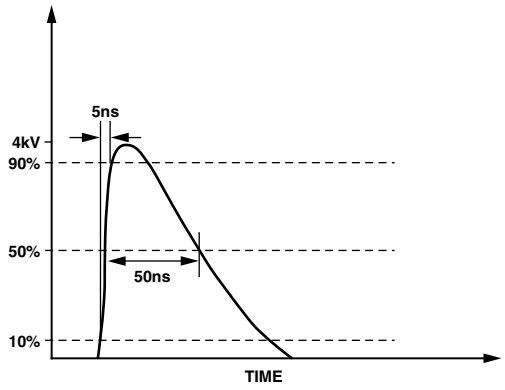

Figure 15. Single EFT Pulse Characteristics

Another possible issue with conducted EFT is that the effects of the radiation will, like ESD, generally be cumulative for electronic components. The energy in an EFT pulse can be as high as 4 mJ and deliver 40 A into a 50 Ω load (see Figure 19). Therefore, continued exposure to EFT due to inductive load switching, among other things, may have implications for the long-term reliability of components. The best approach is to protect those parts of the system that could be sensitive to EFT.

The protection techniques described in the previous section (Electromagnetic HF Fields) also apply equally well in the case of EFT. The electronics should be isolated as much as possible from the source of the disturbance through PCB layout (i.e., moating) and filtering signal and power connections. In addition, the input capacitor to the power supply provides a low impedance shunt to an EFT pulse. A Zener completes the low impedance path to ground for the EFT pulse.

A varistor or metal oxide varistor (MOV) can be used to add protection. This device acts as a nonlinear voltage-dependent resistor. See the following section for a description of this device.

Care should be taken to minimize trace lengths in the power supply to reduce the effect of parasitic trace inductance. Stray inductance due to leads and PCB traces will mean that the MOV will not be as effective in attenuating the differential EFT pulse. The MOV is very effective in attenuating high energy, relatively long duration disturbances due to lightning strikes for example.

MOV TYPE S20K275

The MOV used in this design is type S20K275 from Siemens. An MOV is a voltage-dependant resistor whose resistance decreases with increasing voltage. It is typically connected in parallel with the device or circuit being protected. During an overvoltage event, it forms a low resistance shunt and thus prevents any further rise in the voltage across the circuit being protected. The overvoltage is essentially dropped across the source impedance of the overvoltage source, e.g., the mains network source impedance. Figure 16 illustrates the principle of operation.

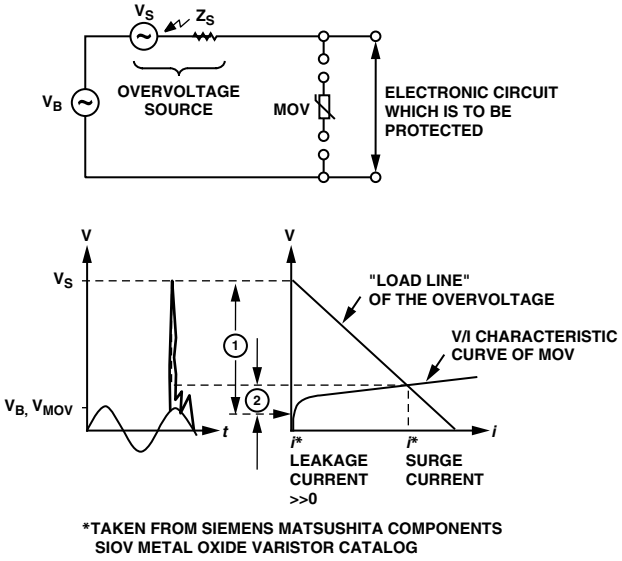

Figure 16. Principle of MOV Overvoltage Protection

Figure 16 shows how the MOV voltage and current can be estimated for a given overvoltage and source impedance. A load line (open-circuit voltage, short-circuit current) is plotted on the same graph as the MOV characteristic curve. Where the curves intersect, the MOV clamping voltage and current can be read. Note that care must be taken when determining the short circuit current. The frequency content of the overvoltage must be taken into account as the source impedance (mains) may vary considerably with frequency. A typical impedance of 50 Ω is used for mains source impedance during fast transience (high frequency) pulse testing. The following section discusses IEC 61000-4-4 and IEC 61000-4-5, which are transience and overvoltage EMC compliance tests.

IEC 61000-4-4 and the S20K275

While the graphic technique just described is useful, a better approach is to use simulation to obtain a better understanding of MOV operation. EPCOS components provide PSPICE models for all their MOVs and these are very useful in determining device operation under the various IEC EMC compliance tests. For more information on EPCOS PSPICE models and their applications, visit www.epcos.com.

The purpose of IEC 61000-4-4 is to determine the effect of repetitive, low energy, high voltage, fast rise time pulses on an electronic system. This test is intended to simulate transient disturbances such as those originating from switching transience (e.g., interruption of inductive loads or relay contact bounce).

Figure 17 shows an equivalent circuit intended to replicate the EFT test pulse as specified in IEC 61000-4-4. The generator circuit is based on Figure 1 IEC 61000-4-4 (1995-01). The characteristics of operation are:

- Maximum energy of 4 mJ/pulse at 2 kV into 50 Ω
- Source impedance of 50 Ω ± 20%
- Pulse rise time of 5 ns ± 30%
- Pulse duration (50% value) of 50 ns ± 30%
- Pulse shape as shown in Figure 23

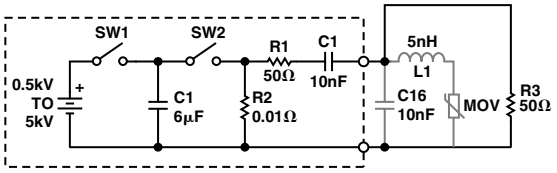

Figure 17. EFT Generator

The simulated output of this generator delivered to a purely resistive 50 Ω load is shown in Figure 18. The open-circuit output pulse amplitude from the generator is 4 kV. Therefore, the source impedance of the generator is 50 Ω as specified by the IEC 61000-4-4, i.e., ratio of peak pulse output unloaded and loaded (50 Ω) is 2:1.

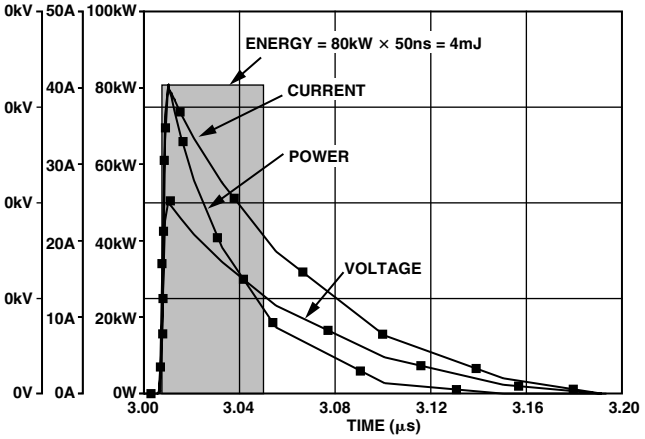

Figure 18. EFT Generator Output into 50 Ω (No Protection)

Figure 18 also shows the current and instantaneous power (V × I) delivered to the load. The total energy is the integral of the power and can be approximated by the rectangle method as shown. It is approximately 4 mJ at 2 kV per specification. Figure 19 shows the generator output into 50 Ω load with the MOV and some inductance (5 nH). This is included to take into account stray inductance due to PCB traces and leads. Although the simulation result shows that the EFT pulse has been attenuated (600 V) and most of the energy being absorbed by the MOV (only 0.8 mJ is delivered to the 50 Ω load), it should be noted that stray inductance and capacitance could render the MOV useless. For example, Figure 20 shows the same simulation with the stray inductance increased to 1 μH, which could easily happen if proper care is not taken with the layout. The pulse amplitude reaches 2 kV once again.

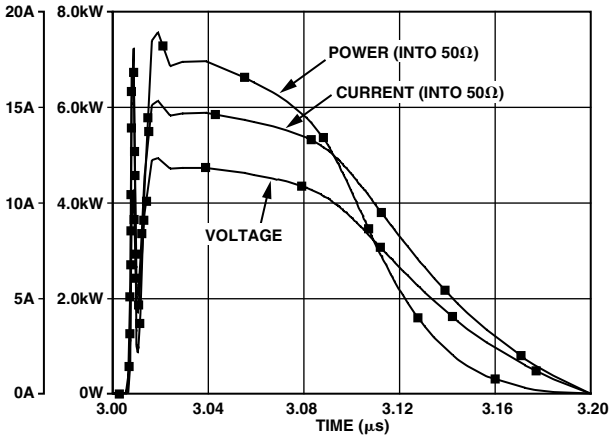

Figure 19. EFT Generator Output into 50 Ω with MOV in Place

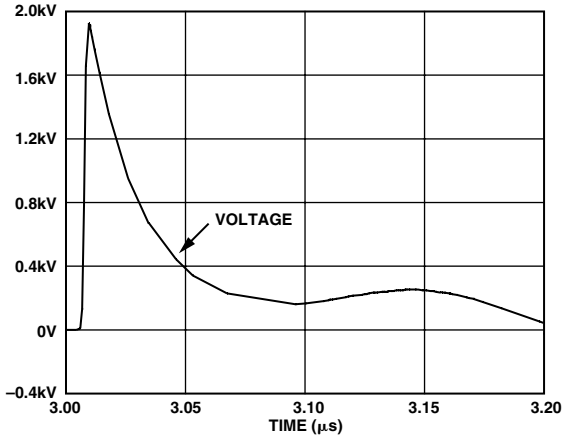

Figure 20. EFT Generator Output into 50 Ω with MOV in Place and Stray Inductance of 1 μH

In this application particular attention is paid to trace lengths, spark gaps, and isolating various signals. Adding a high voltage 10 nF input capacitor can also help reduce the high frequency content of the EFT pulse. In this design, the performance met the IEC specifications and therefore the capacitor was not used. Stray inductance was kept to a minimum for this design by keeping all leads short and using a ground plane.

IEC 61000-4-5

The purpose of IEC 61000-4-5 is to establish a common reference for evaluating the performance of equipment when subjected to high energy disturbances on the power and interconnect lines. Figure 21 shows a circuit that was used to generate the combinational wave (hybrid) pulse described in IEC 61000-4-5. It is based on the circuit shown in Figure 1 of IEC 61000-4-5 (2001-04).

Such a generator produces a 1.2 μs/50 μs open-circuit voltage waveform and an 8 μs/20 μs short-circuit current waveform, which is why it is referred to as a hybrid generator. The surge generator has an effective output impedance of 2 Ω. This is defined as the ratio of peak open-circuit voltage to peak short-circuit current.

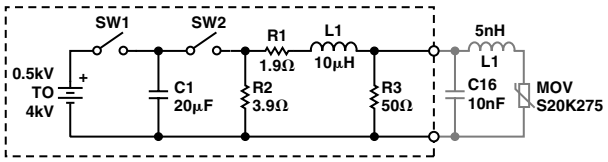

Figure 21. Surge Generator (IEC 61000-4-5)

Figure 22 shows the generator voltage and current output waveforms. The characteristics of the combination wave generator are as follows:

- Open-circuit voltage
  - 0.5 kV to at least 4.0 kV
  - Waveform as shown in Figure 22
  - Tolerance on open-circuit voltage is ±10%

- Short-circuit current
  - 0.25 kA to 2.0 kA
  - Waveform as shown in Figure 31
  - Tolerance on short-circuit current is ±10%
- Repetition rate of at least 60 seconds

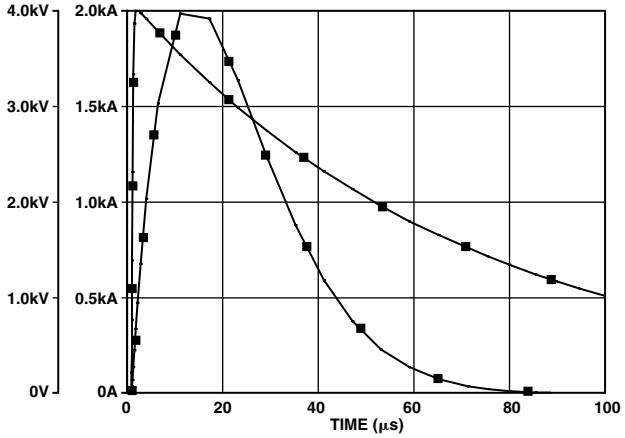

Figure 22. Open-Circuit Voltage/Short-Circuit Current

The MOV is very effective in suppressing these kinds of high energy/long duration surges. Figure 23 shows the voltage across the MOV when it is connected to the generator as shown in Figure 21. Current and instantaneous power waveforms are also shown. The energy absorbed by the MOV is readily estimated using the rectangle method as illustrated.

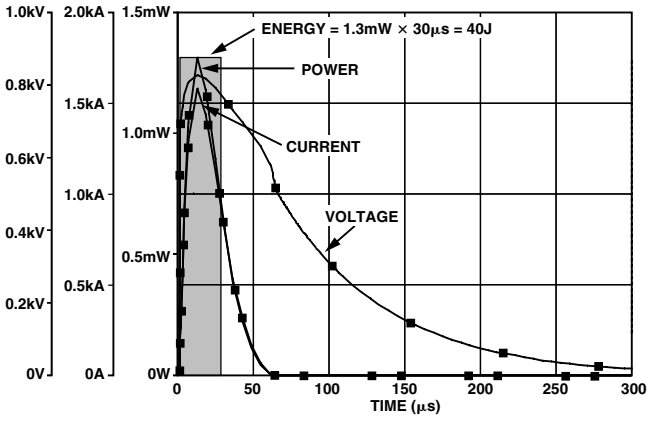

Figure 23. Energy Absorbed by MOV During 4 kV Surge

Derating the MOV Surge Current

The maximum surge current (and, therefore, energy absorbed) that an MOV can handle is dependent on the number of times the MOV will be exposed to surges over its lifetime. The life of an MOV is shortened every time it is exposed to a surge event. The data sheet for an MOV device will list the maximum nonrepetitive surge current for an 8 μs/20 μs current pulse. If the current pulse is of longer duration, and if it occurs more than once during the life of the device, this maximum current must be derated. Figure 24 shows the derating curve for the S20K275. Assuming exposures of 30 μs duration, and a peak current shown in Figure 23, the maximum number of surges the MOV can handle before it goes out of specification is about 10. After repeated loading (10 times in the case just described) the MOV voltage will change. After initially increasing, it will rapidly decay.

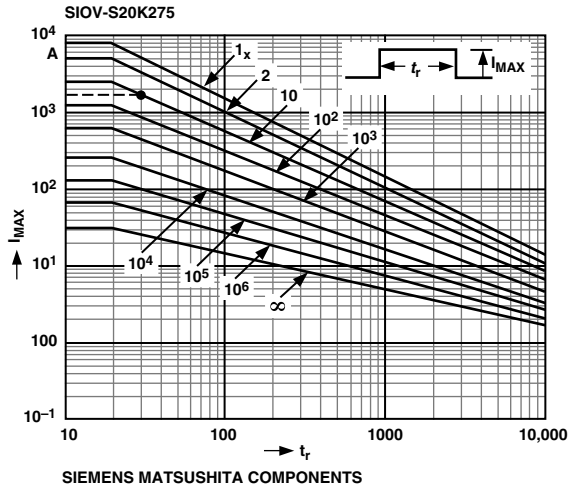

Figure 24. Derating Curve for S20K275

PCB DESIGN

Both susceptibility to conducted or radiated electromagnetic disturbances and analog performance were considered at the PCB design stage. Fortunately, many of the design techniques used to enhance analog and mixed-signal performance also lend themselves well to improving the EMI robustness of the design. The key point is to isolate that part of the circuit which is sensitive to noise and electromagnetic disturbances. Since the ADE7761 carries out all the data conversion and signal processing, the robustness of the meter will be determined to a large extent by how well protected the ADE7761 is.

Layout for maximizing surge immunity is critical. Distances between traces and various components on the board can affect the overall performance for high voltage immunity. The material used in this application is proprog with a dielectric strength of 1000 V/mil. Spacing around the high voltage traces was increased to minimize breakdown of the insulation during a high voltage event. Additional precautions include spacing between various components. The air gap between components has a dielectric strength of 75 V/mil, far less than the proprog. For this reason, any exposed leads or components should be spaced 100 mils apart for a breakdown voltage of 7500 V. Placing components too close together can cause a breakdown between components. During manufacturing, additional steps should be taken to ensure the circuit board is cleaned of impurities. This minimizes any resistive paths that may cause a leakage path during a high voltage event.

In order to ensure accuracy over a wide dynamic range, the data acquisition portion of the PCB should be kept as quiet as possible, i.e., minimal electrical noise. Noise will cause inaccuracies in the analog-to-digital conversion process that takes place in the ADE7761. One common source of noise in any mixed-signal system is the ground return for the power supply. Here high frequency noise (from fast edge rise times) can be coupled into the analog portion of the PCB by the common impedance of the ground return path. Figure 25 illustrates the mechanism.

One common technique used to overcome this problem is to use separate analog and digital return paths for the supply. Every effort should be made to keep the impedance of these return paths as low as possible. A circuit board can have trace inductance on the order of 33 nH/inch which can increase the sensitivity to high frequency signals. As shown in Figure 25, a common path for the ground currents can couple between the digital and analog sections of the meter. Decoupling signals to a narrow ground trace can in effect couple unwanted noise to other parts of the circuit. In the PCB design for the ADE7761, a ground plane was used to minimize the impedance of these return paths. High frequency noise sources from the digital circuit were decoupled as close to the ADE7761 as possible with high frequency ceramic capacitors. It should be noted that large capacitors such as aluminum electrolytics will not work because they have a typical residual series inductance of 6.8 nF which tends to reduce the decoupling effect of the capacitor at high frequencies.

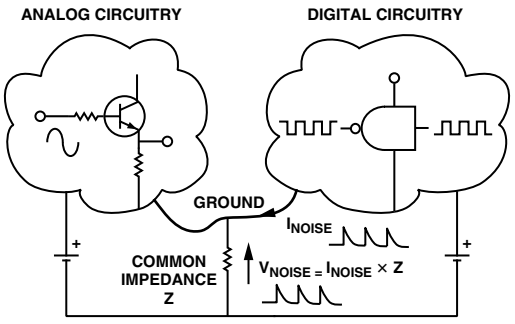

Figure 25. Noise Coupling via Ground Return Impedance

The power supply portion of the PCB is the only place where both phase and neutral wires are connected. Since the PSU is capacitor-based, a substantial current will flow in the ground return back to the phase wire (system ground). This portion of the PCB contains the transience suppression circuitry (MOV, ferrite, etc.) and power supply circuitry. The length of the path for the power supply return current is kept to a minimum to isolate it from the analog circuitry.

The ADE7761 and sensitive signal paths are located in a quiet part of the board that is isolated from the noisy elements of the design, such as the power supply and flashing LED, among other things. The ground currents from the power supply are at the same frequency as the signals being measured and could cause accuracy issues (e.g., crosstalk between the PSU as analog inputs) if care is not taken with the routing of the return current. Also, part of the attenuation network for Channel 2 (the voltage channel) is in the power supply portion of the PCB. This helps to eliminate possible crosstalk to Channel 1 by ensuring analog signal amplitudes are kept as low as possible in the analog (quiet) portion of the PCB. Remember that with a burden resistor of 14.8 Ω, the input voltage signal on Channel 1 is 29 mV rms at I_B.

METER ACCURACY/TEST RESULTS

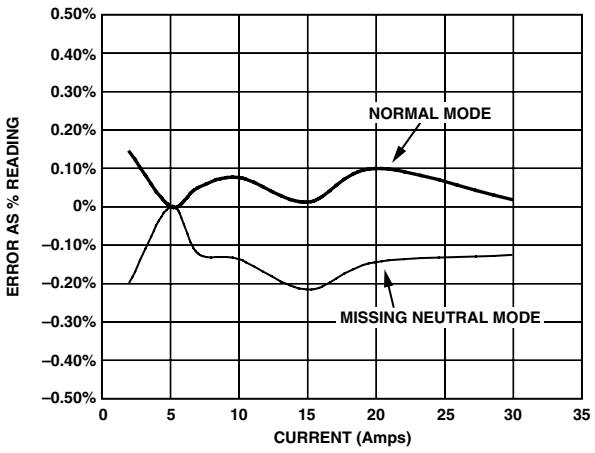

Figure 26. ADE7761 Reference Design Linearity

Bill of Materials

Parts	Details	Comments
C1, C2, C3, C4, C9	Chip Cap 0.033 µF Case 0805	Digi-Key Part No. PCC1834CT-ND
C5, C7, C10, C12, C14, C15	Chip Cap 0.1 µF Case 0805	Digi-Key Part No. BC1300CT-ND
C6, C13	Cap 10 µF ACASE 6.3 V	Digi-Key Part No. PCS1106CT-ND
C17	Cap 0.47 µF CR1K2400	Digi-Key Part No. EF6474-ND
C18	Cap 470 µF CAPT394-35 V	Digi-Key Part No. P5554-ND
D1, D4, D5	HLMPD150 LED Case DIOT1-34	Digi-Key Part No. HLMPD150A-ND
D2, D6, D7, D8, D9, D10	1N4004 Case DO41 Diode	Digi-Key Part No. 1N4004DICT-ND
D3	1N4739 Case DO41 Zener Diode	Digi-Key Part No. 1N4739ADICT-ND
R1, R2, R3, R4, R17, R24	1 kΩ, 1%, Case 0805, 1/8 W	Digi-Key Part No. 311-1.00KCCT-ND
R5	300 kΩ, 1%, Case 2020, 1/2 W	Digi-Key Part No. P301KACCT-ND
R6	110 kΩ, 1%, Case 0805, 1/8 W	Digi-Key Part No. 311-150KCCT-ND
R7	75 kΩ, 1%, Case 0805, 1/8 W	Digi-Key Part No. 311-75.0KCCT-ND
R8	39 kΩ, 1%, Case 0805, 1/8 W	Digi-Key Part No. 311-39.0KCCT-ND
R9	18 kΩ, 1%, Case 0805, 1/8 W	Digi-Key Part No. 311-18.0KCCT-ND
R10	9.1 kΩ, 1%, Case 0805, 1/8 W	Digi-Key Part No. 311-9.10KCCT-ND
R11	5.1 kΩ, 1%, Case 0805, 1/8 W	Digi-Key Part No. 311-5.10KCCT-ND
R12	2.2 kΩ, 1%, Case 0805, 1/8 W	Digi-Key Part No. 311-2.20KCCT-ND
R13	1.2 kΩ, 1%, Case 0805, 1/8 W	Digi-Key Part No. 311-1.20KCCT-ND
R14	560 Ω, 1%, Case 0805, 1/8 W	Digi-Key Part No. 311-560CCT-ND
R15, R16	330 kΩ, 1%, Case 2010, 1/2 W	Digi-Key Part No. P330KACCT-ND
R18, R22, R29	2 kΩ, 1%, Case 1206, 1/4 W	Digi-Key Part No. 311-2.00KFCT-ND
R19, R20	20 Ω, Case 0805, 1/8 W	Digi-Key Part No. 311-20.0CCT-ND
R21	470 Ω, 5%, Case 32, 1 W	Digi-Key Part No. P470W-1BK-ND
R23	6.2 kΩ, 0.5%, Case 0805, 1/8 W ± 25 ppm	Digi-Key Part No. RR12P6.2KDCT-ND

Parts	Details	Comments
R25, R26, R27, R32	14.7 Ω, 1%, Case 0805, 1/8 W	Digi-Key Part No. 311-14.7CCT-ND
R28	6.2 kΩ, 1%, Case 0805, 1/8 W	Digi-Key Part No. 311-6.20KCCT-ND
R30	470 Ω, 2 W	Digi-Key Part No. P470W-1BK-ND
R31	150 kΩ, 1%, Case 0805, 1/8 W	Digi-Key Part No. 311-150KCCT-ND
R33	560 kΩ, 1%, Case 0805, 1/8 W	Digi-Key Part No. 311-560KCCT-ND
R34	56 kΩ, 1%, Case 0805, 1/8 W	Digi-Key Part No. 311-56.0KCCT-ND
R35	27 kΩ, 1%, Case 0805, 1/8 W	Digi-Key Part No. 311-27.0KCCT-ND
R36	12 kΩ, 1%, Case 0805, 1/8 W	Digi-Key Part No. 311-12.0KCCT-ND
R37	3 kΩ, 1%, Case 0805, 1/8 W	Digi-Key Part No. 311-3.00KCCT-ND
R38	1.5 kΩ, 1%, Case 0805, 1/8 W	Digi-Key Part No. 311-1.50KCCT-ND
R39	750 Ω, 1%, Case 0805, 1/8 W	Digi-Key Part No. 311-750CCT-ND
R40	330 Ω, 1%, Case 0805, 1/8 W	Digi-Key Part No. 311-330CCT-ND
R41	160 Ω, 1%, Case 0805, 1/8 W	Digi-Key Part No. 311-160CCT-ND
U1	ADE7761 SSOP-20	
U2	ADP3330	
U3	PS250 Opto-isolator Case DIP04	Digi-Key Part No. PS2501-1-ND
Z1, Z2 (Z2 No-Stuff)	Filter Choke LA600140	Digi-Key Part No. P9818BK-ND
MOV1	140 J MOV VAR9026	Siemens S20K275

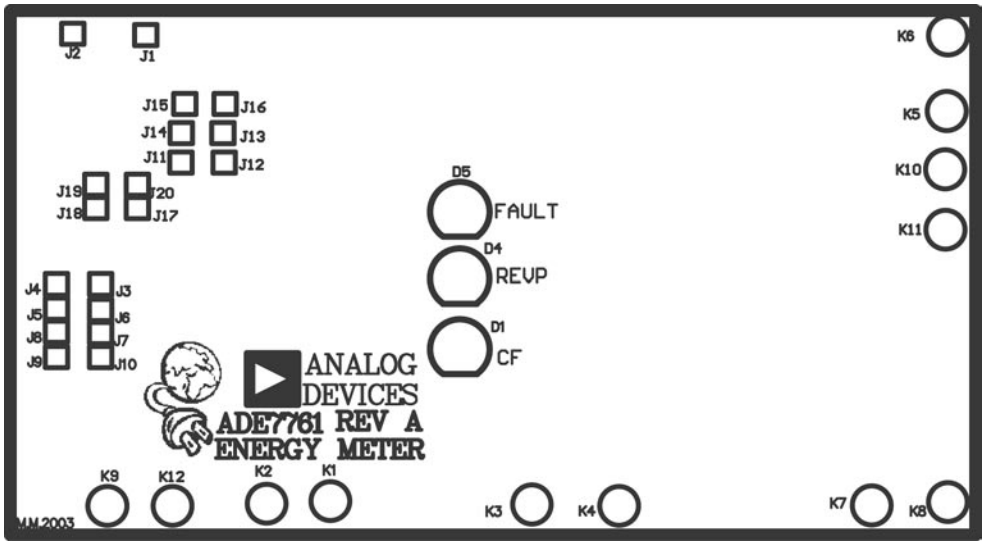

Figure 27. PCB Assembly (Top Layer)

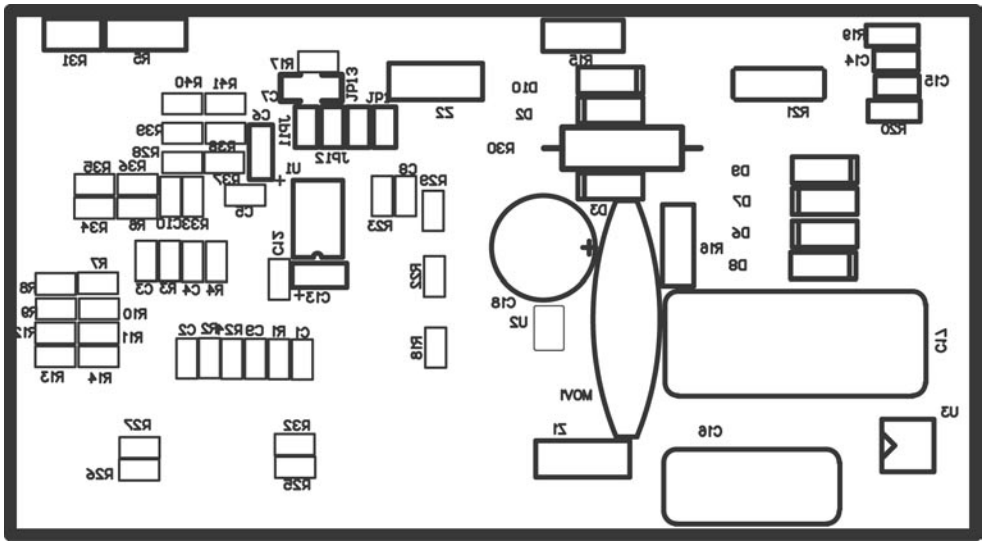

Figure 28. PCB Assembly (Bottom Layer)

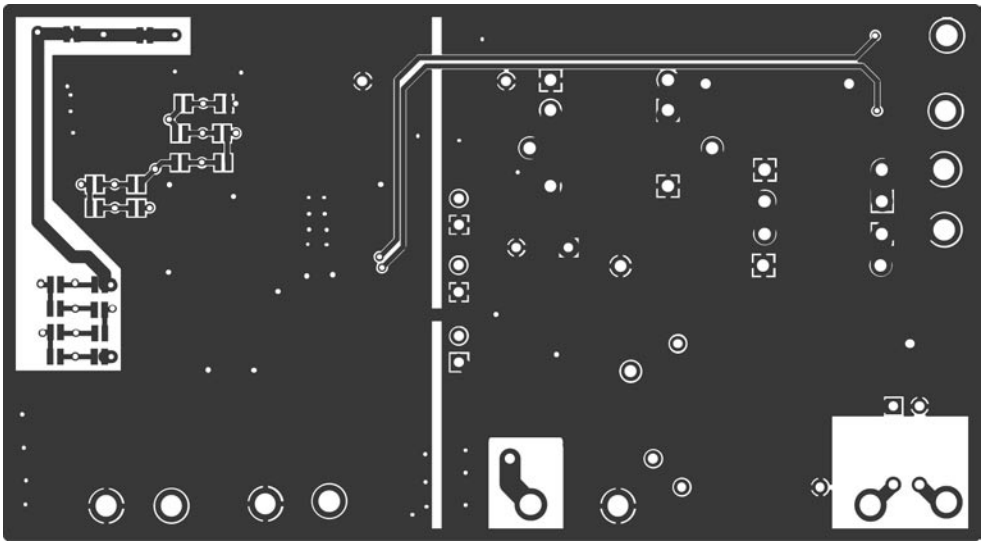

Figure 29. PCB (Top Layer)

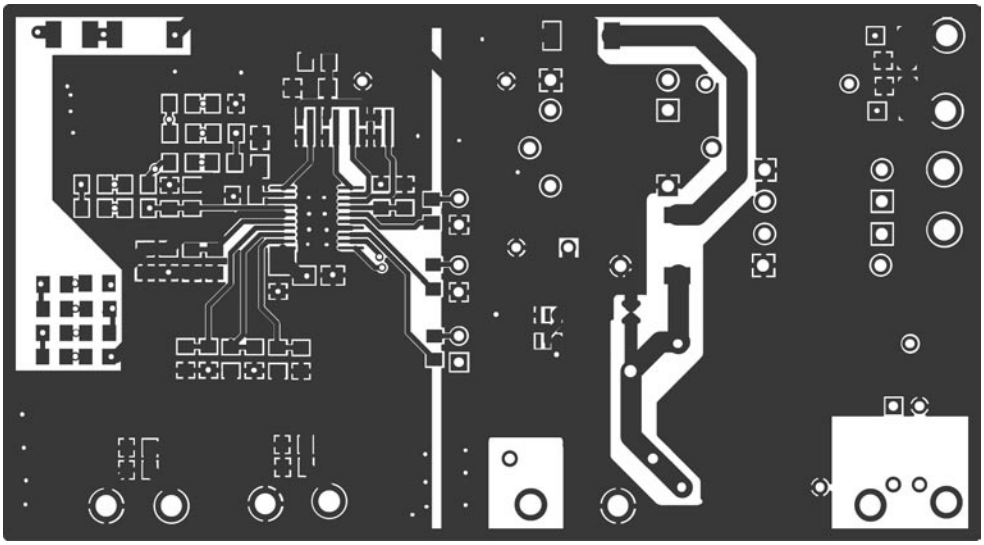

Figure 30. PCB (Bottom Layer)

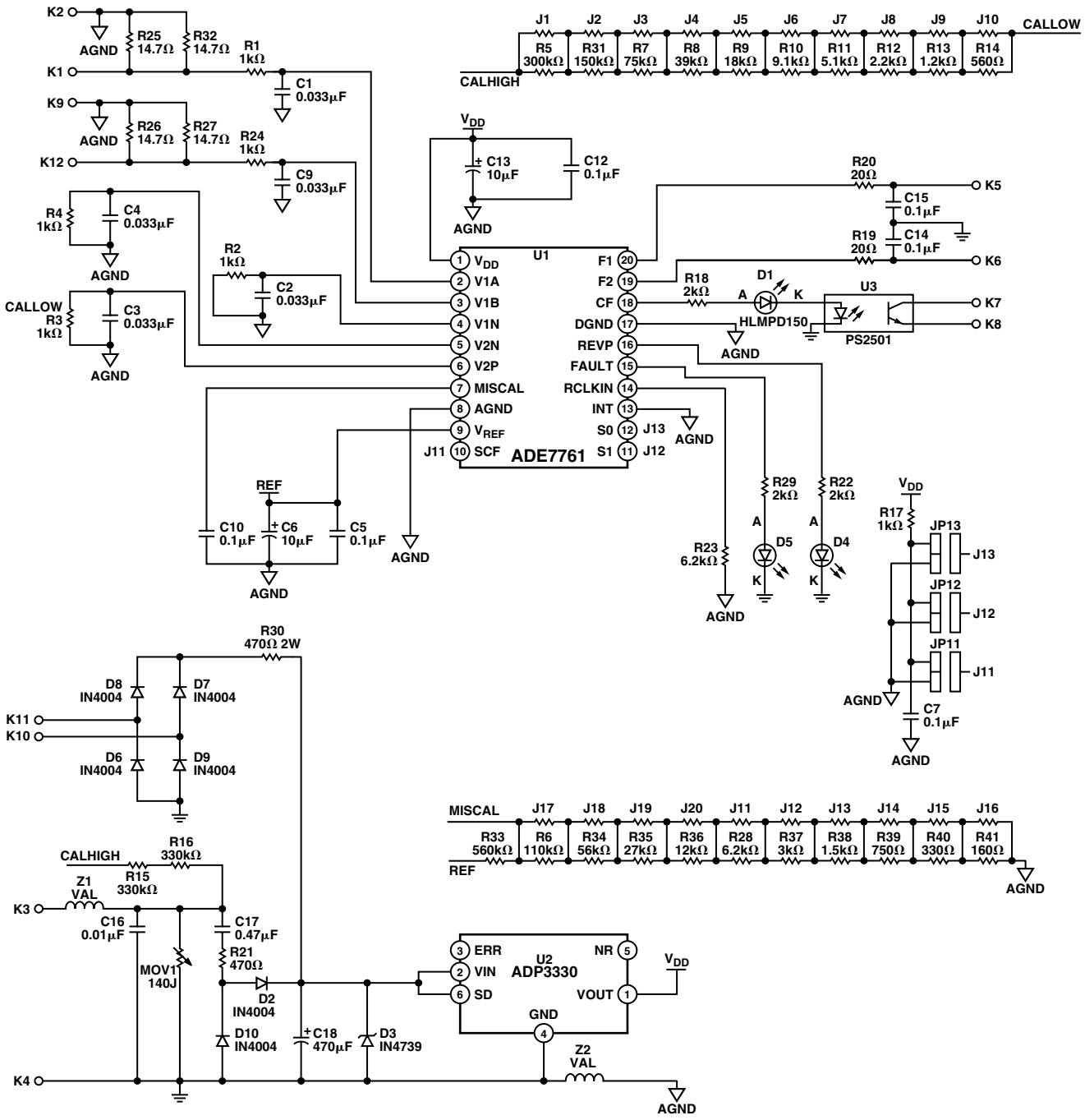

Figure 31. ADE7761 Reference Design Schematic

E04545–0–3/04(0)